19-5321; Rev 2; 6/11

ERRATA SHEET
MAXQ613

Revision A1 Errata

The errata listed below describe situations where MAXQ613 revision A1 components perform differently than expected or differently than described in the data sheet. Maxim Integrated Products, Inc., intends to correct these errata when the opportunity to redesign the product presents itself.

*This errata sheet only applies to MAXQ613 revision A1 components. Revision A1 components are branded on the topside of the package with a six-digit code in the form yywwA1, where yy and ww are two-digit numbers representing the year and work week of manufacture, respectively. To obtain an errata sheet on another MAXQ613 die revision, visit our website at **www.maxim-ic.com/errata**.*

1) FLASH PROGRAM/ERASE OPERATIONS FAIL IN CLOCK DIVIDED MODE

Description:
Flash word programming and page erase operations do not complete successfully when invoked with clock divide-by-2, divide-by-4, or divide-by-8 modes active.

Workaround:
When using the flash controller directly, write and erase functions exercised through the FCNTL and FDATA registers must be performed with a nondivided system mode setting (see the CKCN register). In addition, the following utility ROM function calls access the FCNTL and FDATA registers and have the same requirement prior to being called: UROM_flashWrite, UROM_flashErasePage, and UROM_flashEraseAll. The system clock must be set to divide-by-1 mode before calling any of these routines.

2) PUSH INSTRUCTION CAUSES CODE EXECUTION ERROR WHEN THE MOD[1:0] BITS HAVE BEEN CHANGED FROM THEIR DEFAULT VALUES

Description:
Changing the MOD[1:0] bits (APC[2:0]) from their default value can cause the device to operate incorrectly any time a PUSH instruction is followed by any instruction which reads the active accumulator.

Workaround:
The user must ensure that software never changes the MOD[1:0] bits of the AP register from their default value of 00b.

3) USE OF INTERRUPT PRIORITY FEATURE CAN CAUSE INCORRECT PROCESSING OF INTERRUPTS

Description:
An interrupt that is followed immediately by a higher priority interrupt can cause the CPU to incorrectly service the interrupts.

Workaround:
Do not use high-priority interrupts. Do not modify the IPR0 or IPR1 registers from their reset value. This sets all interrupt sources to the lowest (default) priority level.

REVISION HISTORY

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/10	Initial release	—
1	11/10	Added erratum #2 (PUSH Instruction)	1
2	6/11	Added erratum #3 (Interrupt Priority)	2