19-5634; Rev 2; 6/11

ERRATA SHEET
MAXQ61C

Revision B1 Errata

The errata listed below describe situations where MAXQ61C revision B1 components perform differently than expected or differently than described in the data sheet. Maxim Integrated Products, Inc., intends to correct these errata when the opportunity to redesign the product presents itself.

*This errata sheet only applies to MAXQ61C revision B1 components. Revision B1 components are branded on the topside of the package with a six-digit code in the form yywwB1, where yy and ww are two-digit numbers representing the year and work week of manufacture, respectively. To obtain an errata sheet on another MAXQ61C die revision, visit our website at **www.maxim-ic.com/errata**.*

1) PUSH INSTRUCTION CAUSES CODE EXECUTION ERROR WHEN THE MOD[1:0] BITS HAVE BEEN CHANGED FROM THEIR DEFAULT VALUES

Description:
Changing the MOD[1:0] bits (APC[2:0]) from their default value can cause the device to operate incorrectly any time a PUSH instruction is followed by any instruction which reads the active accumulator.

Workaround:
The user must ensure that software never changes the MOD[1:0] bits of the AP register from their default value of 00b.

2) USE OF INTERRUPT PRIORITY FEATURE CAN CAUSE INCORRECT PROCESSING OF INTERRUPTS

Description:
An interrupt that is followed immediately by a higher priority interrupt can cause the CPU to incorrectly service the interrupts.

Workaround:
Do not use high-priority interrupts. Do not modify the IPR0 or IPR1 registers from their reset value. This sets all interrupt sources to the lowest (default) priority level.

REVISION HISTORY

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/10	Initial release/no errata for this revision	—
1	11/10	Added erratum #1 (PUSH Instruction)	1
2	6/11	Added erratum #2 (Interrupt Priority)	1