Revision 4.1
January 2008

VSC055-01 Data Sheet

Enhanced Two-Wire Serial Backplane Controller

FEATURES

- Up to 64 bits of user-definable, bidirectional general-purpose inputs and outputs
- Integrated port bypass, clock recovery and signal detect support for up to 16 drives
- Eight programmable fan speed monitoring inputs
- Eight programmable pulse-width modulated fan control outputs
- Up to 32 programmable input-to-output bypass pairs
- Two clock input ranges: 8.0 MHz to 12.5 MHz (external crystal or external clock source) and 32.0 MHz to 75.0 MHz (external clock source)
- Selectable direct LED drive flashing capability
- Pin-programmable addressing for up to 16 devices on a single serial bus
- 5-V tolerant high current I/O, Slave mode two-wire serial interface and interrupt output
- Ten programmable LED pulse train circuits
- One 24-bit general-purpose timer (supports a timeout greater than four seconds with a 12.5 MHz core clock)
- Up to 16 subaddressed Master mode two-wire serial interface ports
- Enhanced fan speed monitor input filters
- 20% of package pins are power and ground for excellent noise immunity and long-term reliability

APPLICATIONS

- Enterprise storage environments
- Storage Area Network (SAN) appliances
- Network Attached Storage (NAS) systems
- Fabric Attached Storage (FAS) systems
- Rack-mounted servers with RAID
- JBOD arrays
- Disk-based backup storage
- Near-line storage replacement systems
- Fixed-content storage systems

To order the VSC055-01 device, see “Ordering Information,” page 133.

GENERAL DESCRIPTION

The VSC055-01 device is an I/O-intensive peripheral device that is intended to be part of a cost-effective Fibre Channel Arbitrated Loop (FC-AL), Small Computer System Interface (SCSI), Serial Attached SCSI (SAS), or Serial ATA (SATA) enclosure management solution. The device contains an address-programmable two-wire serial interface, a block of control and status registers, I/O port control logic, specialized port bypass control logic, and a clock-generation block.

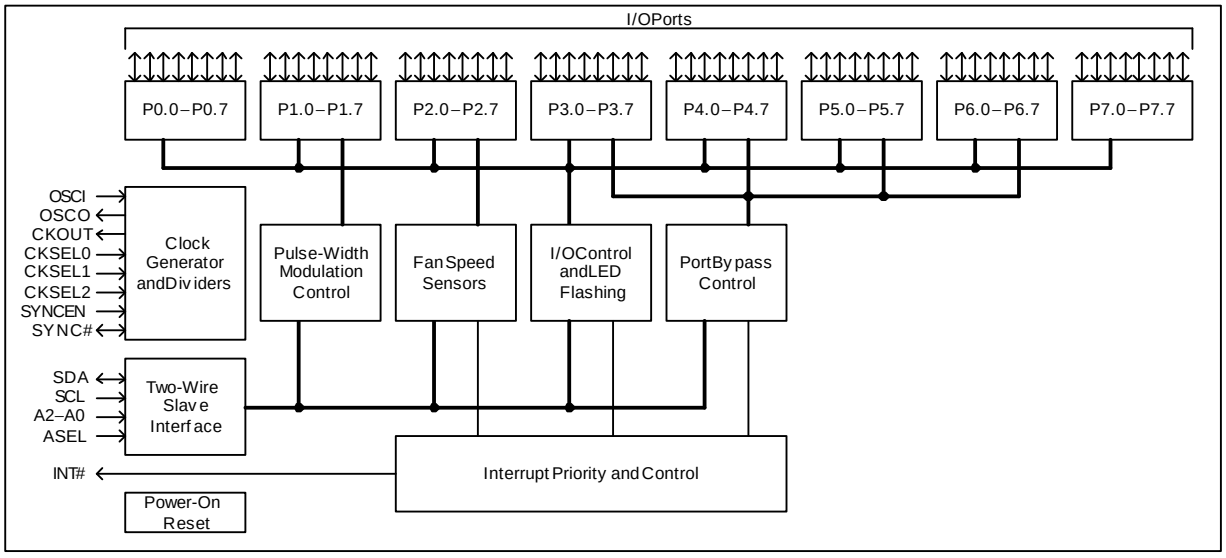
Along with an external crystal, the device can be configured to support up to 64 bits of general-purpose I/O; or 16 bits of general-purpose I/O, 32 bits of port bypass control (16 pairs supporting 16 drives), eight fan speed monitoring inputs, and eight pulse-width modulated general-purpose control outputs.

The VSC055-01 supports various combinations of individual port bypass circuit (PBC), clock recovery unit (CRU), and signal detect unit (SDU) functions, as well as integrated solutions. The control register portion of the device allows the user to individually program each I/O pin as an input, an output, or an open-drain or open-source output.

Additional control features include: selectable flash rates for direct LED drive, input edge detection for interrupt generation, input to output bypass capability, fan speed monitoring control, and pulse-width modulated output control. Support for sub-addressing additional two-wire serial slave devices using a set of seven control registers is included. This capability allows up to 16 independent Master mode two-wire serial slave ports to be created using 32 of the I/O pins.

The addressing capability of the VSC055-01 includes three pins, which are used for device addressing, as well as one pin that can be used to select two device type identifiers. Sixteen VSC055-01 devices can be used in a single two-wire serial interface system.

Block Diagram

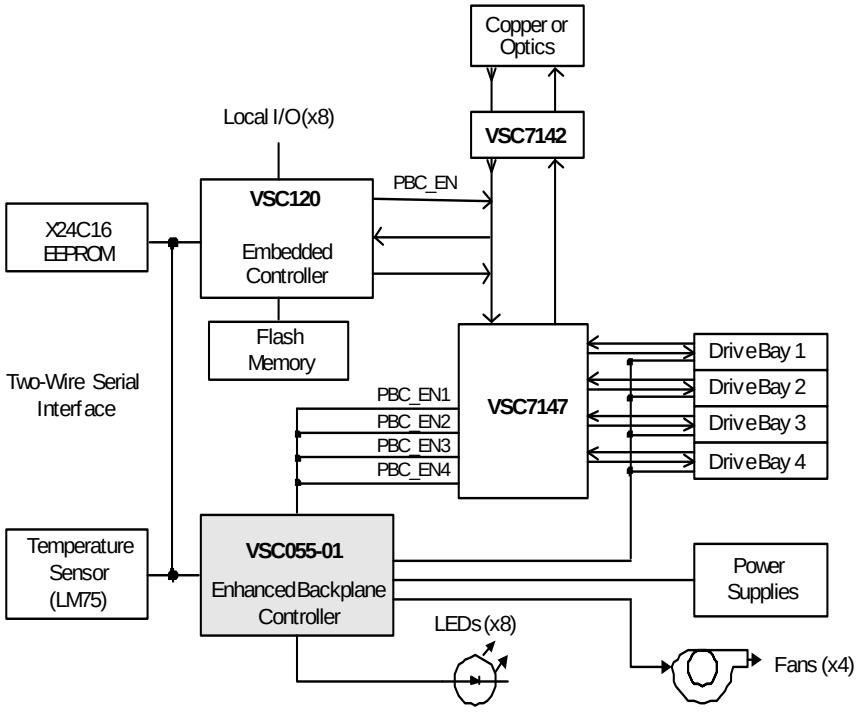


TYPICAL APPLICATIONS

FC-AL Drive Enclosure Configuration

- Basic port bypass configuration
- Support for up to 128 drives: Backplane Controller supports up to two sets of CRU/SDU functions and eight drives, and 16 Backplane Controllers can be attached simultaneously to the serial bus
- Four-drive implementation is shown below; four-channel PBC with two CRU/SDU functions and 36 general-purpose I/O lines for drive control and status, and other enclosure control functions.

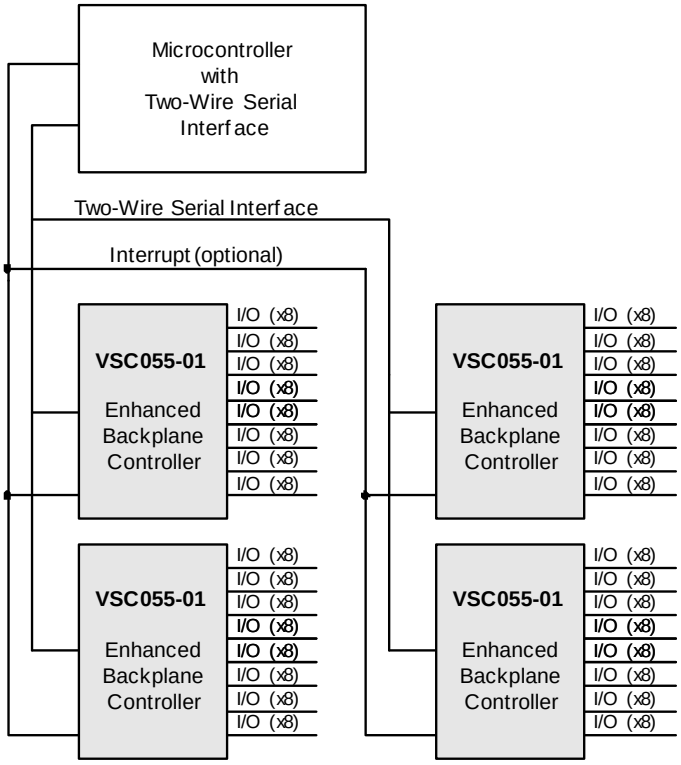
Figure 1. Single Loop, Single Controller with Four Drives



General-Purpose I/O Configuration

- Controlled by general-purpose microcontroller with two-wire serial interface
- Support for up to 1024 I/O lines: Backplane controller supports up to 64 I/O lines and 16 backplane controllers can be simultaneously attached to the serial bus
- Four-backplane controller implementation is shown here with shared open-drain interrupt

Figure 2. Four Backplane Controllers, 256 Bidirectional I/O Lines



Contents

REVISION HISTORY

This section describes changes that have been implemented in this document. The changes are listed by revision, starting with the most recent publication.

Revision 4.1

Revision 4.1 of this data sheet was published in January 2008. The following is a summary of the changes implemented in the data sheet.

- The power supply voltage for the recommended operating conditions were corrected. The minimum power supply voltage is 3.0 V and maximum is 3.6 V. For more information, see Table 23, page 121.

Revision 4.0

Revision 4.0 of this data sheet was published in April 2007. The following is a summary of the changes implemented in the data sheet:

- The electrostatic discharge voltage was added. For charged device model, it is ±1500 V. For human body model, it is a Class 2 rating.
- The moisture sensitivity is now specified as level 3.

Revision 2.0

Revision 2.0 of this data sheet was published in October 2006. This is the first publication of this document.

1 Introduction

This data sheet provides reference information for the Maxim Enhanced Two-Wire Serial Backplane Controller, VSC055-01. It is intended for system designers and software and firmware developers who are using this device to support enclosure management functions or other related remote I/O expansion tasks. The VSC055-01 is pin, function, feature, package, and power supply compatible with the VSC055.

This document assumes that the user is familiar with the two-wire serial interfaces, the programmable I/O control, and the operation of FC-AL control functions, such as a PBC (port bypass controller), a CRU (clock recovery unit), and an SDU (signal detect unit). The user may also need to be familiar with Fibre Channel Arbitrated Loop (FC-AL) operation and SCSI Enclosure Services (SES).

2 Functional Descriptions

The VSC055-01 device is composed of five major functional blocks:

- a Slave mode two-wire serial interface
- a block of control registers
- general-purpose I/O and specialized port bypass control logic
- a clock generator
- power-on reset control logic

The VSC055-01 fully supports a generic two-wire serial interface and is compatible with other industry-standard devices that support this interface at both 100 kHz and 400 kHz.

2.1 Two-Wire Serial Interface

The VSC055-01 device supports a single Slave mode two-wire serial interface. All interchip communication to a microcontroller takes place over this bus. The interface supports a 3-bit address bus that allows the user to select one of eight possible addresses. The address bus is compared to bits 3:1 of the slave address byte. The slave address byte is the first byte transmitted to the device after a START condition. The VSC055-01 supports two pin-selectable, 4-bit device type identifier values, 1000b and 1100b. The address bits and the device identifier allow the use of up to 16 devices on a single two-wire serial interface. The serial interface control logic includes:

- a slave state machine
- address comparison logic
- serial-to-parallel and parallel-to-serial conversion
- register read/write control
- filtering for the clock and data line

A read or write transaction is determined by the least significant bit (R/W) of the first byte transferred. Write accesses require a 3-byte transfer. The first byte is the slave address with the R/W bit LOW, the second byte contains the register address, and the third byte is the write data. Read access requires a 4-byte transfer since data transfer direction can not change after receipt of the slave address byte. The first byte is the slave address with the R/W bit LOW, the second byte contains the register address, the third byte is a repeated slave address with the R/W bit HIGH, and the fourth byte is the read data. If the transaction is a write, the data will be latched into the appropriate register during the acknowledge of the third byte. All transactions to or from the device complete during the acknowledge of the third byte allowing the user to immediately initiate another transfer to the device. Sequential read or write transactions are allowed and are extensions of the above protocol with additional data bytes added to the end of the transaction. All sequential transactions cause the internal address to increment by one, regardless of the register address.

2.2 Control Registers

The VSC055-01 device contains six groups of control registers. Each group supports a specific function within the device as follows:

- the first group is the port data registers
- the second group is the data direction registers
- the third group contains special bit control features

- the fourth group supports the port bypass control function
- the fifth group supports fan speed monitoring
- the sixth group supports pulse-width modulated fan speed control

The VSC055-01 device contains 164 registers to support all required functions. In normal I/O operation, each 8-bit group of I/O pins are controlled by a pair of registers, Port Data and Data Direction. The use of these pairs of registers allows each I/O line to be individually configured as an input with internal pull-up, output or open-drain output with internal pull-up.

The bit control features are enabled through a separate register for each I/O pin. The Bit Control registers allow the user to independently configure each I/O pin to enable one of the special control features, as well as to control Port Data and Data Direction (which are shadowed copies of the standard control bits found in the Port Data and Data Direction registers). Each I/O pin that has been configured as an input can also be configured to assert the open-drain interrupt pin when a rising edge, a falling edge, or either edge is detected on the I/O pin. An Interrupt Status register provides the user with a binary indication of which I/O pin is the source of the current interrupt. Each I/O pin that is configured as an output can automatically generate one of seven selectable flashing rates, which can be driven in an open source or open drain mode. Additionally, two of the standard flash rates can be modified as well as eight dedicated programmable circuits to generate user defined pulse trains for unique flashing sequences. By providing all I/O control capability in a single register, the user can control the operation of the I/O on a pin-by-pin basis. Two additional bits in the odd-numbered bit control registers of each port can configure the pin as an output, which follows the corresponding even-numbered input of each port. As an example, P0.0 becomes the input source of P0.1, which would be programmed as an output operating in one of the three available modes. The outputs can be configured as totem pole, open-drain or open-source drive, allowing a closer approximation of the input driver.

The Port Bypass registers control the operation of a selected group of I/O lines, which can be dedicated to support various combinations of individual PBC/CRU/SDU functions and integrated solutions. Enabling port bypass control causes the normal or bit control register settings to be overridden. Any further changes to the affected registers have no effect. Each Port Bypass Control register automatically configures the I/O lines to support a Force Bypass output and a Signal Detected input.

The Fan Speed registers control the operation of eight programmable inputs that can be used to monitor signals from fans equipped with tachometer outputs. Enabling fan speed control causes the normal or bit control register settings to be overridden. Any further changes to the affected registers have no effect. Each group of three registers provides the capability to enable the function, to establish a user-defined RPM overflow value that indicates a failure, and to determine the current RPM value of the fan. The digital filters on the fan speed inputs can be enabled to increase the normal 100 ns to 200 ns filter to 400 ns to 500 ns.

The Pulse-Width Modulation Control registers enable internal logic to provide duty cycles of 0% to 100% in 3% increments at default frequencies of 26 kHz, 52 kHz, and 104 kHz. Optionally, the PWM outputs can be programmed for three additional frequency ranges of 5.2 kHz, 10.4 kHz, and 20.8 kHz or 1.04 kHz 2.08 kHz, and 4.16 kHz or 208 Hz, 416 Hz and 833 Hz. These outputs can vary the speed of up to eight fans through the use of external drivers and power MOSFETs or pulse-width to voltage converters. They can also be used to support other pulse-width modulated requirements within the system.

2.3 I/O Logic

Each general-purpose 5-V tolerant I/O pin is controlled by a set of registers in the Control register block. The I/O supports a high current drive output buffer that can be configured as a totem pole or open-drain driver. The input section of the I/O supports TTL signaling and includes an internal weak pull-up device. This allows unused I/O pins to be left unconnected without high-current drain issues. The port bypass control I/O pins, which are shared with Port 3, Port 4, Port 5, and Port 6, are generated using the same buffer logic as the other ports. When enabled in Port Bypass Control mode, internal logic overrides the existing configuration, with each I/O pin dedicated to the specific port bypass function. All I/O lines default as inputs with the weak internal pull-up enabled.

2.4 Clock Generator

Clock generation for the device is composed of an internal oscillator, divider circuits, and a distribution network. It supports nominal clock frequencies of:

- 8.0 MHz
- 8.33 MHz
- 8.854 MHz
- 10.0 MHz
- 33.33 MHz
- 40.0 MHz
- 50.0 MHz
- 53.125 MHz

The three CKSEL inputs select one of the eight available fixed clock frequencies, as well as determining the frequency of the CKOUT output. The internal low-frequency clock (8.0 MHz to 12.5 MHz) is used for filtering incoming serial interface signals and interrupt sources, as well as for clocking the slave state machine. Divided clocks provide the source for LED flash rate generators. The oscillator provides a stable clock source for the device and requires the use of an off-chip crystal with a frequency of 8.0 MHz, 8.33 MHz, 8.854 MHz, or 10.0 MHz and related passive components or external clock source. The available fixed clock rates have been selected to allow the use of other system clocks which may be available as well as low-cost crystals. Additionally, when using a high frequency clock, the CKOUT pin provides a divided clock that can be used to drive other VSC055-01 devices within the system. This mechanism ensures that a single additional load is placed on the system clock with all subsequent clock inputs daisy-chained from the first VSC055-01.

The following table describes the CKSEL settings for the available fixed input clocks and the associated divider value and CKOUT frequency.

Table 1. CKSEL Settings

CKSEL2	CKSEL1	CKSEL0	Input Clock	Divider	Internal Clock
VSS	VSS	VSS	10.0 MHz	N/A	10.0 MHz
VSS	VSS	VDD	8.33 MHz	N/A	8.33 MHz
VSS	VDD	VSS	8.854 MHz	N/A	8.854 MHz
VSS	VDD	VDD	8.0 MHz	N/A	8.0 MHz
VDD	VSS	VSS	40.0 MHz	÷4	10.0 MHz

Table 1. CKSEL Settings *(continued)*

CKSEL2	CKSEL1	CKSEL0	Input Clock	Divider	Internal Clock
VDD	VSS	VDD	33.33 MHz	÷4	8.33 MHz
VDD	VDD	VSS	53.125 MHz	÷6	8.854 MHz
VDD	VDD	VDD	50.0 MHz	÷6	8.33 MHz

The VSC055-01 device can operate at frequencies other than those listed in the above table and maintain accurate fan speed and LED control frequencies, as well as continue to meet both the Standard mode (100 kHz) and Fast mode (400 kHz) serial interface timings. Frequencies from 8.0 MHz to 12.5 MHz and 32.0 MHz to 75.0 MHz are allowable as long as they meet the AC timing requirements. For information on AC timing requirements, see "AC Characteristics," page 119.

The Clock Divider Control Register (CDC), located at FEh, can be programmed to override the divider value selected by the CKSEL input pins and adjust the divided clock source used for the fan speed and LED control logic. The pulse-width modulated outputs are not controlled by this logic and can vary based on the input frequency. For examples of various frequency settings, based on both the CKSEL inputs and the appropriate CDC register value, see"FEh: Clock Divider Control (CDC)," page 113.

Logic within the VSC055-01 synchronizes the divided clocks between devices attached to the same two-wire serial bus with no more than 200 ns of skew when the fixed divider frequencies are used. Multiple devices can then be used to drive different LEDs at the same frequency, providing a synchronized visible indication. Devices attached to different two-wire serial busses can be synchronized by enabling the SYNC# pin. This pin, which is connected to the SYNC# pin of all VSC055-01 devices in the system, provides a sync pulse based on a programmable delay that is greater than the slowest selected LED flash rate. For more information about the programmable capabilities of this feature, see "FDh: Clock Select Control (CSC)," page 111.

2.5 Power-on Reset

Power-on reset (POR) is accomplished by the use of an internal POR cell. After power on, the serial interface state machine always returns an idle state while waiting for a START condition to appear on the SCL and SDA pins. A proper power-on reset sequence clears the serial interface state machine, the clock generators, the control registers, the I/O control logic, and the port bypass control logic. The divided clocks used for LED flash rate generation are also in a known state. Regardless of the effectiveness of the power-on reset mechanism, it is strongly recommended that the control registers and the I/O control logic be cleared through the Soft Reset register bit. This can be accomplished by writing a 80h to the BCT Register (FCh), followed immediately by a STOP condition. This bit is self-resetting and does not require further attention.

3 Registers

This section contains descriptions for the device-specific control registers. All register locations are fixed within the device and are mapped for easy access, as well as for future enhancements.

3.1 Control Registers

The control register section is separated into three sub-sections: a register map, an address map, and bit level descriptions of all registers. The register map lists all registers by operating address. The address map shows the relative layout of all control registers.

Although all registers can be accessed at any time and no register function interferes with the operation of the serial interface, changing register bits does have an immediate effect on the respective I/O lines.

The following table provides the mapping of the registers.

Table 2. Register Map

Data Memory Address	Access	Label	Description
00h	R/W	GPD0	General-Purpose I/O Port 0 Data Register
01h	R/W	GPD1	General-Purpose I/O Port 1 Data Register
02h	R/W	GPD2	General-Purpose I/O Port 2 Data Register
03h	R/W	GPD3	General-Purpose I/O Port 3 Data Register
04h	R/W	GPD4	General-Purpose I/O Port 4 Data Register
05h	R/W	GPD5	General-Purpose I/O Port 5 Data Register
06h	R/W	GPD6	General-Purpose I/O Port 6 Data Register
07h	R/W	GPD7	General-Purpose I/O Port 7 Data Register
10h	R/W	DDP0	I/O Port 0 Data Direction Register
11h	R/W	DDP1	I/O Port 1 Data Direction Register
12h	R/W	DDP2	I/O Port 2 Data Direction Register
13h	R/W	DDP3	I/O Port 3 Data Direction Register
14h	R/W	DDP4	I/O Port 4 Data Direction Register
15h	R/W	DDP5	I/O Port 5 Data Direction Register
16h	R/W	DDP6	I/O Port 6 Data Direction Register
17h	R/W	DDP7	I/O Port 7 Data Direction Register
20h	R/W	PBC0	Port Bypass Control 0 Register
21h	R/W	PBC1	Port Bypass Control 1 Register
22h	R/W	PBC2	Port Bypass Control 2 Register
23h	R/W	PBC3	Port Bypass Control 3 Register
24h	R/W	PBC4	Port Bypass Control 4 Register
25h	R/W	PBC5	Port Bypass Control 5 Register
26h	R/W	PBC6	Port Bypass Control 6 Register
27h	R/W	PBC7	Port Bypass Control 7 Register
28h	R/W	PBC8	Port Bypass Control 8 Register

Table 2. Register Map *(continued)*

Data Memory Address	Access	Label	Description
29h	R/W	PBC9	Port Bypass Control 9 Register
2Ah	R/W	PBC10	Port Bypass Control 10 Register
2Bh	R/W	PBC11	Port Bypass Control 11 Register
2Ch	R/W	PBC12	Port Bypass Control 12 Register
2Dh	R/W	PBC13	Port Bypass Control 13 Register
2Eh	R/W	PBC14	Port Bypass Control 14 Register
2Fh	R/W	PBC15	Port Bypass Control 15 Register
30h	R/W	FSC0	Fan Speed Control 0 Register
31h	R/W	FSCO0	Fan Speed Count Overflow 0 Register
32h	R	FSCC0	Fan Speed Current Count 0 Register
34h	R/W	FSC1	Fan Speed Control 1 Register
35h	R/W	FSCO1	Fan Speed Count Overflow 1 Register
36h	R	FSCC1	Fan Speed Current Count 1 Register
38h	R/W	FSC2	Fan Speed Control 2 Register
39h	R/W	FSCO2	Fan Speed Count Overflow 2 Register
3Ah	R	FSCC2	Fan Speed Current Count 2 Register
3Ch	R/W	FSC3	Fan Speed Control 3 Register
3Dh	R/W	FSCO3	Fan Speed Count Overflow 3 Register
3Eh	R	FSCC3	Fan Speed Current Count 3 Register
40h	R/W	FSC4	Fan Speed Control 4 Register
41h	R/W	FSCO4	Fan Speed Count Overflow 4 Register
42h	R	FSCC4	Fan Speed Current Count 4 Register
44h	R/W	FSC5	Fan Speed Control 5 Register
45h	R/W	FSCO5	Fan Speed Count Overflow 5 Register
46h	R	FSCC5	Fan Speed Current Count 5 Register
48h	R/W	FSC6	Fan Speed Control 6 Register
49h	R/W	FSCO6	Fan Speed Count Overflow 6 Register
4Ah	R	FSCC6	Fan Speed Current Count 6 Register
4Ch	R/W	FSC7	Fan Speed Control 7 Register
4Dh	R/W	FSCO7	Fan Speed Count Overflow 7 Register
4Eh	R	FSCC7	Fan Speed Current Count 7 Register
70h	R/W	PTC00	Pulse Train 0 Control 0 Register
71h	R/W	PTC01	Pulse Train 0 Control 1 Register
72h	R/W	PTC10	Pulse Train 1 Control 0 Register
73h	R/W	PTC11	Pulse Train 1 Control 1 Register
74h	R/W	PTC20	Pulse Train 2 Control 0 Register
75h	R/W	PTC21	Pulse Train 2 Control 1 Register
76h	R/W	PTC30	Pulse Train 3 Control 0 Register
77h	R/W	PTC31	Pulse Train 3 Control 1 Register
78h	R/W	PTC40	Pulse Train 4 Control 0 Register

Table 2. Register Map *(continued)*

Data Memory Address	Access	Label	Description
79h	R/W	PTC41	Pulse Train 4 Control 1 Register
7Ah	R/W	PTC50	Pulse Train 5 Control 0 Register
7Bh	R/W	PTC51	Pulse Train 5 Control 1 Register
7Ch	R/W	PTC60	Pulse Train 6 Control 0 Register
7Dh	R/W	PTC61	Pulse Train 6 Control 1 Register
7Eh	R/W	PTC70	Pulse Train 7 Control 0 Register
7Fh	R/W	PTC71	Pulse Train 7 Control 1 Register
80h	R/W	BCP00	Bit Control Port 0 - Bit 0 Register
81h	R/W	BCP01	Bit Control Port 0 - Bit 1 Register
82h	R/W	BCP02	Bit Control Port 0 - Bit 2 Register
83h	R/W	BCP03	Bit Control Port 0 - Bit 3 Register
84h	R/W	BCP04	Bit Control Port 0 - Bit 4 Register
85h	R/W	BCP05	Bit Control Port 0 - Bit 5 Register
86h	R/W	BCP06	Bit Control Port 0 - Bit 6 Register
87h	R/W	BCP07	Bit Control Port 0 - Bit 7 Register
88h	R/W	PTC80	Pulse Train 8 Control 0 Register
89h	R/W	PTC81	Pulse Train 8 Control 1 Register
8Ch	R/W	PTC90	Pulse Train 9 Control 0 Register
8Dh	R/W	PTC91	Pulse Train 9 Control 1 Register
90h	R/W	BCP10	Bit Control Port 1 - Bit 0 Register
91h	R/W	BCP11	Bit Control Port 1 - Bit 1 Register
92h	R/W	BCP12	Bit Control Port 1 - Bit 2 Register
93h	R/W	BCP13	Bit Control Port 1 - Bit 3 Register
94h	R/W	BCP14	Bit Control Port 1 - Bit 4 Register
95h	R/W	BCP15	Bit Control Port 1 - Bit 5 Register
96h	R/W	BCP16	Bit Control Port 1 - Bit 6 Register
97h	R/W	BCP17	Bit Control Port 1 - Bit 7 Register
98h	R/W	PWMC0	Pulse-Width Modulation Control 0 Register
99h	R/W	PWMC1	Pulse-Width Modulation Control 1 Register
9Ah	R/W	PWMC2	Pulse-Width Modulation Control 2 Register
9Bh	R/W	PWMC3	Pulse-Width Modulation Control 3 Register
9Ch	R/W	PWMC4	Pulse-Width Modulation Control 4 Register
9Dh	R/W	PWMC5	Pulse-Width Modulation Control 5 Register
9Eh	R/W	PWMC6	Pulse-Width Modulation Control 6 Register
9Fh	R/W	PWMC7	Pulse-Width Modulation Control 7 Register
A0h	R/W	BCP20	Bit Control Port 2 - Bit 0 Register
A1h	R/W	BCP21	Bit Control Port 2 - Bit 1 Register
A2h	R/W	BCP22	Bit Control Port 2 - Bit 2 Register
A3h	R/W	BCP23	Bit Control Port 2 - Bit 3 Register
A4h	R/W	BCP24	Bit Control Port 2 - Bit 4 Register

Table 2. Register Map *(continued)*

Data Memory Address	Access	Label	Description
A5h	R/W	BCP25	Bit Control Port 2 - Bit 5 Register
A6h	R/W	BCP26	Bit Control Port 2 - Bit 6 Register
A7h	R/W	BCP27	Bit Control Port 2 - Bit 7 Register
B0h	R/W	BCP30	Bit Control Port 3 - Bit 0 Register
B1h	R/W	BCP31	Bit Control Port 3 - Bit 1 Register
B2h	R/W	BCP32	Bit Control Port 3 - Bit 2 Register
B3h	R/W	BCP33	Bit Control Port 3 - Bit 3 Register
B4h	R/W	BCP34	Bit Control Port 3 - Bit 4 Register
B5h	R/W	BCP35	Bit Control Port 3 - Bit 5 Register
B6h	R/W	BCP36	Bit Control Port 3 - Bit 6 Register
B7h	R/W	BCP37	Bit Control Port 3 - Bit 7 Register
C0h	R/W	BCP40	Bit Control Port 4 - Bit 0 Register
C1h	R/W	BCP41	Bit Control Port 4 - Bit 1 Register
C2h	R/W	BCP42	Bit Control Port 4 - Bit 2 Register
C3h	R/W	BCP43	Bit Control Port 4 - Bit 3 Register
C4h	R/W	BCP44	Bit Control Port 4 - Bit 4 Register
C5h	R/W	BCP45	Bit Control Port 4 - Bit 5 Register
C6h	R/W	BCP46	Bit Control Port 4 - Bit 6 Register
C7h	R/W	BCP47	Bit Control Port 4 - Bit 7 Register
CCh	R/W	GPTC0	General-Purpose Timer Count 0 Register
CDh	R/W	GPTC1	General-Purpose Timer Count 1 Register
CEh	R/W	GPTC2	General-Purpose Timer Count 2 Register
CFh	R/W	GPTE	General-Purpose Timer Enable Register
D0h	R/W	BCP50	Bit Control Port 5 - Bit 0 Register
D1h	R/W	BCP51	Bit Control Port 5 - Bit 1 Register
D2h	R/W	BCP52	Bit Control Port 5 - Bit 2 Register
D3h	R/W	BCP53	Bit Control Port 5 - Bit 3 Register
D4h	R/W	BCP54	Bit Control Port 5 - Bit 4 Register
D5h	R/W	BCP55	Bit Control Port 5 - Bit 5 Register
D6h	R/W	BCP56	Bit Control Port 5 - Bit 6 Register
D7h	R/W	BCP57	Bit Control Port 5 - Bit 7 Register
E0h	R/W	BCP60	Bit Control Port 6 - Bit 0 Register
E1h	R/W	BCP61	Bit Control Port 6 - Bit 1 Register
E2h	R/W	BCP62	Bit Control Port 6 - Bit 2 Register
E3h	R/W	BCP63	Bit Control Port 6 - Bit 3 Register
E4h	R/W	BCP64	Bit Control Port 6 - Bit 4 Register
E5h	R/W	BCP65	Bit Control Port 6 - Bit 5 Register
E6h	R/W	BCP66	Bit Control Port 6 - Bit 6 Register
E7h	R/W	BCP67	Bit Control Port 6 - Bit 7 Register
E8h	R/W	MICD	Master Interface Clock Divider Register

Table 2. Register Map *(continued)*

Data Memory Address	Access	Label	Description
E9h	R/W	MIPS	Master Interface Port Select Register
EAh	R/W	MID	Master Interface Data Register
EBh	R/W	MIC	Master Interface Command Register
ECh	R/W	MILC	Master Interface Low-Level Control Register
EDh	R	MIS	Master Interface Status Register
EEh	R	MIRD	Master Interface Read Data Register
F0h	R/W	BCP70	Bit Control Port 7 - Bit 0 Register
F1h	R/W	BCP71	Bit Control Port 7 - Bit 1 Register
F2h	R/W	BCP72	Bit Control Port 7 - Bit 2 Register
F3h	R/W	BCP73	Bit Control Port 7 - Bit 3 Register
F4h	R/W	BCP74	Bit Control Port 7 - Bit 4 Register
F5h	R/W	BCP75	Bit Control Port 7 - Bit 5 Register
F6h	R/W	BCP76	Bit Control Port 7 - Bit 6 Register
F7h	R/W	BCP77	Bit Control Port 7 - Bit 7 Register
F8h	R/W	BCIS	Backplane Controller Interrupt Status Register
FCh	R/W	BCT	Backplane Controller Test Register
FDh	R/W	CSC	Clock Select Control Register
FEh	R/W	CDC	Clock Divider Control Register
FFh	R	VER	Backplane Controller Version Register

The following table provides the mapping of the register sets by address.

Table 3. Address Map

11b	10b	01b	00b	Address
GPD3	GPD2	GPD1	GPD0	00h
GPD7	GPD6	GPD5	GPD4	04h
reserved	reserved	reserved	reserved	08h-0Ch
DDP3	DDP2	DDP1	DDP0	10h
DDP7	DDP6	DDP5	DDP4	14h
reserved	reserved	reserved	reserved	18h-1Ch
PBC3	PBC2	PBC1	PBC0	20h
PBC7	PBC6	PBC5	PBC4	24h
PBC11	PBC10	PBC9	PBC8	28h
PBC15	PBC14	PBC13	PBC12	2Ch
reserved	FSCC0	FSCO0	FSC0	30h
reserved	FSCC1	FSCO1	FSC1	34h
reserved	FSCC2	FSCO2	FSC2	38h
reserved	FSCC3	FSCO3	FSC3	3Ch
reserved	FSCC4	FSCO4	FSC4	40h
reserved	FSCC5	FSCO5	FSC5	44h
reserved	FSCC6	FSCO6	FSC6	48h

Table 3. Address Map *(continued)*

11b	10b	01b	00b	Address
reserved	FSCC7	FSCO7	FSC7	4Ch
reserved	reserved	reserved	reserved	50h-6Ch
PTC11	PTC10	PTC01	PTC00	70h
PTC31	PTC30	PTC21	PTC20	74h
PTC51	PTC50	PTC41	PTC40	78h
PTC71	PTC70	PTC51	PTC50	7Ch
BCP03	BCP02	BCP01	BCP00	80h
BCP07	BCP06	BCP05	BCP04	84h
reserved	reserved	PTC41	PTC40	88h
reserved	reserved	PTC51	PTC50	8Ch
BCP13	BCP12	BCP11	BCP10	90h
BCP17	BCP16	BCP15	BCP14	94h
PWMC3	PWMC2	PWMC1	PWMC0	98h
PWMC7	PWMC6	PWMC5	PWMC4	9Ch
BCP23	BCP22	BCP21	BCP20	A0h
BCP27	BCP26	BCP25	BCP24	A4h
reserved	reserved	reserved	reserved	A8h-ACh
BCP33	BCP32	BCP31	BCP30	B0h
BCP37	BCP36	BCP35	BCP34	B4h
reserved	reserved	reserved	reserved	B8h-BCh
BCP43	BCP42	BCP41	BCP40	C0h
BCP47	BCP46	BCP45	BCP44	C4h
reserved	reserved	reserved	reserved	C8h
GPTE	GPTC2	GPTC1	GPTC0	CCh
BCP53	BCP52	BCP51	BCP50	D0h
BCP57	BCP56	BCP55	BCP54	D4h
reserved	reserved	reserved	reserved	D8h-DCh
BCP63	BCP62	BCP61	BCP60	E0h
BCP67	BCP66	BCP65	BCP64	E4h
MIC	MID	MIPS	MICD	E8h
reserved	MIRD	MIS	MILC	ECh
BCP73	BCP72	BCP71	BCP70	F0h
BCP77	BCP76	BCP75	BCP74	F4h
reserved	reserved	reserved	BCIS	F8h
VER	CDC	CSC	BCT	FCh

3.2 Control Register Definitions

The control register definitions provides a bit-level description of all register bits, including power on and default values. The terms set and assert refer to bits that are programmed to a binary 1. The terms reset, de-assert, and clear refer to bits that are programmed to a binary 0. Reserved bits are represented by RES and always return an unknown value. These bits should be masked. Bits that are reserved should never be set to a binary 1, because these bits may be defined in future versions of the device.

3.2.1 00h: General-Purpose I/O Port 0 Data (GPD0)

The following table shows the bit assignments for the General-Purpose I/O Port 0 Data register.

Register Name: GPD0
Address: 00h
Reset Value: XXXX_XXXXb

Bit	Bit Label	Access	Description
7:0	GPD0.7–0	R/W	General-Purpose Data When the I/O pin is enabled as an output, writing these bits determines the data value that will be present on the corresponding I/O pin. If the I/O pin is enabled as an input, reading these register bits represent the current voltage applied to the pin. At no time do the bits directly represent the value latched into the data register. If a pin is enabled as an input and there is no signal applied, weak internal pull-up resistors hold the pin at a binary 1. After a reset or power on, the register bits are set to a binary 1, however, the value returned from a register read is the level applied to the pin since each pin is an input by default.

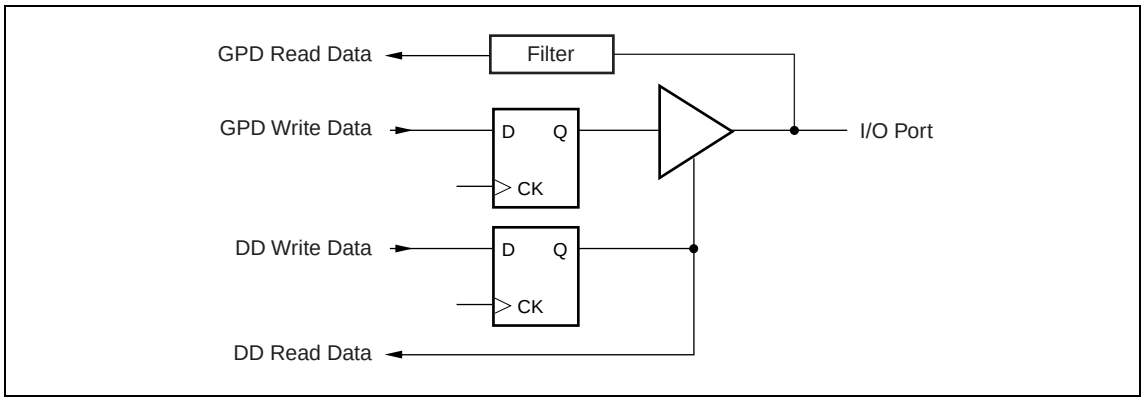


Figure 3. I/O Port Block Diagram

3.2.2 01h: General-Purpose I/O Port 1 Data (GPD1)

The following table shows the bit assignments for the General-Purpose I/O Port 1 Data register.

Register Name: GPD1
Address: 01h
Reset Value: XXXX_XXXXb

Bit	Bit Label	Access	Description
7:0	GPD1.7-0	R/W	General-Purpose Data When the I/O pin is enabled as an output, writing these bits determines the data value that will be present on the corresponding I/O pin. If the I/O pin is enabled as an input, reading these register bits represents the current voltage applied to the pin. At no time do the bits directly represent the value latched into the data register If a pin is enabled as an input and there is no signal applied, weak internal pull-up resistors hold the pin at a binary 1. After a reset or power on, the register bits are set to a binary 1, however, the value returned from a register read is the level applied to the pin since each pin is an input by default.

3.2.3 02h: General-Purpose I/O Port 2 Data (GPD2)

The following table shows the bit assignments for the General-Purpose I/O Port 2 Data register.

Register Name: GPD2
Address: 02h
Reset Value: XXXX_XXXXb

Bit	Bit Label	Access	Description
7:0	GPD2.7-0	R/W	General-Purpose Data When the I/O pin is enabled as an output, writing these bits determines the data value that will be present on the corresponding I/O pin. If the I/O pin is enabled as an input, reading these register bits represents the current voltage applied to the pin. At no time do the bits directly represent the value latched into the data register. If a pin is enabled as an input and there is no signal applied, weak internal pull-up resistors hold the pin at a binary 1. After a reset or power on, the register bits are set to a binary 1, however, the value returned from a register read is the level applied to the pin since each pin is an input by default.

3.2.4 03h: General-Purpose I/O Port 3 Data (GPD3)

The following table shows the bit assignments for the General-Purpose I/O Port 3 Data register. Control of the individual I/O pins in this register can be overridden by the PBC0, PBC1, PBC2, and PBC3 registers when port bypass control is required.

Register Name: GPD3
Address: 03h
Reset Value: XXXX_XXXXb

Bit	Bit Label	Access	Description
7:0	GPD3.7-0	R/W	General-Purpose Data When the I/O pin is enabled as an output, writing these bits determines the data value that will be present on the corresponding I/O pin. If the I/O pin is enabled as an input, reading these register bits represents the current voltage applied to the pin. At no time do the bits directly represent the value latched into the data register. If a pin is enabled as an input and there is no signal applied, weak internal pull-up resistors hold the pin at a binary 1. After a reset or power on, the register bits are set to a binary 1, but the value returned from a register read is the level applied to the pin since each pin is an input by default.

3.2.5 04h: General-Purpose I/O Port 4 Data (GPD4)

The following table shows the bit assignments for the General-Purpose I/O Port 4 Data register. Control of the individual I/O pins in this register can be overridden by the PBC4, PBC5, PBC6, and PBC7 registers when port bypass control is required.

Register Name: GPD4
Address: 04h
Reset Value: XXXX_XXXXb

Bit	Bit Label	Access	Description
7:0	GPD4.7-0	R/W	General-Purpose Data When the I/O pin is enabled as an output, writing these bits determines the data value that will be present on the corresponding I/O pin. If the I/O pin is enabled as an input, reading these register bits represents the current voltage applied to the pin. At no time do the bits directly represent the value latched into the data register. If a pin is enabled as an input and there is no signal applied, weak internal pull-up resistors hold the pin at a binary 1. After a reset or power on, the register bits are set to a binary 1, but the value returned from a register read is the level applied to the pin since each pin is an input by default.

3.2.6 05h: General-Purpose I/O Port 5 Data (GPD5)

The following table shows the bit assignments for the General-Purpose I/O Port 5 Data register. Control of the individual I/O pins in this register can be overridden by the PBC8, PBC9, PBC10, and PBC11 registers when port bypass control is required.

Register Name: GPD5
Address: 05h
Reset Value: XXXX_XXXXb

Bit	Bit Label	Access	Description
7:0	GPD5.7-0	R/W	General-Purpose Data When the I/O pin is enabled as an output, writing these bits determines the data value that will be present on the corresponding I/O pin. If the I/O pin is enabled as an input, reading these register bits represents the current voltage applied to the pin. At no time do the bits directly represent the value latched into the data register. If a pin is enabled as an input and there is no signal applied, weak internal pull-up resistors hold the pin at a binary 1. After a reset or power on, the register bits are set to a binary 1, but the value returned from a register read is the level applied to the pin since each pin is an input by default.

3.2.7 06h: General-Purpose I/O Port 6 Data (GPD6)

The following table shows the bit assignments for the General-Purpose I/O Port 6 Data register. Control of the individual I/O pins in this register can be overridden by the PBC12, PBC13, PBC14, and PBC15 registers when port bypass control is required.

Register Name: GPD6
Address: 06h
Reset Value: XXXX_XXXXb

Bit	Bit Label	Access	Description
7:0	GPD6.7-0	R/W	General-Purpose Data When the I/O pin has been enabled as an output, writing these bits determines the data value that will be present on the corresponding I/O pin. If the I/O pin has been enabled as an input, reading these register bits represents the current voltage applied to the pin. At no time do the bits directly represent the value latched into the data register. If a pin is enabled as an input and there is no signal applied, weak internal pull-up resistors hold the pin at a binary 1. After a reset or power on, the register bits are set to a binary 1, however, the value returned from a register read is the level applied to the pin since each pin is an input by default.

3.2.8 07h: General-Purpose I/O Port 7 Data (GPD7)

The following table shows the bit assignments for the General-Purpose I/O Port 7 Data register.

Register Name: GPD7
Address: 07h
Reset Value: XXXX_XXXXb

Bit	Bit Label	Access	Description
7:0	GPD7.7-0	R/W	General-Purpose Data When the I/O pin is enabled as an output, writing these bits determines the data value that will be present on the corresponding I/O pin. If the I/O pin is enabled as an input, reading these register bits represents the current voltage applied to the pin. At no time do the bits directly represent the value latched into the data register. If a pin is enabled as an input and there is no signal applied, weak internal pull-up resistors hold the pin at a binary 1. After a reset or power on, the register bits are set to a binary 1, however, the value returned from a register read is the level applied to the pin since each pin is an input by default.

3.2.9 10h: I/O Port 0 Data Direction (DDP0)

The following table shows the bit assignments for the I/O Port 0 Data Direction register.

Register Name: DDP0
Address: 10h
Reset Value: 1111_1111b

Bit	Bit Label	Access	Description
7:0	DDP0.7-0	R/W	Data Direction These bits determine the direction of the data flow through the I/O pin. To enable the respective I/O pin as an input, set the appropriate bit. To enable the respective I/O pin as an output, reset the appropriate bit. Each I/O pin can be individually configured as a true bidirectional function. To implement an open-drain or open-source function, set or reset the appropriate data bit using the data direction bit as the programmed data value. After a reset or power on, these bits are set to a binary 1, enabling the I/O as an input with weak pull-up.

3.2.10 11h: I/O Port 1 Data Direction (DDP1)

The following table shows the bit assignments for the I/O Port 1 Data Direction register.

Register Name: DDP1
Address: 11h
Reset Value: 1111_1111b

Bit	Bit Label	Access	Description
7:0	DDP1.7-0	R/W	Data Direction These bits determine the direction of the data flow through the I/O pin. To enable the respective I/O pin as an input, set the appropriate bit. To enable the respective I/O pin as an output, reset the appropriate bit. Each I/O pin can be individually configured as a true bidirectional function. To implement an open-drain or open-source function, set or reset the appropriate data bit using the data direction bit as the programmed data value. After a reset or power on, these bits are set to a binary 1, enabling the I/O as an input with weak pull-up.

3.2.11 12h: I/O Port 2 Data Direction (DDP2)

The following table shows the bit assignments for the I/O Port 2 Data Direction register.

Register Name: DDP2
Address: 12h
Reset Value: 1111_1111b

Bit	Bit Label	Access	Description
7:0	DDP2.7-0	R/W	Data Direction These bits determine the direction of the data flow through the I/O pin. To enable the respective I/O pin as an input, set the appropriate bit. To enable the respective I/O pin as an output, reset the appropriate bit. Each I/O pin can be individually configured as a true bidirectional function. To implement an open-drain or open-source function, set or reset the appropriate data bit using the data direction bit as the programmed data value. After a reset or power on, these bits are set to a binary 1, enabling the I/O as an input with weak pull-up.

3.2.12 13h: I/O Port 3 Data Direction (DDP3)

The following table shows the bit assignments for the I/O Port 3 Data Direction register. Control of the individual I/O pins in this register can be overridden by the PBC0, PBC1, PBC2, and PBC3 registers when port bypass control is required.

Register Name: DDP3
Address: 13h
Reset Value: 1111_1111b

Bit	Bit Label	Access	Description
7:0	DDP3.7-0	R/W	Data Direction These bits determine the direction of the data flow through the I/O pin. To enable the respective I/O pin as an input, set the appropriate bit. To enable the respective I/O pin as an output, reset the appropriate bit. Each I/O pin can be individually configured as a true bidirectional function. To implement an open-drain or open-source function, set or reset the appropriate data bit using the data direction bit as the programmed data value. After a reset or power on, these bits are set to a binary 1, enabling the I/O as an input with weak pull-up.

3.2.13 14h: I/O Port 4 Data Direction (DDP4)

The following table shows the bit assignments for the I/O Port 4 Data Direction register.

Control of the individual I/O pins in this register can be overridden by the PBC4, PBC5, PBC6, and PBC7 registers when port bypass control is required.

Register Name: DDP4
Address: 14h
Reset Value: 1111_1111b

Bit	Bit Label	Access	Description
7:0	DDP4.7-0	R/W	Data Direction These bits determine the direction of the data flow through the I/O pin. To enable the respective I/O pin as an input, set the appropriate bit. To enable the respective I/O pin as an output, reset the appropriate bit. Each I/O pin can be individually configured as a true bidirectional function. To implement an open-drain or open-source function, set or reset the appropriate data bit using the data direction bit as the programmed data value. After a reset or power on, these bits are set to a binary 1, enabling the I/O as an input with weak pull-up.

3.2.14 15h: I/O Port 5 Data Direction (DDP5)

The following table shows the bit assignments for the I/O Port 5 Data Direction register.

Control of the individual I/O pins in this register can be overridden by the PBC8, PBC9, PBC10, and PBC11 registers when port bypass control is required.

Register Name: DDP5
Address: 15h
Reset Value: 1111_1111b

Bit	Bit Label	Access	Description
7:0	DDP5.7-0	R/W	Data Direction These bits determine the direction of the data flow through the I/O pin. To enable the respective I/O pin as an input, set the appropriate bit. To enable the respective I/O pin as an output, reset the appropriate bit. Each I/O pin can be individually configured as a true bidirectional function. To implement an open-drain or open-source function, set or reset the appropriate data bit using the data direction bit as the programmed data value. After a reset or power on, these bits are set to a binary 1, enabling the I/O as an input with weak pull-up.

3.2.15 16h: I/O Port 6 Data Direction (DDP6)

The following table shows the bit assignments for the I/O Port 6 Data Direction register.

Control of the individual I/O pins in this register can be overridden by the PBC12, PBC13, PBC14, and PBC15 registers when port bypass control is required.

Register Name: DDP6
Address: 16h
Reset Value: 1111_1111b

Bit	Bit Label	Access	Description
7:0	DDP6.7-0	R/W	Data Direction These bits determine the direction of the data flow through the I/O pin. To enable the respective I/O pin as an input, set the appropriate bit. To enable the respective I/O pin as an output, reset the appropriate bit. Each I/O pin can be individually configured as a true bidirectional function. To implement an open-drain or open-source function, set or reset the appropriate data bit using the data direction bit as the programmed data value. After a reset or power on, these bits are set to a binary 1, enabling the I/O as an input with weak pull-up.

3.2.16 17h: I/O Port 7 Data Direction (DDP7)

The following table shows the bit assignments for the I/O Port 7 Data Direction register.

Register Name: DDP7
Address: 17h
Reset Value: 1111_1111b

Bit	Bit Label	Access	Description
7:0	DDP7.7-0	R/W	Data Direction These bits determine the direction of the data flow through the I/O pin. To enable the respective I/O pin as an input, set the appropriate bit. To enable the respective I/O pin as an output, reset the appropriate bit. Each I/O pin can be individually configured as a true bidirectional function. To implement an open-drain or open-source function, set or reset the appropriate data bit using the data direction bit as the programmed data value. After a reset or power on, these bits are set to a binary 1, enabling the I/O as an input with weak pull-up.

3.2.17 20h: Port Bypass Control 0 (PBC0)

The following table shows the bit assignments for the Port Bypass Control 0 register. This register affects the P3.1 and P3.0 pins.

Register Name: PBC0
Address: 20h
Reset Value: 00XX_XX1Xb

Bit	Bit Label	Access	Description
7	PBCEN	R/W	Port Bypass Control Enable When this bit is set, P3.1 and P3.0 are automatically configured as a Force Bypass (FB) output pin and a Signal Detected (SD) input pin. Configurations for these I/O pins that may have been previously enabled through other control registers are overridden, except for the bypass select function (bits 6 and 5 of the appropriate bit control registers). When this bit is reset, the remaining bits in this register have no effect on the operation of P3.1 and P3.0.
6	SDIEN	R/W	Signal Detected Interrupt Enable When this bit is set, the SD input generates an interrupt if a transition occurs on the pin. If a transition occurs, the INT# pin asserts and a binary value equal to the address of this register appears in the BCIS register. When this bit is reset, transitions on the signal detected input do not generate an interrupt condition.
5:2	RES	R	Reserved.
1	FB	R/W	Force Bypass This bit controls the P3.1 I/O pin, which is configured as a totem pole output by setting the PBCEN bit. When this bit is set, the force bypass input of a PBC/CRU/SDU function is not enabled and the port bypass circuit is in Normal mode. When this bit is reset, the force bypass function of a PBC/CRU/SDU function is enabled and the port bypass circuit is in Bypass mode. This register bit is automatically cleared when the synchronized and filtered P3.0 input is LOW, resulting in a maximum latency of 400 ns from detection of the loss of a high-speed signal to the de-assertion of the P3.1 output. **Note:** Because all I/O pins on the device power up as inputs with weak internal pull-up resistors, it is possible to define the default state of the force bypass function by using an external pull-down resistor. The default state of the I/O can be determined by reading this register, because the read value of the register bits is always available through an input synchronizer and filter. After the default state is determined, write the default value to the FB bit of this register and set the PBCEN bit to ensure that the port bypass control functions are enabled correctly. Additional writes to this register can enable or disable the force bypass functions at any time as long as the SD input remains HIGH.
0	SD	R/W	Signal Detected When the PBCEN bit is set, this bit becomes a read-only indication of the P3.0 I/O pin, which has been connected to the signal detected output of a PBC/CRU/SDU function. If this bit is set, the signal detect unit detects a high-speed signal. If this bit is reset, the signal detect unit does not detect a high-speed signal.

3.2.18 21h: Port Bypass Control 1 (PBC1)

The following table shows the bit assignments for the Port Bypass Control 1 register. This register functions the same as the Port Bypass Control 0 register except it affects the P3.3 and P3.2 pins.

Register Name: PBC1
Address: 21h
Reset Value: 00XX_XX1Xb

Bit	Bit Label	Access	Description
7	PBCEN	R/W	Port Bypass Control Enable When this bit is set, P3.3 and P3.2 are automatically configured as an FB output pin and an SD input pin. Configurations for these I/O pins that may have been previously enabled through other control registers are overridden, except for the bypass select function (bits 6 and 5 of the appropriate bit control registers). When this bit is reset, the remaining bits in this register have no effect on the operation of P3.3 and P3.2.
6	SDIEN	R/W	Signal Detected Interrupt Enable When this bit is set, the SD input generates an interrupt if a transition occurs on the pin. If a transition occurs, the INT# pin asserts and a binary value equal to the address of this register appears in the BCIS register. When this bit is reset, transitions on the signal detected input do not generate an interrupt condition.
5:2	RES	R	Reserved.
1	FB	R/W	Force Bypass This bit controls the P3.2 I/O pin, which is configured as a totem pole output by setting the PBCEN bit. When this bit is set, the force bypass input of a PBC/CRU/SDU function is not enabled and the port bypass circuit is in Normal mode. When this bit is reset, the force bypass function of a PBC/CRU/SDU function is enabled and the port bypass circuit is in Bypass mode. This register bit is automatically cleared when the synchronized and filtered P3.2 input is LOW, resulting in a maximum latency of 400 ns from detection of the loss of a high-speed signal to the de-assertion of the P3.3 output. **Note:** Because all I/O pins on the device power up as inputs with weak internal pull-up resistors, it is possible to define the default state of the force bypass function by using an external pull-down resistor. The default state of the I/O can be determined by reading this register, because the read value of the register bits is always available through an input synchronizer and filter. After the default state is determined, to ensure that the port bypass control functions are enabled correctly, write the default value to the FB bit of this register and set the PBCEN bit. Additional writes to this register can enable or disable the force bypass functions at any time as long as the SD input remains HIGH.
0	SD	R/W	Signal Detected When the PBCEN bit is set, this bit becomes a read-only indication of the P3.2 I/O pin, which is connected to the signal detected output of a PBC/CRU/SDU function. If this bit is set, the signal detect unit detects a high-speed signal. If this bit is reset, the signal detect unit does not detect a high-speed signal.

3.2.19 22h: Port Bypass Control 2 (PBC2)

The following table shows the bit assignments for the Port Bypass Control 2 register. This register functions the same as the Port Bypass Control 0 register except it affects the P3.5 and P3.4 pins.

Register Name: PBC2
Address: 22h
Reset Value: 00XX_XX1Xb

Bit	Bit Label	Access	Description
7	PBCEN	R/W	Port Bypass Control Enable When this bit is set, P3.5 and P3.4 are automatically configured as an FB output pin and an SD input pin. Configurations for these I/O pins that may have been previously enabled through other control registers are overridden, except for the bypass select function (bits 6 and 5 of the appropriate bit control registers). When this bit is reset, the remaining bits in this register have no effect on the operation of P3.5 and P3.4.
6	SDIEN	R/W	Signal Detected Interrupt Enable When this bit is set, the SD input generates an interrupt if a transition occurs on the pin. If a transition occurs, the INT# pin asserts and a binary value equal to the address of this register appears in the BCIS register. When this bit is reset, transitions on the signal detected input do not generate an interrupt condition.
5:2	RES	R	Reserved.
1	FB	R/W	Force Bypass This bit controls the P3.5 I/O pin, which is configured as a totem pole output by setting the PBCEN bit. When this bit is set, the force bypass input of a PBC/CRU/SDU function is not enabled and the port bypass circuit is in Normal mode. When this bit is reset, the force bypass function of a PBC/CRU/SDU function is enabled and the port bypass circuit is in Bypass mode. This register bit is automatically cleared when the synchronized and filtered P3.4 input is LOW, resulting in a maximum latency of 400 ns from detection of the loss of a high-speed signal to the de-assertion of the P3.5 output. **Note:** Because all I/O pins on the device power up as inputs with weak internal pull-up resistors, it is possible to define the default state of the force bypass function by using an external pull-down resistor. The default state of the I/O can be determined by reading this register, because the read value of the register bits is always available through an input synchronizer and filter. After the default state is determined, write the default value to the FB bit of this register and set the PBCEN bit to ensure that the port bypass control functions are enabled correctly. Additional writes to this register can enable or disable the force bypass functions at any time as long as the SD input remains HIGH.
0	SD	R/W	Signal Detected When the PBCEN bit is set, this bit becomes a read-only indication of the P3.4 I/O pin, which is connected to the signal detected output of a PBC/CRU/SDU function. If this bit is set, the signal detect unit detects a high-speed signal. If this bit is reset, the signal detect unit does not detect a high-speed signal.

3.2.20 23h: Port Bypass Control 3 (PBC3)

The following table shows the bit assignments for the Port Bypass Control 3 register. This register functions the same as the Port Bypass Control 0 register except it affects the P3.7 and P3.6 pins.

Register Name: PBC3
Address: 23h
Reset Value: 00XX_XX1Xb

Bit	Bit Label	Access	Description
7	PBCEN	R/W	Port Bypass Control Enable When this bit is set, P3.7 and P3.6 are automatically configured as an FB output pin and an SD input pin. Configurations for these I/O pins that may have been previously enabled through other control registers are overridden, except for the bypass select function (bits 6 and 5 of the appropriate bit control registers). When this bit is reset, the remaining bits in this register have no effect on the operation of P3.7 and P3.6.
6	SDIEN	R/W	Signal Detected Interrupt Enable When this bit is set, the SD input generates an interrupt if a transition occurs on the pin. If a transition occurs, the INT# pin asserts and a binary value equal to the address of this register appears in the BCIS register. When this bit is reset, transitions on the signal detected input do not generate an interrupt condition.
5:2	RES	R	Reserved.
1	FB	R/W	Force Bypass This bit controls the P3.7 I/O pin, which is configured as a totem pole output by setting the PBCEN bit. When this bit is set, the force bypass input of a PBC/CRU/SDU function is not enabled and the port bypass circuit is in Normal mode. When this bit is reset, the force bypass function of a PBC/CRU/SDU function is enabled and the port bypass circuit is in Bypass mode. This register bit is automatically cleared when the synchronized and filtered P3.6 input is LOW, resulting in a maximum latency of 400 ns from detection of the loss of a high-speed signal to the de-assertion of the P3.7 output. **Note:** Because all I/O pins on the device power up as inputs with weak internal pull-up resistors, it is possible to define the default state of the force bypass function by using an external pull-down resistor. The default state of the I/O can be determined by reading this register, because the read value of the register bits is always available through an input synchronizer and filter. After the default state is determined, write the default value to the FB bit of this register and set the PBCEN bit to ensure that the port bypass control functions are enabled correctly. Additional writes to this register can enable or disable the force bypass functions at any time as long as the SD input remains HIGH.
0	SD	R/W	Signal Detected When the PBCEN bit is set, this bit becomes a read-only indication of the P3.6 I/O pin, which is connected to the signal detected output of a PBC/CRU/SDU function. If this bit is set, the signal detect unit detects a high-speed signal. If this bit is reset, the signal detect unit does not detect a high-speed signal.

3.2.21 24h: Port Bypass Control 4 (PBC4)

The following table shows the bit assignments for the Port Bypass Control 4 register. This register functions the same as the Port Bypass Control 0 register except it affects the P4.1 and P4.0 pins.

Register Name: PBC4
Address: 24h
Reset Value: 00XX_XX1Xb

Bit	Bit Label	Access	Description
7	PBCEN	R/W	Port Bypass Control Enable When this bit is set, P4.1 and P4.0 are automatically configured as an FB output pin and an SD input pin. Configurations for these I/O pins that may have been previously enabled through other control registers are overridden, except for the bypass select function (bits 6 and 5 of the appropriate bit control registers). When this bit is reset, the remaining bits in this register have no effect on the operation of P4.1 and P4.0.
6	SDIEN	R/W	Signal Detected Interrupt Enable When this bit is set, the SD input generates an interrupt if a transition occurs on the pin. If a transition occurs, the INT# pin asserts and a binary value equal to the address of this register appears in the BCIS register. When this bit is reset, transitions on the signal detected input do not generate an interrupt condition.
5:2	RES	R	Reserved.
1	FB	R/W	Force Bypass This bit controls the P4.1 I/O pin, which is configured as a totem pole output by setting the PBCEN bit. When this bit is set, the force bypass input of a PBC/CRU/SDU function is not enabled and the port bypass circuit is in Normal mode. When this bit is reset, the force bypass function of a PBC/CRU/SDU function is enabled and the port bypass circuit is in Bypass mode. This register bit is automatically cleared when the synchronized and filtered P4.0 input is LOW, resulting in a maximum latency of 400 ns from detection of the loss of a high-speed signal to the de-assertion of the P4.1 output. **Note:** Because all I/O pins on the device power up as inputs with weak internal pull-up resistors, it is possible to define the default state of the force bypass function by using an external pull-down resistor. The default state of the I/O can be determined by reading this register, because the read value of the register bits is always available through an input synchronizer and filter. After the default state is determined, write the default value to the FB bit of this register and set the PBCEN bit to ensure that the port bypass control functions are enabled correctly. Additional writes to this register can enable or disable the force bypass functions at any time as long as the SD input remains HIGH.
0	SD	R/W	Signal Detected When the PBCEN bit is set, this bit becomes a read-only indication of the P4.0 I/O pin, which is connected to the signal detected output of a PBC/CRU/SDU function. If this bit is set, the signal detect unit detects a high-speed signal. If this bit is reset, the signal detect unit does not detect a high-speed signal.

3.2.22 25h: Port Bypass Control 5 (PBC5)

The following table shows the bit assignments for the Port Bypass Control 5 register. This register functions the same as the Port Bypass Control 0 register except it affects the P4.3 and P4.2 pins.

Register Name: PBC5
Address: 25h
Reset Value: 00XX_XX1Xb

Bit	Bit Label	Access	Description
7	PBCEN	R/W	Port Bypass Control Enable When this bit is set, P4.3 and P4.2 are automatically configured as an FB output pin and an SD input pin. Configurations for these I/O pins that may have been previously enabled through other control registers are overridden, except for the bypass select function (bits 6 and 5 of the appropriate bit control registers). When this bit is reset, the remaining bits in this register have no effect on the operation of P4.3 and P4.2.
6	SDIEN	R/W	Signal Detected Interrupt Enable When this bit is set, the SD input generates an interrupt if a transition occurs on the pin. If a transition occurs, the INT# pin asserts and a binary value equal to the address of this register appears in the BCIS register. When this bit is reset, transitions on the signal detected input do not generate an interrupt condition.
5:2	RES	R	Reserved.
1	FB	R/W	Force Bypass This bit controls the P4.3 I/O pin, which is configured as a totem pole output by setting the PBCEN bit. When this bit is set, the force bypass input of a PBC/CRU/SDU function is not enabled and the port bypass circuit is in Normal mode. When this bit is reset, the force bypass function of a PBC/CRU/SDU function is enabled and the port bypass circuit is in Bypass mode. This register bit is automatically cleared when the synchronized and filtered P4.2 input is LOW, resulting in a maximum latency of 400 ns from detection of the loss of a high-speed signal to the de-assertion of the P4.3 output. **Note:** Because all I/O pins on the device power up as inputs with weak internal pull-up resistors, it is possible to define the default state of the force bypass function by using an external pull-down resistor. The default state of the I/O can be determined by reading this register, because the read value of the register bits is always available through an input synchronizer and filter. After the default state is determined, write the default value to the FB bit of this register and set the PBCEN bit to ensure that the port bypass control functions are enabled correctly. Additional writes to this register can enable or disable the force bypass functions at any time as long as the SD input remains HIGH.
0	SD	R/W	Signal Detected When the PBCEN bit is set, this bit becomes a read-only indication of the P4.2 I/O pin, which is connected to the signal detected output of a PBC/CRU/SDU function. If this bit is set, the signal detect unit detects a high-speed signal. If this bit is reset, the signal detect unit does not detect a high-speed signal.

3.2.23 26h: Port Bypass Control 6 (PBC6)

The following table shows the bit assignments for the Port Bypass Control 6 register. This register functions the same as the Port Bypass Control 0 register except it affects the P4.5 and P4.4 pins.

Register Name: PBC6
Address: 26h
Reset Value: 00XX_XX1Xb

Bit	Bit Label	Access	Description
7	PBCEN	R/W	Port Bypass Control Enable When this bit is set, P4.5 and P4.4 are automatically configured as an FB output pin and an SD input pin. Configurations for these I/O pins that may have been previously enabled through other control registers are overridden, except for the bypass select function (bits 6 and 5 of the appropriate bit control registers). When this bit is reset, the remaining bits in this register have no effect on the operation of P4.5 and P4.4.
6	SDIEN	R/W	Signal Detected Interrupt Enable When this bit is set, the SD input generates an interrupt if a transition occurs on the pin. If a transition occurs, the INT# pin asserts and a binary value equal to the address of this register appears in the BCIS register. When this bit is reset, transitions on the signal detected input do not generate an interrupt condition.
5:2	RES	R	Reserved.
1	FB	R/W	Force Bypass This bit controls the P4.5 I/O pin, which is configured as a totem pole output by setting the PBCEN bit. When this bit is set, the force bypass input of a PBC/CRU/SDU function is not enabled and the port bypass circuit is in Normal mode. When this bit is reset, the force bypass function of a PBC/CRU/SDU function is enabled and the port bypass circuit is in Bypass mode. This register bit is automatically cleared when the synchronized and filtered P4.4 input is LOW, resulting in a maximum latency of 400 ns from detection of the loss of a high-speed signal to the de-assertion of the P4.5 output. **Note:** Because all I/O pins on the device power up as inputs with weak internal pull-up resistors, it is possible to define the default state of the force bypass function by using an external pull-down resistor. The default state of the I/O can be determined by reading this register, because the read value of the register bits is always available through an input synchronizer and filter. After the default state is determined, write the default value to the FB bit of this register and set the PBCEN bit to ensure that the port bypass control functions are enabled correctly. Additional writes to this register can enable or disable the force bypass functions at any time as long as the SD input remains HIGH.
0	SD	R/W	Signal Detected When the PBCEN bit is set, this bit becomes a read-only indication of the P4.4 I/O pin, which has been connected to the signal detected output of a PBC/CRU/SDU function. If this bit is set, the signal detect unit detects a high-speed signal. If this bit is reset, the signal detect unit does not detect a high-speed signal.

3.2.24 27h: Port Bypass Control 7 (PBC7)

The following table shows the bit assignments for the Port Bypass Control 7 register. This register functions the same as the Port Bypass Control 0 register except it affects the P4.7 and P4.6 pins.

Register Name: PBC7
Address: 27h
Reset Value: 00XX_XX1Xb

Bit	Bit Label	Access	Description
7	PBCEN	R/W	Port Bypass Control Enable When this bit is set, P4.7 and P4.6 are automatically configured as an FB output pin and an SD input pin. Configurations for these I/O pins that may have been previously enabled through other control registers are overridden, except for the bypass select function (bits 6 and 5 of the appropriate bit control registers). When this bit is reset, the remaining bits in this register have no effect on the operation of P4.7 and P4.6.
6	SDIEN	R/W	Signal Detected Interrupt Enable When this bit is set, the SD input generates an interrupt if a transition occurs on the pin. If a transition occurs, the INT# pin asserts and a binary value equal to the address of this register appears in the BCIS register. When this bit is reset, transitions on the signal detected input do not generate an interrupt condition.
5:2	RES	R	Reserved.
1	FB	R/W	Force Bypass This bit controls the P4.7 I/O pin, which is configured as a totem pole output by setting the PBCEN bit. When this bit is set, the force bypass input of a PBC/CRU/SDU function is not enabled and the port bypass circuit is in Normal mode. When this bit is reset, the force bypass function of a PBC/CRU/SDU function is enabled and the port bypass circuit is in Bypass mode. This register bit is automatically cleared when the synchronized and filtered P4.6 input is LOW, resulting in a maximum latency of 400 ns from detection of the loss of a high-speed signal to the de-assertion of the P4.7 output. **Note:** Because all I/O pins on the device power up as inputs with weak internal pull-up resistors, it is possible to define the default state of the force bypass function by using an external pull-down resistor. The default state of the I/O can be determined by reading this register, because the read value of the register bits is always available through an input synchronizer and filter. After the default state is determined, write the default value to the FB bit of this register and set the PBCEN bit to ensure that the port bypass control functions are enabled correctly. Additional writes to this register can enable or disable the force bypass functions at any time as long as the SD input remains HIGH.
0	SD	R/W	Signal Detected When the PBCEN bit is set, this bit becomes a read-only indication of the P4.6 I/O pin, which has been connected to the signal detected output of a PBC/CRU/SDU function. If this bit is set, the signal detect unit detects a high-speed signal. If this bit is reset, the signal detect unit does not detect a high-speed signal.

3.2.25 28h: Port Bypass Control 8 (PBC8)

The following table shows the bit assignments for the Port Bypass Control 8 register. This register functions the same as the Port Bypass Control 0 register except it affects the P5.1 and P5.0 pins.

Register Name: PBC8
Address: 28h
Reset Value: 00XX_XX1Xb

Bit	Bit Label	Access	Description
7	PBCEN	R/W	Port Bypass Control Enable When this bit is set, P5.1 and P5.0 are automatically configured as an FB output pin and an SD input pin. Configurations for these I/O pins that may have been previously enabled through other control registers are overridden, except for the bypass select function (bits 6 and 5 of the appropriate bit control registers). When this bit is reset, the remaining bits in this register have no effect on the operation of P5.1 and P5.0.
6	SDIEN	R/W	Signal Detected Interrupt Enable When this bit is set, the SD input generates an interrupt if a transition occurs on the pin. If a transition occurs, the INT# pin asserts and a binary value equal to the address of this register appears in the BCIS register. When this bit is reset, transitions on the signal detected input do not generate an interrupt condition.
5:2	RES	R	Reserved.
1	FB	R/W	Force Bypass This bit controls the P5.1 I/O pin, which is configured as a totem pole output by setting the PBCEN bit. When this bit is set, the force bypass input of a PBC/CRU/SDU function is not enabled and the port bypass circuit is in Normal mode. When this bit is reset, the force bypass function of a PBC/CRU/SDU function is enabled and the port bypass circuit is in Bypass mode. This register bit is automatically cleared when the synchronized and filtered P5.0 input is LOW, resulting in a maximum latency of 400 ns from detection of the loss of a high-speed signal to the de-assertion of the P5.1 output. **Note:** Because all I/O pins on the device power up as inputs with weak internal pull-up resistors, it is possible to define the default state of the force bypass function by using an external pull-down resistor. The default state of the I/O can be determined by reading this register, because the read value of the register bits is always available through an input synchronizer and filter. After the default state is determined, write the default value to the FB bit of this register and set the PBCEN bit to ensure that the port bypass control functions are enabled correctly. Additional writes to this register can enable or disable the force bypass functions at any time as long as the SD input remains HIGH.
0	SD	R/W	Signal Detected When the PBCEN bit is set, this bit becomes a read-only indication of the P5.0 I/O pin, which is connected to the signal detected output of a PBC/CRU/SDU function. If this bit is set, the signal detect unit detects a high-speed signal. If this bit is reset, the signal detect unit does not detect a high-speed signal.

3.2.26 29h: Port Bypass Control 9 (PBC9)

The following table shows the bit assignments for the Port Bypass Control 9 register. This register functions the same as the Port Bypass Control 0 register except it affects the P5.3 and P5.2 pins.

Register Name: PBC9
Address: 29h
Reset Value: 00XX_XX1Xb

Bit	Bit Label	Access	Description
7	PBCEN	R/W	Port Bypass Control Enable When this bit is set, P5.3 and P5.2 are automatically configured as an FB output pin and an SD input pin. Configurations for these I/O pins that may have been previously enabled through other control registers are overridden, except for the bypass select function (bits 6 and 5 of the appropriate bit control registers). When this bit is reset, the remaining bits in this register have no effect on the operation of P5.3 and P5.2.
6	SDIEN	R/W	Signal Detected Interrupt Enable When this bit is set, the SD input generates an interrupt if a transition occurs on the pin. If a transition occurs, the INT# pin asserts and a binary value equal to the address of this register appears in the BCIS register. When this bit is reset, transitions on the signal detected input do not generate an interrupt condition.
5:2	RES	R	Reserved.
1	FB	R/W	Force Bypass This bit controls the P5.3 I/O pin, which is configured as a totem pole output by setting the PBCEN bit. When this bit is set, the force bypass input of a PBC/CRU/SDU function is not enabled and the port bypass circuit is in Normal mode. When this bit is reset, the force bypass function of a PBC/CRU/SDU function is enabled and the port bypass circuit is in Bypass mode. This register bit is automatically cleared when the synchronized and filtered P5.2 input is LOW, resulting in a maximum latency of 400 ns from detection of the loss of a high-speed signal to the de-assertion of the P5.3 output. **Note:** Because all I/O pins on the device power up as inputs with weak internal pull-up resistors, it is possible to define the default state of the force bypass function by using an external pull-down resistor. The default state of the I/O can be determined by reading this register, because the read value of the register bits is always available through an input synchronizer and filter. After the default state is determined, write the default value to the FB bit of this register and set the PBCEN bit to ensure that the port bypass control functions are enabled correctly. Additional writes to this register can enable or disable the force bypass functions at any time as long as the SD input remains HIGH.
0	SD	R/W	Signal Detected When the PBCEN bit is set, this bit becomes a read-only indication of the P5.2 I/O pin, which is connected to the signal detected output of a PBC/CRU/SDU function. If this bit is set, the signal detect unit detects a high-speed signal. If this bit is reset, the signal detect unit does not detect a high-speed signal.

3.2.27 2Ah: Port Bypass Control 10 (PBC10)

The following table shows the bit assignments for the Port Bypass Control 10 register. This register functions the same as the Port Bypass Control 0 register except it affects the P5.5 and P5.4 pins.

Register Name: PBC10
Address: 2Ah
Reset Value: 00XX_XX1Xb

Bit	Bit Label	Access	Description
7	PBCEN	R/W	Port Bypass Control Enable When this bit is set, P5.5 and P5.4 are automatically configured as an FB output pin and an SD input pin. Configurations for these I/O pins that may have been previously enabled through other control registers are overridden, except for the bypass select function (bits 6 and 5 of the appropriate bit control registers). When this bit is reset, the remaining bits in this register have no effect on the operation of P5.5 and P5.4.
6	SDIEN	R/W	Signal Detected Interrupt Enable When this bit is set, the SD input generates an interrupt if a transition occurs on the pin. If a transition occurs, the INT# pin asserts and a binary value equal to the address of this register appears in the BCIS register. When this bit is reset, transitions on the signal detected input do not generate an interrupt condition.
5:2	RES	R	Reserved.
1	FB	R/W	Force Bypass This bit controls the P5.5 I/O pin, which is configured as a totem pole output by setting the PBCEN bit. When this bit is set, the force bypass input of a PBC/CRU/SDU function is not enabled and the port bypass circuit is in Normal mode. When this bit is reset, the force bypass function of a PBC/CRU/SDU function is enabled and the port bypass circuit is in Bypass mode. This register bit is automatically cleared when the synchronized and filtered P5.4 input is LOW, resulting in a maximum latency of 400 ns from detection of the loss of a high-speed signal to the de-assertion of the P5.5 output. **Note:** Because all I/O pins on the device power up as inputs with weak internal pull-up resistors, it is possible to define the default state of the force bypass function by using an external pull-down resistor. The default state of the I/O can be determined by reading this register, because the read value of the register bits is always available through an input synchronizer and filter. After the default state is determined, write the default value to the FB bit of this register and set the PBCEN bit to ensure that the port bypass control functions are enabled correctly. Additional writes to this register can enable or disable the force bypass functions at any time as long as the SD input remains HIGH.
0	SD	R/W	Signal Detected When the PBCEN bit is set, this bit becomes a read-only indication of the P5.4 I/O pin, which is connected to the signal detected output of a PBC/CRU/SDU function. If this bit is set, the signal detect unit detects a high-speed signal. If this bit is reset, the signal detect unit does not detect a high-speed signal.

3.2.28 2Bh: Port Bypass Control 11 (PBC11)

The following table shows the bit assignments for the Port Bypass Control 11 register. This register functions the same as the Port Bypass Control 0 register except it affects the P5.7 and P5.6 pins.

Register Name: PBC11
Address: 2Bh
Reset Value: 00XX_XX1Xb

Bit	Bit Label	Access	Description
7	PBCEN	R/W	Port Bypass Control Enable When this bit is set, P5.7 and P5.6 are automatically configured as an FB output pin and an SD input pin. Configurations for these I/O pins that may have been previously enabled through other control registers are overridden, except for the bypass select function (bits 6 and 5 of the appropriate bit control registers). When this bit is reset, the remaining bits in this register have no effect on the operation of P5.7 and P5.6.
6	SDIEN	R/W	Signal Detected Interrupt Enable When this bit is set, the SD input generates an interrupt if a transition occurs on the pin. If a transition occurs, the INT# pin asserts and a binary value equal to the address of this register appears in the BCIS register. When this bit is reset, transitions on the signal detected input do not generate an interrupt condition.
5:2	RES	R	Reserved.
1	FB	R/W	Force Bypass This bit controls the P5.7 I/O pin, which is configured as a totem pole output by setting the PBCEN bit. When this bit is set, the force bypass input of a PBC/CRU/SDU function is not enabled and the port bypass circuit is in Normal mode. When this bit is reset, the force bypass function of a PBC/CRU/SDU function is enabled and the port bypass circuit is in Bypass mode. This register bit is automatically cleared when the synchronized and filtered P5.6 input is LOW, resulting in a maximum latency of 400 ns from detection of the loss of a high-speed signal to the de-assertion of the P5.7 output. **Note:** Because all I/O pins on the device power up as inputs with weak internal pull-up resistors, it is possible to define the default state of the force bypass function by using an external pull-down resistor. The default state of the I/O can be determined by reading this register, because the read value of the register bits is always available through an input synchronizer and filter. After the default state is determined, write the default value to the FB bit of this register and set the PBCEN bit to ensure that the port bypass control functions are enabled correctly. Additional writes to this register can enable or disable the force bypass functions at any time as long as the SD input remains HIGH.
0	SD	R/W	Signal Detected When the PBCEN bit is set, this bit becomes a read-only indication of the P5.6 I/O pin, which has been connected to the signal detected output of a PBC/CRU/SDU function. If this bit is set, the signal detect unit detects a high-speed signal. If this bit is reset, the signal detect unit does not detect a high-speed signal.

3.2.29 2Ch: Port Bypass Control 12 (PBC12)

The following table shows the bit assignments for the Port Bypass Control 12 register. This register functions the same as the Port Bypass Control 0 register except it affects the P6.1 and P6.0 pins.

Register Name: PBC12
Address: 2Ch
Reset Value: 00XX_XX1Xb

Bit	Bit Label	Access	Description
7	PBCEN	R/W	Port Bypass Control Enable When this bit is set, P6.1 and P6.0 are automatically configured as an FB output pin and an SD input pin. Configurations for these I/O pins that may have been previously enabled through other control registers are overridden, except for the bypass select function (bits 6 and 5 of the appropriate bit control registers). When this bit is reset, the remaining bits in this register have no effect on the operation of P6.1 and P6.0.
6	SDIEN	R/W	Signal Detected Interrupt Enable When this bit is set, the SD input generates an interrupt if a transition occurs on the pin. If a transition occurs, the INT# pin asserts and a binary value equal to the address of this register appears in the BCIS register. When this bit is reset, transitions on the signal detected input do not generate an interrupt condition.
5:2	RES	R	Reserved.
1	FB	R/W	Force Bypass This bit controls the P6.1 I/O pin, which is configured as a totem pole output by setting the PBCEN bit. When this bit is set, the force bypass input of a PBC/CRU/SDU function is not enabled and the port bypass circuit is in Normal mode. When this bit is reset, the force bypass function of a PBC/CRU/SDU function is enabled and the port bypass circuit is in Bypass mode. This register bit is automatically cleared when the synchronized and filtered P6.0 input is LOW, resulting in a maximum latency of 400 ns from detection of the loss of a high-speed signal to the de-assertion of the P6.1 output. **Note:** Because all I/O pins on the device power up as inputs with weak internal pull-up resistors, it is possible to define the default state of the force bypass function by using an external pull-down resistor. The default state of the I/O can be determined by reading this register, because the read value of the register bits is always available through an input synchronizer and filter. After the default state is determined, write the default value to the FB bit of this register and set the PBCEN bit to ensure that the port bypass control functions are enabled correctly. Additional writes to this register can enable or disable the force bypass functions at any time as long as the SD input remains HIGH.
0	SD	R/W	Signal Detected When the PBCEN bit is set, this bit becomes a read-only indication of the P6.0 I/O pin, which has been connected to the signal detected output of a PBC/CRU/SDU function. If this bit is set, the signal detect unit detects a high-speed signal. If this bit is reset, the signal detect unit does not detect a high-speed signal.

3.2.30 2Dh: Port Bypass Control 13 (PBC13)

The following table shows the bit assignments for the Port Bypass Control 13 register. This register functions the same as the Port Bypass Control 0 register except it affects the P6.3 and P6.2 pins.

Register Name: PBC13
Address: 2Dh
Reset Value: 00XX_XX1Xb

Bit	Bit Label	Access	Description
7	PBCEN	R/W	Port Bypass Control Enable When this bit is set, P6.3 and P6.2 are automatically configured as an FB output pin and an SD input pin. Configurations for these I/O pins that may have been previously enabled through other control registers are overridden, except for the bypass select function (bits 6 and 5 of the appropriate bit control registers). When this bit is reset, the remaining bits in this register have no effect on the operation of P6.3 and P6.2.
6	SDIEN	R/W	Signal Detected Interrupt Enable When this bit is set, the SD input generates an interrupt if a transition occurs on the pin. If a transition occurs, the INT# pin asserts and a binary value equal to the address of this register appears in the BCIS register. When this bit is reset, transitions on the signal detected input do not generate an interrupt condition.
5:2	RES	R	Reserved.
1	FB	R/W	Force Bypass This bit controls the P6.3 I/O pin, which is configured as a totem pole output by setting the PBCEN bit. When this bit is set, the force bypass input of a PBC/CRU/SDU function is not enabled and the port bypass circuit is in Normal mode. When this bit is reset, the force bypass function of a PBC/CRU/SDU function is enabled and the port bypass circuit is in Bypass mode. This register bit is automatically cleared when the synchronized and filtered P6.2 input is LOW, resulting in a maximum latency of 400 ns from detection of the loss of a high-speed signal to the de-assertion of the P6.3 output. **Note:** Because all I/O pins on the device power up as inputs with weak internal pull-up resistors, it is possible to define the default state of the force bypass function by using an external pull-down resistor. The default state of the I/O can be determined by reading this register, because the read value of the register bits is always available through an input synchronizer and filter. After the default state is determined, write the default value to the FB bit of this register and set the PBCEN bit to ensure that the port bypass control functions are enabled correctly. Additional writes to this register can enable or disable the force bypass functions at any time as long as the SD input remains HIGH.
0	SD	R/W	Signal Detected When the PBCEN bit is set, this bit becomes a read-only indication of the P6.2 I/O pin, which has been connected to the signal detected output of a PBC/CRU/SDU function. If this bit is set, the signal detect unit detects a high-speed signal. If this bit is reset, the signal detect unit does not detect a high-speed signal.

3.2.31 2Eh: Port Bypass Control 14 (PBC14)

The following table shows the bit assignments for the Port Bypass Control 14 register. This register functions the same as the Port Bypass Control 0 register except it affects the P6.5 and P6.4 pins.

Register Name: PBC14
Address: 2Eh
Reset Value: 00XX_XX1Xb

Bit	Bit Label	Access	Description
7	PBCEN	R/W	Port Bypass Control Enable When this bit is set, P6.5 and P6.4 are automatically configured as an FB output pin and an SD input pin. Configurations for these I/O pins that may have been previously enabled through other control registers are overridden, except for the bypass select function (bits 6 and 5 of the appropriate bit control registers). When this bit is reset, the remaining bits in this register have no effect on the operation of P6.5 and P6.4.
6	SDIEN	R/W	Signal Detected Interrupt Enable When this bit is set, the SD input generates an interrupt if a transition occurs on the pin. If a transition occurs, the INT# pin asserts and a binary value equal to the address of this register appears in the BCIS register. When this bit is reset, transitions on the signal detected input do not generate an interrupt condition.
5:2	RES	R	Reserved.
1	FB	R/W	Force Bypass This bit controls the P6.5 I/O pin, which is configured as a totem pole output by setting the PBCEN bit. When this bit is set, the force bypass input of a PBC/CRU/SDU function is not enabled and the port bypass circuit is in Normal mode. When this bit is reset, the force bypass function of a PBC/CRU/SDU function is enabled and the port bypass circuit is in Bypass mode. This register bit is automatically cleared when the synchronized and filtered P6.4 input is LOW, resulting in a maximum latency of 400 ns from detection of the loss of a high-speed signal to the de-assertion of the P6.5 output. **Note:** Because all I/O pins on the device power up as inputs with weak internal pull-up resistors, it is possible to define the default state of the force bypass function by using an external pull-down resistor. The default state of the I/O can be determined by reading this register, because the read value of the register bits is always available through an input synchronizer and filter. After the default state is determined, write the default value to the FB bit of this register and set the PBCEN bit to ensure that the port bypass control functions are enabled correctly. Additional writes to this register can enable or disable the force bypass functions at any time as long as the SD input remains HIGH.
0	SD	R/W	Signal Detected When the PBCEN bit is set, this bit becomes a read-only indication of the P6.4 I/O pin, which has been connected to the signal detected output of a PBC/CRU/SDU function. If this bit is set, the signal detect unit detects a high-speed signal. If this bit is reset, the signal detect unit does not detect a high-speed signal.

3.2.32 2Fh: Port Bypass Control 15 (PBC15)

The following table shows the bit assignments for the Port Bypass Control 15 register. This register functions the same as the Port Bypass Control 0 register except it affects the P6.7 and P6.6 pins.

Register Name: PBC15
Address: 2Fh
Reset Value: 00XX_XX1Xb

Bit	Bit Label	Access	Description
7	PBCEN	R/W	Port Bypass Control Enable When this bit is set, P6.7 and P6.6 are automatically configured as an FB output pin and an SD input pin. Configurations for these I/O pins that may have been previously enabled through other control registers are overridden, except for the bypass select function (bits 6 and 5 of the appropriate bit control registers). When this bit is reset, the remaining bits in this register have no effect on the operation of P6.7 and P6.6.
6	SDIEN	R/W	Signal Detected Interrupt Enable When this bit is set, the SD input generates an interrupt if a transition occurs on the pin. If a transition occurs, the INT# pin asserts and a binary value equal to the address of this register appears in the BCIS register. When this bit is reset, transitions on the signal detected input do not generate an interrupt condition.
5:2	RES	R	Reserved.
1	FB	R/W	Force Bypass This bit controls the P6.7 I/O pin, which is configured as a totem pole output by setting the PBCEN bit. When this bit is set, the force bypass input of a PBC/CRU/SDU function is not enabled and the port bypass circuit is in Normal mode. When this bit is reset, the force bypass function of a PBC/CRU/SDU function is enabled and the port bypass circuit is in Bypass mode. This register bit is automatically cleared when the synchronized and filtered P6.6 input is LOW, resulting in a maximum latency of 400 ns from detection of the loss of a high-speed signal to the de-assertion of the P6.7 output. **Note:** Because all I/O pins on the device power up as inputs with weak internal pull-up resistors, it is possible to define the default state of the force bypass function by using an external pull-down resistor. The default state of the I/O can be determined by reading this register, because the read value of the register bits is always available through an input synchronizer and filter. After the default state is determined, write the default value to the FB bit of this register and set the PBCEN bit to ensure that the port bypass control functions are enabled correctly. Additional writes to this register can enable or disable the force bypass functions at any time as long as the SD input remains HIGH.
0	SD	R/W	Signal Detected When the PBCEN bit is set, this bit becomes a read-only indication of the P6.6 I/O pin, which has been connected to the signal detected output of a PBC/CRU/SDU function. If this bit is set, the signal detect unit detects a high-speed signal. If this bit is reset, the signal detect unit does not detect a high-speed signal.

3.2.33 30h: Fan Speed Control 0 (FSC0)

The following table shows the bit assignments for the Fan Speed Control 0 register. This register affects the P2.0 pin.

Register Name: FSC0
Address: 30h
Reset Value: 00XX_XX00b

Bit	Bit Label	Access	Description
7	FSCEN	R/W	Fan Speed Control Enable When this bit is set, P2.0 is automatically configured to provide a fan speed monitoring input. Configurations for this I/O pin that may have been previously enabled through other control registers are overridden, except for the bypass select function (bits 6 and 5 of the appropriate bit control registers). If the appropriate bypass bits are set, the odd-numbered fan speed input pins (P2.1, P2.3, P2.5, or P2.7) are configured as outputs. When this bit is reset, the remaining bits in this register have no effect on the operation of P2.0. When enabled as a fan speed monitoring input, pulses from the fan tachometer output gate an internal 20 kHz clock into an 8-bit counter. A divisor value stored in bits 1 and 0 of this register allow the user to select one of four nominal RPM values based on fan tachometer outputs, which pulse twice per revolution. The FSCC0 register provides the user with an accurate binary fan speed count value that can be used to determine the current RPM value of the fan. Incoming pulses are filtered and conditioned to accommodate the slow rise and fall times typical of fan tachometer outputs. The maximum input signal is limited to a range of V_{SS} to V_{DD}. If this input is supplied from a fan tachometer output that exceeds this range, external components are required to limit the signal to an acceptable range.
6	FSIEN	R/W	Fan Speed Interrupt Enable When this bit is set, the P2.0 input generates an interrupt if the 8-bit counter value is greater than or equal to the count overflow value loaded into the FSCO0 register. If this condition occurs, the INT# pin asserts and a binary value equal to the address of this register appears in the BCIS register. When this bit is reset, the fan speed monitoring logic does not generate an interrupt condition.
5:2	RES	R	Reserved.
1:0	FD1-0	R/W	Fan Divisor These two bits determine the divisor value used to determine the correct range of RPM values supplied to the 8-bit fan speed counter. The available fan divisor values are as follows: FD1 / FD0 / Divisor / Nominal RPM / Decimal Count Value 0 / 0 / 1 / 8000 / 150 (96h) 0 / 1 / 2 / 4000 / 150 (96h) 1 / 0 / 4 / 2000 / 150 (96h) 1 / 1 / 8 / 1000 / 150 (96h) The decimal count value can be calculated using the following equation: Decimal count value = (1,200,000) / (RPM × divisor) Any nominal RPM value can be used in the above equation with the appropriate divisor as long as the maximum non-failure count value does not exceed the limits of an 8-bit counter. Typical applications can consider 60% to 70% of nominal RPM a fan failure, which would result in a decimal count value of 250 (FAh) and 214 (D6h), respectively, at the above stated RPM values.

3.2.34 31h: Fan Speed Count Overflow 0 (FSCO0)

The following table shows the bit assignments for the Fan Speed Count Overflow 0 register. This register affects the P2.0 pin.

Register Name: FSCO0
Address: 31h
Reset Value: 0000_0000b

Bit	Bit Label	Access	Description
7:0	FSCO7-0	R/W	Fan Speed Count Overflow These eight bits are compared to the 8-bit fan speed counter. If the counter exceeds this value, an interrupt is generated. This register should be loaded prior to setting the FSCEN bit in the FSC0 register to avoid generating unintentional interrupts. The overflow count value can be determined using the following equation, where FF% is equal to the percentage of nominal RPM that constitutes a fan failure: Decimal overflow count value = (1,200,000) / (RPM × divisor × FF%) Based on the above equation, a divisor of 8, and a detected fan failure at 70% of nominal RPM, the fan speed monitoring logic can support a low-end nominal RPM of 850. High-end RPM values are basically unlimited; however, counter resolution is diminished above 8000 RPM.

3.2.35 32h: Fan Speed Current Count 0 (FSCC0)

The following table shows the bit assignments for the Fan Speed Current Count 0 register. This register affects the P2.0 pin.

Register Name: FSCC0
Address: 32h
Reset Value: 0000_0000b

Bit	Bit Label	Access	Description
7:0	FSCC7-0	R	These eight bits, when enabled by setting the FSCEN bit in the FSC0 register, provide the user with an accurate binary fan speed count value that can be used to determine the current RPM value of the fan. A minimum of one complete revolution of the fan is required to generate an accurate fan speed count value. The following equation can be used to determine the current RPM value of the fan: RPM = (1,200,000) / (Decimal count value × divisor) When the result of a read of this register is 00h, an accurate fan speed count value is not generated, indicating that the fan has not completed a minimum of one revolution. When the result of a read of this register is FFh, the fan is rotating very slowly or there are no tachometer pulses present. When operating in a polled mode, with the FSIEN bit reset in the FSC0 register, this register is automatically updated with an accurate fan speed count once per revolution of the fan. When operating in an Interrupt mode with the FSIEN bit set in the FSC0 register, this register is automatically updated with an accurate fan speed count, once per revolution of the fan, until an interrupt is generated. After the interrupt is generated, the value remains stable until the interrupt is cleared. When the interrupt is cleared, this register is also cleared, indicating that a valid RPM value is in the process of being generated.

3.2.36 34h: Fan Speed Control 1 (FSC1)

The following table shows the bit assignments for the Fan Speed Control 1 register. This register functions same the Fan Speed Control 0 register except it affects the P2.1 pin.

Register Name: FSC1
Address: 34h
Reset Value: 00XX_XX00b

Bit	Bit Label	Access	Description
7	FSCEN	R/W	Fan Speed Control Enable When this bit is set, P2.1 is automatically configured to provide a fan speed monitoring input. Configurations for this I/O pin that may have been previously enabled through other control registers are overridden, except for the bypass select function (bits 6 and 5 of the appropriate bit control registers). If the appropriate bypass bits are set, the odd-numbered fan speed input pins (P2.1, P2.3, P2.5, or P2.7) are configured as outputs. When this bit is reset, the remaining bits in this register have no effect on the operation of P2.1. When enabled as a fan speed monitoring input, pulses from the fan tachometer output gate an internal 20 kHz clock into an 8-bit counter. A divisor value stored in bits 1 and 0 of this register allow the user to select one of four nominal RPM values based on fan tachometer outputs, which pulse twice per revolution. The FSCC1 register provides the user with an accurate binary fan speed count value that can be used to determine the current RPM value of the fan. Incoming pulses are filtered and conditioned to accommodate the slow rise and fall times typical of fan tachometer outputs. The maximum input signal is limited to a range of V_{SS} to V_{DD}. If this input is supplied from a fan tachometer output that exceeds this range, external components are required to limit the signal to an acceptable range.
6	FSIEN	R/W	Fan Speed Interrupt Enable When this bit is set, the P2.1 input generates an interrupt if the 8-bit counter value is greater than or equal to the count overflow value loaded into the FSCO1 register. If this condition occurs, the INT# pin asserts and a binary value equal to the address of this register appears in the BCIS register. When this bit is reset, the fan speed monitoring logic does not generate an interrupt condition.
5:2	RES	R	Reserved.
1:0	FD1-0	R/W	Fan Divisor These two bits determine the divisor value used to determine the correct range of RPM values supplied to the 8-bit fan speed counter. The available fan divisor values are as follows: FD1 / FD0 / Divisor / Nominal RPM / Decimal Count Value 0 / 0 / 1 / 8000 / 150 (96h) 0 / 1 / 2 / 4000 / 150 (96h) 1 / 0 / 4 / 2000 / 150 (96h) 1 / 1 / 8 / 1000 / 150 (96h) The decimal count value can be calculated using the following equation: Decimal count value = (1,200,000) / (RPM × divisor) Any nominal RPM value can be used in the above equation with the appropriate divisor as long as the maximum non-failure count value does not exceed the limits of an 8-bit counter. Typical applications may consider 60% to 70% of nominal RPM a fan failure, which would result in a decimal count value of 250 (FAh) and 214 (D6h), respectively, at the above stated RPM values.

3.2.37 35h: Fan Speed Count Overflow 1 (FSCO1)

The following table shows the bit assignments for the Fan Speed Count Overflow 1 register. This register functions same the Fan Speed Count Overflow 0 register except it affects the P2.1 pin.

Register Name: FSCO1
Address: 35h
Reset Value: 0000_0000b

Bit	Bit Label	Access	Description
7:0	FSCO7-0	R/W	Fan Speed Count Overflow These eight bits are compared to the 8-bit fan speed counter. If the counter exceeds this value, an interrupt is generated. This register should be loaded prior to setting the FSCEN bit in the FSC1 register to avoid generating unintentional interrupts. The overflow count value can be determined using the following equation, where FF% is equal to the percentage of nominal RPM that constitutes a fan failure: Decimal overflow count value = (1,200,000) / (RPM × divisor × FF%) Based on the above equation, a divisor of 8, and a detected fan failure at 70% of nominal RPM, the fan speed monitoring logic can support a low-end nominal RPM of 850. High-end RPM values are basically unlimited; however, counter resolution is diminished above 8000 RPM.

3.2.38 36h: Fan Speed Current Count 1 (FSCC1)

The following table shows the bit assignments for the Fan Speed Current Count 1 register. This register functions same the Fan Speed Current Count 0 register except it affects the P2.1 pin.

Register Name: FSCC1
Address: 36h
Reset Value: 0000_0000b

Bit	Bit Label	Access	Description
7:0	FSCC7-0	R	These eight bits, when enabled by setting the FSCEN bit in the FSC1 register, provide the user with an accurate binary fan speed count value that can be used to determine the current RPM value of the fan. A minimum of one complete revolution of the fan is required to generate an accurate fan speed count value. The following equation can be used to determine the current RPM value of the fan: RPM = (1,200,000) / (Decimal count value × divisor) When the result of a read of this register is 00h, an accurate fan speed count value is not generated, indicating that the fan has not completed a minimum of one revolution. When the result of a read of this register is FFh, the fan is rotating very slowly or there are no tachometer pulses present. When operating in a polled mode, with the FSIEN bit reset in the FSC1 register, this register is automatically updated with an accurate fan speed count once per revolution of the fan. When operating in an Interrupt mode with the FSIEN bit set in the FSC1 register, this register is automatically updated with an accurate fan speed count, once per revolution of the fan, until an interrupt is generated. After the interrupt is generated, the value remains stable until the interrupt is cleared. When the interrupt is cleared, this register is also cleared, indicating that a valid RPM value is in the process of being generated.

3.2.39 38h: Fan Speed Control 2 (FSC2)

The following table shows the bit assignments for the Fan Speed Control 2 register. This register functions same the Fan Speed Control 0 register except it affects the P2.2 pin.

Register Name: FSC2
Address: 38h
Reset Value: 00XX_XX00b

Bit	Bit Label	Access	Description
7	FSCEN	R/W	Fan Speed Control Enable When this bit is set, P2.2 is automatically configured to provide a fan speed monitoring input. Configurations for this I/O pin that may have been previously enabled through other control registers are overridden, except for the bypass select function (bits 6 and 5 of the appropriate bit control registers). If the appropriate bypass bits are set, the odd-numbered fan speed input pins (P2.1, P2.3, P2.5, or P2.7) are configured as outputs. When this bit is reset, the remaining bits in this register have no effect on the operation of P2.2. When enabled as a fan speed monitoring input, pulses from the fan tachometer output gate an internal 20 kHz clock into an 8-bit counter. A divisor value stored in bits 1 and 0 of this register allow the user to select one of four nominal RPM values based on fan tachometer outputs, which pulse twice per revolution. The FSCC2 register provides the user with an accurate binary fan speed count value that can be used to determine the current RPM value of the fan. Incoming pulses are filtered and conditioned to accommodate the slow rise and fall times typical of fan tachometer outputs. The maximum input signal is limited to a range of V_{SS} to V_{DD}. If this input is supplied from a fan tachometer output that exceeds this range, external components are required to limit the signal to an acceptable range.
6	FSIEN	R/W	Fan Speed Interrupt Enable When this bit is set, the P2.2 input generates an interrupt if the 8-bit counter value is greater than or equal to the count overflow value loaded into the FSCO2 register. If this condition occurs, the INT# pin asserts and a binary value equal to the address of this register appears in the BCIS register. When this bit is reset, the fan speed monitoring logic does not generate an interrupt condition.
5:2	RES	R	Reserved.
1:0	FD1-0	R/W	Fan Divisor These two bits determine the divisor value used to determine the correct range of RPM values supplied to the 8-bit fan speed counter. The available fan divisor values are as follows: FD1 / FD0 / Divisor / Nominal RPM / Decimal Count Value 0 / 0 / 1 / 8000 / 150 (96h) 0 / 1 / 2 / 4000 / 150 (96h) 1 / 0 / 4 / 2000 / 150 (96h) 1 / 1 / 8 / 1000 / 150 (96h) The decimal count value can be calculated using the following equation: Decimal count value = (1,200,000) / (RPM × divisor) Any nominal RPM value can be used in the above equation with the appropriate divisor as long as the maximum non-failure count value does not exceed the limits of an 8-bit counter. Typical applications may consider 60% to 70% of nominal RPM a fan failure, which would result in a decimal count value of 250 (FAh) and 214 (D6h), respectively, at the above stated RPM values.

3.2.40 39h: Fan Speed Count Overflow 2 (FSCO2)

The following table shows the bit assignments for the Fan Speed Count Overflow 2 register. This register functions same the Fan Speed Count Overflow 0 register except it affects the P2.2 pin.

Register Name: FSCO2
Address: 39h
Reset Value: 0000_0000b

Bit	Bit Label	Access	Description
7:0	FSCO7-0	R/W	Fan Speed Count Overflow These eight bits are compared to the 8-bit fan speed counter. If the counter exceeds this value, an interrupt is generated. This register should be loaded prior to setting the FSCEN bit in the FSC2 register to avoid generating unintentional interrupts. The overflow count value can be determined using the following equation, where FF% is equal to the percentage of nominal RPM that constitutes a fan failure: Decimal overflow count value = (1,200,000) / (RPM × divisor × FF%) Based on the above equation, a divisor of 8, and a detected fan failure at 70% of nominal RPM, the fan speed monitoring logic can support a low-end nominal RPM of 850. High-end RPM values are basically unlimited; however, counter resolution is diminished above 8000 RPM.

3.2.41 3Ah: Fan Speed Current Count 2 (FSCC2)

The following table shows the bit assignments for the Fan Speed Current Count 2 register. This register functions same the Fan Speed Current Count 0 register except it affects the P2.2 pin.

Register Name: FSCC2
Address: 3Ah
Reset Value: 0000_0000b

Bit	Bit Label	Access	Description
7:0	FSCC7-0	R	These eight bits, when enabled by setting the FSCEN bit in the FSC2 register, provide the user with an accurate binary fan speed count value that can be used to determine the current RPM value of the fan. A minimum of one complete revolution of the fan is required to generate an accurate fan speed count value. The following equation can be used to determine the current RPM value of the fan: RPM = (1,200,000) / (Decimal count value × divisor) When the result of a read of this register is 00h, an accurate fan speed count value is not generated, indicating that the fan has not completed a minimum of one revolution. When the result of a read of this register is FFh, the fan is rotating very slowly or there are no tachometer pulses present. When operating in a polled mode, with the FSIEN bit reset in the FSC2 register, this register is automatically updated with an accurate fan speed count once per revolution of the fan. When operating in an Interrupt mode with the FSIEN bit set in the FSC2 register, this register is automatically updated with an accurate fan speed count, once per revolution of the fan, until an interrupt is generated. Once the interrupt is generated, the value remains stable until the interrupt is cleared. When the interrupt is cleared, this register is also cleared, indicating that a valid RPM value is in the process of being generated.

3.2.42 3Ch: Fan Speed Control 3 (FSC3)

The following table shows the bit assignments for the Fan Speed Control 3 register. This register functions same the Fan Speed Control 0 register except it affects the P2.3 pin.

Register Name: FSC3
Address: 3Ch
Reset Value: 00XX_XX00b

Bit	Bit Label	Access	Description
7	FSCEN	R/W	Fan Speed Control Enable When this bit is set, P2.3 is automatically configured to provide a fan speed monitoring input. Configurations for this I/O pin that may have been previously enabled through other control registers are overridden, except for the bypass select function (bits 6 and 5 of the appropriate bit control registers). If the appropriate bypass bits are set, the odd-numbered fan speed input pins (P2.1, P2.3, P2.5, or P2.7) are configured as outputs. When this bit is reset, the remaining bits in this register have no effect on the operation of P2.3. When enabled as a fan speed monitoring input, pulses from the fan tachometer output gate an internal 20 kHz clock into an 8-bit counter. A divisor value stored in bits 1 and 0 of this register allow the user to select one of four nominal RPM values based on fan tachometer outputs, which pulse twice per revolution. The FSCC3 register provides the user with an accurate binary fan speed count value that can be used to determine the current RPM value of the fan. Incoming pulses are filtered and conditioned to accommodate the slow rise and fall times that are typical of fan tachometer outputs. The maximum input signal is limited to a range of V_{SS} to V_{DD}. If this input is supplied from a fan tachometer output that exceeds this range, external components are required to limit the signal to an acceptable range.
6	FSIEN	R/W	Fan Speed Interrupt Enable When this bit is set, the P2.3 input generates an interrupt if the 8-bit counter value is greater than or equal to the count overflow value loaded into the FSCO3 register. If this condition occurs, the INT# pin asserts and a binary value equal to the address of this register appears in the BCIS register. When this bit is reset, the fan speed monitoring logic does not generate an interrupt condition.
5:2	RES	R	Reserved.
1:0	FD1-0	R/W	Fan Divisor These two bits determine the divisor value used to determine the correct range of RPM values supplied to the 8-bit fan speed counter. The available fan divisor values are as follows: FD1 / FD0 / Divisor / Nominal RPM / Decimal Count Value 0 / 0 / 1 / 8000 / 150 (96h) 0 / 1 / 2 / 4000 / 150 (96h) 1 / 0 / 4 / 2000 / 150 (96h) 1 / 1 / 8 / 1000 / 150 (96h) The decimal count value can be calculated using the following equation: Decimal count value = (1,200,000) / (RPM × divisor) Any nominal RPM value can be used in the above equation with the appropriate divisor as long as the maximum non-failure count value does not exceed the limits of an 8-bit counter. Typical applications may consider 60% to 70% of nominal RPM a fan failure, which would result in a decimal count value of 250 (FAh) and 214 (D6h), respectively, at the above stated RPM values.

3.2.43 3Dh: Fan Speed Count Overflow 3 (FSCO3)

The following table shows the bit assignments for the Fan Speed Count Overflow 3 register. This register functions same the Fan Speed Count Overflow 0 register except it affects the P2.3 pin.

Register Name: FSCO3
Address: 3Dh
Reset Value: 0000_0000b

Bit	Bit Label	Access	Description
7:0	FSCO7-0	R/W	Fan Speed Count Overflow These eight bits are compared to the 8-bit fan speed counter. If the counter exceeds this value, an interrupt is generated. This register should be loaded prior to setting the FSCEN bit in the FSC3 register to avoid generating unintentional interrupts. The overflow count value can be determined using the following equation, where FF% is equal to the percentage of nominal RPM that constitutes a fan failure: Decimal overflow count value = (1,200,000) / (RPM × divisor × FF%) Based on the above equation, a divisor of 8, and a detected fan failure at 70% of nominal RPM, the fan speed monitoring logic can support a low-end nominal RPM of 850. High-end RPM values are basically unlimited; however, counter resolution is diminished above 8000 RPM.

3.2.44 3Eh: Fan Speed Current Count 3 (FSCC3)

The following table shows the bit assignments for the Fan Speed Current Count 3 register. This register functions same the Fan Speed Current Count 0 register except it affects the P2.3 pin.

Register Name: FSCC3
Address: 3Eh
Reset Value: 0000_0000b

Bit	Bit Label	Access	Description
7:0	FSCC7-0	R	These eight bits, when enabled by setting the FSCEN bit in the FSC3 register provide the user with an accurate binary fan speed count value that can be used to determine the current RPM value of the fan. A minimum of one complete revolution of the fan is required to generate an accurate fan speed count value. The following equation can be used to determine the current RPM value of the fan: RPM = (1,200,000) / (Decimal count value × divisor) When the result of a read of this register is 00h, an accurate fan speed count value has not been generated indicating that the fan has not completed a minimum of one revolution. When the result of a read of this register is FFh, the fan is rotating very slowly or there are no tachometer pulses present. When operating in a polled mode, with the FSIEN bit reset in the FSC3 register, this register is automatically updated with an accurate fan speed count once per revolution of the fan. When operating in an Interrupt mode with the FSIEN bit set in the FSC3 register, this register is automatically updated with an accurate fan speed count, once per revolution of the fan, until an interrupt is generated. After the interrupt is generated, the value remains stable until the interrupt is cleared. When the interrupt is cleared, this register is also cleared, indicating that a valid RPM value is in the process of being generated.

3.2.45 40h: Fan Speed Control 4 (FSC4)

The following table shows the bit assignments for the Fan Speed Control 4 register. This register functions same the Fan Speed Control 0 register except it affects the P2.4 pin.

Register Name: FSC4
Address: 40h
Reset Value: 00XX_XX00b

Bit	Bit Label	Access	Description
7	FSCEN	R/W	Fan Speed Control Enable When this bit is set, P2.4 is automatically configured to provide a fan speed monitoring input. Configurations for this I/O pin that may have been previously enabled through other control registers are overridden, except for the bypass select function (bits 6 and 5 of the appropriate bit control registers). If the appropriate bypass bits are set, the odd-numbered fan speed input pins (P2.1, P2.3, P2.5, or P2.7) are configured as outputs. When this bit is reset, the remaining bits in this register have no effect on the operation of P2.4. When enabled as a fan speed monitoring input, pulses from the fan tachometer output gate an internal 20 kHz clock into an 8-bit counter. A divisor value stored in bits 1 and 0 of this register allow the user to select one of four nominal RPM values based on fan tachometer outputs, which pulse twice per revolution. The FSCC4 register provides the user with an accurate binary fan speed count value that can be used to determine the current RPM value of the fan. Incoming pulses are filtered and conditioned to accommodate the slow rise and fall times typical of fan tachometer outputs. The maximum input signal is limited to a range of V_{SS} to V_{DD}. If this input is supplied from a fan tachometer output that exceeds this range, external components are required to limit the signal to an acceptable range.
6	FSIEN	R/W	Fan Speed Interrupt Enable When this bit is set, the P2.4 input generates an interrupt if the 8-bit counter value is greater than or equal to the count overflow value loaded into the FSCO4 register. If this condition occurs, the INT# pin asserts and a binary value equal to the address of this register appears in the BCIS register. When this bit is reset, the fan speed monitoring logic does not generate an interrupt condition.
5:2	RES	R	Reserved.
1:0	FD1-0	R/W	Fan Divisor These two bits determine the divisor value used to determine the correct range of RPM values supplied to the 8-bit fan speed counter. The available fan divisor values are as follows: FD1 / FD0 / Divisor / Nominal RPM / Decimal Count Value 0 / 0 / 1 / 8000 / 150 (96h) 0 / 1 / 2 / 4000 / 150 (96h) 1 / 0 / 4 / 2000 / 150 (96h) 1 / 1 / 8 / 1000 / 150 (96h) The decimal count value can be calculated using the following equation: Decimal count value = (1,200,000) / (RPM × divisor) Any nominal RPM value can be used in the above equation with the appropriate divisor as long as the maximum non-failure count value does not exceed the limits of an 8-bit counter. Typical applications may consider 60% to 70% of nominal RPM a fan failure, which would result in a decimal count value of 250 (FAh) and 214 (D6h), respectively, at the above stated RPM values.

3.2.46 41h: Fan Speed Count Overflow 4 (FSCO4)

The following table shows the bit assignments for the Fan Speed Count Overflow 4 register. This register functions same the Fan Speed Count Overflow 0 register except it affects the P2.4 pin.

Register Name: FSCO4
Address: 41h
Reset Value: 0000_0000b

Bit	Bit Label	Access	Description
7:0	FSCO7-0	R/W	Fan Speed Count Overflow These eight bits are compared to the 8-bit fan speed counter. If the counter exceeds this value, an interrupt is generated. This register should be loaded prior to setting the FSCEN bit in the FSC4 register to avoid generating unintentional interrupts. The overflow count value can be determined using the following equation, where FF% is equal to the percentage of nominal RPM, which constitutes a fan failure: Decimal overflow count value = (1,200,000) / (RPM × divisor × FF%) Based on the above equation, a divisor of 8, and a detected fan failure at 70% of nominal RPM, the fan speed monitoring logic can support a low-end nominal RPM of 850. High-end RPM values are basically unlimited; however, counter resolution is diminished above 8000 RPM.

3.2.47 42h: Fan Speed Current Count 4 (FSCC4)

The following table shows the bit assignments for the Fan Speed Current Count 4 register. This register functions the same as Fan Speed Current Count 0 register except it affects the P2.4 pin.

Register Name: FSCC4
Address: 42h
Reset Value: 0000_0000b

Bit	Bit Label	Access	Description
7:0	FSCC7-0	R	These eight bits, when enabled by setting the FSCEN bit in the FSC4 register, provide the user with an accurate binary fan speed count value that can be used to determine the current RPM value of the fan. A minimum of one complete revolution of the fan is required to generate an accurate fan speed count value. The following equation can be used to determine the current RPM value of the fan: RPM = (1,200,000) / (Decimal count value × divisor) When the result of a read of this register is 00h, an accurate fan speed count value is not generated, indicating that the fan has not completed a minimum of one revolution. When the result of a read of this register is FFh, the fan is rotating very slowly or there are no tachometer pulses present. When operating in a polled mode, with the FSIEN bit reset in the FSC4 register, this register is automatically updated with an accurate fan speed count once per revolution of the fan. When operating in an Interrupt mode with the FSIEN bit set in the FSC4 register, this register is automatically updated with an accurate fan speed count, once per revolution of the fan, until an interrupt is generated. After the interrupt is generated, the value remains stable until the interrupt is cleared. When the interrupt is cleared, this register is also cleared, indicating that a valid RPM value is in the process of being generated.

3.2.48 44h: Fan Speed Control 5 (FSC5)

The following table shows the bit assignments for the Fan Speed Control 5 register. This register functions same the Fan Speed Control 0 register, except it affects the P2.5 pin.

Register Name: FSC5
Address: 44h
Reset Value: 00XX_XX00b

Bit	Bit Label	Access	Description
7	FSCEN	R/W	Fan Speed Control Enable When this bit is set, P2.5 is automatically configured to provide a fan speed monitoring input. Configurations for this I/O pin that may have been previously enabled through other control registers are overridden, except for the bypass select function (bits 6 and 5 of the appropriate bit control registers). If the appropriate bypass bits are set, the odd-numbered fan speed input pins (P2.1, P2.3, P2.5, or P2.7) are configured as outputs. When this bit is reset, the remaining bits in this register have no effect on the operation of P2.5. When enabled as a fan speed monitoring input, pulses from the fan tachometer output gate an internal 20 kHz clock into an 8-bit counter. A divisor value stored in bits 1 and 0 of this register allow the user to select one of four nominal RPM values based on fan tachometer outputs, which pulse twice per revolution. The FSCC5 register provides the user with an accurate binary fan speed count value that can be used to determine the current RPM value of the fan. Incoming pulses are filtered and conditioned to accommodate the slow rise and fall times typical of fan tachometer outputs. The maximum input signal is limited to a range of V_{SS} to V_{DD}. If this input is supplied from a fan tachometer output that exceeds this range, external components are required to limit the signal to an acceptable range.
6	FSIEN	R/W	Fan Speed Interrupt Enable When this bit is set, the P2.5 input generates an interrupt if the 8-bit counter value is greater than or equal to the count overflow value loaded into the FSCO5 register. If this condition occurs, the INT# pin asserts and a binary value equal to the address of this register appears in the BCIS register. When this bit is reset, the fan speed monitoring logic does not generate an interrupt condition.
5:2	RES	R	Reserved.
1:0	FD1-0	R/W	Fan Divisor These two bits determine the divisor value used to determine the correct range of RPM values supplied to the 8-bit fan speed counter. The available fan divisor values are as follows: FD1 / FD0 / Divisor / Nominal RPM / Decimal Count Value 0 / 0 / 1 / 8000 / 150 (96h) 0 / 1 / 2 / 4000 / 150 (96h) 1 / 0 / 4 / 2000 / 150 (96h) 1 / 1 / 8 / 1000 / 150 (96h) The decimal count value can be calculated using the following equation: Decimal count value = (1,200,000) / (RPM × divisor) Any nominal RPM value can be used in the above equation with the appropriate divisor as long as the maximum non-failure count value does not exceed the limits of an 8-bit counter. Typical applications may consider 60% to 70% of nominal RPM a fan failure, which would result in a decimal count value of 250 (FAh) and 214 (D6h), respectively, at the above stated RPM values.

3.2.49 45h: Fan Speed Count Overflow 5 (FSCO5)

The following table shows the bit assignments for the Fan Speed Count Overflow 5 register. This register functions same the Fan Speed Count Overflow 0 register except it affects the P2.5 pin.

Register Name: FSCO5
Address: 45h
Reset Value: 0000_0000b

Bit	Bit Label	Access	Description
7:0	FSCO7-0	R/W	Fan Speed Count Overflow These eight bits are compared to the 8-bit fan speed counter. If the counter exceeds this value, an interrupt is generated. This register should be loaded prior to setting the FSCEN bit in the FSC5 register to avoid generating unintentional interrupts. The overflow count value can be determined using the following equation, where FF% is equal to the percentage of nominal RPM, which constitutes a fan failure: Decimal overflow count value = (1,200,000) / (RPM × divisor × FF%) Based on the above equation, a divisor of 8, and a detected fan failure at 70% of nominal RPM, the fan speed monitoring logic can support a low-end nominal RPM of 850. High-end RPM values are basically unlimited; however, counter resolution is diminished above 8000 RPM.

3.2.50 46h: Fan Speed Current Count 5 (FSCC5)

The following table shows the bit assignments for the Fan Speed Current Count 5 register. This register functions the same as Fan Speed Current Count 0 register except it affects the P2.5 pin.

Register Name: FSCC5
Address: 46h
Reset Value: 0000_0000b

Bit	Bit Label	Access	Description
7:0	FSCC7-0	R	These eight bits, when enabled by setting the FSCEN bit in the FSC5 register, provide the user with an accurate binary fan speed count value that can be used to determine the current RPM value of the fan. A minimum of one complete revolution of the fan is required to generate an accurate fan speed count value. The following equation can be used to determine the current RPM value of the fan: RPM = (1,200,000)/(Decimal count value × divisor) When the result of a read of this register is 00h, an accurate fan speed count value is not generated, indicating that the fan has not completed a minimum of one revolution. When the result of a read of this register is FFh, the fan is rotating very slowly or there are no tachometer pulses present. When operating in a polled mode, with the FSIEN bit reset in the FSC5 register, this register is automatically updated with an accurate fan speed count once per revolution of the fan. When operating in an Interrupt mode with the FSIEN bit set in the FSC5 register, this register is automatically updated with an accurate fan speed count, once per revolution of the fan until an interrupt is generated. After the interrupt is generated, the value remains stable until the interrupt is cleared. When the interrupt is cleared, this register is also be cleared, indicating that a valid RPM value is in the process of being generated.

3.2.51 48h: Fan Speed Control 6 (FSC6)

The following table shows the bit assignments for the Fan Speed Control 6 register. This register functions same the Fan Speed Control 0 register except it affects the P2.6 pin.

Register Name: FSC6
Address: 48h
Reset Value: 00XX_XX00b

Bit	Bit Label	Access	Description
7	FSCEN	R/W	Fan Speed Control Enable When this bit is set, P2.6 is automatically configured to provide a fan speed monitoring input. Configurations for this I/O pin that may have been previously enabled through other control registers are overridden, except for the bypass select function (bits 6 and 5 of the appropriate bit control registers). If the appropriate bypass bits are set, the odd-numbered fan speed input pins (P2.1, P2.3, P2.5, or P2.7) are configured as outputs. When this bit is reset, the remaining bits in this register have no effect on the operation of P2.6. When enabled as a fan speed monitoring input, pulses from the fan tachometer output gate an internal 20 kHz clock into an 8-bit counter. A divisor value stored in bits 1 and 0 of this register allow the user to select one of four nominal RPM values based on fan tachometer outputs, which pulse twice per revolution. The FSCC6 register provides the user with an accurate binary fan speed count value that can be used to determine the current RPM value of the fan. Incoming pulses are filtered and conditioned to accommodate the slow rise and fall times typical of fan tachometer outputs. The maximum input signal is limited to a range of V_{SS} to V_{DD}. If this input is supplied from a fan tachometer output that exceeds this range, external components are required to limit the signal to an acceptable range.
6	FSIEN	R/W	Fan Speed Interrupt Enable When this bit is set, the P2.6 input generates an interrupt if the 8-bit counter value is greater than or equal to the count overflow value loaded into the FSCO6 register. If this condition occurs, the INT# pin asserts and a binary value equal to the address of this register appears in the BCIS register. When this bit is reset, the fan speed monitoring logic will not generate an interrupt condition.
5:2	RES	R	Reserved.
1:0	FD1-0	R/W	Fan Divisor These two bits determine the divisor value used to determine the correct range of RPM values supplied to the 8-bit fan speed counter. The available fan divisor values are as follows: FD1 FD0 Divisor Nominal RPM Decimal Count Value 0 0 1 8000 150 (96h) 0 1 2 4000 150 (96h) 1 0 4 2000 150 (96h) 1 1 8 1000 150 (96h) The decimal count value can be calculated using the following equation: Decimal count value = (1,200,000) / (RPM × divisor) Any nominal RPM value can be used in the above equation with the appropriate divisor as long as the maximum non-failure count value does not exceed the limits of an 8-bit counter. Typical applications may consider 60% to 70% of nominal RPM a fan failure, which would result in a decimal count value of 250 (FAh) and 214 (D6h), respectively, at the above stated RPM values.

3.2.52 49h: Fan Speed Count Overflow 6 (FSCO6)

The following table shows the bit assignments for the Fan Speed Count Overflow 6 register. This register functions same the Fan Speed Count Overflow 0 register except it affects the P2.6 pin.

Register Name: FSCO6
Address: 49h
Reset Value: 0000_0000b

Bit	Bit Label	Access	Description
7:0	FSCO7-0	R/W	Fan Speed Count Overflow These eight bits are compared to the 8-bit fan speed counter. If the counter exceeds this value, an interrupt is generated. This register should be loaded prior to setting the FSCEN bit in the FSC6 register to avoid generating unintentional interrupts. The overflow count value can be determined using the following equation, where FF% is equal to the percentage of nominal RPM that constitutes a fan failure: Decimal overflow count value = (1,200,000) / (RPM × divisor × FF%) Based on the above equation, a divisor of 8, and a detected fan failure at 70% of nominal RPM, the fan speed monitoring logic can support a low-end nominal RPM of 850. High-end RPM values are basically unlimited; however, counter resolution is diminished above 8000 RPM.

3.2.53 4Ah: Fan Speed Current Count 6 (FSCC6)

The following table shows the bit assignments for the Fan Speed Current Count 6 register. This register functions the same as Fan Speed Current Count 0 register except it affects the P2.6 pin.

Register Name: FSCC6
Address: 4Ah
Reset Value: 0000_0000b

Bit	Bit Label	Access	Description
7:0	FSCC7-0	R	These eight bits, when enabled by setting the FSCEN bit in the FSC6 register, provide the user with an accurate binary fan speed count value that can be used to determine the current RPM value of the fan. A minimum of one complete revolution of the fan is required to generate an accurate fan speed count value. The following equation can be used to determine the current RPM value of the fan: RPM = (1,200,000) /(Decimal count value × divisor) When the result of a read of this register is 00h, an accurate fan speed count value is not generated, indicating that the fan has not completed a minimum of one revolution. When the result of a read of this register is FFh, the fan is rotating very slowly or no tachometer pulses are present. When operating in a polled mode, with the FSIEN bit reset in the FSC6 register, this register is automatically updated with an accurate fan speed count once per revolution of the fan. When operating in an Interrupt mode with the FSIEN bit set in the FSC6 register, this register is automatically updated with an accurate fan speed count, once per revolution of the fan, until an interrupt is generated. After the interrupt is generated, the value remains stable until the interrupt is cleared. When the interrupt is cleared, this register is also cleared, indicating that a valid RPM value is in the process of being generated.

3.2.54 4Ch: Fan Speed Control 7 (FSC7)

The following table shows the bit assignments for the Fan Speed Control 7 register. This register functions same the Fan Speed Control 0 register except it affects the P2.7 pin.

Register Name: FSC7
Address: 4Ch
Reset Value: 00XX_XX00b

Bit	Bit Label	Access	Description
7	FSCEN	R/W	Fan Speed Control Enable When this bit is set, P2.7 is automatically configured to provide a fan speed monitoring input. Configurations for this I/O pin that may have been previously enabled through other control registers are overridden, except for the bypass select function (bits 6 and 5 of the appropriate bit control registers). If the appropriate bypass bits are set, the odd-numbered fan speed input pins (P2.1, P2.3, P2.5, or P2.7) are configured as outputs. When this bit is reset, the remaining bits in this register have no effect on the operation of P2.7. When enabled as a fan speed monitoring input, pulses from the fan tachometer output gate an internal 20 kHz clock into an 8-bit counter. A divisor value stored in bits 1 and 0 of this register allow the user to select one of four nominal RPM values based on fan tachometer outputs, which pulse twice per revolution. The FSCC7 register provides the user with an accurate binary fan speed count value that can be used to determine the current RPM value of the fan. Incoming pulses are filtered and conditioned to accommodate the slow rise and fall times typical of fan tachometer outputs. The maximum input signal is limited to a range of V_{SS} to V_{DD}. If this input is supplied from a fan tachometer output that exceeds this range, external components are required to limit the signal to an acceptable range.
6	FSIEN	R/W	Fan Speed Interrupt Enable When this bit is set, the P2.7 input generates an interrupt if the 8-bit counter value is greater than or equal to the count overflow value loaded into the FSCO7 register. If this condition occurs, the INT# pin asserts and a binary value equal to the address of this register appears in the BCIS register. When this bit is reset, the fan speed monitoring logic does not generate an interrupt condition.
5:2	RES	R	Reserved.
1:0	FD1-0	R/W	Fan Divisor These two bits determine the divisor value used to determine the correct range of RPM values supplied to the 8-bit fan speed counter. The available fan divisor values are as follows: FD1 FD0 Divisor Nominal RPM Decimal Count Value 0 0 1 8000 150 (96h) 0 1 2 4000 150 (96h) 1 0 4 2000 150 (96h) 1 1 8 1000 150 (96h) The decimal count value can be calculated using the following equation: Decimal count value = (1,200,000) / (RPM × divisor) Any nominal RPM value can be used in the above equation with the appropriate divisor as long as the maximum non-failure count value does not exceed the limits of an 8-bit counter. Typical applications may consider 60% to 70% of nominal RPM a fan failure, which would result in a decimal count value of 250 (FAh) and 214 (D6h), respectively, at the above stated RPM values.

3.2.55 4Dh: Fan Speed Count Overflow 7 (FSCO7)

The following table shows the bit assignments for the Fan Speed Count Overflow 7 register. This register functions same the Fan Speed Count Overflow 0 register except it affects the P2.7 pin.

Register Name: FSCO7
Address: 4Dh
Reset Value: 0000_0000b

Bit	Bit Label	Access	Description
7:0	FSCO7-0	R/W	Fan Speed Count Overflow These eight bits are compared to the 8-bit fan speed counter. If the counter exceeds this value, an interrupt is generated. This register should be loaded prior to setting the FSCEN bit in the FSC7 register to avoid generating unintentional interrupts. The overflow count value can be determined using the following equation, where FF% is equal to the percentage of nominal RPM that constitutes a fan failure: Decimal overflow count value = (1,200,000) / (RPM × divisor × FF%) Based on the above equation, a divisor of 8, and a detected fan failure at 70% of nominal RPM, the fan speed monitoring logic can support a low-end nominal RPM of 850. High-end RPM values are basically unlimited; however, counter resolution is diminished above 8000 RPM.

3.2.56 4Eh: Fan Speed Current Count 7 (FSCC7)

The following table shows the bit assignments for the Fan Speed Current Count 7 register. This register functions the same as Fan Speed Current Count 0 except it affects the P2.7 pin.

Register Name: FSCC7
Address: 4Eh
Reset Value: 0000_0000b

Bit	Bit Label	Access	Description
7:0	FSCC7-0	R	These eight bits, when enabled by setting the FSCEN bit in the FSC7 register, provide the user with an accurate binary fan speed count value that can be used to determine the current RPM value of the fan. A minimum of one complete revolution of the fan is required to generate an accurate fan speed count value. The following equation can be used to determine the current RPM value of the fan: RPM = (1,200,000) / (Decimal count value × divisor) When the result of a read of this register is 00h, an accurate fan speed count value is not generated, indicating that the fan has not completed a minimum of one revolution. When the result of a read of this register is FFh, the fan is rotating very slowly or no tachometer pulses are present. When operating in a polled mode, with the FSIEN bit reset in the FSC7 register, this register is automatically updated with an accurate fan speed count once per revolution of the fan. When operating in an Interrupt mode with the FSIEN bit set in the FSC7 register, this register is automatically updated with an accurate fan speed count, once per revolution of the fan, until an interrupt is generated. After the interrupt is generated, the value remains stable until the interrupt is cleared. When the interrupt is cleared, this register is also cleared, indicating that a valid RPM value is in the process of being generated.

3.2.57 70h: Pulse Train Control 00 (PTC00)

This register, along with the PTC01 register, provides a user-programmable LED flashing pulse train. The user can adjust the pulse duration, the pulse train length, and the on/off time to derive a specific visual indication. The PTC00 register provides eight of the twelve bits available in the programmable pulse train. The PTC01 register contains two bits of pulse-width programmability, two bits of pulse train length programmability, and the remaining four bits of the programmable pulse train.

As an example, the pulse train can be used to develop a visual heartbeat indication by programming the PTC00 register with a 45h and the PTC01 register with a C1h. This combination develops a pulse train with two blinks followed by a gap with the on times of the LED equal to 125 ms.

If the default values of this register or the PTC01 register are modified, and synchronization to other LED flash rates is desired, the SYNC# pin must be enabled. To enable the SYNC# pin, tie the SYNCEN pin to V_{DD}, connect an external 10 kΩ pull-up resistor to the SYNC# pin, and place the proper synchronization value in bits 3:0 of the Clock Select Control register. For information on the Clock Select Control register, see "FDh: Clock Select Control (CSC)," page 111.

The following table shows the bit assignments for the Pulse Train Control 00 register.

Register Name: PTC00
Address: 70h
Reset Value: 0000_0000b

Bit	Bit Label	Access	Description
7:0	PT7-0	R/W	Pulse Train These eight bits are the first bits shifted out from 0 to 7 and define the on/off time for the flash rate. 1: defines LED on time. 0: defines LED off time.

3.2.58 71h: Pulse Train Control 01 (PTC01)

This register, along with the PTC00 register, provides a user-programmable LED flashing pulse train. The user can adjust the pulse duration, the pulse train length, and the on/off time to derive a specific visual indication. The PTC00 register provides eight of the twelve bits available in the programmable pulse train. The PTC01 register contains two bits of pulse-width programmability, two bits of pulse train length programmability, and the remaining four bits of the programmable pulse train.

As an example, the pulse train can be used to develop a visual heartbeat indication by programming the PTC00 register with a 45h and the PTC01 register with a C1h. This combination develops a pulse train with two blinks followed by a gap with the on times of the LED equal to 125 ms.

If the default values of this register or the PTC00 register are modified, and synchronization to other LED flash rates is desired, the SYNC# pin must be enabled. To enable the SYNC# pin, tie the SYNCEN pin to V_{DD}, connect an external 10 kΩ pull-up resistor to the SYNC# pin, and place the proper synchronization value in bits 3:0 of the Clock Select Control register. For information on the Clock Select Control register, see "FDh: Clock Select Control (CSC)," page 111.

The following table shows the bit assignments for the Pulse Train Control 01 register.

Register Name: PTC01
Address: 71h
Reset Value: 0000_0000b

Bit	Bit Label	Access	Description
7:6	TPW1-0	R/W	Train Pulse Width These two bits define the pulse width of each of the pulse train bits. The available pulse widths are as follows: TPW1 / TPW0 / Train Pulse Width 0 / 0 / 41.67 ms 0 / 1 / 55.55 ms 1 / 0 / 83.33 ms 1 / 1 / 125 ms
5:4	PTL1-0	R/W	Pulse Train Length These two bits define the pulse-train length, which is the number of pulse train bits that is shifted out before returning to bit 0. The available pulse train lengths are as follows: PTL1 / PTL0 / Pulse-Train Length 0 / 0 / 12 pulse train bits from 0 to 11 0 / 1 / 10 pulse train bits from 0 to 9 1 / 0 / 9 pulse train bits from 0 to 8 1 / 1 / 8 pulse train bits from 0 to 7
3:0	PT11-8	R/W	Pulse Train These four bits are the last bits shifted out from 0 to 3 and define the on/off time for the flash rate. 1: defines LED on time. 0: defines LED off time.

3.2.59 72h: Pulse Train Control 10 (PTC10)

This register, along with the PTC11 register, provides a user-programmable LED flashing pulse train. The user can adjust the pulse duration, the pulse train length, and the on/off time to derive a specific visual indication. The PTC10 register provides eight of the twelve bits available in the programmable pulse train. The PTC11 register contains two bits of pulse-width programmability, two bits of pulse train length programmability, and the remaining four bits of the programmable pulse train.

As an example, the pulse train can be used to develop a visual heartbeat indication by programming the PTC10 register with a 45h and the PTC11 register with a C1h. This combination develops a pulse train with two blinks followed by a gap with the on times of the LED equal to 125 ms.

If the default values of this register or the PTC11 register are modified, and synchronization to other LED flash rates is desired, the SYNC# pin must be enabled. To enable the SYNC# pin, tie the SYNCEN pin to V_{DD}, connect an external 10 kΩ pull-up resistor to the SYNC# pin, and place the proper synchronization value in bits 3:0 of the Clock Select Control register. For information on the Clock Select Control register, see "FDh: Clock Select Control (CSC)," page 111.

The following table shows the bit assignments for the Pulse Train Control 10 register.

Register Name: PTC10
Address: 72h
Reset Value: 0000_0000b

Bit	Bit Label	Access	Description
7:0	PT7-0	R/W	Pulse Train These eight bits are the first bits shifted out from 0 to 7 and define the on/off time for the flash rate. 1: defines LED on time 0: defines LED off time.

3.2.60 73h: Pulse Train Control 11 (PTC11)

This register, along with the PTC10 register, provides a user-programmable LED flashing pulse train. The user can adjust the pulse duration, the pulse train length, and the on/off time to derive a specific visual indication. The PTC10 register provides eight of the twelve bits available in the programmable pulse train. The PTC11 register contains two bits of pulse-width programmability, two bits of pulse train length programmability, and the remaining four bits of the programmable pulse train.

As an example, the pulse train can be used to develop a visual heartbeat indication by programming the PTC10 register with a 45h and the PTC11 register with a C1h. This combination develops a pulse train with two blinks followed by a gap with the on times of the LED equal to 125 ms.

If the default values of this register or the PTC10 register are modified, and synchronization to other LED flash rates is desired, the SYNC# pin must be enabled. To enable the SYNC# pin, tie the SYNCEN pin to V_{DD}, connect an external 10 kΩ pull-up resistor to the SYNC# pin, and place the proper synchronization value in bits 3:0 of the Clock Select Control register. For information on the Clock Select Control register, see "FDh: Clock Select Control (CSC)," page 111.

The following table shows the bit assignments for the Pulse Train Control 11 register.

Register Name: PTC11
Address: 73h
Reset Value: 0000_0000b

Bit	Bit Label	Access	Description
7:6	TPW1-0	R/W	Train Pulse Width These two bits define the pulse width of each of the pulse train bits. The available pulse widths are as follows: TPW1 TPW0 Train Pulse Width 0 0 41.67 ms 0 1 55.55 ms 1 0 83.33 ms 1 1 125 ms
5:4	PTL1-0	R/W	Pulse Train Length These two bits define the pulse train length, which is the number of pulse train bits that is shifted out before returning to bit 0. The available pulse train lengths are as follows: PTL1 PTL0 Pulse Train Length 0 0 12 pulse train bits from 0 to 11 0 1 10 pulse train bits from 0 to 9 1 0 9 pulse train bits from 0 to 8 1 1 8 pulse train bits from 0 to 7
3:0	PT11-8	R/W	Pulse Train These four bits are the last bits shifted out from 0 to 3 and define the on/off time for the flash rate. 1: defines LED on time. 0: defines LED off time.

3.2.61 74h: Pulse Train Control 20 (PTC20)

This register, along with the PTC21 register, provides a user-programmable LED flashing pulse train. The user can adjust the pulse duration, the pulse train length, and the on/off time to derive a specific visual indication. The PTC20 register provides eight of the twelve bits available in the programmable pulse train. The PTC21 register contains two bits of pulse-width programmability, two bits of pulse train length programmability, and the remaining four bits of the programmable pulse train.

As an example, the pulse train can be used to develop a visual heartbeat indication by programming the PTC20 register with a 45h and the PTC21 register with a C1h. This combination develops a pulse train with two blinks followed by a gap with the on times of the LED equal to 125 ms.

If the default values of this register or the PTC21 register are modified, and synchronization to other LED flash rates is desired, the SYNC# pin must be enabled. To enable the SYNC# pin, tie the SYNCEN pin to V_{DD}, connect an external 10 kΩ pull-up resistor to the SYNC# pin, and place the proper synchronization value in bits 3:0 of the Clock Select Control register. For information on the Clock Select Control register, see "FDh: Clock Select Control (CSC)," page 111.

The following table shows the bit assignments for the Pulse Train Control 20 register.

Register Name: PTC20
Address: 74h
Reset Value: 0000_0000b

Bit	Bit Label	Access	Description
7:0	PT7-0	R/W	Pulse Train These eight bits are the first bits shifted out from 0 to 7 and define the on/off time for the flash rate. 1: defines LED on time 0: defines LED off time.

3.2.62 75h: Pulse Train Control 21 (PTC21)

This register, along with the PTC20 register, provides a user-programmable LED flashing pulse train. The user can adjust the pulse duration, the pulse train length, and the on/off time to derive a specific visual indication. The PTC20 register provides eight of the twelve bits available in the programmable pulse train. The PTC21 register contains two bits of pulse-width programmability, two bits of pulse train length programmability, and the remaining four bits of the programmable pulse train.

As an example, the pulse train can be used to develop a visual heartbeat indication by programming the PTC20 register with a 45h and the PTC21 register with a C1h. This combination develops a pulse train with two blinks followed by a gap with the on times of the LED equal to 125 ms.

If the default values of this register or the PTC20 register are modified, and synchronization to other LED flash rates is desired, the SYNC# pin must be enabled. To enable the SYNC# pin, tie the SYNCEN pin to V_{DD}, connect an external 10 kΩ pull-up resistor to the SYNC# pin, and place the proper synchronization value in bits 3:0 of the Clock Select Control register. For information on the Clock Select Control register, see "FDh: Clock Select Control (CSC)," page 111.

The following table shows the bit assignments for the Pulse Train Control 21 register.

Register Name: PTC21
Address: 75h
Reset Value: 0000_0000b

Bit	Bit Label	Access	Description
7:6	TPW1-0	R/W	Train Pulse Width These two bits define the pulse width of each of the pulse train bits. The available pulse widths are as follows: TPW1 / TPW0 / Train Pulse Width 0 / 0 / 41.67 ms 0 / 1 / 55.55 ms 1 / 0 / 83.33 ms 1 / 1 / 125 ms
5:4	PTL1-0	R/W	Pulse Train Length These two bits define the pulse train length, which is the number of pulse train bits that is shifted out before returning to bit 0. The available pulse train lengths are as follows: PTL1 / PTL0 / Pulse Train Length 0 / 0 / 12 pulse train bits from 0 to 11 0 / 1 / 10 pulse train bits from 0 to 9 1 / 0 / 9 pulse train bits from 0 to 8 1 / 1 / 8 pulse train bits from 0 to 7
3:0	PT11-8	R/W	Pulse Train These four bits are the last bits shifted out from 0 to 3 and define the on/off time for the flash rate. 1: defines LED on time. 0: defines LED off time.

3.2.63 76h: Pulse Train Control 30 (PTC30)

This register, along with the PTC31 register, provides a user-programmable LED flashing pulse train. The user can adjust the pulse duration, the pulse train length, and the on/off time to derive a specific visual indication. The PTC30 register provides eight of the twelve bits available in the programmable pulse train. The PTC31 register contains two bits of pulse-width programmability, two bits of pulse train length programmability, and the remaining four bits of the programmable pulse train.

As an example, the pulse train can be used to develop a visual heartbeat indication by programming the PTC30 register with a 45h and the PTC31 register with a C1h. This combination develops a pulse train with two blinks followed by a gap with the on times of the LED equal to 125 ms.

If the default values of this register or the PTC31 register are modified, and synchronization to other LED flash rates is desired, the SYNC# pin must be enabled. To enable the SYNC# pin, tie the SYNCEN pin to V_{DD}, connect an external 10 kΩ pull-up resistor to the SYNC# pin, and place the proper synchronization value in bits 3:0 of the Clock Select Control register. For information on the Clock Select Control register, see "FDh: Clock Select Control (CSC)," page 111.

The following table shows the bit assignments for the Pulse Train Control 30 register.

Register Name: PTC30
Address: 76h
Reset Value: 0000_0000b

Bit	Bit Label	Access	Description
7:0	PT7-0	R/W	Pulse Train These eight bits are the first bits shifted out from 0 to 7 and define the on/off time for the flash rate. 1: defines LED on time. 0: defines LED off time.

3.2.64 77h: Pulse Train Control 31 (PTC31)

This register, along with the PTC30 register, provides a user-programmable LED flashing pulse train. The user can adjust the pulse duration, the pulse train length, and the on/off time to derive a specific visual indication. The PTC30 register provides eight of the twelve bits available in the programmable pulse train. The PTC31 register contains two bits of pulse-width programmability, two bits of pulse train length programmability, and the remaining four bits of the programmable pulse train.

As an example, the pulse train can be used to develop a visual heartbeat indication by programming the PTC30 register with a 45h and the PTC31 register with a C1h. This combination develops a pulse train with two blinks followed by a gap with the on times of the LED equal to 125 ms.

If the default values of this register or the PTC30 register are modified, and synchronization to other LED flash rates is desired, the SYNC# pin must be enabled. To enable the SYNC# pin, tie the SYNCEN pin to V_{DD}, connect an external 10 kΩ pull-up resistor to the SYNC# pin, and place the proper synchronization value in bits 3:0 of the Clock Select Control register. For information on the Clock Select Control register, see "FDh: Clock Select Control (CSC)," page 111.

The following table shows the bit assignments for the Pulse Train Control 31 register.

Register Name: PTC31
Address: 77h
Reset Value: 0000_0000b

Bit	Bit Label	Access	Description
7:6	TPW1-0	R/W	Train Pulse Width These two bits define the pulse width of each of the pulse train bits.The available pulse widths are as follows: TPW1 / TPW0 / Train Pulse Width 0 / 0 / 41.67 ms 0 / 1 / 55.55 ms 1 / 0 / 83.33 ms 1 / 1 / 125 ms
5:4	PTL1-0	R/W	Pulse Train Length These two bits define the pulse train length, which is the number of pulse train bits that is shifted out before returning to bit 0. The available pulse train lengths are as follows: PTL1 / PTL0 / Pulse Train Length 0 / 0 / 12 pulse train bits from 0 to 11 0 / 1 / 10 pulse train bits from 0 to 9 1 / 0 / 9 pulse train bits from 0 to 8 1 / 1 / 8 pulse train bits from 0 to 7
3:0	PT11-8	R/W	Pulse Train These four bits are the last bits shifted out from 0 to 3 and define the on/off time for the flash rate. 1: defines LED on time. 0: defines LED off time.

3.2.65 78h: Pulse Train Control 40 (PTC40)

This register, along with the PTC41 register, provides a user-programmable LED flashing pulse train. The user can adjust the pulse duration, the pulse train length and the on/off time to derive a specific visual indication. The PTC40 register provides eight of the twelve bits available in the programmable pulse train. The PTC41 register contains two bits of pulse-width programmability, two bits of pulse train length programmability, and the remaining four bits of the programmable pulse train.

As an example, the pulse train can be used to develop a visual heartbeat indication by programming the PTC40 register with a 45h and the PTC41 register with a 01h. This combination develops a pulse train with two blinks followed by a gap with the on times of the LED equal to 166.67 ms.

If the default values of this register or the PTC41 register are modified, and synchronization to other LED flash rates is desired, the SYNC# pin must be enabled. To enable the SYNC# pin, tie the SYNCEN pin to V_{DD}, connect an external 10 kΩ pull-up resistor to the SYNC# pin, and place the proper synchronization value in bits 3:0 of the Clock Select Control register. For information on the Clock Select Control register, see "FDh: Clock Select Control (CSC)," page 111.

The following table shows the bit assignments for the Pulse Train Control 40 register.

Register Name: PTC40
Address: 78h
Reset Value: 0000_0000b

Bit	Bit Label	Access	Description
7:0	PT7-0	R/W	Pulse Train These eight bits are the first bits shifted out from 0 to 7 and define the on/off time for the flash rate. 1: defines LED on time. 0: defines LED off time.

3.2.66 79h: Pulse Train Control 41 (PTC41)

This register, along with the PTC40 register, provides a user-programmable LED flashing pulse train. The user can adjust the pulse duration, the pulse train length, and the on/off time to derive a specific visual indication. The PTC40 register provides eight of the twelve bits available in the programmable pulse train. The PTC41 register contains two bits of pulse-width programmability, two bits of pulse train length programmability, and the remaining four bits of the programmable pulse train.

As an example, the pulse train can be used to develop a visual heartbeat indication by programming the PTC40 register with a 45h and the PTC41 register with a 01h. This combination develops a pulse train with two blinks followed by a gap with the on times of the LED equal to 166.67 ms.

If the default values of this register or the PTC40 register are modified, and synchronization to other LED flash rates is desired, the SYNC# pin must be enabled. To enable the SYNC# pin, tie the SYNCEN pin to V_{DD}, connect an external 10 kΩ pull-up resistor to the SYNC# pin, and place the proper synchronization value in bits 3:0 of the Clock Select Control register. For information on the Clock Select Control register, see "FDh: Clock Select Control (CSC)," page 111.

The following table shows the bit assignments for the Pulse Train Control 41 register.

Register Name: PTC41
Address: 79h
Reset Value: 0000_0000b

Bit	Bit Label	Access	Description
7:6	TPW1-0	R/W	Train Pulse Width These two bits define the pulse width of each of the pulse train bits. The available pulse widths are as follows: TPW1 / TPW0 / Train Pulse Width 0 / 0 / 41.67 ms 0 / 1 / 55.55 ms 1 / 0 / 83.33 ms 1 / 1 / 125 ms
5:4	PTL1-0	R/W	Pulse Train Length These two bits define the pulse train length, which is the number of pulse train bits that is shifted out before returning to bit 0. The available pulse train lengths are as follows: PTL1 / PTL0 / Pulse Train Length 0 / 0 / 12 pulse train bits from 0 to 11 0 / 1 / 10 pulse train bits from 0 to 9 1 / 0 / 9 pulse train bits from 0 to 8 1 / 1 / 8 pulse train bits from 0 to 7
3:0	PT11-8	R/W	Pulse Train These four bits are the last bits shifted out from 0 to 3 and define the on/off time for the flash rate. 1: defines LED on time. 0: defines LED off time.

3.2.67 7Ah: Pulse Train Control 50 (PTC50)

This register, along with the PTC51 register, provides a user-programmable LED flashing pulse train. The user can adjust the pulse duration, the pulse train length, and the on/off time to derive a specific visual indication. The PTC50 register provides eight of the twelve bits available in the programmable pulse train. The PTC51 register contains two bits of pulse-width programmability, two bits of pulse train length programmability, and the remaining four bits of the programmable pulse train.

As an example, the pulse train can be used to develop a visual heartbeat indication by programming the PTC50 register with a 45h and the PTC51 register with a 01h. This combination develops a pulse train with two blinks followed by a gap with the on times of the LED equal to 166.67 ms.

If the default values of this register or the PTC51 register are modified, and synchronization to other LED flash rates is desired, the SYNC# pin must be enabled. To enable the SYNC# pin, tie the SYNCEN pin to V_{DD}, connect an external 10 kΩ pull-up resistor to the SYNC# pin, and place the proper synchronization value in bits 3:0 of the Clock Select Control register. For information on the Clock Select Control register, see "FDh: Clock Select Control (CSC)," page 111.

The following table shows the bit assignments for the Pulse Train Control 50 register.

Register Name: PTC50
Address: 7Ah
Reset Value: 0000_0000b

Bit	Bit Label	Access	Description
7:0	PT7-0	R/W	Pulse Train These eight bits are the first bits shifted out from 0 to 7 and define the on/off time for the flash rate. 1: defines LED on time. 0: defines LED off time.

3.2.68 7Bh: Pulse Train Control 51 (PTC51)

This register, along with the PTC50 register, provides a user-programmable LED flashing pulse train. The user can adjust the pulse duration, the pulse train length, and the on/off time to derive a specific visual indication. The PTC50 register provides eight of the twelve bits available in the programmable pulse train. The PTC51 register contains two bits of pulse-width programmability, two bits of pulse train length programmability, and the remaining four bits of the programmable pulse train.

As an example, the pulse train can be used to develop a visual heartbeat indication by programming the PTC50 register with a 45h and the PTC51 register with a 01h. This combination develops a pulse train with two blinks followed by a gap with the on times of the LED equal to 166.67 ms.

If the default values of this register or the PTC50 register are modified, and synchronization to other LED flash rates is desired, the SYNC# pin must be enabled. To enable the SYNC# pin, tie the SYNCEN pin to V_{DD}, connect an external 10 kΩ pull-up resistor to the SYNC# pin, and place the proper synchronization value in bits 3:0 of the Clock Select Control register. For information on the Clock Select Control register, see "FDh: Clock Select Control (CSC)," page 111.

The following table shows the bit assignments for the Pulse Train Control 51 register.)

Register Name: PTC51
Address: 7Bh
Reset Value: 0000_0000b

Bit	Bit Label	Access	Description
7:6	TPW1-0	R/W	Train Pulse Width These two bits define the pulse width of each of the pulse train bits. The available pulse widths are as follows: TPW1 TPW0 Train Pulse Width 0 0 41.67 ms 0 1 55.55 ms 1 0 83.33 ms 1 1 125 ms
5:4	PTL1-0	R/W	Pulse Train Length These two bits define the pulse train length, which is the number of pulse train bits that is shifted out before returning to bit 0. The available pulse train lengths are as follows: PTL1 PTL0 Pulse Train Length 0 0 12 pulse train bits from 0 to 11 0 1 10 pulse train bits from 0 to 9 1 0 9 pulse train bits from 0 to 8 1 1 8 pulse train bits from 0 to 7
3:0	PT11-8	R/W	Pulse Train These four bits are the last bits shifted out from 0 to 3 and define the on/off time for the flash rate. 1: defines LED on time. 0: defines LED off time.

3.2.69 7Ch: Pulse Train Control 60 (PTC60)

This register, along with the PTC61 register, provides a user-programmable LED flashing pulse train. The user can adjust the pulse duration, the pulse train length and the on/off time to derive a specific visual indication. The PTC60 register provides eight of the twelve bits available in the programmable pulse train. The PTC61 register contains two bits of pulse-width programmability, two bits of pulse train length programmability, and the remaining four bits of the programmable pulse train.

As an example, the pulse train can be used to develop a visual heartbeat indication by programming the PTC60 register with a 45h and the PTC61 register with a 01h. This combination develops a pulse train with two blinks followed by a gap with the on times of the LED equal to 166.67 ms.

If the default values of this register or the PTC61 register are modified, and synchronization to other LED flash rates is desired, the SYNC# pin must be enabled. To enable the SYNC# pin, tie the SYNCEN pin to V_{DD}, connect an external 10 kΩ pull-up resistor to the SYNC# pin, and place the proper synchronization value in bits 3:0 of the Clock Select Control register. For information on the Clock Select Control register, see "FDh: Clock Select Control (CSC)," page 111.

The following table shows the bit assignments for the Pulse Train Control 60 register.

Register Name: PTC60
Address: 7Ch
Reset Value: 0000_0000b

Bit	Bit Label	Access	Description
7:0	PT7-0	R/W	Pulse Train These eight bits are the first bits shifted out from 0 to 7 and define the on/off time for the flash rate. 1: defines LED on time. 0: defines LED off time.

3.2.70 7Dh: Pulse Train Control 61 (PTC61)

This register, along with the PTC60 register, provides a user-programmable LED flashing pulse train. The user can adjust the pulse duration, the pulse train length and the on/off time to derive a specific visual indication. The PTC60 register provides eight of the twelve bits available in the programmable pulse train. The PTC61 register contains two bits of pulse-width programmability, two bits of pulse train length programmability, and the remaining four bits of the programmable pulse train.

As an example, the pulse train can be used to develop a visual heartbeat indication by programming the PTC60 register with a 45h and the PTC61 register with a 01h. This combination develops a pulse train with two blinks followed by a gap with the on times of the LED equal to 166.67 ms.

If the default values of this register or the PTC60 register are modified, and synchronization to other LED flash rates is desired, the SYNC# pin must be enabled. To enable the SYNC# pin, tie the SYNCEN pin to V_{DD}, connect an external 10 kΩ pull-up resistor to the SYNC# pin, and place the proper synchronization value in bits 3:0 of the Clock Select Control register. For information on the Clock Select Control register, see "FDh: Clock Select Control (CSC)," page 111.

The following table shows the bit assignments for the Pulse Train Control 61 register.

Register Name: PTC61
Address: 7Dh
Reset Value: 0000_0000b

Bit	Bit Label	Access	Description
7:6	TPW1-0	R/W	Train Pulse Width These two bits define the pulse width of each of the pulse train bits. The available pulse widths are as follows: TPW1 / TPW0 / Train Pulse Width 0 / 0 / 41.67 ms 0 / 1 / 55.55 ms 1 / 0 / 83.33 ms 1 / 1 / 125 ms
5:4	PTL1-0	R/W	Pulse Train Length These two bits define the pulse train length, which is the number of pulse train bits that is shifted out before returning to bit 0. The available pulse train lengths are as follows: PTL1 / PTL0 / Pulse Train Length 0 / 0 / 12 pulse train bits from 0 to 11 0 / 1 / 10 pulse train bits from 0 to 9 1 / 0 / 9 pulse train bits from 0 to 8 1 / 1 / 8 pulse train bits from 0 to 7
3:0	PT11-8	R/W	Pulse Train These four bits are the last bits shifted out from 0 to 3 and define the on/off time for the flash rate. 1: defines LED on time. 0: defines LED off time.

3.2.71 7Eh: Pulse Train Control 70 (PTC70)

This register, along with the PTC71 register, provides a user-programmable LED flashing pulse train. The user can adjust the pulse duration, the pulse train length, and the on/off time to derive a specific visual indication. The PTC70 register provides eight of the twelve bits available in the programmable pulse train. The PTC71 register contains two bits of pulse-width programmability, two bits of pulse train length programmability, and the remaining four bits of the programmable pulse train.

As an example, the pulse train can be used to develop a visual heartbeat indication by programming the PTC70 register with a 45h and the PTC71 register with a 01h. This combination develops a pulse train with two blinks followed by a gap with the on times of the LED equal to 166.67 ms.

If the default values of this register or the PTC71 register are modified, and synchronization to other LED flash rates is desired, the SYNC# pin must be enabled. To enable the SYNC# pin, tie the SYNCEN pin to V_{DD}, connect an external 10 kΩ pull-up resistor to the SYNC# pin, and place the proper synchronization value in bits 3:0 of the Clock Select Control register. For information on the Clock Select Control register, see "FDh: Clock Select Control (CSC)," page 111.

The following table shows the bit assignments for the Pulse Train Control 71 register.

Register Name: PTC70
Address: 7Eh
Reset Value: 0000_0000b

Bit	Bit Label	Access	Description
7:0	PT7-0	R/W	Pulse Train These eight bits are the first bits shifted out from 0 to 7 and define the on/off time for the flash rate. 1: defines LED on time. 0: defines LED off time.

3.2.72 7Fh: Pulse Train Control 71 (PTC71)

This register, along with the PTC70 register, provides a user-programmable LED flashing pulse train. The user can adjust the pulse duration, the pulse train length, and the on/off time to derive a specific visual indication. The PTC70 register provides eight of the twelve bits available in the programmable pulse train. The PTC71 register contains two bits of pulse-width programmability, two bits of pulse train length programmability, and the remaining four bits of the programmable pulse train.

As an example, the pulse train can be used to develop a visual heartbeat indication by programming the PTC70 register with a 45h and the PTC71 register with a 01h. This combination develops a pulse train with two blinks followed by a gap with the on times of the LED equal to 166.67 ms.

If the default values of this register or the PTC70 register are modified, and synchronization to other LED flash rates is desired, the SYNC# pin must be enabled. To enable the SYNC# pin, tie the SYNCEN pin to V_{DD}, connect an external 10 kΩ pull-up resistor to the SYNC# pin, and place the proper synchronization value in bits 3:0 of the Clock Select Control register. For information on the Clock Select Control register, see "FDh: Clock Select Control (CSC)," page 111.

The following table shows the bit assignments for the Pulse Train Control 71 register.

Register Name: PTC71
Address: 7Fh
Reset Value: 0000_0000b

Bit	Bit Label	Access	Description
7:6	TPW1-0	R/W	Train Pulse Width These two bits define the pulse width of each of the pulse train bits. The available pulse widths are as follows: TPW1 / TPW0 / Train Pulse Width 0 / 0 / 41.67 ms 0 / 1 / 55.55 ms 1 / 0 / 83.33 ms 1 / 1 / 125 ms
5:4	PTL1-0	R/W	Pulse Train Length These two bits define the pulse train length, which is the number of pulse train bits that is shifted out before returning to bit 0. The available pulse train lengths are as follows: PTL1 / PTL0 / Pulse Train Length 0 / 0 / 12 pulse train bits from 0 to 11 0 / 1 / 10 pulse train bits from 0 to 9 1 / 0 / 9 pulse train bits from 0 to 8 1 / 1 / 8 pulse train bits from 0 to 7
3:0	PT11-8	R/W	Pulse Train These four bits are the last bits shifted out from 0 to 3 and define the on/off time for the flash rate. 1: defines LED on time. 0: defines LED off time.

3.2.73 80h-87h: Bit Control Port 0 (BCP00-BCP07)

These eight registers provide individual bit control for the Port 0 I/O pins. All register bits are identical from a control and status perspective, with the only difference being the individual I/O pin controlled and the presence of the bypass function. The Data Direction (bit 1) and General-Purpose Data (bit 0) bits are effectively the same bits found in the DDP0 and GPD0 registers, with parallel read and write paths.

The following table shows the bit assignments for the Bit Control Port 0 registers.

Register Name: BCP00-BCP07
Address: 80h - 87h
Reset Value: 0000_001Xb

Bit	Bit Label	Access	Description
7	PTE	R/W	Pulse Train Enable This bit, along with the FS (Function Select) bits, enables one of eight pulse train circuits controlled by the pulse train registers PTC00 through PTC71 (70h through 7Fh) as the output drive function for this I/O pin. When this bit is set, the FS bits select one of eight pulse train circuits instead of the normal fixed-rate LED flashing circuits or the normal output drive mode. For the various LED drive control modes, see Table 5, page 80. After a reset or power on, this bit is cleared.
6:5	BYP1-0	R/W	Bypass Select These two bits determine the bypass function of the odd-numbered I/O pins P0.7, P0.5, P0.3, and P0.1. Setting either or both of these bits causes the I/O pin to be configured as an output that reflects the input state of the corresponding even-numbered I/O pins P0.6, P0.4, P0.2, and P0.0. As an example, P0.1 can be configured as an output that follows the signal applied to the P0.0 input. These two register bits only appear in the odd-numbered bit control registers BCP07, BCP05, BCP03, and BCP01. For the available output drive combinations, see Table 4, page 80. **Note:** These bits are only used when the bypass function is desired. They should not be set when normal GPIO operation, PBC operation, or fan speed monitoring are selected through the appropriate registers or through the use of the FS, DD, and GPD bits. The PWM function (Port 0 only) and bypass function are the highest priority controls for the appropriate I/O pin. The next highest priorities are the PBC function (Port 3 through Port 6) and fan speed monitoring (Port 1 and Port 2). The lowest priorities are the bit control features found in the GPD, DD, and BCP registers. Only one mode of operation should be enabled for each I/O pin at any time. If a mode change is desired, first disable the existing mode, then enable the new mode.

Bit	Bit Label	Access	Description
4:2	FS2-0	R/W	Function Select These three bits, along with the PTE, DD, and GPD bits, determine the function of each I/O pin. When configured as an output, the FS2-0 bits determine the rate at which the high current drive I/O toggles, providing a simple mechanism for flashing LEDs. The DD and GPD bits can be used to drive each I/O individually and to take the place of the byte wide controls found in the DD and GPD registers. Note that the DD bit is always de-asserted to configure the I/O as an output. Asserting the DD bit tri-states the I/O and effectively configures the I/O as an input. The six bits allow the user to select one of seven flash rates or eight user-programmable pulse trains, as well as to drive the LED both on and off. The output can be enabled to drive in an open-source (output drives to V_{DD} with an external pull-down resistor) or open-drain (output drives to V_{SS} with an external pull-up) configuration when using the flashing mechanism. For available combinations to drive an LED, see Table 5, page 80. When configured as an input, the DD bit is asserted. These bits determine the type of I/O pin edge transition that generates an interrupt condition. Transition detectors within the device filter the changes observed at the I/O pin and determine if a valid transition has occurred. If a valid transition occurs, the INT# pin asserts and a binary value equal to the address of this register appears in the BCIS register. For available input edge combinations, see Table 6, page 81. **Note**: When configuring an I/O pin from an output to an input with interrupt enabled, it is recommended that the data direction change and interrupt enabling be accomplished with separate register write operations. This guarantees that any I/O transition that occurs as a result of the data direction change, which may rely on the weak internal pull-up resistor, does not generate an unexpected interrupt.
1	DD	R/W	Data Direction This bit determines the direction of the data flow through the I/O pin. To enable the respective I/O pin as an input, set the appropriate bit. To enable the respective I/O pin as an output, reset the appropriate bit. Each I/O pin can be individually configured as a true bidirectional function. To implement an open-drain or open-source function, set or reset the appropriate data bit using the data direction bit as the programmed data value. After a reset or power on, these bits are set to a binary 1, enabling the I/O as an input with weak pull-up.
0	GPD	R/W	General-Purpose Data When the I/O pin has been enabled as an output, writing this bit determines the data value that is present on the corresponding I/O pin. If the I/O pin is enabled as an input, reading this register bit represents the current voltage applied to the pin. At no time does this bit directly represent the value latched into the data register. If the pin is enabled as an input and there is no signal applied, a weak internal pull-up resistor holds the pin at a binary 1. After a reset or power on, this register bit is set to a binary 1, however, the value returned from a register read is the level applied to the pin since each pin is an input by default.

Table 4 shows the available output drive combinations.

Table 4. Bypass Driving Modes

BYP0	BYP1	Bypass Driving Mode
0	0	Normal GPIO operation, control is defined by the FS2-0, DD, and GPD bits
0	1	Open-drain drive, active driver to V_{SS} only
1	0	Open-drain source, active driver to V_{DD} only
1	1	Totem pole drive, active driver to V_{SS} and V_{DD}

Table 5 shows the available combinations that can be used to drive an LED.

Table 5. LED Options

PTE	FS2	FS1	FS0	DD	GPD	I/O State
0	0	0	0	1	X	Input with weak internal pull-up resistor, default state
0	0	0	0	0	0	Output driven LOW to V_{SS}
0	0	0	1	0	0	Output toggling at 0.25 Hz, drive to V_{SS} only
0	0	1	0	0	0	Output toggling at 0.33 Hz, drive to V_{SS} only
0	0	1	1	0	0	Output toggling at 0.50 Hz, drive to V_{SS} only
0	1	0	0	0	0	Output toggling at 1.00 Hz, drive to V_{SS} only
0	1	0	1	0	0	Output toggling at 2.00 Hz, drive to V_{SS} only
0	1	1	0	0	0	Output toggling at 3.08 Hz, drive to V_{SS} only
0	1	1	1	0	0	Output toggling at 4.00 Hz, drive to V_{SS} only
1	0	0	0	0	0	Pulse Train 0 selected, drive to V_{SS} only
1	0	0	1	0	0	Pulse Train 1 selected, drive to V_{SS} only
1	0	1	0	0	0	Pulse Train 2 selected, drive to V_{SS} only
1	0	1	1	0	0	Pulse Train 3 selected, drive to V_{SS} only
1	1	0	0	0	0	Pulse Train 4 selected, drive to V_{SS} only
1	1	0	1	0	0	Pulse Train 5 selected, drive to V_{SS} only
1	1	1	0	0	0	Pulse Train 6 selected, drive to V_{SS} only
1	1	1	1	0	0	Pulse Train 7 selected, drive to V_{SS} only
0	0	0	0	0	1	Output driven HIGH to V_{DD}
0	0	0	1	0	1	Output toggling at 0.25 Hz, drive to V_{DD} only
0	0	1	0	0	1	Output toggling at 0.33 Hz, drive to V_{DD} only
0	0	1	1	0	1	Output toggling at 0.50 Hz, drive to V_{DD} only
0	1	0	0	0	1	Output toggling at 1.00 H, drive to V_{DD} only
0	1	0	1	0	1	Output toggling at 2.00 Hz, drive to V_{DD} only
0	1	1	0	0	1	Output toggling at 3.08 Hz, drive to V_{DD} only
0	1	1	1	0	1	Output toggling at 4.00 Hz, drive to V_{DD} only
1	0	0	0	0	1	Pulse Train 0 selected, drive to V_{DD} only
1	0	0	1	0	1	Pulse Train 1 selected, drive to V_{DD} only
1	0	1	0	0	1	Pulse Train 2 selected, drive to V_{DD} only
1	0	1	1	0	1	Pulse Train 3 selected, drive to V_{DD} only
1	1	0	0	0	1	Pulse Train 4 selected, drive to V_{DD} only
1	1	0	1	0	1	Pulse Train 5 selected, drive to V_{DD} only

Table 5. LED Options *(continued)*

PTE	FS2	FS1	FS0	DD	GPD	I/O State
1	1	1	0	0	1	Pulse Train 6 selected, drive to V_{DD} only
1	1	1	1	0	1	Pulse Train 7 selected, drive to V_{DD} only

Table 6 shows the available input edge combinations.

Table 6. Input Edge Combinations

FS2	FS1	FS0	DD	GPD	Interrupt Condition
0	0	0	1	X	No interrupt generated, default
X	0	1	1	X	Interrupt generated on a rising edge
X	1	0	1	X	Interrupt generated on a falling edge
X	1	1	1	X	Interrupt generated on either edge
1	0	0	1	X	No interrupt generated

3.2.74 88h: Pulse Train Control 80 (PTC80)

This register, along with the PTC81 register, provides a user-programmable LED flashing pulse train that defines the 0.33 Hz flash rate (selectable in the bit control registers) at power on. The user can adjust the pulse duration, the pulse train length, and the on/off time to derive a specific visual indication. The PTC80 register provides eight of the twelve bits available in the programmable pulse train. The PTC81 register contains two bits of pulse-width programmability, two bits of pulse train length programmability, and the remaining four bits of the programmable pulse train.

As an example, the pulse train can be used to develop a visual heartbeat indication by programming the PTC80 register with a 45h and the PTC81 register with a 01h. This combination develops a pulse train with two blinks followed by a gap with the on times of the LED equal to 166.67 ms.

If the default values of this register or the PTC51 register are modified, and synchronization to other LED flash rates is desired, the SYNC# pin must be enabled. To enable the SYNC# pin, tie the SYNCEN pin to V_{DD}, connect an external 10 kΩ pull-up resistor to the SYNC# pin, and place the proper synchronization value in bits 3:0 of the Clock Select Control register. For information on the Clock Select Control register, see “FDh: Clock Select Control (CSC),” page 111.

The following table shows the bit assignments for the Pulse Train Control 80 register.

Register Name: PTC80
Address: 88h
Reset Value: 0011_1111b

Bit	Bit Label	Access	Description
7:0	PT7-0	R/W	Pulse Train These eight bits are the first bits shifted out from 0 to 7 and define the on/off time for the 0.33 Hz (FS2-FS0 = 010b in the selected Bit Control register) flash rate. 1: defines LED on time. 0: defines LED off time.

3.2.75 89h: Pulse Train Control 81 (PTC81)

This register, along with the PTC80 register, provides a user-programmable LED flashing pulse train that defines the 0.33 Hz flash rate (selectable in the bit control registers) at power on. The user can adjust the pulse duration, pulse train length, and the on/off time to derive a specific visual indication. The PTC80 register provides eight of the twelve bits available in the programmable pulse train. The PTC81 register contains two bits of pulse-width programmability, two bits of pulse train length programmability, and the remaining four bits of the programmable pulse train.

As an example, the pulse train can be used to develop a visual heartbeat indication by programming the PTC80 register with a 45h and the PTC81 register with a 01h. This combination develops a pulse train with two blinks followed by a gap with the on times of the LED equal to 166.67 ms.

If the default values of this register or the PTC80 register are modified, and synchronization to other LED flash rates is desired, the SYNC# pin must be enabled. To enable the SYNC# pin, tie the SYNCEN pin to V_{DD}, connect an external 10 kΩ pull-up resistor to the SYNC# pin, and place the proper synchronization value in bits 3:0 of the Clock Select Control register. For information on the Clock Select Control register, see "FDh: Clock Select Control (CSC)," page 111.

The following table shows the bit assignments for the Pulse Train Control 81 register.

Register Name: PTC81
Address: 89h
Reset Value: 0100_0000b

Bit	Bit Label	Access	Description
7:6	TPW1-0	R/W	Train Pulse Width These two bits define the pulse width of each of the pulse train bits. The available pulse widths are as follows: TPW1 TPW0 Train Pulse Width 0 0 166.67 ms 0 1 250.0 ms 1 0 333.3 ms 1 1 500.0 ms
5:4	PTL1-0	R/W	Pulse Train Length These two bits define the pulse train length, which is the number of pulse train bits that is shifted out before returning to bit 0. The available pulse train lengths are as follows: PTL1 PTL0 Pulse Train Length 0 0 12 pulse train bits from 0 to 11 0 1 10 pulse train bits from 0 to 9 1 0 9 pulse train bits from 0 to 8 1 1 8 pulse train bits from 0 to 7
3:0	PT11-8	R/W	Pulse Train These four bits are the last bits shifted out from 0 to 3 and define the on/off time for the flash rate. 1: defines LED on time. 0: defines LED off time.

3.2.76 8Ch: Pulse Train Control 90 (PTC90)

This register, along with the PTC91 register, provides a user-programmable LED flashing pulse train that defines the 0.25 Hz flash rate (selectable in the bit control registers) at power on. The user can adjust the pulse duration, pulse train length, and the on/off time to derive a specific visual indication. The PTC90 register provides eight of the twelve bits available in the programmable pulse train. The PTC91 register contains two bits of pulse-width programmability, two bits of pulse train length programmability, and the remaining four bits of the programmable pulse train.

As an example, the pulse train can be used to develop a visual heartbeat indication by programming the PTC90 register with a 45h and the PTC91 register with a 01h. This combination develops a pulse train with two blinks followed by a gap with the on times of the LED equal to 166.67 ms.

If the default values of this register or the PTC91 register are modified, and synchronization to other LED flash rates is desired, the SYNC# pin must be enabled. To enable the SYNC# pin, tie the SYNCEN pin to V_{DD}, connect an external 10 kΩ pull-up resistor to the SYNC# pin, and place the proper synchronization value in bits 3:0 of the Clock Select Control register. For information on the Clock Select Control register, see "FDh: Clock Select Control (CSC)," page 111.

The following table shows the bit assignments for the Pulse Train Control 90 registers.

Register Name: PTC90
Address: 8Ch
Reset Value: 0011_1111b
Description Pulse Train Control 90

Bit	Bit Label	Access	Description
7:0	PT7-0	R/W	Pulse Train These eight bits are the first bits shifted out from 0 to 7 and define the on/off time for the 0.25 Hz (FS2-FS0 = 001b in the selected bit control register) flash rate. 1: defines LED on time. 0: defines LED off time.

3.2.77 8Dh: Pulse Train Control 91 (PTC91)

This register, along with the PTC90 register, provides a user-programmable LED flashing pulse train that defines the 0.25 Hz flash rate (selectable in the bit control registers) at power on. The user can adjust the pulse duration, the pulse train length, and the on/off time to derive a specific visual indication. The PTC90 register provides eight of the twelve bits available in the programmable pulse train. The PTC91 register contains two bits of pulse-width programmability, two bits of pulse train length programmability, and the remaining four bits of the programmable pulse train.

As an example, the pulse train can be used to develop a visual heartbeat indication by programming the PTC90 register with a 45h and the PTC91 register with a 01h. This combination develops a pulse train with two blinks followed by a gap with the on times of the LED equal to 166.67 ms.

If the default values of this register or the PTC90 register are modified, and synchronization to other LED flash rates is desired, the SYNC# pin must be enabled. To enable the SYNC# pin, tie the SYNCEN pin to V_{DD}, connect an external 10 kΩ pull-up resistor to the SYNC# pin, and place the proper synchronization value in bits 3:0 of the Clock Select Control register. For information on the Clock Select Control register, see "FDh: Clock Select Control (CSC)," page 111.

The following table shows the bit assignments for the Pulse Train Control 91 registers.

Register Name: PTC91
Address: 8Bh
Reset Value: 1000_0000b

Bit	Bit Label	Access	Description
7:6	TPW1-0	R/W	Train Pulse Width These two bits define the pulse width of each of the pulse train bits. The available pulse widths are as follows: TPW1 TPW0 Train Pulse Width 0 0 166.67 ms 0 1 250.0 ms 1 0 333.3 ms 1 1 500.0 ms
5:4	PTL1-0	R/W	Pulse Train Length These two bits define the pulse train length, which is the number of pulse train bits that is shifted out before returning to bit 0. The available pulse train lengths are given below. PTL1 PTL0 Pulse Train Length 0 0 12 pulse train bits from 0 to 11 0 1 10 pulse train bits from 0 to 9 1 0 9 pulse train bits from 0 to 8 1 1 8 pulse train bits from 0 to 7
3:0	PT11-8	R/W	Pulse Train These four bits are the last bits shifted out from 0 to 3 and define the on/off time for the flash rate. 1: defines an LED on time. 0: defines an LED off time.

3.2.78 90h-97h: Bit Control Port 1 (BCP10-BCP17)

These eight registers function the same as the Bit Control Port 0 register except they provide individual bit control for the Port 1 I/O pins. All register bits are identical from a control and status perspective, with the only difference being the individual I/O pin controlled and the presence of the bypass function. The Data Direction (bit 1) and General-Purpose Data (bit 0) bits are effectively the same bits found in the DDP0 and GPD0 registers, with parallel read and write paths. For information about the functionality of the Bit Control Port 0 registers, see "80h-87h: Bit Control Port 0 (BCP00-BCP07)," page 78.

The following table shows the bit assignments for the Bit Control Port 1 registers.

Register Name: BCP10-BCP17
Address: 90h-97h
Reset Value: 0000_001Xb

Bit	Bit Label	Access	Description
7	PTE	R/W	Pulse Train Enable This bit, along with the FS bits, enables one of eight pulse train circuits controlled by the pulse train registers, PTC00 through PTC71 (70h through 7Fh), as the output drive function for this I/O pin. When this bit is set, the FS bits select one of eight pulse train circuits instead of the normal fixed-rate LED flashing circuits or the normal output drive mode. For the various LED drive control modes, see Table 5, page 80. After a reset or power on, this bit is cleared.
6:5	BYP1-0	R/W	Bypass Select These two bits determine the bypass function of the odd-numbered I/O pins P0.7, P0.5, P0.3, and P0.1. Setting either or both of these bits causes the I/O pin to be configured as an output that reflects the input state of the corresponding even-numbered I/O pins P0.6, P0.4, P0.2, and P0.0. As an example, P0.1 can be configured as an output that follows the signal applied to the P0.0 input. These two register bits only appear in the odd-numbered bit control registers BCP07, BCP05, BCP03, and BCP01. For available output drive combinations, see Table 4, page 80. **Note:** These bits are only used when the bypass function is desired. They should not be set when normal GPIO operation, PBC operation, or fan speed monitoring are selected through the appropriate registers or through the use of the FS, DD, and GPD bits. The PWM function (Port 0 only) and bypass function are the highest priority controls for the appropriate I/O pin. The next highest priorities are the PBC function (Port 3 through Port 6) and fan speed monitoring (Port 1 and Port 2). The lowest priorities are the bit control features found in the GPD, DD, and BCP registers. Only one mode of operation should be enabled for each I/O pin at any time. If a mode change is desired, first disable the existing mode and then enable the new mode.

Bit	Bit Label	Access	Description
4:2	FS2-0	R/W	Function Select These three bits, along with the PTE, DD, and GPD bits, determine the function of each I/O pin. When configured as an output, the FS2-0 bits determine the rate at which the high current drive I/O toggles, providing a simple mechanism for flashing LEDs. The DD and GPD bits can be used to drive each I/O individually and to take the place of the byte wide controls found in the DD and GPD registers. Note that the DD bit is always de-asserted to configure the I/O as an output. Asserting the DD bit tri-states the I/O and effectively configures the I/O as an input. The six bits allow the user to select one of seven flash rates or eight user-programmable pulse trains, as well as to drive the LED both on and off. The output can be enabled to drive in an open-source (output drives to V_{DD} with an external pull-down resistor) or open-drain (output drives to V_{SS} with an external pull-up) configuration when using the flashing mechanism. For available combinations to drive an LED, see Table 5, page 80. When configured as an input, the DD bit is asserted. These bits determine the type of I/O pin edge transition that generates an interrupt condition. Transition detectors within the device filter the changes observed at the I/O pin and determine if a valid transition has occurred. If a valid transition occurs, the INT# pin asserts and a binary value equal to the address of this register appears in the BCIS register. For available input edge combinations, see Table 6, page 81. **Note**: When configuring an I/O pin from an output to an input with interrupt enabled, it is recommended that the data direction change and interrupt enabling be accomplished with separate register write operations. This guarantees that any I/O transition that occurs as a result of the data direction change, which may rely on the weak internal pull-up resistor, does not generate an unexpected interrupt.
1	DD	R/W	Data Direction This bit determines the direction of the data flow through the I/O pin. To enable the respective I/O pin as an input, set the appropriate bit. To enable the respective I/O pin as an output, reset the appropriate bit. Each I/O pin can be individually configured as a true bidirectional function. To implement an open-drain or open-source function, set or reset the appropriate data bit using the data direction bit as the programmed data value. After a reset or power on, these bits are set to a binary 1, enabling the I/O as an input with weak pull-up.
0	GPD	R/W	General-Purpose Data When the I/O pin has been enabled as an output, writing this bit determines the data value that is present on the corresponding I/O pin. If the I/O pin has been enabled as an input, reading this register bit represents the current voltage applied to the pin. At no time does this bit directly represent the value latched into the data register. If the pin is enabled as an input and there is no signal applied, a weak internal pull-up resistor holds the pin at a binary 1. After a reset or power on, this register bit is set to a binary 1; however, the value returned from a register read is the level applied to the pin since each pin is an input by default.

3.2.79 98h-9Fh: Pulse-Width Modulation Control (PWMC0-PWMC7)

These eight registers provide a pulse-width modulated output that can optionally be made available on each of the Port 1 I/O pins. Configurations for these I/O pins that may have been previously enabled through other control registers are overridden if either one or both of the PWBF bits are set. The PWBF bits have higher priority control over the Port 1 I/O pins than any other mode of operation. The pulse-width modulated outputs are based on a 32-step counter and provide values from a 3.125% to a 100% duty cycle in 3.125% increments.

The following table shows the bit assignments for the Pulse-Width Modulation Control registers.

Register Name: PWMC0-PWMC7
Address: 98h-9Fh
Reset Value: X000_0000b

Bit	Bit Label	Access	Description
6:5	PWBF1-0	R/W	Pulse-Width Base Frequency These two bits determine the base operating frequency of the pulse-width modulated output. These frequencies vary with the input clock rate and are nominally based on a 10.0 MHz clock source. The available base frequencies are as follows. PWBF1 / PWBF0 / Pulse-Width Base Frequency 0 / 0 / Normal operation—control is provided through GPD1/DDP1 or BCP1 0 / 1 / 26 kHz base frequency 1 / 0 / 52 kHz base frequency 1 / 1 / 104 kHz base frequency
4:0	PWP4-0	R/W	Pulse-Width Percentage These five bits determine the percentage of high time that the output pulse contains. There are 32 steps that can be adjusted in 3.125% increments. For the available percentages of high time, see Table 7, page 87.

The following table shows the available percentages of high time for the pulse width for the PWP4-0 bits.

Table 7. Pulse-Width Percentages

PWP4	PWP3	PWP2	PWP1	PWP0	Pulse-Width Percentage
0	0	0	0	0	3.125% on/high time
0	0	0	0	1	6.25% on/high time
0	0	0	1	0	9.375% on/high time
0	0	0	1	1	12.5% on/high time
0	0	1	0	0	15.625% on/high time
0	0	1	0	1	18.75% on/high time
0	0	1	1	0	21.875% on/high time
0	0	1	1	1	25.0% on/high time
0	1	0	0	0	28.125% on/high time
0	1	0	0	1	31.25% on/high time
0	1	0	1	0	34.375% on/high time
0	1	0	1	1	37.5% on/high time
0	1	1	0	0	40.625% on/high time

Table 7. Pulse-Width Percentages *(continued)*

PWP4	PWP3	PWP2	PWP1	PWP0	Pulse-Width Percentage
0	1	1	0	1	43.75% on/high time
0	1	1	1	0	46.875% on/high time
0	1	1	1	1	50.0% on/high time
1	0	0	0	0	53.125% on/high time
1	0	0	0	1	56.25% on/high time
1	0	0	1	0	59.375% on/high time
1	0	0	1	1	62.5% on/high time
1	0	1	0	0	65.625% on/high time
1	0	1	0	1	68.75% on/high time
1	0	1	1	0	71.875% on/high time
1	0	1	1	1	75.0% on/high time
1	1	0	0	0	78.125% on/high time
1	1	0	0	1	81.25% on/high time
1	1	0	1	0	84.375% on/high time
1	1	0	1	1	87.5% on/high time
1	1	1	0	0	90.625% on/high time
1	1	1	0	1	93.75% on/high time
1	1	1	1	0	96.875% on/high time
1	1	1	1	1	100% on/high time

3.2.80 A0h-A7h: Bit Control Port 2 (BCP20-BCP27)

These eight registers function the same as the Bit Control Port 0 registers except they provide individual bit control for the Port 2 I/O pins. All register bits are identical from a control and status perspective, with the only difference being the individual I/O pin controlled and the presence of the bypass function. The Data Direction (bit 1) and General-Purpose Data (bit 0) bits are effectively the same bits found in the DDP0 and GPD0 registers, with parallel read and write paths. For information about the functionality of the Bit Control Port 0 registers, see "80h-87h: Bit Control Port 0 (BCP00-BCP07)," page 78.

The following table shows the bit assignments for the Bit Control Port 2 registers.

Register Name: BCP20-BCP27
Address: A0h-A7h
Reset Value: 0000_001Xb

Bit	Bit Label	Access	Description
7	PTE	R/W	Pulse Train Enable This bit, along with the FS bits, enables one of eight pulse train circuits controlled by the pulse train registers, PTC00 through PTC71 (70h through 7Fh), as the output drive function for this I/O pin. When the PTE bit set, the FS bits select one of eight pulse train circuits instead of the normal fixed-rate LED flashing circuits or the normal output drive mode. For the various LED drive control modes, see Table 5, page 80. After a reset or power on, this bit is cleared.
6:5	BYP1-0	R/W	Bypass Select These two bits determine the bypass function of the odd-numbered I/O pins P0.7, P0.5, P0.3, and P0.1. Setting either one or both of these bits causes the I/O pin to be configured as an output that reflects the input state of the corresponding even-numbered I/O pins P0.6, P0.4, P0.2, and P0.0. As an example, P0.1 can be configured as an output that follows the signal applied to the P0.0 input. These two register bits only appear in the odd-numbered bit control registers BCP07, BCP05, BCP03, and BCP01. For the available output drive combinations, see Table 4, page 80. **Note:** These bits are only used when the bypass function is desired. They should not be set when normal GPIO operation, PBC operation, or fan speed monitoring are selected through the appropriate registers or through the use of the FS, DD, and GPD bits. The PWM function (Port 0 only) and bypass function are the highest priority controls for the appropriate I/O pin. The next highest priorities are the PBC function (Port 3 through Port 6) and fan speed monitoring (Port 1 and Port 2). The lowest priorities are the bit control features found in the GPD, DD, and BCP registers. Only one mode of operation should be enabled for each I/O pin at any time. If a mode change is desired, first disable the existing mode, then enable the new mode.

Bit	Bit Label	Access	Description
4:2	FS2-0	R/W	Function Select These three bits, along with the PTE, DD, and GPD bits, determine the function of each I/O pin. When configured as an output, the FS2-0 bits determine the rate at which the high current drive I/O toggles, providing a simple mechanism for flashing LEDs. The DD and GPD bits can be used to drive each I/O individually and to take the place of the byte wide controls found in the DD and GPD registers. Note that the DD bit is always de-asserted to configure the I/O as an output. Asserting the DD bit tri-states the I/O and effectively configures the I/O as an input. The six bits allow the user to select one of seven flash rates or eight user-programmable pulse trains, as well as to drive the LED both on and off. The output can be enabled to drive in an open-source (output drives to V_{DD} with an external pull-down resistor) or open-drain (output drives to V_{SS} with an external pull-up) configuration when using the flashing mechanism. For available combinations to drive an LED, see Table 5, page 80. When configured as an input, the DD bit is asserted. These bits determine the type of I/O pin edge transition that generates an interrupt condition. Transition detectors within the device filter the changes observed at the I/O pin and determine if a valid transition has occurred. If a valid transition occurs, the INT# pin asserts and a binary value equal to the address of this register appears in the BCIS register. For available input edge combinations, see Table 6, page 81. **Note**: When configuring an I/O pin from an output to an input with interrupt enabled, it is recommended that the data direction change and interrupt enabling be accomplished with separate register write operations. This guarantees that any I/O transition that occurs as a result of the data direction change, which may rely on the weak internal pull-up resistor, does not generate an unexpected interrupt.
1	DD	R/W	Data Direction This bit determines the direction of the data flow through the I/O pin. To enable the respective I/O pin as an input, set the appropriate bit. To enable the respective I/O pin as an output, reset the appropriate bit. Each I/O pin can be individually configured as a true bidirectional function. To implement an open-drain or open-source function, set or reset the appropriate data bit using the data direction bit as the programmed data value. After a reset or power on, these bits are set to a binary 1, enabling the I/O as an input with weak pull-up.
0	GPD	R/W	General-Purpose Data When the I/O pin is enabled as an output, writing this bit determines the data value, which is present on the corresponding I/O pin. If the I/O pin has been enabled as an input, reading this register bit represents the current voltage applied to the pin. At no time does this bit directly represent the value latched into the data register. If the pin is enabled as an input and there is no signal applied, a weak internal pull-up resistor holds the pin at a binary 1. After a reset or power on, this register bit is set to a binary 1; however, the value returned from a register read is the level applied to the pin since each pin is an input by default.

3.2.81 B0h-B7h: Bit Control Port 3 (BCP30-BCP37)

These eight registers function the same as the Bit Control Port 0 registers except they provide individual bit control for the Port 3 I/O pins. All register bits are identical from a control and status perspective, with the only difference being the individual I/O pin controlled and the presence of the bypass function. The Data Direction (bit 1) and General-Purpose Data (bit 0) bits are effectively the same bits found in the DDP0 and GPD0 registers, with parallel read and write paths. Additionally, the control of the individual I/O pins assigned to these registers can be overridden by the PBC0, PBC1, PBC2, and PBC3 registers when port bypass control is required. For information about the functionality of the Bit Control Port 0 registers, see "80h-87h: Bit Control Port 0 (BCP00-BCP07)," page 78.

The following table shows the bit assignments for the Bit Control Port 3 registers.

Register Name: BCP30-BCP37
Address: B0h-B7h
Reset Value: 0000_001Xb

Bit	Bit Label	Access	Description
7	PTE	R/W	Pulse Train Enable This bit, along with the FS bits, enables one of eight pulse train circuits controlled by the pulse train registers, PTC00 through PTC71 (70h through 7Fh), as the output drive function for this I/O pin. When this bit is set, the FS bits select one of eight pulse train circuits instead of the normal fixed-rate LED flashing circuits or the normal output drive mode. For the various LED drive control modes, see Table 5, page 80. After a reset or power on, this bit is cleared.
6:5	BYP1-0	R/W	Bypass Select These two bits determine the bypass function of the odd-numbered I/O pins P0.7, P0.5, P0.3, and P0.1. Setting either or both of these bits causes the I/O pin to be configured as an output that reflects the input state of the corresponding even-numbered I/O pins P0.6, P0.4, P0.2, and P0.0. As an example, P0.1 can be configured as an output that follows the signal applied to the P0.0 input. These two register bits only appear in the odd-numbered bit control registers BCP07, BCP05, BCP03, and BCP01. For the available output drive combinations, see Table 4, page 80. **Note:** These bits are only used when the bypass function is desired. They should not be set when normal GPIO operation, PBC operation, or fan speed monitoring are selected through the appropriate registers or through the use of the FS, DD, and GPD bits. The PWM function (Port 0 only) and bypass function are the highest priority controls for the appropriate I/O pin. The next highest priorities are the PBC function (Port 3 through Port 6) and fan speed monitoring (Port 1 and Port 2). The lowest priorities are the bit control features found in the GPD, DD, and BCP registers. Only one mode of operation should be enabled for each I/O pin at any time. If a mode change is desired, first disable the existing mode, then enable the new mode.

Bit	Bit Label	Access	Description
4:2	FS2-0	R/W	Function Select These three bits, along with the PTE, DD, and GPD bits, determine the function of each I/O pin. When configured as an output, the FS2-0 bits determine the rate at which the high current drive I/O toggles, providing a simple mechanism for flashing LEDs. The DD and GPD bits can be used to drive each I/O individually and to take the place of the byte wide controls found in the DD and GPD registers. Note that the DD bit is always de-asserted to configure the I/O as an output. Asserting the DD bit tri-states the I/O and effectively configures the I/O as an input. The six bits allow the user to select one of seven flash rates or eight user-programmable pulse trains, as well as to drive the LED both on and off. The output can be enabled to drive in an open-source (output drives to V_{DD} with an external pull-down resistor) or open-drain (output drives to V_{SS} with an external pull-up) configuration when using the flashing mechanism. For available combinations to drive an LED, see Table 5, page 80. When configured as an input, the DD bit is asserted. These bits determine the type of I/O pin edge transition that generates an interrupt condition. Transition detectors within the device filter the changes observed at the I/O pin and determine if a valid transition has occurred. If a valid transition occurs, the INT# pin asserts and a binary value equal to the address of this register appears in the BCIS register. For available input edge combinations, see Table 6, page 81. **Note**: When configuring an I/O pin from an output to an input with interrupt enabled, it is recommended that the data direction change and interrupt enabling be accomplished with separate register write operations. This guarantees that any I/O transition that occurs as a result of the data direction change, which may rely on the weak internal pull-up resistor, does not generate an unexpected interrupt.
1	DD	R/W	Data Direction This bit determines the direction of the data flow through the I/O pin. To enable the respective I/O pin as an input, set the appropriate bit. To enable the respective I/O pin as an output, reset the appropriate bit. Each I/O pin can be individually configured as a true bidirectional function. To implement an open-drain or open-source function, set or reset the appropriate data bit using the data direction bit as the programmed data value. After a reset or power on, these bits are set to a binary 1, enabling the I/O as an input with weak pull-up.
0	GPD	R/W	General-Purpose Data When the I/O pin is enabled as an output, writing this bit determines the data value that is present on the corresponding I/O pin. If the I/O pin is enabled as an input, reading this register bit represents the current voltage applied to the pin. At no time does this bit directly represent the value latched into the data register. If the pin is enabled as an input and there is no signal applied, a weak internal pull-up resistor holds the pin at a binary 1. After a reset or power on, this register bit is set to a binary 1; however, the value returned from a register read is the level applied to the pin since each pin is an input by default.

3.2.82 C0h-C7h: Bit Control Port 4 (BCP40-BCP47)

These eight registers function the same as the Bit Control Port 0 registers except they provide individual bit control for the Port 4 I/O pins. All register bits are identical from a control and status perspective, with the only difference being the individual I/O pin controlled and the presence of the bypass function. The Data Direction (bit 1) and General-Purpose Data (bit 0) bits are effectively the same bits found in the DDP0 and GPD0 registers, with parallel read and write paths. Additionally, the control of the individual I/O pins assigned to these registers can be overridden by the PBC4, PBC5, PBC6, and PBC7 registers when port bypass control is required. For information about the functionality of the Bit Control Port 0 registers, see "80h-87h: Bit Control Port 0 (BCP00-BCP07)," page 78.

The following table shows the bit assignments for the Bit Control Port 4 registers.

Register Name: BCP40-BCP47
Address: C0h-C7h
Reset Value: 0000_001Xb

Bit	Bit Label	Access	Description
7	PTE	R/W	Pulse Train Enable This bit, along with the FS bits, enables one of eight pulse train circuits controlled by the pulse train registers, PTC00 through PTC71 (70h through 7Fh), as the output drive function for this I/O pin. When this bit is set, the FS bits select one of eight pulse train circuits instead of the normal fixed-rate LED flashing circuits or the normal output drive mode. For the various LED drive control modes, see Table 5, page 80. After a reset or power on, this bit is cleared.
6:5	BYP1-0	R/W	Bypass Select These two bits determine the bypass function of the odd-numbered I/O pins P0.7, P0.5, P0.3, and P0.1. Setting either or both of these bits causes the I/O pin to be configured as an output that reflects the input state of the corresponding even-numbered I/O pins P0.6, P0.4, P0.2, and P0.0. As an example, P0.1 can be configured as an output that follows the signal applied to the P0.0 input. These two register bits only appear in the odd-numbered bit control registers BCP07, BCP05, BCP03, and BCP01. For the available output drive combinations, see Table 4, page 80. **Note:** These bits are only used when the bypass function is desired. They should not be set when normal GPIO operation, PBC operation, or fan speed monitoring are selected through the appropriate registers or through the use of the FS, DD, and GPD bits. The PWM function (Port 0 only) and bypass function are the highest priority controls for the appropriate I/O pin. The next highest priorities are the PBC function (Port 3 through Port 6) and fan speed monitoring (Port 1 and Port 2). The lowest priorities are the bit control features found in the GPD, DD, and BCP registers. Only one mode of operation should be enabled for each I/O pin at any time. If a mode change is desired, first disable the existing mode, then enable the new mode.

Bit	Bit Label	Access	Description
4:2	FS2-0	R/W	Function Select These three bits, along with the PTE, DD, and GPD bits, determine the function of each I/O pin. When configured as an output, the FS2-0 bits determine the rate at which the high current drive I/O toggles, providing a simple mechanism for flashing LEDs. The DD and GPD bits can be used to drive each I/O individually and to take the place of the byte wide controls found in the DD and GPD registers. Note that the DD bit is always de-asserted to configure the I/O as an output. Asserting the DD bit tri-states the I/O and effectively configures the I/O as an input. The six bits allow the user to select one of seven flash rates or eight user-programmable pulse trains, as well as to drive the LED both on and off. The output can be enabled to drive in an open-source (output drives to V_{DD} with an external pull-down resistor) or open-drain (output drives to V_{SS} with an external pull-up) configuration when using the flashing mechanism. For available combinations to drive an LED, see Table 5, page 80. When configured as an input, the DD bit is asserted. These bits determine the type of I/O pin edge transition that generates an interrupt condition. Transition detectors within the device filter the changes observed at the I/O pin and determine if a valid transition has occurred. If a valid transition occurs, the INT# pin asserts and a binary value equal to the address of this register appears in the BCIS register. For available input edge combinations, see Table 6, page 81. **Note**: When configuring an I/O pin from an output to an input with interrupt enabled, it is recommended that the data direction change and interrupt enabling be accomplished with separate register write operations. This guarantees that any I/O transition that occurs as a result of the data direction change, which may rely on the weak internal pull-up resistor, does not generate an unexpected interrupt.
1	DD	R/W	Data Direction This bit determines the direction of the data flow through the I/O pin. To enable the respective I/O pin as an input, set the appropriate bit. To enable the respective I/O pin as an output, reset the appropriate bit. Each I/O pin can be individually configured as a true bidirectional function. To implement an open-drain or open-source function, set or reset the appropriate data bit using the data direction bit as the programmed data value. After a reset or power on, these bits are set to a binary 1, enabling the I/O as an input with weak pull-up.
0	GPD	R/W	General-Purpose Data When the I/O pin is enabled as an output, writing this bit determines the data value that is present on the corresponding I/O pin. If the I/O pin is enabled as an input, reading this register bit represents the current voltage applied to the pin. At no time does this bit directly represent the value latched into the data register. If the pin is enabled as an input and there is no signal applied, a weak internal pull-up resistor holds the pin at a binary 1. After a reset or power on, this register bit is set to a binary 1; however, the value returned from a register read is the level applied to the pin since each pin is an input by default.

3.2.83 CCh: General-Purpose Timer Count 0 (GPTC0)

The following table shows the bit assignments for the General-Purpose Timer Count 0 register.

Register Name: GPTC0
Address: CCh
Reset Value: 0000_0000b

Bit	Bit Label	Access	Description
7:0	TC7-0	R/W	Timer Count These eight bits are part of the 24-bit general-purpose timer down counter initial count value. Writing to this register causes the timer to update and to initiate a countdown from the new value if the timer has been enabled in the GPTE register. Clearing this register, along with the GPTC1 and GPTC2 registers, stops the down counter and disables the interrupt generation logic. After a reset or power on, these bits are cleared.

3.2.84 CDh: General-Purpose Timer Count 1 (GPTC1)

The following table shows the bit assignments for the General-Purpose Timer Count 1 register.

Register Name: GPTC1
Address: CDh
Reset Value: 0000_0000b

Bit	Bit Label	Access	Description
7:0	TC15-8	R/W	Timer Count These eight bits are part of the 24-bit general-purpose timer down counter initial count value. Writing to this register causes the timer to update and to initiate a countdown from the new value if the timer has been enabled in the GPTE register. Clearing this register, along with the GPTC0 and GPTC2 registers, stops the down counter and disables the interrupt generation logic. After a reset or power on, these bits are cleared.

3.2.85 CEh: General-Purpose Timer Count 2 (GPTC2)

The following table shows the bit assignments for the General-Purpose Timer Count 2 register.

Register Name: GPTC2
Address: CEh
Reset Value: 0000_0000b

Bit	Bit Label	Access	Description
7:0	TC23-16	R/W	Timer Count These eight bits are part of the 24-bit general-purpose timer down counter initial count value. Writing to this register causes the timer to update and initiate a countdown from the new value if the timer has been enabled in the GPTE register. Clearing this register, along with the GPTC0 and GPTC1 registers, stops the down counter and disables the interrupt generation logic. After a reset or power on, these bits are cleared.

3.2.86 CFh: General-Purpose Timer Enable (GPTE)

The following table shows the bit assignments for the General-Purpose Timer Enable register.

Register Name: GPTE
Address: CFh
Reset Value: 0000_0000b

Bit	Bit Label	Access	Description
7:1	RES	R	Reserved.
0	GPTE	R/W	General-Purpose Timer Enable This bit enables the general-purpose timer to down count and generate an interrupt when the timer reaches zero. The general-purpose timer down counts using a clock source that is a divide-by-three of the core clock (8.0 MHz to 12.5 MHz), resulting in a timer count resolution of 375 ns to 240 ns. When the timer initial count is set to all 1s, the maximum timeout is greater than four seconds when using a 12.5 MHz core clock. When the 24-bit timer reaches a value of zero, the interrupt output of the VSC055-01 is asserted. The timer then re-loads with the initial count value found in the GPTC0, GPTC1, and GPTC2 registers and begins counting down again. Writing a value of FFh to the BCIS register clears this interrupt. After a reset or power on, this bit is cleared, disabling the timer and timer interrupt.

3.2.87 D0h-D7h: Bit Control Port 5 (BCP50-BCP57)

These eight registers function the same as the eight Bit Control Port 0 registers except that they relate to the Port 5 I/O pins. In addition, the control of the individual I/O pins assigned to these registers can be overridden by the PBC8, PBC9, PBC10, and PBC11 registers when port bypass control is required. For information about the functionality of the Bit Control Port 0 registers, see "80h-87h: Bit Control Port 0 (BCP00-BCP07)," page 78.

The following table shows the bit assignments for the Bit Control Port 5 registers.

Register Name: BCP50-BCP57
Address: D0h-D7h
Reset Value: 0000_001Xb

Bit	Bit Label	Access	Description
7	PTE	R/W	Pulse Train Enable This bit, along with the FS bits, enables one of eight pulse train circuits controlled by the pulse train registers, PTC00 through PTC71 (70h through 7Fh), as the output drive function for this I/O pin. When the PTE bit set, the FS bits select one of eight pulse train circuits instead of the normal fixed-rate LED flashing circuits or the normal output drive mode. For the various LED drive control modes, see Table 5, page 80. After a reset or power on, this bit is cleared.
6:5	BYP1-0	R/W	Bypass Select These two bits determine the bypass function of the odd-numbered I/O pins P0.7, P0.5, P0.3, and P0.1. Setting either or both of these bits causes the I/O pin to be configured as an output that reflects the input state of the corresponding even-numbered I/O pins P0.6, P0.4, P0.2, and P0.0. As an example, P0.1 can be configured as an output that follows the signal applied to the P0.0 input. These two register bits only appear in the odd-numbered bit control registers BCP07, BCP05, BCP03, and BCP01. For the available output drive combinations, see Table 4, page 80. **Note:** These bits are only used when the bypass function is desired. They should not be set when normal GPIO operation, PBC operation, or fan speed monitoring are selected through the appropriate registers or through the use of the FS, DD, and GPD bits. The PWM function (Port 0 only) and bypass function are the highest priority controls for the appropriate I/O pin. The next highest priorities are the PBC function (Port 3 through Port 6) and fan speed monitoring (Port 1 and Port 2). The lowest priorities are the bit control features found in the GPD, DD, and BCP registers. Only one mode of operation should be enabled for each I/O pin at any time. If a mode change is desired, first disable the existing mode, then enable the new mode.

Bit	Bit Label	Access	Description
4:2	FS2-0	R/W	Function Select These three bits, along with the PTE, DD, and GPD bits, determine the function of each I/O pin. When configured as an output, the FS2-0 bits determine the rate at which the high current drive I/O toggles, providing a simple mechanism for flashing LEDs. The DD and GPD bits can be used to drive each I/O individually and to take the place of the byte wide controls found in the DD and GPD registers. Note that the DD bit is always de-asserted to configure the I/O as an output. Asserting the DD bit tri-states the I/O and effectively configures the I/O as an input. The six bits allow the user to select one of seven flash rates or eight user-programmable pulse trains, as well as to drive the LED both on and off. The output can be enabled to drive in an open-source (output drives to V_{DD} with an external pull-down resistor) or open-drain (output drives to V_{SS} with an external pull-up) configuration when using the flashing mechanism. For available combinations to drive an LED, see Table 5, page 80. When configured as an input, the DD bit is asserted. These bits determine the type of I/O pin edge transition that generates an interrupt condition. Transition detectors within the device filter the changes observed at the I/O pin and determine if a valid transition has occurred. If a valid transition occurs, the INT# pin asserts and a binary value equal to the address of this register appears in the BCIS register. For available input edge combinations, see Table 6, page 81. **Note**: When configuring an I/O pin from an output to an input with interrupt enabled, it is recommended that the data direction change and interrupt enabling be accomplished with separate register write operations. This guarantees that any I/O transition that occurs as a result of the data direction change, which may rely on the weak internal pull-up resistor, does not generate an unexpected interrupt.
1	DD	R/W	Data Direction This bit determines the direction of the data flow through the I/O pin. To enable the respective I/O pin as an input, set the appropriate bit. To enable the respective I/O pin as an output, reset the appropriate bit. Each I/O pin can be individually configured as a true bidirectional function. To implement an open-drain or open-source function, set or reset the appropriate data bit using the data direction bit as the programmed data value. After a reset or power on, these bits are set to a binary 1, enabling the I/O as an input with weak pull-up.
0	GPD	R/W	General-Purpose Data When the I/O pin is enabled as an output, writing this bit determines the data value that is present on the corresponding I/O pin. If the I/O pin has been enabled as an input, reading this register bit represents the current voltage applied to the pin. At no time does this bit directly represent the value latched into the data register. If the pin is enabled as an input and there is no signal applied, a weak internal pull-up resistor holds the pin at a binary 1. After a reset or power on, this register bit is set to a binary 1; however, the value returned from a register read is the level applied to the pin since each pin is an input by default.

3.2.88 E0h-E7h: Bit Control Port 6 (BCP60-BCP67)

These eight registers function the same as the eight Bit Control Port 0 registers except that they relate to the Port 6 I/O pins. In addition, the control of the individual I/O pins assigned to these registers can be overridden by the PBC12, PBC13, PBC14, and PBC15 registers when port bypass control is required. For information about the functionality of the Bit Control Port 0 registers, see "80h-87h: Bit Control Port 0 (BCP00-BCP07)," page 78.

The following table shows the bit assignments for the Bit Control Port 6 registers.

Register Name: BCP60-BCP67
Address: E0h-E7h
Reset Value: 0000_001Xb

Bit	Bit Label	Access	Description
7	PTE	R/W	Pulse Train Enable This bit, along with the FS bits, enables one of eight pulse train circuits controlled by the pulse train registers, PTC00 through PTC71 (70h through 7Fh), as the output drive function for this I/O pin. When the PTE bit is set, the FS bits select one of eight pulse train circuits instead of the normal fixed-rate LED flashing circuits or the normal output drive mode. For the various LED drive control modes, see Table 5, page 80. After a reset or power on, this bit is cleared.
6:5	BYP1-0	R/W	Bypass Select These two bits determine the bypass function of the odd-numbered I/O pins P0.7, P0.5, P0.3, and P0.1. Setting either or both of these bits causes the I/O pin to be configured as an output that reflects the input state of the corresponding even-numbered I/O pins P0.6, P0.4, P0.2, and P0.0. As an example, P0.1 can be configured as an output that follows the signal applied to the P0.0 input. These two register bits only appear in the odd-numbered bit control registers BCP07, BCP05, BCP03, and BCP01. For the available output drive combinations, see Table 4, page 80. **Note:** These bits are only used when the bypass function is desired. They should not be set when normal GPIO operation, PBC operation, or fan speed monitoring are selected through the appropriate registers or through the use of the FS, DD, and GPD bits. The PWM function (Port 0 only) and bypass function are the highest priority controls for the appropriate I/O pin. The next highest priorities are the PBC function (Port 3 through Port 6) and fan speed monitoring (Port 1 and Port 2). The lowest priorities are the bit control features found in the GPD, DD, and BCP registers. Only one mode of operation should be enabled for each I/O pin at any time. If a mode change is desired, first disable the existing mode, then enable the new mode.

Bit	Bit Label	Access	Description
4:2	FS2-0	R/W	Function Select These three bits, along with the PTE, DD, and GPD bits, determine the function of each I/O pin. When configured as an output, the FS2-0 bits determine the rate at which the high current drive I/O toggles, providing a simple mechanism for flashing LEDs. The DD and GPD bits can be used to drive each I/O individually and to take the place of the byte wide controls found in the DD and GPD registers. Note that the DD bit is always de-asserted to configure the I/O as an output. Asserting the DD bit tri-states the I/O and effectively configures the I/O as an input. The six bits allow the user to select one of seven flash rates or eight user-programmable pulse trains, as well as to drive the LED both on and off. The output can be enabled to drive in an open-source (output drives to V_{DD} with an external pull-down resistor) or open-drain (output drives to V_{SS} with an external pull-up) configuration when using the flashing mechanism. For available combinations to drive an LED, see Table 5, page 80. When configured as an input, the DD bit is asserted. These bits determine the type of I/O pin edge transition that generates an interrupt condition. Transition detectors within the device filter the changes observed at the I/O pin and determine if a valid transition has occurred. If a valid transition occurs, the INT# pin asserts and a binary value equal to the address of this register appears in the BCIS register. For available input edge combinations, see Table 6, page 81. **Note**: When configuring an I/O pin from an output to an input with interrupt enabled, it is recommended that the data direction change and interrupt enabling be accomplished with separate register write operations. This guarantees that any I/O transition that occurs as a result of the data direction change, which may rely on the weak internal pull-up resistor, does not generate an unexpected interrupt.
1	DD	R/W	Data Direction This bit determines the direction of the data flow through the I/O pin. To enable the respective I/O pin as an input, set the appropriate bit. To enable the respective I/O pin as an output, reset the appropriate bit. Each I/O pin can be individually configured as a true bidirectional function. To implement an open-drain or open-source function, set or reset the appropriate data bit using the data direction bit as the programmed data value. After a reset or power on, these bits are set to a binary 1, enabling the I/O as an input with weak pull-up.
0	GPD	R/W	General-Purpose Data When the I/O pin has been enabled as an output, writing this bit determines the data value that is present on the corresponding I/O pin. If the I/O pin is enabled as an input, reading this register bit represents the current voltage applied to the pin. At no time does this bit directly represent the value latched into the data register. If the pin is enabled as an input and there is no signal applied, a weak internal pull-up resistor holds the pin at a binary 1. After a reset or power on, this register bit is set to a binary 1, but the value returned from a register read is the level applied to the pin since, by default, each pin is an input.

3.2.89 E8h: Master Interface Clock Divider (MICD)

The following seven registers comprise the Master Interface function. This function provides the ability to re-configure 32 of the I/O pins on a pair-by-pair basis as a Master mode two-wire serial interface. Ports 4, 5, 6, and 7 can be re-configured with four interface pairs per port. Each even-numbered port pin can be configured as an SDA function, with the corresponding odd-numbered port pins configured as an SCL function.

The following table shows the bit assignments for the Master Interface Clock Divider register.

Register Name: MICD
Address: E8h
Reset Value: 0X00_0000b

Bit	Bit Label	Access	Description
7	MSCE	R/W	Master Interface SCL Clock Low Extend Setting this bit changes the duty cycle of the Master Interface SCL clock output from a 50% low-50% high duty cycle to a 75% low-25% high duty cycle. This allows for better matching of fast mode (400 kHz) interface timings. After a reset or power on, this bit is cleared, enabling the default duty cycle.
6	RES	R	Reserved.
5:0	DIV5-0	R/W	Master Interface Clock Divider These six bits determine the SCL clock frequency of the Master Interface. The Master Interface uses a four-cycle state machine to drive the SCL output. All timings for the Master Interface are based on this four-cycle state machine. The frequency of operation desired is based on the divider value along with the core clock frequency of the VSC055-01. For the various divider values that result in common frequencies of operation, see Table 8, page 101.

The following table lists the various divider values that result in common frequencies of operation.

Table 8. Master Interface Clock Divider

Core Clock	DIV5-0	Divider	SM	Master Interface SCL Clock Frequency
8.0 MHz	27h	40	4	50.0 kHz
10.0 MHz	31h	50	4	50.0 kHz
12.5 MHz	3Eh	63	4	49.6 kHz
8.0 MHz	13h	20	4	100.0 kHz
10.0 MHz	18h	25	4	100.0 kHz
12.5 MHz	1Fh	32	4	97.6 kHz
8.0 MHz	04h	4	4	400.0 kHz
10.0 MHz	06h	7	4	357.1 kHz
12.5 MHz	07h	8	4	390.6 kHz

3.2.90 E9h: Master Interface Port Select (MIPS)

The following table shows the bit assignments for the Master Interface Port Select register.

Register Name: MIPS
Address: E9h
Reset Value: 0X00_0000b

Bit	Bit Label	Access	Description
7	MIPE	R/W	Master Interface Port Enable This bit enables the Master Interface on to the selected set of GPIO pins based on the port select and bit select bits. Setting this bit enables the interface allowing the Master Interface to transfer data over the selected GPIO pins based on register control. Clearing this bit disables the interface and returns control of the GPIO pins to other functions within this device. After a reset or power on, this bit is cleared.
6:5	RES	R	Reserved.
4:2	PS2-0	R/W	These three bits determine the port selected for Master mode two-wire serial transfers. Valid ports for the VSC055-01 include Port 4 (4h), Port 5 (5h), Port 6 (6h), and Port 7 (7h). Values other than those specified do not enable the interface. After a reset or power on, these bits are cleared.
1:0	BS1-0	R/W	Master Interface Bit Select These two bits determine the bits within a port selected for master mode two-wire serial transfers. 00b: enables the SDA function on bit 0 and the SCL function on bit 1 of the port. 01b: enables the SDA function on bit 2 and the SCL function on bit 3 of the port. 10b: enables the SDA function on bit 4 and the SCL function on bit 5 of the port. 11b: enables the SDA function on bit 6 and the SCL function on bit 7 of the port. After a reset or power on, these bits are cleared.

3.2.91 EAh: Master Interface Data (MID)

The following table shows the bit assignments for the Master Interface Data register.

Register Name: MID
Address: EAh
Reset Value: 0000_0000b

Bit	Bit Label	Access	Description
7:0	MD7-0	R/W	Master Interface Data These eight bits store data to be used for serial write operations or received from serial read operations. After a reset or power on, these bits are cleared.

3.2.92 EBh: Master Interface Command (MIC)

The following table shows the bit assignments for the Master Interface Command register.

Register Name: MIC
Address: EBh
Reset Value: 1100_0000b

Bit	Bit Label	Access	Description
7	SDAI	R	Serial Data Input This read-only bit indicates the current state of the master serial interface SDA input. 1: SDA signal is tri-stated and is being pulled HIGH by an external pull-up resistor. 0: device (including the VSC055-01) is actively driving a low value onto the SDA wire. After a reset or power on, this bit is unknown.
6	SDAO	R/W	Serial Data Output This bit provides low-level drive control of the master serial interface SDA signal. Setting this bit allows the automatic functions of this master serial interface to control the SDA output value. Clearing this bit forces a zero value onto the serial bus, regardless of the state of the automatic controls. Under normal circumstances, this bit should always be written to a 1. The read value for this bit returns the programmed wired-AND output value being driven, not the live value on the serial bus. After a reset or power on, this bit is set.
5	SRST	R/W	Soft Reset Setting this bit performs a soft reset operation. The soft reset operation clears all state machines and returns the master serial interface to an idle (non-driving) state with regard to SCL and SDA. The soft reset is one clock in duration. This bit is self-clearing. After a reset or power on, this bit is cleared.
4	GO	R/W	GO Setting this bit initiates a byte transfer on the serial bus. This bit automatically clears itself when the transfer is complete. After a reset or power on, this bit is cleared.
3	RW	R/W	Read/Write This bit determines whether the immediate byte to be transferred is a read or a write transaction. If this bit is set, the transfer is a read. If this bit is cleared, the transfer is a write. After a reset or power on, this bit is cleared.
2	ACK	R/W	Serial Bus Acknowledge This bit provides control for the acknowledge bit of a serial byte transfer. Setting this bit for a read transaction causes the serial interface to drive the ACK bit at the end of the transaction's bit sequence. This must be used for all but the last byte of sequential read operations. Reading this bit after a write transaction has completed indicates whether or not the targeted slave device acknowledged the byte transfer. After a reset or power on, this bit is cleared.

Bit	Bit Label	Access	Description
1	STO	R/W	Stop Condition This bit controls the STOP condition of a serial transfer. Setting this bit directs the master serial interface to generate a stop bit sequence (rising edge on SDA while SCL is HIGH) after transferring the immediate byte. This should only be done to end a telegram. After a reset or power on, this bit is cleared.
0	STA	R/W	Start Condition This bit provides control for the start condition of a serial transfer. Setting this bit directs the master serial interface to generate a start bit sequence (falling edge on SDA while SCL is HIGH) prior to transferring the immediate byte. This operation should be initiated at the beginning of a telegram and as required for restarts during read transactions. After a reset or power on, this bit is cleared.

Operating Notes for the Master Serial Interface

Encoded Two-Wire Serial Commands

52h - Read byte with stop, no acknowledge (used at the end of read telegrams)

54h - Read byte with acknowledge (used for middle bytes during sequential reads)

58h - Write byte (used for end of address writes or middle bytes of sequential writes)

59h - Write byte with start (used for the beginning of all telegrams and restarts)

5Ah - Write byte with stop (used for end of write telegrams)

60h - Soft reset

The sequence for normal two-wire serial protocol compliant write operations is:

1. Issue start bit, send the slave device address and write bit (0) in the LSB.

2. Send the slave device's register address, this can zero bytes or in some slave devices this may be multiple bytes.

3. Send the byte to be written to the slave device, followed by a stop bit.

```
Pseudo-code to perform two-wire serial protocol compliant writes
using this core:

Send slave device address:
1) <{slave_address[6:0],1'b0}>  -->  MID register (data)
2)  Write 59h to the MIC register (command)
3)  Poll the MIS register (status) until bit 0 = 1
4)  Test bit 1, if set continue, if clear then the slave device
did not respond

Send register address:
5)  <slave's register address>  -->  MID register (data)
6)  Write 58h to MIC register (command)
7)  Poll the MIS register (status) until bit 0 = 1
8)  Test bit 1, if set continue, if clear then the slave device
did not acknowledge
```

(repeat steps 5-8 if there are multiple register address bytes or data bytes)

Send data written to slave device register with a stop:
9) <data byte> --> MID register (data)
10) Write 5Ah to the MIC register (command)
11) Poll the MIS register until bit 0 = 1
12) Test bit 1, if set continue, if clear then the slave device did not acknowledge

The sequence for normal two-wire serial protocol compliant read operations is:

1) Issue start bit, send the slave device address and write bit (0) in LSB
2) Send the slave device's register address, this can zero bytes or in some slave devices this may be multiple bytes.
3) Issue another start bit (re-start condition), send the slave device address and read bit (1) in the LSB.
4) Read a byte from the slave device, or multiple bytes if the slave device supports sequential reads.
4a) For sequential reads, issue the Read Byte with ACK command (54h) for all but the last byte.
4b) Issue the Read Byte with stop, no ACK command (52h) for the last byte.

Pseudo-code to perform two-wire serial protocol compliant reads using this core:

Send slave device address:
1) <{slave_address[6:0],1'b0}> --> MID register (data)
2) Write 59h to the MIC register (command)
3) Poll the MIS register (status) until bit 0 = 1
4) Test bit 1, if set continue, if clear then the slave device did not respond

Send register address:
5) <slave's register address> --> MID register (data)
6) Write 58h to MIC register (command)
7) Poll the MIS register (status) until bit 0 = 1
8) Test bit 1, if set continue, if clear then the slave device did not acknowledge

(repeat steps 5-8 if there are multiple register address bytes)

Issue re-start with slave device address and read bit:
9) <{slave_address[6:0],1'b1}> --> MID register (data)
10) Write 59h to the MIC register (command)
11) Poll the MIS register (status) until bit 0 = 1
12) Test bit 1, if set continue, if clear then the slave device did not acknowledge

Read a byte: (if only one byte is to be read, skip to "Read last byte")
13) write 54h to the MIC register (command)
14) Poll the MIS register (status) until bit 0 = 1
15) Read data is now available in the MID register (data) and in the MIRD register (read data)

(repeat steps 13 through 15 until the next byte is the last)

Read last byte with a stop:
16) Write 52h to the MIC register (command)
17) Poll the MIS register (status) until bit 0 = 1
18) Read data is now available in the MID register (data) and in the MIRD register (read data)

Pseudo-code to perform two-wire serial bus cleanup to return the bus to an idle state:

Check that SDA is de-asserted. If not, pulse SCL:
1) Read the MIC register (control) and check that bit 7=1.
2) If bit 7 in the MIC register is reset, continue. If bit 7 in the MIC register is set, go to step 6.
3) Set bit 0 in the MILC register (low level control) low, drive SCL low.
4) Set bit 0 in the MILC register (low level control) high, release.
5) Go back to step 1 and check SDA again.

Drive a start condition followed by one bit of data and then finish with a stop condition:
6) Drive SDA low (start condition) by setting bit 6 low in the MIC register
7) Drive SCL low by setting bit 0 low in the MILC register.
8) Release SCL by setting bit 0 high in the MILC register (clock out one data bit)
9) Release SDA (stop-condition) by setting bit 6 high in the MIC register
10) Begin normal two-wire serial transfers

3.2.93 ECh: Master Interface Low-Level Control (MILC)

The following table shows the bit assignments for the Master Interface Low-Level Control register.

Register Name: MILC
Address: ECh
Reset Value: XXXX_XXX1b

Bit	Bit Label	Access	Description
7:1	RES	R	Reserved.
0	SCLO	R/W	Serial Clock Output This bit provides low-level control of the master interface SCL output. This register bit provides set or clear capability on the SCL output control register within this core. As such, writing any value to this register may interfere with automatic interface activity. During normal core operation, this register should not be written. Reading this register bit returns the SCL output value that this core is currently driving on the serial bus. After a reset or power on, this bit is set (SCL inactive).

3.2.94 EDh: Master Interface Status (MIS)

The following table shows the bit assignments for the Master Interface Status register.

Register Name: MIS
Address: EDh
Reset Value: XXXX_XX00b

Bit	Bit Label	Access	Description
7:2	RES	R	Reserved.
1	ACKR	R	Acknowledge Received This bit indicates if an acknowledge is received after a write operation. 1: An acknowledge has been received. 0: An acknowledge has not been received. After a reset or power on, this bit is cleared.
0	DONE	R	Transfer Complete This bit indicates when the current transfer is complete. 1: the current transfer is complete. 0: the current transfer is not complete. After a reset or power on, this bit is cleared. **Note**: The status bits provided in this register are also effectively available by reading the MIC register (bit 2, ACK and bit 4, GO). The intention of this optional register is to provide a simple programming model with only the required status bits included so that other bit positions do not need to be masked off to determine the result of a two-wire serial transfer operation. During master serial interface write operations, it is possible to write the MID (data) and MIC (command) registers, perform a restart, read the current address (the MILC register), and then poll the MIS (status) register to determine if the current write operation is complete.

3.2.95 EEh: Master Interface Read Data (MIRD)

This register allows a sequential read operation of the MIC (command), MILC (low-level control, delay to allow transfer to complete), MIS (status), and MIRD (read data) registers by an external microcontroller to form a complete read transfer. It returns the same data as the MID (data) register.

The following table shows the bit assignments for the Master Interface Read Data register.

Register Name: MIRD
Address: EEh
Reset Value: 0000_0000b

Bit	Bit Label	Access	Description
7:0	MD7-0	R	Master Interface Data These eight read-only bits provide the data value received from serial read operations. After a reset or power on, these bits are cleared.

3.2.96 F0h-F7h: Bit Control Port 7 (BCP70-BCP77)

These eight registers provide individual bit control for the Port 7 I/O pins. All register bits are identical from a control and status perspective, with the only difference being the individual I/O pin controlled and the presence of the bypass function. The Data Direction (bit 1) and General-Purpose Data (bit 0) bits are effectively the same bits found in the DDP0 and GPD0 registers, with parallel read and write paths.

These eight registers function the same as the eight Bit Control Port 0 registers except that they relate to the Port 7 I/O pins. For information about the functionality of the Bit Control Port 0 registers, see "80h-87h: Bit Control Port 0 (BCP00-BCP07)," page 78.

The following table shows the bit assignments for the Bit Control Port 7 registers.

Register Name: BCP70-BCP77
Address: F0h-F7h
Reset Value: 0000_001Xb

Bit	Bit Label	Access	Description
7	PTE	R/W	Pulse Train Enable This bit, along with the FS bits, enables one of eight pulse train circuits controlled by the pulse train registers, PTC00 through PTC71 (70h through 7Fh), as the output drive function for this I/O pin. When this bit is set, the FS bits select one of eight pulse train circuits instead of the normal fixed-rate LED flashing circuits or the normal output drive mode. For the various LED drive control modes, see Table 5, page 80. After a reset or power on, this bit is cleared.

Bit	Bit Label	Access	Description
6:5	BYP1-0	R/W	Bypass Select These two bits determine the bypass function of the odd-numbered I/O pins P0.7, P0.5, P0.3, and P0.1. Setting either or both of these bits causes the I/O pin to be configured as an output that reflects the input state of the corresponding even-numbered I/O pins P0.6, P0.4, P0.2, and P0.0. As an example, P0.1 can be configured as an output that follows the signal applied to the P0.0 input. These two register bits only appear in the odd-numbered bit control registers BCP07, BCP05, BCP03, and BCP01. For the available output drive combinations, see Table 4, page 80. **Note:** These bits are only used when the bypass function is desired. They should not be set when normal GPIO operation, PBC operation, or fan speed monitoring are selected through the appropriate registers or through the use of the FS, DD, and GPD bits. The PWM function (Port 0 only) and bypass function are the highest priority controls for the appropriate I/O pin. The next highest priorities are the PBC function (Port 3 through Port 6) and fan speed monitoring (Port 1 and Port 2). The lowest priorities are the bit control features found in the GPD, DD, and BCP registers. Only one mode of operation should be enabled for each I/O pin at any time. If a mode change is desired, first disable the existing mode, then enable the new mode.
4:2	FS2-0	R/W	Function Select These three bits, along with the PTE, DD, and GPD bits, determine the function of each I/O pin. When configured as an output, the FS2-0 bits determine the rate at which the high current drive I/O toggles, providing a simple mechanism for flashing LEDs. The DD and GPD bits can be used to drive each I/O individually and to take the place of the byte wide controls found in the DD and GPD registers. Note that the DD bit is always de-asserted to configure the I/O as an output. Asserting the DD bit tri-states the I/O and effectively configures the I/O as an input. The six bits allow the user to select one of seven flash rates or eight user-programmable pulse trains, as well as to drive the LED both on and off. The output can be enabled to drive in an open-source (output drives to V_{DD} with an external pull-down resistor) or open-drain (output drives to V_{SS} with an external pull-up) configuration when using the flashing mechanism. For available combinations to drive an LED, see Table 5, page 80. When configured as an input, the DD bit is asserted. These bits determine the type of I/O pin edge transition that generates an interrupt condition. Transition detectors within the device filter the changes observed at the I/O pin and determine if a valid transition has occurred. If a valid transition occurs, the INT# pin asserts and a binary value equal to the address of this register appears in the BCIS register. For available input edge combinations, see Table 6, page 81. **Note**: When configuring an I/O pin from an output to an input with interrupt enabled, it is recommended that the data direction change and interrupt enabling be accomplished with separate register write operations. This guarantees that any I/O transition that occurs as a result of the data direction change, which may rely on the weak internal pull-up resistor, does not generate an unexpected interrupt.
1	DD	R/W	Data Direction This bit determines the direction of the data flow through the I/O pin. To enable the respective I/O pin as an input, set the appropriate bit. To enable the respective I/O pin as an output, reset the appropriate bit. Each I/O pin can be individually configured as a true bidirectional function. To implement an open-drain or open-source function, set or reset the appropriate data bit using the data direction bit as the programmed data value. After a reset or power on, these bits are set to a binary 1, enabling the I/O as an input with weak pull-up.

Bit	Bit Label	Access	Description
0	GPD	R/W	General-Purpose Data When the I/O pin has been enabled as an output, writing this bit determines the data value that is present on the corresponding I/O pin. If the I/O pin is enabled as an input, reading this register bit represents the current voltage applied to the pin. At no time does this bit directly represent the value latched into the data register. If the pin is enabled as an input and there is no signal applied, a weak internal pull-up resistor holds the pin at a binary 1. After a reset or power on, this register bit is set to a binary 1; however, the value returned from a register read is the level applied to the pin since each pin is an input by default.

3.2.97 F8h: Backplane Controller Interrupt Status (BCIS)

The following table shows the bit assignments for the Backplane Controller Interrupt Status register.

Register Name: BCIS
Address: F8h
Reset Value: 0000_0000b

Bit	Bit Label	Access	Description
7:0	IA7-0	R	Interrupt Active These eight bits determine the currently active interrupt source, which is enabled through the following registers: Port Bypass Control, Fan Speed Control, Bit Control, or General-Purpose Timer. The addresses of these registers are generated as an indicator of the currently active interrupt source. If multiple interrupt sources are active, the value generated is prioritized from the lowest binary value to the highest binary value. To clear the current interrupt and de-assert the INT# pin, a value of FFh must be written to this register. If a higher binary value or lower priority interrupt source is still active, the new value is generated and the INT# pin re-asserts.

3.2.98 FCh: Backplane Controller Test (BCT)

The following table shows the bit assignments for the Backplane Controller Test register.

Register Name: BCT
Address: FCh
Reset Value: 0XXX_X000b

Bit	Bit Label	Access	Description
7	SRST	R/W	Soft Reset Setting this bit resets the device at the end of the current serial transfer. All inputs and outputs, control registers, clock dividers, and the slave state machine are reset by this bit. This bit is self-clearing. Writing a 0 to this bit has no effect on the current state of the device.
6:3	RES	R	Reserved.
2	FSB	R/W	Fan Speed Bypass Setting this bit causes the main clock divider for the fan speed monitors to be bypassed. Bypassing the main clock divider causes the fan speed counters to operate 500 times faster than normal. When reset or after power on, the normal clock divider is activated. Do not set this bit during normal operation.
1	FRB		Flash Rate Bypass Setting this bit causes the main clock divider for the flash rate generators to be bypassed. Bypassing the main clock divider causes the expected flash rates to be 125,000 times faster than normal. When reset or after power on, the normal clock divider is activated. This bit should not be set during normal operation.
0	SIFB		Serial Interface Filter Bypass Setting this bit causes the digital filters on the SCL and SDA pins to be bypassed. Bypassing the filters allows the serial transfer speed to be increased for test purposes. When reset or after power on, normal filtering is activated. Do not set this bit during normal operation.

3.2.99 FDh: Clock Select Control (CSC)

The following table shows the bit assignments for the Clock Select Control register.

Register Name: CSC
Address: FDh
Reset Value: 0000_0000b

Bit	Bit Label	Access	Description
7	TFE	R/W	Tach Filter Extend Setting this bit causes the input filters on P2.0 through P2.7 to be extended from a two-stage voting circuit to a five-stage voting circuit. Additional noise immunity of approximately 300 ns is achieved. This bit enables the filter extension logic on all tach inputs and is independent of the tach control logic. The extended filters on P2.0 through P2.7 can be used in other applications with noisy signaling that require an enhanced input filter. After a reset or power on, this register bit is cleared to a 0, enabling normal input filter operation.

Bit	Bit Label	Access	Description
6	COD	R/W	CKOUT Output Disable This bit enables or disables the CKOUT pin. If this bit is set, the CKOUT pin stops toggling with the output set to a logic 1. If this bit is reset, the CKOUT pin reflects the input clock rate when CKSEL2 is LOW and reflects a divided clock rate when CKSEL2 is HIGH. The default state of this bit is LOW, which enables normal operation. This bit is cleared when a soft reset operation occurs, re-enabling the CKOUT pin if it was previously disabled through a write to this register bit.
5:4	PDS1-0	R/W	Pulse-Width Modulation Divider Select These two bits determine the divider that is used for the pulse-width modulation circuits. The base frequency range of all pulse-width modulation circuits are controlled by these bits. Each pulse-width modulation circuit can be programmed to select one of the three available frequencies within the range. After a reset or power on, these register bits are cleared to a 0. The available frequency ranges are as follows: PDS1 PDS0 Pulse-Width Modulation Frequency Range 0 0 26 kHz, 52 kHz or 104 kHz (divide-by-3) 0 1 5.2 kHz, 10.4 kHz or 20.8 kHz (divide-by-15) 1 0 1.04 kHz, 2.08 kHz or 4.16 kHz (divide-by-75) 1 1 208Hz, 416Hz, 833Hz (divide-by-375)
3:0	SP3-0		Synchronization Period These four bits determine the synchronization period of the device. The synchronization function can be used by a single VSC055-01 device for internal synchronization or by multiple VSC055-01devices for chip-to-chip synchronization. At the end of the synchronization period, a pulse is generated on the SYNC# pin that causes this device, as well as all other devices attached to the SYNC# pin, to re-synchronize their internal dividers. The device that asserts the SYNC# pin first determines the base synchronization period and effectively controls all other devices. The synchronization period can vary from 2 seconds (0001b) to 16 seconds (1111b), depending on the value in these four bits. The user must ensure that all devices use the same synchronization period and that the period selected is a multiple of all selected LED flash rate periods, including the pulse train values. These four bits are enabled when the SYNCEN pin is tied to V_{DD} and must be non-zero to enable device synchronization. Additionally, an external pull-up resistor (10 kΩ) must be connected to the SYNC# pin.

3.2.100 FEh: Clock Divider Control (CDC)

The following table shows the bit assignments for the Clock Divider Control register.

Register Name: CDC
Address: FEh
Reset Value: 0000_0000b

Bit	Bit Label	Access	Description
7:0	ICD	R/W	Internal Clock Divider These bits enable an internal clock divider that adjusts the clock source for the fan speed control and LED blink control logic to provide a 20 kHz base frequency. Under normal conditions, when these bits remain reset, the CKSEL inputs determine the divide-by value used for generation of the 20 kHz base frequency. If an external clock source between 8.0 MHz and 12.5 MHz or 32.0 MHz and 75.0 MHz that is not equal to one of the available frequencies defined by the CKSEL inputs is desired, this register should be programmed appropriately to adjust the divider. To simplify programming and provide an 8-bit value that can cover the desired range, the input clock source is divided by 3. This divider is positioned after the primary high-frequency divider, therefore proper connection of the CKSEL2 and CKSEL1 inputs is required to determine if both the source is a high-frequency source and whether it should be divided by 4 or divided by 6. For example, if 66.67 MHz is the input clock frequency, the CKSEL2 and CKSEL1 inputs would be connected to V_{DD} (divide by 6), yielding an 11.11 MHz internal clock, which is within the 8.0 MHz to 12.5 MHz operating range of the VSC055-01. The 11.11 MHz internal clock is then divided by 3 (3.7 MHz) and then divided by 185 (B8h is loaded into the CDC register) to achieve 20.02 kHz. To enable the divider, set bit 7 of this register to a 1. This limits the available divide by values from 129 (80h) to 256 (FFh), with a useful range of 133 (84h) to 208 (CFh). Table 9, page 113 describes the appropriate CKSEL input and divider values required to achieve the desired results with several input clock frequencies that are not available as part of the fixed divider logic. The CKSEL inputs must always be connected to either V_{SS} or V_{DD} based on the desired input clock range but in some cases, the value on CKSEL1 and CKSEL0 may not be important when using the CDC register. After a reset or power on, these register bits are cleared to a 0. These bits are not reset by the Soft Reset function.

The following table lists the appropriate CKSEL input clock divider values for the ICD bit.

Table 9. Clock Divider

CKSEL2	CKSEL1	CKSEL0	Input Clock	Main Divider	CDC Register	20 kHz Clock
VSS	NA	NA	8.5 MHz	NA	142 (8Dh)	19.95 kHz
VSS	NA	NA	9.0 MHz	NA	150 (95h)	20.0 kHz
VSS	NA	NA	11.0 MHz	NA	183 (B6h)	20.03 kHz
VSS	NA	NA	12.0 MHz	NA	200 (C7h)	20.0 kHz
VSS	NA	NA	12.5 MHz	NA	208 (CFh)	20.03 kHz
VDD	VSS	NA	32.0 MHz	Divide-by-4	133 (84h)	20.05 kHz
VDD	VSS	NA	36.0 MHz	Divide-by-4	150 (95h)	20.0 kHz
VDD	VSS	NA	37.5 MHz	Divide-by-4	156 (9Bh)	20.03 kHz
VDD	VSS	NA	48.0 MHz	Divide-by-4	200 (C7h)	20.0 kHz

Table 9. Clock Divider *(continued)*

CKSEL2	CKSEL1	CKSEL0	Input Clock	Main Divider	CDC Register	20 kHz Clock
VDD	VDD	NA	48.0 MHz	Divide-by-6	133 (84h)	20.05 kHz
VDD	VDD	NA	60.0 MHz	Divide-by-6	167(A6h)	19.96 kHz
VDD	VDD	NA	66.67 MHz	Divide-by-6	185 (B8h)	20.02 kHz
VDD	VDD	NA	75.0 MHz	Divide-by-6	208 (CFh)	20.03 kHz

3.2.101 FFh: Backplane Controller Version (VER)

The following table shows the bit assignments for the Backplane Controller Version register.

Register Name: VER
Address: FFh
Reset Value: 0011_0001b

Bit	Bit Label	Access	Description
7:0	VER7-0	R	Version These bits define the current version of the backplane controller. If revisions are required, these bits change to reflect the latest version of the device. Generally, changes to bits 3:0 reflect a minor revision, and changes to bits 7:4 reflect a major revision or different device type. Firmware should check this register to determine the current capabilities of the device.

4 Electrical Specifications

This section provides the DC characteristics, AC characteristics, recommended operating conditions, and stress ratings for the VSC055-01 device.

The DC and AC specifications listed in this section are guaranteed over the recommended operating conditions unless otherwise noted. For information about operating conditions, see "Operating Conditions," page 121.

4.1 DC Characteristics

The following section shows the DC specifications for the VSC055-01 device. The tables are grouped by functionality.

4.1.1 General-Purpose I/O Ports

The following table lists the DC specifications for the VSC055-01 when the device is configured in general-purpose I/O port mode for ports P7, P6, P5, P4, P3, P2, P1, and P0.

Table 10. General-Purpose I/O Ports

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Output HIGH voltage	V_{OH}	2.4	V_{DD}	V	I_{OH} = 12 mA
Output LOW voltage	V_{OL}	V_{SS}	0.4	V	I_{OL} = 12 mA
Input HIGH voltage	V_{IH}	2.0	5.5	V	
Input LOW voltage	V_{IL}	V_{SS} – 0.5	0.8	V	
Schmitt threshold, positive	V_{T+}		2.0	V	
Schmitt threshold, negative	V_{T-}	0.8		V	
Schmitt hysteresis	V_H	0.4		V	
Input current with pull-up	I_{IN}	–25	–125	µA	$V_{IN} = V_{SS}$
Three-state output leakage (device test mode)	I_{OZ}	–10	10	µA	

4.1.2 Two-Wire Serial Interface

The following table lists the DC specifications for the two-wire serial interfaces for the SDA pin.

Table 11. Two-Wire Serial Interface, SDA

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Output LOW voltage	V_{OL}	V_{SS}	0.4	V	I_{OL} = 4 mA
Input HIGH voltage	V_{IH}	2.0	5.5	V	
Input LOW voltage	V_{IL}	V_{SS} – 0.5	0.8	V	
Schmitt threshold, positive	V_{T+}		2.0	V	
Schmitt threshold, negative	$V_{T–}$	0.8		V	
Schmitt hysteresis	V_H	0.4		V	
Input current with pull-up	I_{IN}	–25	–125	µA	$V_{IN} = V_{DD}/V_{SS}$
Three-state output leakage (device test mode)	I_{OZ}	–10	10	µA	

The following table lists the DC specifications for the two-wire serial interfaces for the SCL pin.

Table 12. Two-Wire Serial Interface, SCL

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Input HIGH voltage	V_{IH}	2.0	5.5	V	
Input LOW voltage	V_{IL}	V_{SS} – 0.5	0.8	V	
Schmitt threshold, positive	V_{T+}		2.0	V	
Schmitt threshold, negative	$V_{T–}$	0.8		V	
Schmitt hysteresis	V_H	0.4		V	
Input current	I_{IN}	–10	10	µA	$V_{IN} = V_{DD}/V_{SS}$

4.1.3 Address Inputs

The following table lists the DC specifications for address inputs, pins A2, A1, A0, and ASEL.

Table 13. Address Inputs

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Input HIGH voltage	V_{IH}	2.0	5.5	V	
Input LOW voltage	V_{IL}	V_{SS} – 0.5	0.8	V	
Schmitt threshold, positive	V_{T+}		2.0	V	
Schmitt threshold, negative	$V_{T–}$	0.8		V	
Schmitt hysteresis	V_H	0.4		V	
Input current	I_{IN}	–10	10	µA	$V_{IN} = V_{DD}/V_{SS}$

4.1.4 Interrupt Output

The following table lists the DC specifications for the interrupt output, INT#.

Table 14. Interrupt Output

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Output LOW voltage	V_{OL}	V_{SS} – 0.5	0.4	V	I_{OL} = 4 mA

4.1.5 Test and Synchronization Clock Control Inputs

The following table lists the DC specifications for the test and synchronization clock control inputs, TEST, SYNCEN, CKSEL2, CKSEL1, and CKSEL0.

Table 15. Test and Synchronization Clock Control Inputs

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Input HIGH voltage	V_{IH}	2.0	5.5	V	
Input LOW voltage	V_{IL}	V_{SS} – 0.5	0.8	V	
Schmitt threshold, positive	V_{T+}		2.0	V	
Schmitt threshold, negative	$V_{T–}$	0.8		V	
Schmitt hysteresis	V_H	0.4		V	
Input current	I_{IN}	–10	10	µA	$V_{IN} = V_{DD}/V_{SS}$

4.1.6 Device Synchronization

The following table lists the DC specifications for the multiple device synchronization, SYNC#.

Table 16. Multiple Device Synchronization

Parameter	Symbol	Condition	Minimum	Maximum	Unit
Output HIGH voltage	V_{OH}	I_{OH} = 6 mA	2.4	V_{DD}	V
Output LOW voltage	V_{OL}	I_{OL} = 6 mA	V_{SS}	0.4	V
Input HIGH voltage	V_{IH}		2.0	5.5	V
Input LOW voltage	V_{IL}		V_{SS} – 0.5	0.8	V
Schmitt threshold, positive	V_{T+}			2.0	V
Schmitt threshold, negative	$V_{T–}$		0.8		V
Schmitt hysteresis	V_H		0.4		V
Input current with pull-up	I_{IN}	$V_{IN} = V_{DD}/V_{SS}$	–25	25	µA
Three-state output leakage (device test mode)	I_{OZ}		–10	10	µA

4.1.7 Clock Output

The following table lists the DC specifications for the clock output, CKOUT.

Table 17. Clock Output

Parameter	Symbol	Condition	Minimum	Maximum	Unit
Output HIGH voltage	V_{OH}	I_{OH} = 4 mA	V_{DD} – 0.5	V_{DD}	V
Output LOW voltage	V_{OL}	I_{OL} = 4 mA	V_{SS}	V_{SS} + 0.3	V

4.1.8 Oscillator and Clock Input

The following table lists the DC specifications for the oscillator and clock input, OSCI.

Table 18. Oscillator and Clock Input

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Input HIGH voltage	V_{IH}	V_{DD}/2	V_{DD} + 0.3	V	
Input LOW voltage	V_{IL}	V_{SS} – 0.5	V_{DD}/2	V	
Switching threshold	V_T	0.8	V_{DD}/2	V	
Input current	I_{IN}	–10	10	µA	$V_{IN} = V_{DD}/V_{SS}$

4.1.9 Oscillator Output

The following table lists the DC specifications for the oscillator output, OSCO.

Table 19. Oscillator Output

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Output HIGH voltage	V_{OH}	V_{DD} – 0.3	V_{DD}	V	I_{OH} = 4 mA
Output LOW voltage	V_{OL}	V_{SS}	V_{SS} + 0.3	V	I_{OL} = 4 mA

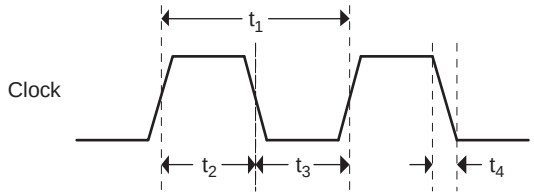
4.2 AC Characteristics

The following section shows the AC specifications for the VSC055-01 device.

4.2.1 External Clock Timing

The following section contains the external clock cycle timing waveform and parameters for low-frequency and high-frequency operation for the external clock.

Figure 4. Clock Cycle Timing Waveform



The following table lists the AC characteristics in low-frequency operation.

Table 20. Low-Frequency Operation

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Frequency range	f	8.0	12.5	MHz	CKSEL2 = V_{SS}
Clock cycle time	t_1	80	125	ns	CKSEL2 = V_{SS}
Clock LOW time	t_2	32	75	ns	CKSEL2 = V_{SS}
Clock HIGH time	t_3	32	75	ns	CKSEL2 = V_{SS}
Clock slew rate	t_4	1		V/ns	

The following table lists the AC characteristics in high-frequency operation.

Table 21. High-Frequency Operation

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Frequency range	f	32.0	75.0	MHz	CKSEL2 = V_{DD}
Clock cycle time	t_1	13.3	31.3	ns	CKSEL2 = V_{DD}
Clock LOW time	t_2	5.3	18.8	ns	CKSEL2 = V_{DD}
Clock HIGH time	t_3	5.3	18.8	ns	CKSEL2 = V_{DD}
Clock slew rate	t_4	1		V/ns	

4.2.2 Two-Wire Serial Interface Timing

This section provides information associated with device parameters that control the timing of the two-wire serial interface.

The two-wire serial interface conforms to industry-standard timing for standard and fast mode operation.

Figure 5. Two-Wire Serial Interface Timing Diagram

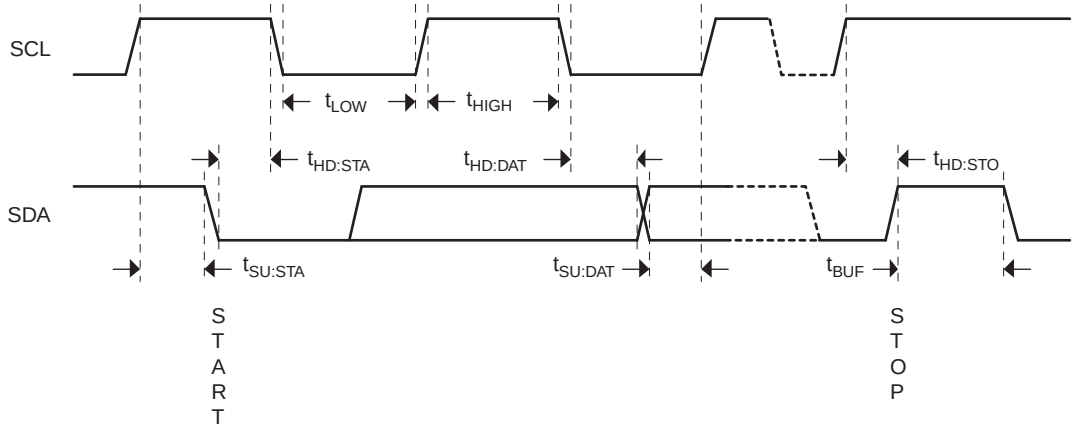


Table 22. Two-Wire Serial Interface Timing Characteristics

Parameter	Symbol	Standard Mode		Fast Mode		Unit
		Minimum	Maximum	Minimum	Maximum	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
Bus free time	t_{BUF}	4.7		1.3		µs
Hold time—START condition	$t_{HD:STA}$	4.0		0.6		µs
SCL LOW time	t_{LOW}	4.7		1.3		µs
SCL HIGH time	t_{HIGH}	4.0		0.6		µs
Setup time, START condition	$t_{SU:STA}$	4.7		0.6		µs
Hold time, data	$t_{HD:DAT}$	0		0	0.9	µs
Setup time, data	$t_{SU:DAT}$	250		100		µs
Setup time, STOP condition	$t_{SU:STO}$	4.0		0.6		µs

4.3 Operating Conditions

The following table lists the recommended operating conditions for the VSC055-01 device.

Table 23. Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Power supply voltage	V_{DD}	3.0	3.3	3.6	V
Operating temperature(1)	T	0		85	°C

1. *Lower limit of specification is ambient temperature, and upper limit is case temperature.*

4.4 Maximum Ratings

Stresses listed under Absolute Maximum Ratings may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

Table 24. Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Unit
Power supply voltage	V_{DD}	–0.3	3.9	V
LVTTL input voltage	V_{IN}	–1.0	V_{DD} + 0.3	V
5-V compatible input voltage	V_{IN}	–1.0	6.5	V
DC input current	I_{IN}	–10	10	µA
Latchup current	I_{LP}	–150	150	mA
Storage temperature	T_S	–40	125	°C
Electrostatic discharge voltage, charged device model	V_{ESD_CDM}	–1500	1500	V
Electrostatic discharge voltage, human body model	V_{ESD_HBM}	See note 1.		V

1. This device has completed all required testing as specified in the JEDEC standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*, and complies with a Class 2 rating. The definition of Class 2 is any part that passes an ESD pulse of 2000 V, but fails an ESD pulse of 4000 V.

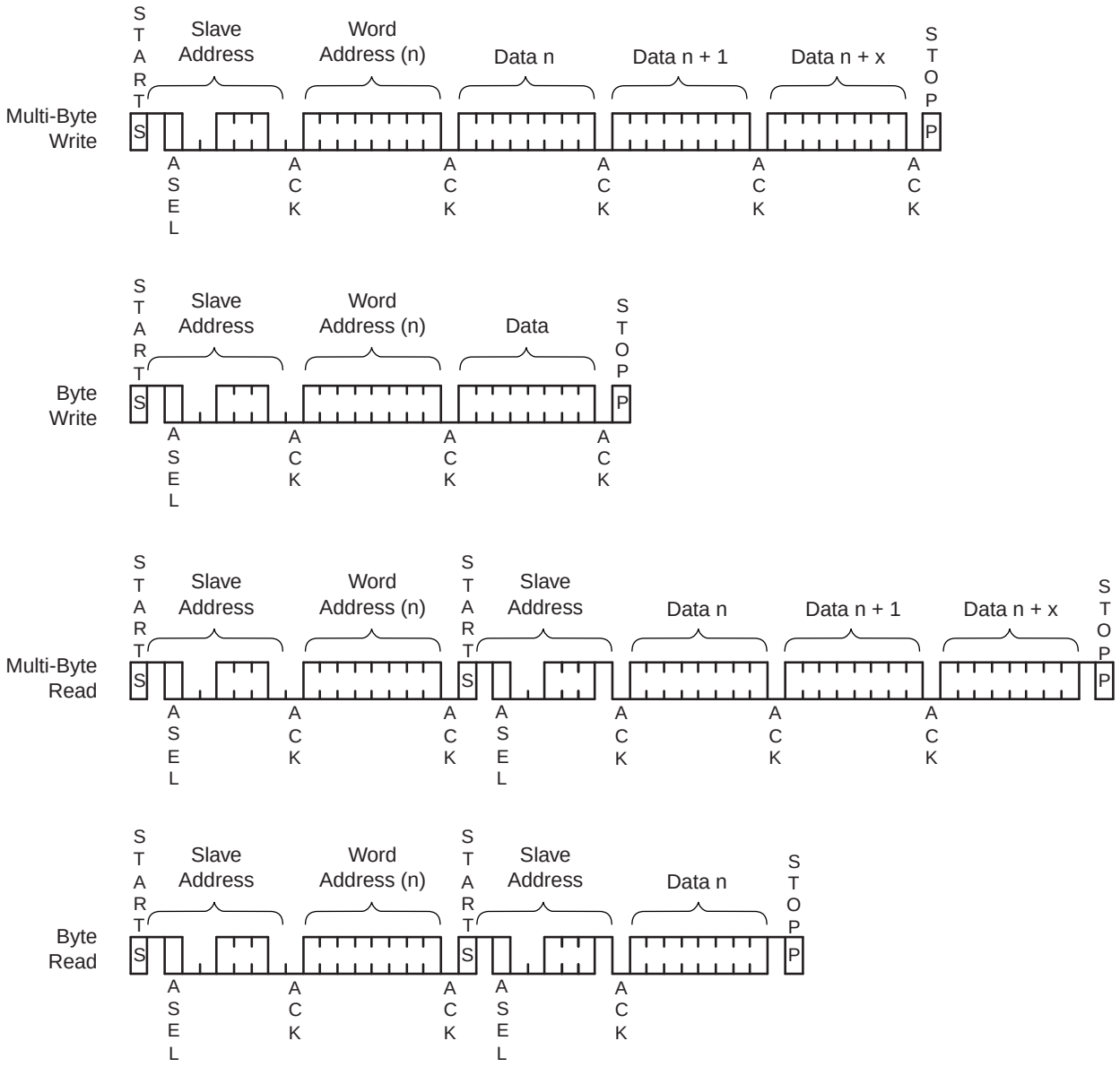
ELECTROSTATIC DISCHARGE

This device can be damaged by ESD. Maxim recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures may adversely affect reliability of the device.

4.5 Two-Wire Serial Interface Operation

The following illustration shows the two-wire serial interface read and write capabilities of the VSC055-01. All operations can be performed in any order.

Figure 6. Two-Wire Serial Interface Operation

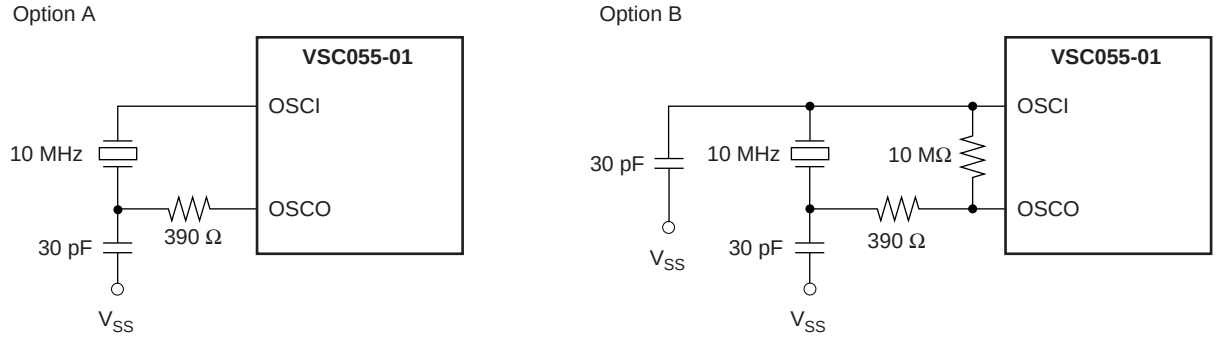


4.6 Oscillator Requirements

The VSC055-01 can use an external 3.3-V, 8.0 MHz to 12.5 MHz clock source connected to the OSCI pin, with CKSEL2 tied to V_{SS}. An external 3.3-V, 32.0 MHz to 50.0 MHz clock source can be connected to the OSCI pin with CKSEL2 tied to V_{DD} and CKSEL1 tied to V_{SS}. An external 3.3-V 48.0 MHz to 75.0 MHz clock source can be connected to the OSCI pin with CKSEL2 tied to V_{DD} and CKSEL1 tied to V_{DD}. Alternatively, an 8.0 MHz to 12.5 MHz crystal and several passive components may be used.

The following illustration shows two options when using a crystal. The passive components shown function properly for all crystal frequencies. Option A requires fewer external components due to the high input capacitance of the OSCI pin and results in a stable configuration. Option B represents a classic approach with a higher level of stability.

Figure 7. Oscillator Options

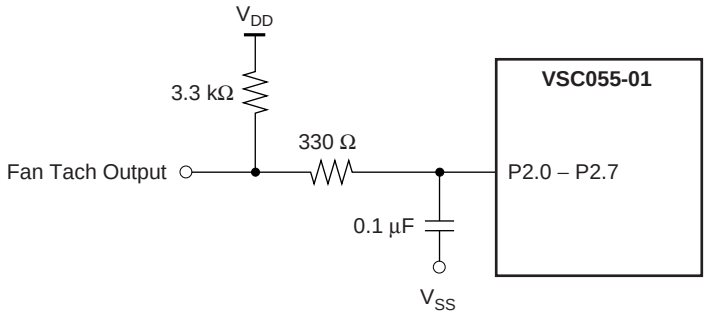


4.7 Optional External Tach Filter

The fan tach inputs of the VSC055-01 use Schmitt trigger input buffers and are also internally digitally filtered. However, excessive external noise on a tach input can result in inaccurate fan speed current count values. The use of an external low-pass filter, along with the use of the extended tach filter mode (Tach Filter Extend, bit 7 of register FDh) of the VSC055-01 eliminates inaccurate current count values.

The circuit in the following illustration provides excellent noise rejection at all possible RPM ranges supported by the VSC055-01.

Figure 8. Optional External Tach Filter



5 Pin Descriptions

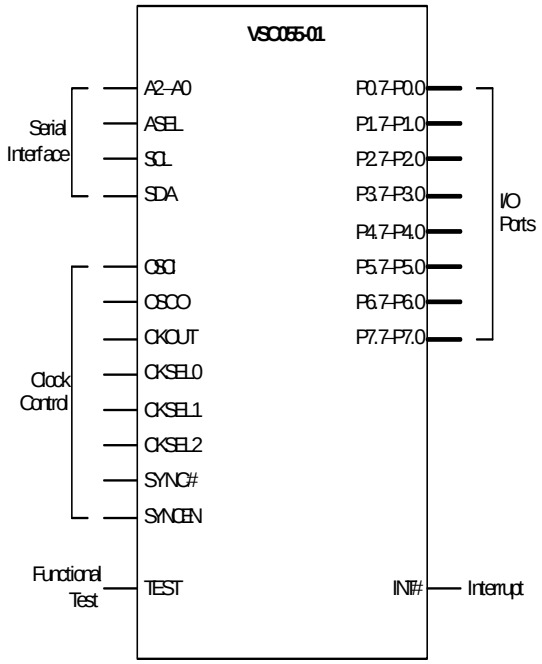
This section contains the pin diagram and descriptions for the VSC055-01 device.

5.1 Pin Diagram

The VSC055-01 has 100 pins. All pins have been placed to optimize their connection to external components. Power and ground distribution is also optimized for core and high current I/O connections. All high current I/O pins, serial interface pins, and the interrupt output are 5-V tolerant. Connect V_{DD} and V_{DD2} to a 3.3 V power supply with no more than ±10% tolerances.

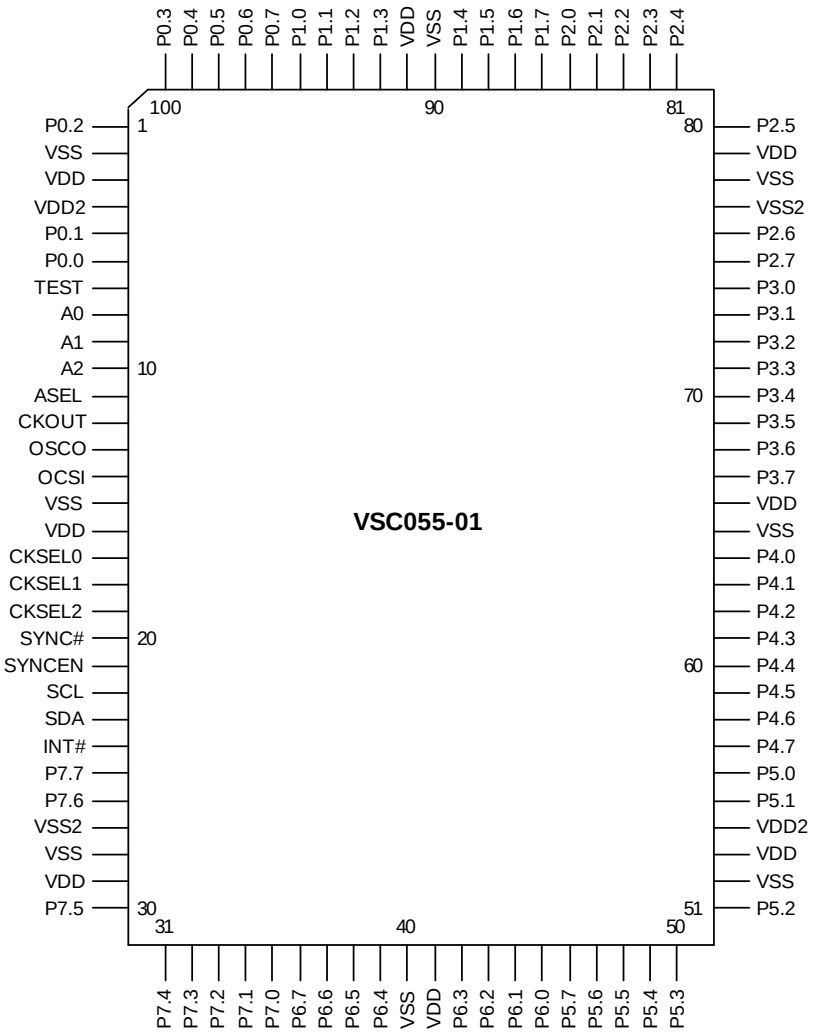
The following illustration shows the functional grouping of the signals.

Figure 9. Functional Signal Grouping



The following illustration shows the top view of the pin diagram.

Figure 10. Pin Diagram, Top View



5.2 Pin Identifications

This section contains the functional descriptions for the VSC055-01device.

Table 25. Serial Interface

Pin Name	Pin Number	I/O	Pin Description
A2 A1 A0	10 9 8	Input	Address Select Bus This pin group provides the value that is compared to bits 3:1 of the serial slave address. These pins should be strapped to V_{DD} or V_{SS} to provide the appropriate binary value.
ASEL	11	Input	Device Type Address Select This pin provides the ability to select between two-device type address values in the serial slave address. When tied to V_{SS}, the device type address is 1000b, and when tied to V_{DD}, the device type address is 1100b.
SCL	22	Input	Two-wire Serial Interface Clock This pin is used by the device to latch the data present on the SDA pin. This pin, in conjunction with the SDA pin, also determines START and STOP conditions on the serial bus.
SDA	23	Bidirectional	Two-Wire Serial Interface Data This pin is used to transfer all serial data into and out of the device. This pin, in conjunction with the SCL pin, also determines START and STOP conditions on the serial bus.

Table 26. Clock

Pin Name	Pin Number	Type	Pin Description
OSCI	14	Input	Oscillator Input This pin is connected to one side of an external 8.0 MHz to 12.5 MHz crystal to produce the clock required for the VSC055-01. 8.0 MHz, 8.33 MHz, 8.854 MHz and 10.0 MHz are pre-defined fixed frequencies supported by the CKSEL pins when using a crystal. An alternate external 3.3 V, 8.0MHz to 12.5MHz or 32.0MHz to 75.0MHz clock source can be connected to this pin. 8.0MHz, 8.33MHz, 8.854MHz, 10.0MHz, 33.33MHz, 40.0MHz, 50.0MHz and 53.125MHz are pre-defined fixed frequencies supported by the CKSEL pins when using an external clock source.
OSCO	13	Output	Oscillator Output This pin is connected to the other side of an external crystal. Leave unconnected when using an external clock source.
CKOUT	12	Output	Clock Output This pin provides a low-speed clock output that can be used to drive other VSC055-01 devices, as well as other peripheral devices. This output can be disabled through register control if unused.

Table 27. Clock Control

Pin Name	Pin Number	I/O	Pin Description
CKSEL2 CKSEL1 CKSEL0	19 18 17	Input	Clock Select These three pins determine the input frequency of the clock or crystal that is connected to the VSC055-01 on the OSCI and OSCO pins. These pins also enable or disable the internal system clock divider and adjust the flash rate and fan tach dividers to maintain the proper internal clock rates.

Table 28. Interrupt

Pin Name	Pin Number	I/O	Pin Description
INT#	24	Open-drain output	Interrupt This pin can be used to signal the microcontroller that an event has occurred on an I/O pin that is configured as an input or a special function event has occurred. It can be wire ORed with other open-drain outputs to provide a single interrupt input source.

Table 29. Multiple Device Synchronization

Pin Name	Pin Number	I/O	Pin Description
SYNC#	20	Open-drain Bidirectional	Synchronization Control This pin provides an internal or external clock synchronization mechanism when the SYNCEN pin is tied HIGH. It can be connected to the SYNC# pin of other VSC055-01 devices or can be used independently to synchronize internally. When enabled, all devices re-synchronize their internal clock dividers to the first device that pulls this pin LOW. The synchronization pulse causes all devices to clear their internal dividers and ensures that devices on different two-wire serial busses have synchronized LED flashing. The Clock Select Control register provides additional programmability to determine the appropriate re-synchronization timing. An external 10 kΩ resistor should be connected to this pin if the function is enabled. If not enabled, a weak internal pull-up will maintain a high level.
SYNCEN	21	Input	Synchronization Enable Input This pin enables the Synchronization Control feature. When tied to V_{SS}, Synchronization Control is disabled. When tied to V_{DD}, Synchronization Control is enabled. When enabled, additional control is available in the Clock Select Control register.

Table 30. I/O Ports

Pin Name	Pin Number	I/O	Description
P0.7 P0.6 P0.5 P0.4 P0.3 P0.2 P0.1 P0.0	96 97 98 99 100 1 5 6	Bidirectional	I/O Port 0, Pulse-Width Outputs Port 0 is a dedicated 8-bit bidirectional I/O port. The user can select between an input, totem pole output, or open-drain or open-source output. Capability to detect input edge changes and select various output flashing rates is also available. Through bit control register setup, each odd-numbered bit of this port can be enabled as an output, which on a pair-by-pair basis, reflects the current state of each even-numbered bit of this port. Individual control is provided that allows programming each output as a totem pole or an open-drain/source driver.
P1.7 P1.6 P1.5 P1.4 P1.3 P1.2 P1.1 P1.0	86 87 88 89 92 93 94 95	Bidirectional	I/O Port 1, Pulse-Width Outputs Port 1 is a dedicated 8-bit bidirectional I/O port. The user can select between an input, totem pole output, or open-drain or open-source output. Capability to detect input edge changes and select various output flashing rates is also available. Through control register setup, P1.7-P1.0 can be enabled as pulse-width modulated outputs, with duty cycles of 0% to 100% in 3% increments at nominal frequencies of 104 kHz, 52 kHz, and 26 kHz. Through bit control register setup, each odd-numbered bit of this port can be enabled as an output, which on a pair-by-pair basis, reflects the current state of each even-numbered bit of this port. Individual control is provided that allows programming each output as a totem pole or an open-drain/source driver.
P2.7 P2.6 P2.5 P2.4 P2.3 P2.2 P2.1 P2.0	75 76 80 81 82 83 84 85	Bidirectional	I/O Port 2, Tach Inputs Port 2 is an 8-bit bidirectional I/O port. The user can select between an input, totem pole output, or open-drain or open-source output. Capability to detect input edge changes and select various output flashing rates is also available. Through control register setup, P2.7-P2.0 can be dedicated to monitoring fans equipped with tachometer outputs. Through bit control register setup, each odd-numbered bit of this port can be enabled as an output, which on a pair-by-pair basis, reflects the current state of each even-numbered bit of this port. Individual control is provided that allows programming each output as a totem pole or an open-drain/source driver.
P3.7 P3.6 P3.5 P3.4 P3.3 P3.2 P3.1 P3.0	67 68 69 70 71 72 73 74	Bidirectional	I/O Port 3, Bypass I/Os Port 3 is a shared 8-bit bidirectional I/O port that can be used as a general-purpose I/O port or as Port Bypass control. The user can select between an input, totem pole output, or open-drain or open-source output. Capability to detect input edge changes and select various output flashing rates is also available. Through control register setup, four 2-bit portions of this port can be dedicated to the control of a combination of PBC/CRU/SDU functions. Any combination of port bypass control functions can be enabled with the remaining I/O pins used for general-purpose functions. Through bit control register setup, each odd-numbered bit of this port can be enabled as an output, which on a pair-by-pair basis, reflects the current state of each even-numbered bit of this port. Individual control is provided that allows programming each output as a totem pole or an open-drain/source driver.

Table 30. I/O Ports *(continued)*

Pin Name	Pin Number	I/O	Description
P4.7 P4.6 P4.5 P4.4 P4.3 P4.2 P4.1 P4.0	57 58 59 60 61 62 63 64	Bidirectional	I/O Port 4, Bypass I/Os Port 4 is a shared 8-bit bidirectional I/O port that can be used as a general-purpose I/O port or as Port Bypass control. The user can select between an input, totem pole output, or open-drain or open-source output. Capability to detect input edge changes and select various output flashing rates is also available. Through control register setup, four 2-bit portions of this port can be dedicated to the control of a combination of PBC/CRU/SDU functions. Any combination of port bypass control functions can be enabled with the remaining I/O pins used for general-purpose functions. Through bit control register setup, each odd-numbered bit of this port can be enabled as an output, which on a pair-by-pair basis, reflects the current state of each even-numbered bit of this port. Individual control is provided that allows programming each output as a totem pole or an open-drain/source driver.
P5.7 P5.6 P5.5 P5.4 P5.3 P5.2 P5.1 P5.0	46 47 48 49 50 51 55 56	Bidirectional	I/O Port 5, Bypass I/Os Port 5 is a shared 8-bit bidirectional I/O port that can be used as a general-purpose I/O port or as Port Bypass control. The user can select between an input, totem pole output, or open-drain or open-source output. Capability to detect input edge changes and select various output flashing rates is also available. Through control register setup, four 2-bit portions of this port can be dedicated to the control of a combination of PBC/CRU/SDU functions. Any combination of port bypass control functions can be enabled with the remaining I/O pins used for general-purpose functions. Through bit control register setup, each odd bit of this port can be enabled as an output which on a pair by pair basis, reflects the current state of each even bit of this port. Individual control is provided that allows programming each output as a totem pole or an open-drain/source driver.
P6.7 P6.6 P6.5 P6.4 P6.3 P6.2 P6.1 P6.0	36 37 38 39 42 43 44 45	Bidirectional	I/O Port 6, Bypass I/Os Port 6 is a shared 8-bit bidirectional I/O port that can be used as a general-purpose I/O port or as Port Bypass control. The user can select between an input, totem pole output, or open-drain or open-source output. Capability to detect input edge changes and select various output flashing rates is also available. Through control register setup, four 2-bit portions of this port can be dedicated to the control of a combination of PBC/CRU/SDU functions. Any combination of port bypass control functions can be enabled with the remaining I/O pins used for general-purpose functions. Through bit control register setup, each odd-numbered bit of this port can be enabled as an output, which on a pair-by-pair basis, reflects the current state of each even-numbered bit of this port. Individual control is provided that allows programming each output as a totem pole or an open-drain/source driver.

Table 30. I/O Ports *(continued)*

Pin Name	Pin Number	I/O	Description
P7.7 P7.6 P7.5 P7.4 P7.3 P7.2 P7.1 P7.0	25 26 30 31 32 33 34 35	Bidirectional	I/O Port 7, Bypass I/Os Port 7 is a dedicated 8-bit bidirectional I/O port. The user can select between an input, totem pole output, or open-drain or open-source output. Capability to detect input edge changes and select various output flashing rates is also available. Through bit control register setup, each odd-numbered bit of this port can be enabled as an output, which on a pair-by-pair basis, reflects the current state of each even-numbered bit of this port. Individual control is provided that allows programming each output as a totem pole or an open-drain/source driver.

Table 31. Test

Pin Name	Pin No.	Type	Description
TEST	7	Input	Functional Test This pin allows the device to be placed in specific test modes for device level testing. Connect to V_{SS} for normal operation.

Table 32. Power Supplies

Pin Name	Pin Number	I/O	Description
VDD	3, 16, 29, 41, 53, 66, 79, 91	Power	I/O Power Supply These pins are the power sources for the I/O drivers of all non-analog output and bidirectional pins.
VSS	2, 15, 28, 40, 52, 65, 78, 90	Ground	I/O Ground These pins are the ground connections for the I/O drivers of all non-analog output and bidirectional pins.
VDD2	4, 54	Power	Digital Core Power Supply These pins are the power sources for the digital core logic and receivers of all non-analog input and bidirectional pins.
VSS2	27, 77	Ground	Digital Core Ground These pins are the ground connections for the digital core logic and receivers of all non-analog input and bidirectional pins.

6 Package Information

The VSC055-01 device is available in two package types. VSC055KM-01 is a 100-pin, plastic quad flat package (QFP) with a 20 mm body width, 14 mm body length, 2.7 mm body thickness, 0.65 mm pitch, and 3.1 mm maximum height. The device is also available in a lead(Pb)-free package, VSC055XKM-01.

Lead(Pb)-free products from Maxim comply with the temperatures and profiles defined in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

6.1 Thermal Specifications

Thermal specifications for this device are based on the JEDEC standard EIA/JESD51-2 and have been modeled using a four-layer test board with two signal layers, a power plane, and a ground plane (2s2p PCB). For more information, see the JEDEC standard.

Table 33. Thermal Resistances

Part Order Number	θ_{JC}	θ_{JA} (°C/W) vs. Airflow (ft/min)		
		0	100	200
VSC055KM-01	25.9	48.78	45.04	43.31
VSC055XKM-01	21.6	45.68	41.94	40.22

To achieve results similar to the modeled thermal resistance measurements, the guidelines for board design described in the JEDEC standard EIA/JESD51 series must be applied. For information about specific applications, see the following:

EIA/JESD51-5, *Extension of Thermal Test Board Standards for Packages with Direct Thermal Attachment Mechanisms*

EIA/JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*

EIA/JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

EIA/JESD51-10, *Test Boards for Through-Hole Perimeter Leaded Package Thermal Measurements*

EIA/JESD51-11, *Test Boards for Through-Hole Area Array Leaded Package Thermal Measurements*

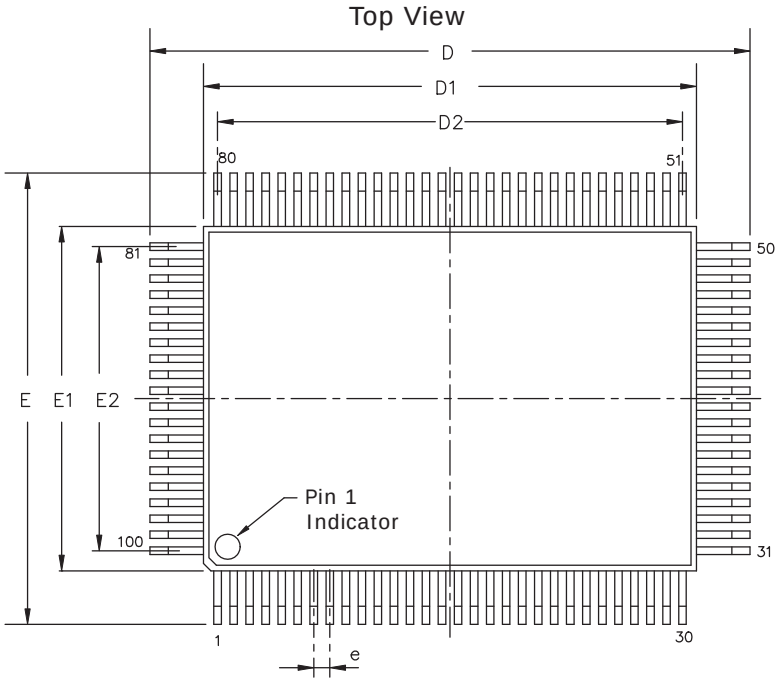
6.2 Moisture Sensitivity

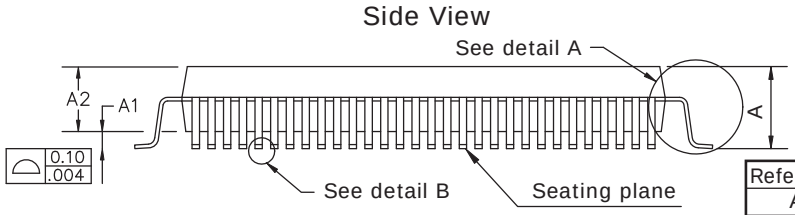
This device is rated moisture sensitivity level 3 or better as specified in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

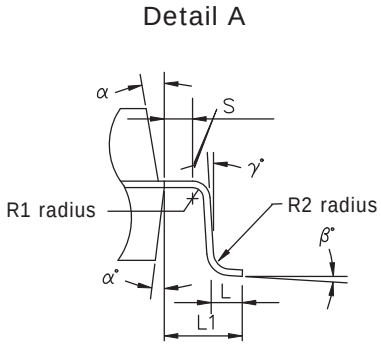
6.3 Package Drawing

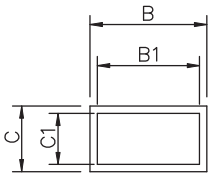
The following illustration shows the package drawing for the VSC055-01 device. The drawing contains the top view, side view, detail views, dimensions, tolerances, and notes.

Figure 11. Package Drawing









All dimensions and tolerances in millimeters.

Dimensions and Tolerances

Reference	Minimum	Nominal	Maximum
A		3.04	3.10
A1	0.10	0.23	0.36
A2	2.57	2.71	2.87
B	0.22		0.38
B1	0.22	0.30	0.36
C	0.13		0.23
C1	0.11	0.15	0.19
D	23.65	23.90	24.15
D1	19.90	20.00	20.10
D2		18.85	
E	17.65	17.90	18.15
E1	13.90	14.00	14.10
E2		12.35	
e		0.65	
L	0.73	0.88	1.03
L1		1.95 REF.	
R1	0.13		
R2		0.30	
S	0.40		
α°	12		16
β°	0		7
γ°	0		

7 Ordering Information

The VSC055-01 device is available in two package types. VSC055KM-01 is a 100-pin plastic QFP. The device is also available in a lead(Pb)-free package, VSC055XKM-01.

Lead(Pb)-free products from Maxim comply with the temperatures and profiles defined in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

Table 34. Ordering Information

Part Number	Description
VSC055KM-01	100-pin, plastic quad flat package (QFP) with a 20 mm body width, 14 mm body length, 2.7 mm body thickness, 0.65 mm pitch, and 3.1 mm maximum height
VSC055XKM-01	Lead(Pb)-free, 100-pin, plastic quad flat package (QFP) with a 20 mm body width, 14 mm body length, 2.7 mm body thickness, 0.65 mm pitch, and 3.1 mm maximum height

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