19-4614; Rev 0; 4/09

Z86L88

Low-Voltage IR Micro-controller

Product Specification

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Features

Table 1 lists some of the features of the Z86L88 microcontroller.

Table 1. Z86L88 Features

Device	ROM (KB)	RAM* (Bytes)	I/O Lines	Voltage Range
Z86L88	16	237	23	2.0 V to 3.6 V

Note: *General purpose

- Low power consumption—40 mW (typical)
- Three standby modes
  - STOP—2 μA (typical)
  - HALT—0.8 mA (typical)
  - Low voltage
- Special architecture to automate both generation and reception of complex pulses or signals:
  - One programmable 8-bit counter/timer with two capture registers and two load registers
  - One programmable 16-bit counter/timer with one 16-bit capture register pair and one 16-bit load register pair
  - Programmable input glitch filter for pulse reception
- Five priority interrupts
  - Three external
  - Two assigned to counter/timers
- Low voltage protection
- Programmable watch-dog/power-on reset circuits
- Two independent comparators with programmable interrupt polarity
- Mask-selectable pull-up transistor on Ports 0, 2, and 3
- Programmable mask options:
  - Oscillator selection: RC oscillator versus crystal or other clock source

- Oscillator operational mode: normal high-frequency operation enabled versus 32-KHz operation enabled
- Port 0: 0–3 pull-ups
- Port 0: 4–7 pull-ups
- Port 2: 0–7 pull-ups
- Port 3: pull-ups
- Port 0: 0–3 Mouse Mode: Normal Mode (.5V_{DD} input threshold) versus Mouse Mode (.4V_{DD} input threshold)

Note: The mask option pull-up transistor has a *typical* equivalent resistance of 200 KΩ ±50% at V_{CC}=3 V and 450 KΩ ±50% at V_{CC}=2 V.

General Description

The Z86L88 is a ROM-based member of the Z8 MCU single-chip family of infrared (IR) controllers, featuring 237 bytes of general-purpose RAM and 16 KB of ROM, respectively. Maxim's CMOS microcontrollers offer fast executing, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, automated pulse generation/reception, and internal key-scan pull-up transistors.

The Z86L88 architecture is based on Maxim's 8-bit microcontroller core featuring an Expanded Register File to allow access to register-mapped peripherals, I/O circuits, and powerful counter/timer circuitry. The Z8 offers a flexible I/O scheme, an efficient register and address-space structure, and a number of ancillary features that are useful in many consumer, automotive, computer peripheral, and battery-operated hand-held applications.

Three basic address spaces are available to support a wide range of configurations: program memory, register file, and Expanded Register File. The register file consists of 256 bytes of RAM. It includes 4 I/O port registers, 16 control and status registers, and 236 general-purpose registers. [Register FEh (SPH) can be used as a general-purpose register.] The Expanded Register File consists of two additional register groups (F and D).

The Z86L88 offers a new intelligent counter/timer architecture with 8-bit and 16-bit counter/timers (Figure 1). Also included are a large number of user-selectable modes and two on-board comparators to process analog signals with separate reference voltages (see Figure 9 on page 18).

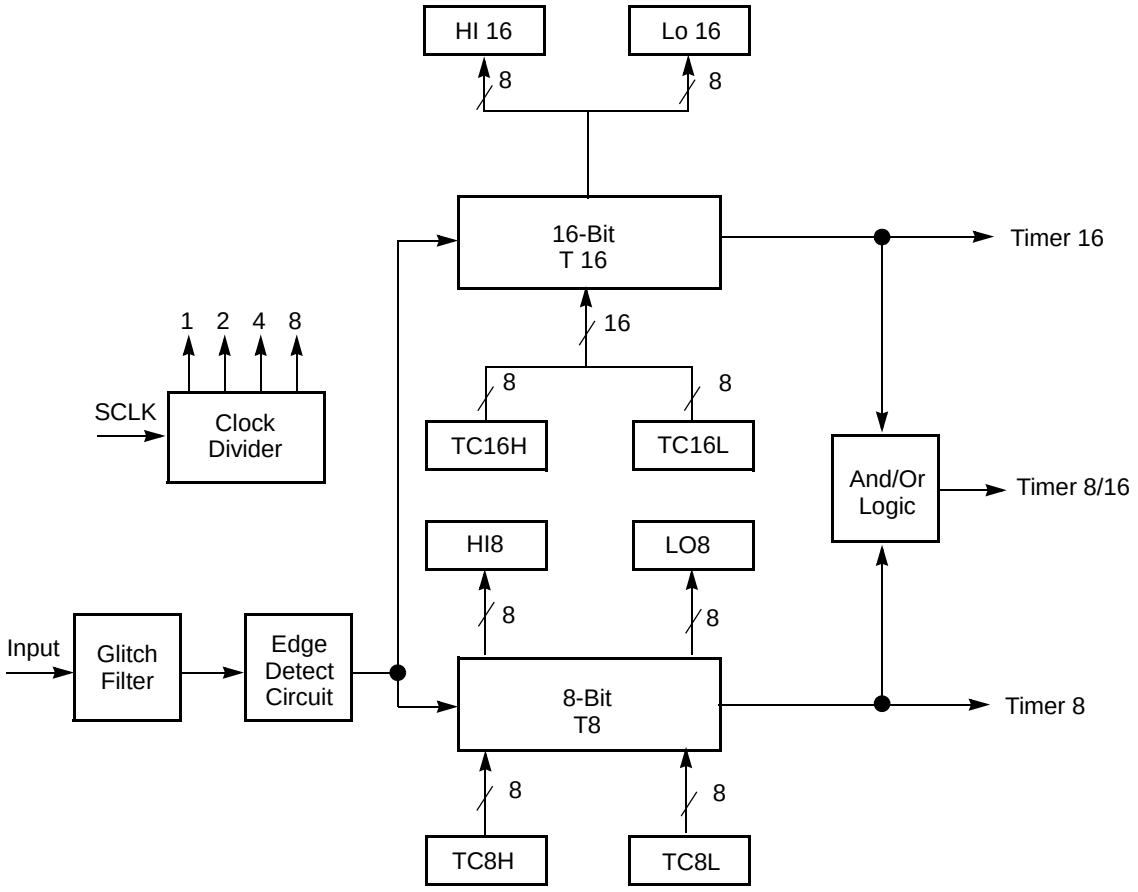


Figure 1. Counter/Timers Diagram

Note: All signals with an overline, "‾", are active Low. For example, B/$\overline{W}$, in which WORD is active Low, and $\overline{B}$/W, in which BYTE is active Low.

Power connections follow the conventions listed in Table 2.

Table 2. Power Conventions

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

Figure 2 shows the functional block diagram.

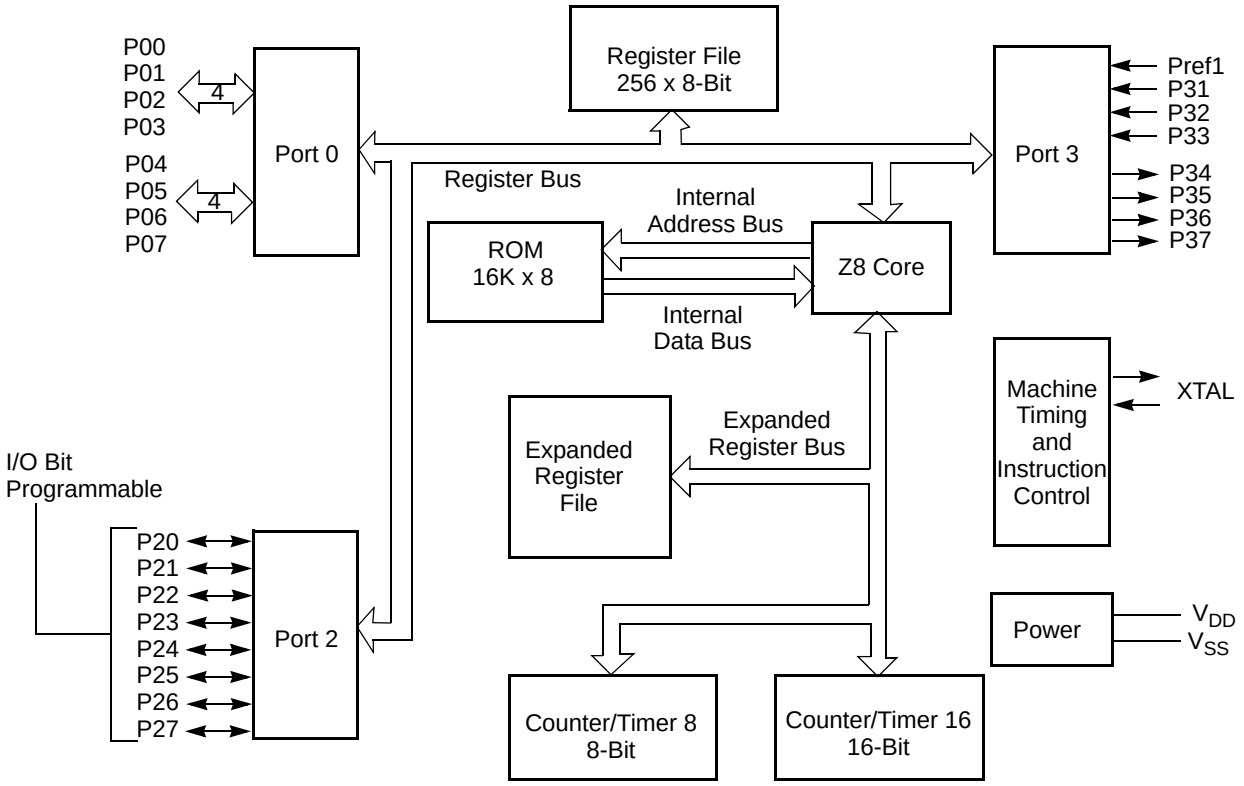


Figure 2. Functional Block Diagram

Pin Description

The pin assignment for the 28-pin dual in-line package (DIP)/small outline integrated circuit (SOIC) is shown in Figure 3. The pins are identified in Table 3.

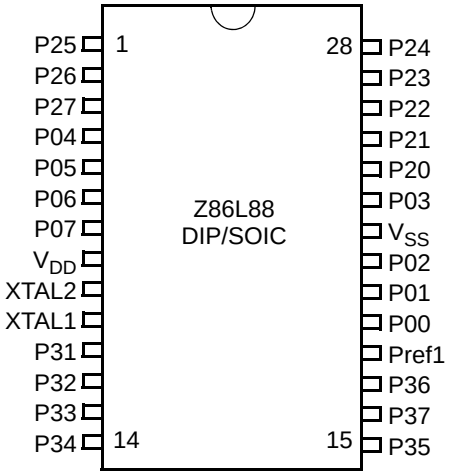


Figure 3. 28-Pin DIP/SOIC Pin Assignment

Table 3. 28-Pin DIP and SOIC Pin Identification

28-Pin DIP and SOIC	Standard Mode	Direction	Description
19	P00	Input/Output	Port 0 is nibble programmable.
20	P01	Input/Output	Port 0–3 can be configured as a
21	P02	Input/Output	mouse/trackball input.
23	P03	Input/Output	
4	P04	Input/Output	
5	P05	Input/Output	
6	P06	Input/Output	
7	P07	Input/Output	
24	P20	Input/Output	Port 2 pins are individually
25	P21	Input/Output	configurable as input or output.
26	P22	Input/Output	
27	P23	Input/Output	
28	P24	Input/Output	
1	P25	Input/Output	
2	P26	Input/Output	
3	P27	Input/Output	
18	Pref1	Input	Analog ref input; connect to V_{CC} if not used

Table 3. 28-Pin DIP and SOIC Pin Identification (Continued)

28-Pin DIP and SOIC	Standard Mode	Direction	Description
11	P31	Input	IRQ2/modulator input
12	P32	Input	IRQ0
13	P33	Input	IRQ1
14	P34	Output	T8 output
15	P35	Output	T16 output
17	P36	Output	T8/T16 output
16	P37	Output	
10	XTAL1	Input	Crystal, oscillator clock
9	XTAL2	Output	Crystal, oscillator clock
8	V_{DD}		Power supply
22	V_{SS}		Ground

Absolute Maximum Ratings

Table 4 lists the absolute maximum ratings for the Z86L88 microcontroller.

Table 4. Absolute Maximum Ratings

Symbol	Description	Min	Max	Units
V_{max}	Supply Voltage (*)	–0.3	+7.0	V
T_{STG}	Storage Temperature	–65°	+150°	C
T_A	Oper. Ambient Temperature		†	C

Notes:
* Voltage on all pins with respect to GND
† See “Ordering Information” on page 69.

Stresses greater than those listed under Absolute Maximum Ratings might cause permanent damage to the device. This rating is a stress rating only. Functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period might affect device reliability.

Standard Test Conditions

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Figure 4).

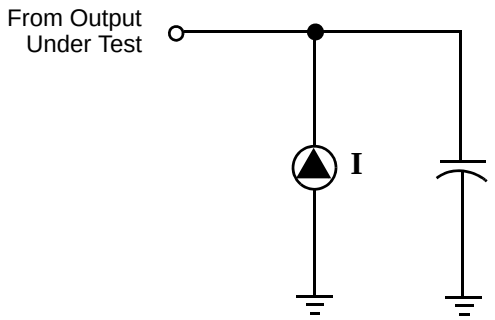


Figure 4. Test Load Diagram

Capacitance

Table 5 lists the capacitance for the Z86L88 microcontrollers.

Table 5. Capacitance

Parameter	Max
Input capacitance	12 pF
Output capacitance	12 pF
I/O capacitance	12 pF

Note: T_A = 25°C, V_{CC} = GND = 0 V, f = 1.0 MHz, unmeasured pins returned to GND.

DC Characteristics

Table 6 lists the direct current (DC) characteristics.

Table 6. DC Characteristics

			T_A = 0 °C to +70 °C				
Symbol	**Parameter**	**V_{CC}**	**Min**	**Max**	**Units**	**Conditions**	**Notes**
	Max Input Voltage	2.0 V		7	V	I_{IN} <250 µA	
		3.6 V		7	V	I_{IN} <250 µA	
V_{CH}	Clock Input High Voltage	2.0 V	0.8 V_{CC}	V_{CC} + 0.3	V	Driven by External Clock Generator	
		3.6 V	0.8 V_{CC}	V_{CC} + 0.3	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	2.0 V	V_{SS}–0.3	0.2 V_{CC}	V	Driven by External Clock Generator	
		3.6 V	V_{SS}–0.3	0.2 V_{CC}	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	2.0 V	0.7 V_{CC}	V_{CC} + 0.3	V		
		3.6 V	0.7 V_{CC}	V_{CC} + 0.3	V		
V_{IL}	Input Low Voltage	2.0 V	V_{SS}–0.3	0.2 V_{CC}	V		
		3.6 V	V_{SS}–0.3	0.2 V_{CC}	V		
V_{OH1}	Output High Voltage	2.0 V	V_{CC}–0.4		V	I_{OH} = –0.5 mA	1
		3.6 V	V_{CC}–0.4		V	I_{OH} = –0.5 mA	
V_{OH2}	Output High Voltage	2.0 V	V_{CC}–0.8		V	I_{OH} = –7 mA	
	(P00, P01, P36, and P37)	3.6 V	V_{CC}–0.8		V	I_{OH} = –7 mA	
V_{OL1}	Output Low Voltage	2.0 V		0.4	V	I_{OL} = 1.0 mA	1
		3.6 V		0.4	V	I_{OL} = 4.0 mA	
V_{OL2}	Output Low Voltage	2.0 V		0.8	V	I_{OL} = 5.0 mA	1
		3.6 V		0.8	V	I_{OL} = 7.0 mA	
V_{OL2}	Output Low Voltage	2.0 V		0.8	V	I_{OL} = 10 mA	
	(P00, P01, P36, and P37)	3.6 V		0.8	V	I_{OL} = 10 mA	
V_{OFFSET}	Comparator Input Offset Voltage	2.0 V		25	mV		
		3.6 V		25	mV		
I_{IL}	Input Leakage	2.0 V	–1	1	µA	V_{IN} = 0 V, V_{CC}	
		3.6 V	–1	1	µA	V_{IN} = 0 V, V_{CC}	
I_{OL}	Output Leakage	2.0 V	–1	1	µA	V_{IN} = 0 V, V_{CC}	
		3.6 V	–1	1	µA	V_{IN} = 0 V, V_{CC}	

Table 6. DC Characteristics (Continued)

			T_A = 0 °C to +70 °C				
Symbol	**Parameter**	**V_{CC}**	**Min**	**Max**	**Units**	**Conditions**	**Notes**
I_{CC}	Supply Current	2.0 V		10	mA	at 8.0 MHz	2, 3
		3.6 V		15	mA	at 8.0 MHz	2, 3
		2.0 V		250	µA	at 32 kHz	2, 3, 8
		3.6 V		850	µA	at 32 kHz	2, 3, 8
I_{CC1}	Standby Current (HALT Mode)	2.0 V		3	mA	V_{IN} = 0 V, V_{CC} at 8.0 MHz	2, 3
		3.6 V		5	mA	Same as above	2, 3
		2.0 V		2	mA	Clock Divide-by-16 at 8.0 MHz	2, 3
		3.6 V		4	mA	Same as above	2, 3
I_{CC2}	Standby Current (STOP Mode)	2.0 V		8	µA	V_{IN} = 0 V, V_{CC} WDT is not Running	4, 6, 9
		3.6 V		10	µA	Same as above	4, 6, 9
		2.0 V		500	µA	V_{IN} = 0 V, V_{CC} WDT is Running	4, 6, 9
		3.6 V		800	µA	Same as above	4, 6, 9
T_{POR}	Power-On Reset	2.0 V	12	75	ms		
		3.6 V	5	20	ms		
V_{BO}	V_{CC} Low Voltage Protection			2.0	V	8 MHz max Ext. CLK Freq.	5

Notes:
1. All outputs excluding P00, P01, P36, and P37
2. All outputs unloaded, inputs at rail
3. CL1 = CL2 = 100 pF
4. Same as note 2 except inputs at V_{CC}
5. The V_{BO} is measured at room temperature and typically is 1.6 V. V_{BO} increases as the temperature decreases.
6. Oscillator stopped
7. Not applicable
8. 32-kHz clock driver input
9. WDT, Comparators, Low Voltage Detection, and ADC (if applicable) are disabled. The IC might draw more current if any of the above peripherals is enabled.

AC Characteristics

This section discusses the alternating current (AC) characteristics. The timing diagram is shown in Figure 5 and described in Table 7.

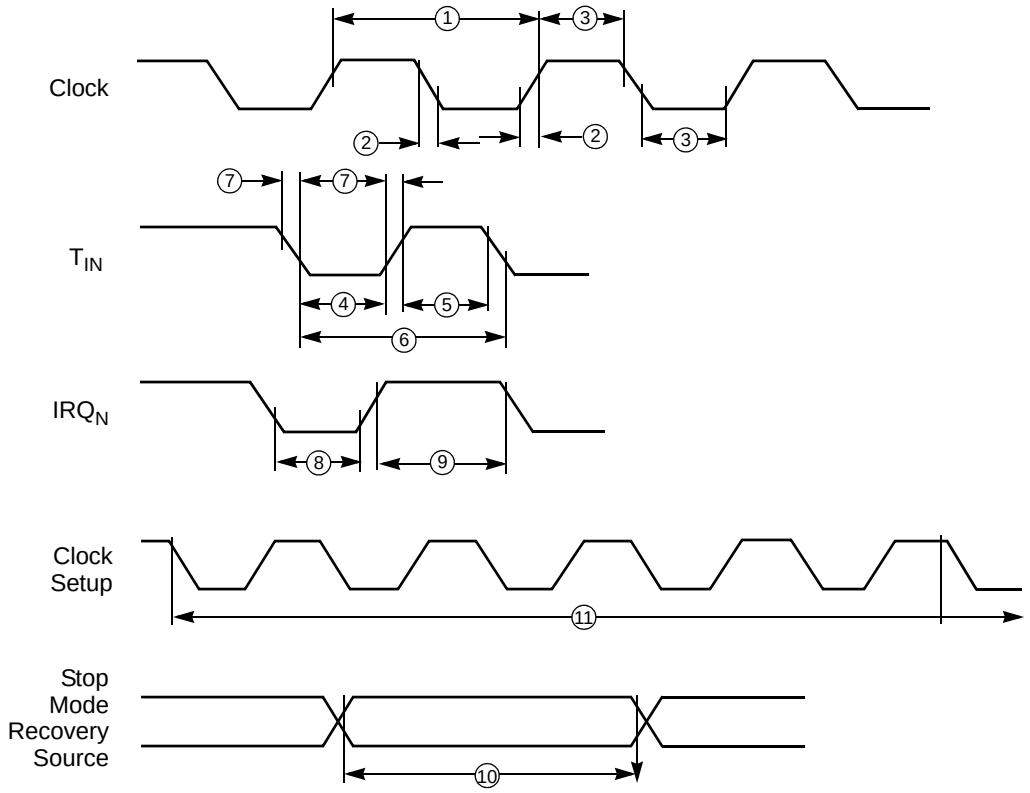


Figure 5. Timing Diagram

Table 7. AC Characteristics

				T_A = 0°C to +70°C 8.0 MHz				Stop-Mode Recovery (D1, D0)
Number	**Symbol**	**Parameter**	**V_{CC}**	**Min**	**Max**	**Units**	**Notes**	
1	TpC	Input Clock Period	2.0 V	121	DC	ns	1	
			3.6 V	121	DC	ns	1	
2	TrC,TfC	Clock Input Rise and Fall Times	2.0 V		25	ns	1	
			3.6 V		25	ns	1	
3	TwC	Input Clock Width	2.0 V	37		ns	1	
			3.6 V	37		ns	1	
4	TwTinL	Timer Input Low Width	2.0 V	100		ns	1	
			3.6 V	70		ns	1	
5	TwTinH	Timer Input High Width	2.0 V	3TpC			1	
			5.5 V	3TpC			1	
6	TpTin	Timer Input Period	2.0 V	8TpC			1	
			3.6 V	8TpC			1	
7	TrTin,TfTin	Timer Input Rise and Fall Times	2.0 V		100	ns	1	
			3.6 V		100	ns	1	
8A	TwIL	Interrupt Request Low Time	2.0 V	100		ns	1, 2	
			3.6 V	70		ns	1, 2	
8B	TwIL	Interrupt Request Low Time	2.0 V	5TpC			1, 3	
			3.6 V	5TpC			1, 3	
9	TwIH	Interrupt Request Input High Time	2.0 V	5TpC			1, 2	
			3.6 V	5TpC			1, 2	
10	Twsm	Stop-Mode Recovery Width Spec	2.0 V	12		ns		
			3.6 V	12		ns		
11	Tost	Oscillator Start-Up Time	2.0 V		5TpC		4	
			3.6 V		5TpC		4	

Table 7. AC Characteristics (Continued)

			T_A = 0°C to +70°C 8.0 MHz					Stop-Mode Recovery (D1, D0)
Number	**Symbol**	**Parameter**	**V_{CC}**	**Min**	**Max**	**Units**	**Notes**	
12	Twdt	Watch-Dog Timer Delay Time	2.0 V	20		ms	5	0, 0
			3.6 V	7.5		ms	5	
			2.0 V	20		ms	5	0, 1
			3.6 V	7.5		ms	5	
			2.0 V	40		ms	5	1, 0
			3.6 V	15		ms	5	
		(60 ms)	2.0 V	160		ms	5	1, 1
			3.6 V	60		ms	5	

Notes:
1. Timing Reference uses 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0.
2. Interrupt request through Port 3 (P33–P31)
3. Interrupt request through Port 3 (P30)
4. SMR – D5 = 0.
5. For internal RC oscillator

Pin Functions

XTAL1 Crystal 1 (Time-Based Input)

This pin connects a parallel-resonant crystal, ceramic resonator, LC, or RC network to the on-chip oscillator input. An external single-phase clock to the on-chip oscillator input is also an option.

XTAL2 Crystal 2 (Time-Based Output)

This pin connects a parallel-resonant crystal, ceramic resonant, LC, or RC network to the on-chip oscillator output.

Port 0 (P07–P00)

Port 0 is an 8-bit, bidirectional, CMOS-compatible port. These eight I/O lines are configured under software control as a nibble I/O port. The output drivers are push-pull or open drain controlled by bit D2 in the PCON register. If one or both nibbles are required for I/O operation, they must be configured by writing to the Port 0 mode register. After a hardware reset, Port 0 is configured as an input port.

A mask option is available to program 0.4 V_{DD} CMOS trip inputs on P00–P03. This option allows direct interface to mouse/trackball IR sensors.

An optional pull-up transistor is available as a mask option on all Port 0 bits with nibble select. See Figure 6.

Note: Internal pull-ups are disabled on any given pin or group of port pins when programmed into output mode.

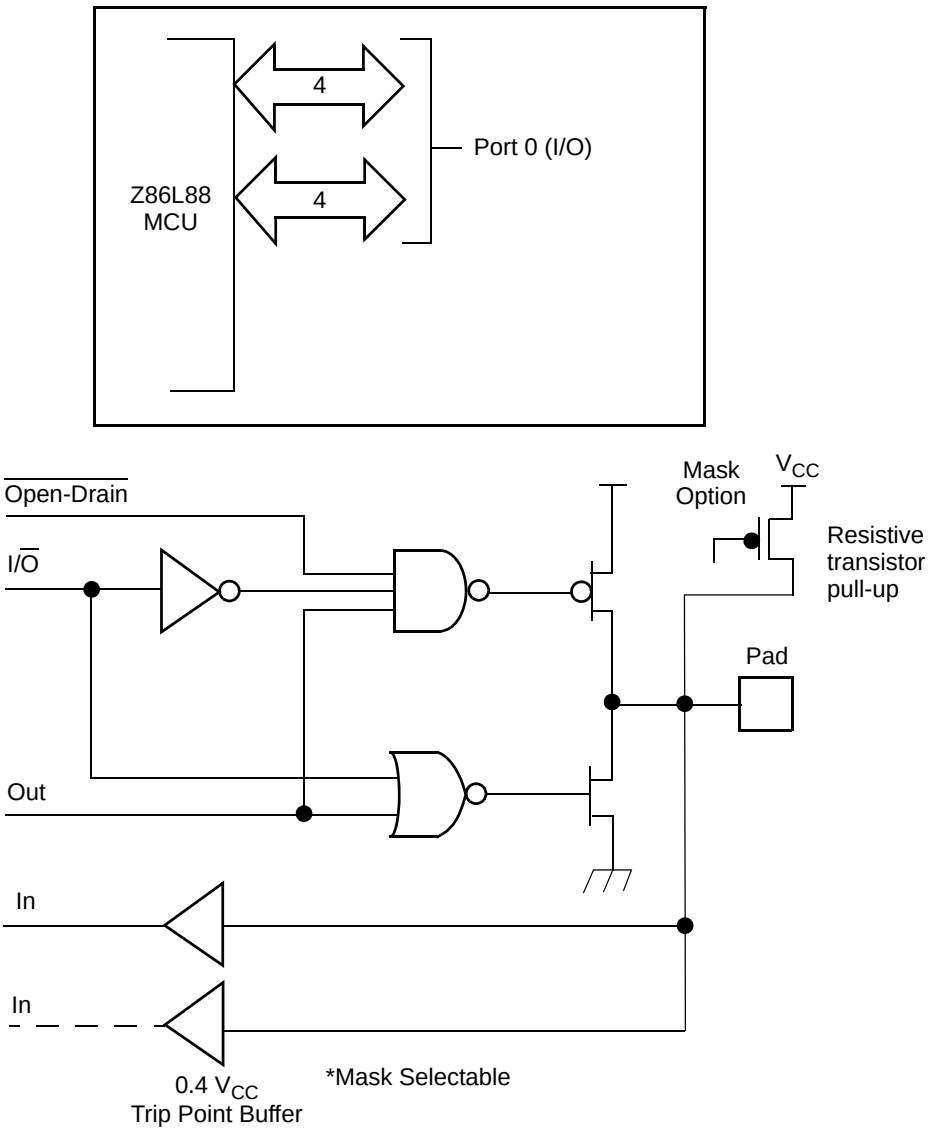


Figure 6. Port 0 Configuration

Port 2 (P27–P20)

Port 2 is an 8-bit, bidirectional, CMOS-compatible I/O port. These eight I/O lines can be independently configured under software control as inputs or outputs. Port 2 is always available for I/O operation. A mask option is available to connect eight pull-up transistors on this port. Bits programmed as outputs are globally programmed as either push-pull or open-drain. The POR resets with the 8 bits of Port 2 configured as inputs.

Port 2 also has an 8-bit input OR and AND gate that can be used to wake up the part. P20 can be programmed to access the edge-detection circuitry in demodulation mode. See Figure 7.

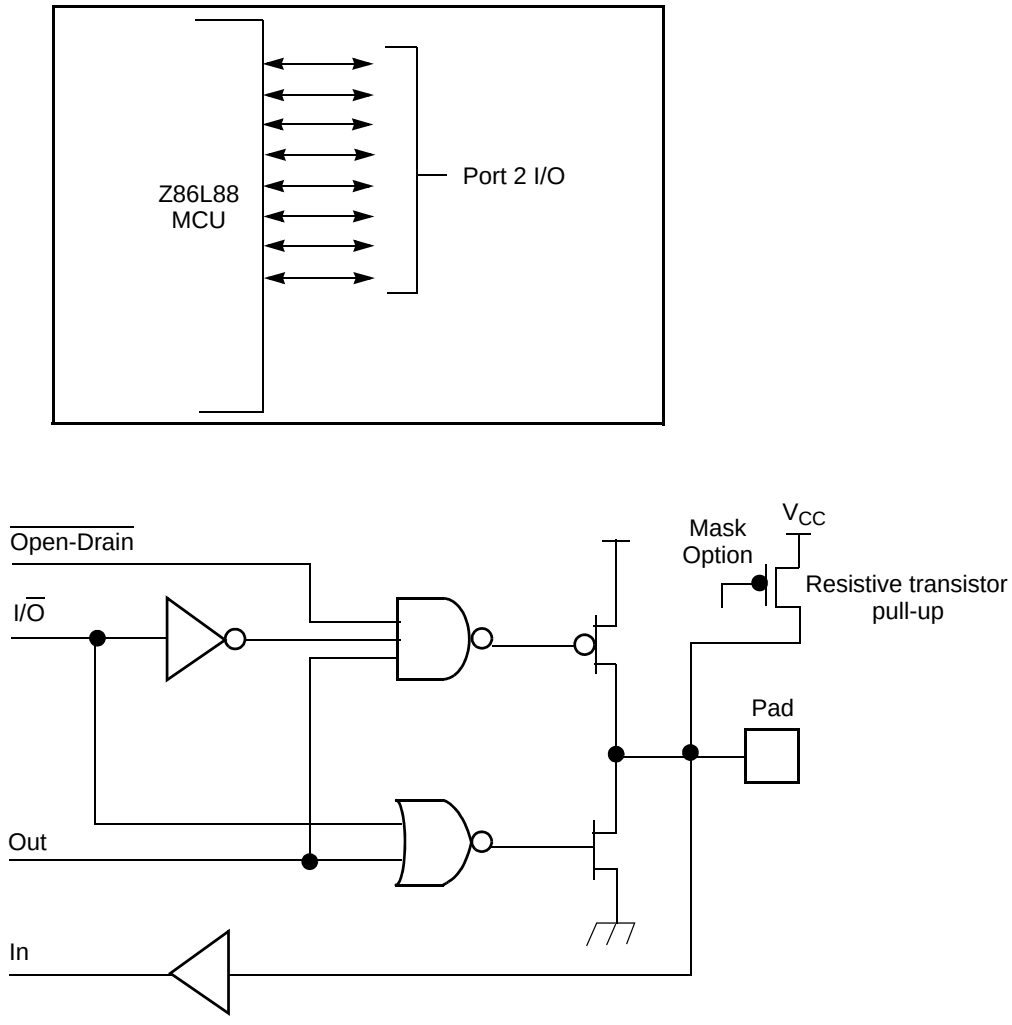


Figure 7. Port 2 Configuration

Port 3 (P37–P31)

Port 3 (see Figure 8) is a 7-bit, CMOS-compatible, fixed I/O port. Port 3 consists of three fixed input (P33–P31) and four fixed output (P37–P34) ports, and each can be configured under software control for interrupt and output from the counter/timers. P31, P32, and P33 are standard CMOS inputs; P34, P35, P36, and P37 are push-pull outputs.

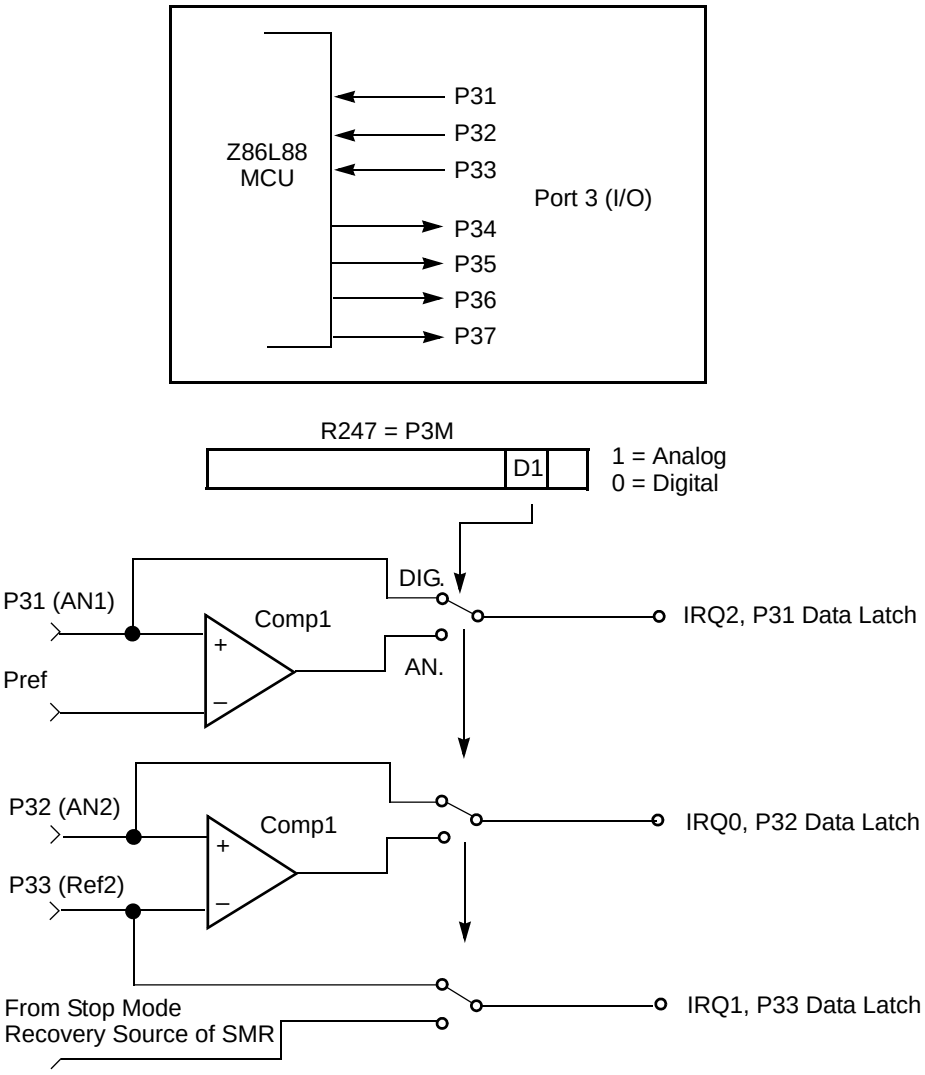


Figure 8. Port 3 Configuration

Two on-board comparators process analog signals on P31 and P32 with reference to the voltage on Pref1 and P33. The analog function is enabled by

programming the Port 3 Mode Register (bit 1). P31 and P32 are programmable as rising, falling, or both edge-triggered interrupts (IRQ register bits 6 and 7). Pref1 and P33 are the comparator reference voltage inputs. Access to the counter/timer edge-detection circuit is through P31 or P20 (see “Common Control Register to Counter/Timer T8 and T16” on page 39). Other edge-detect and IRQ modes are described in Table 8.

Table 8. Pin Assignments

Pin	I/O	C/T	Comp.	Int.
Pref1			RF1	
P31	IN	IN	AN1	IRQ2
P32	IN		AN2	IRQ0
P33	IN		RF2	IRQ1
P34	OUT	T8	AO1	
P35	OUT	T16		
P36	OUT	T8/16		
P37	OUT		AO2	
P20	I/O	IN		

Port 3 also provides output for the counter/timers and the AND/OR logic. Control is performed by programming bits D5–D4 of CTR1, bit 0 of CTR0, and bit 0 of CTR2.

Comparator Inputs

In analog mode, P31 and P32 have a comparator front end. The comparator reference is supplied to Pref1 and P33. In this mode, the P33 internal data latch and its corresponding IRQ1 are diverted to the SMR sources (excluding P31, P32, and P33) as indicated in Figure 8 on page 16. In digital mode, P33 is used as D3 of the Port 3 input register, which then generates IRQ1.

Note: Comparators are powered down by entering STOP Mode. For P31–P33 to be used in a Stop-Mode Recovery source, these inputs must be placed into digital mode.

Comparator Outputs

These outputs can be programmed to be output on P34 and P37 through the PCON register. See Figure 9.

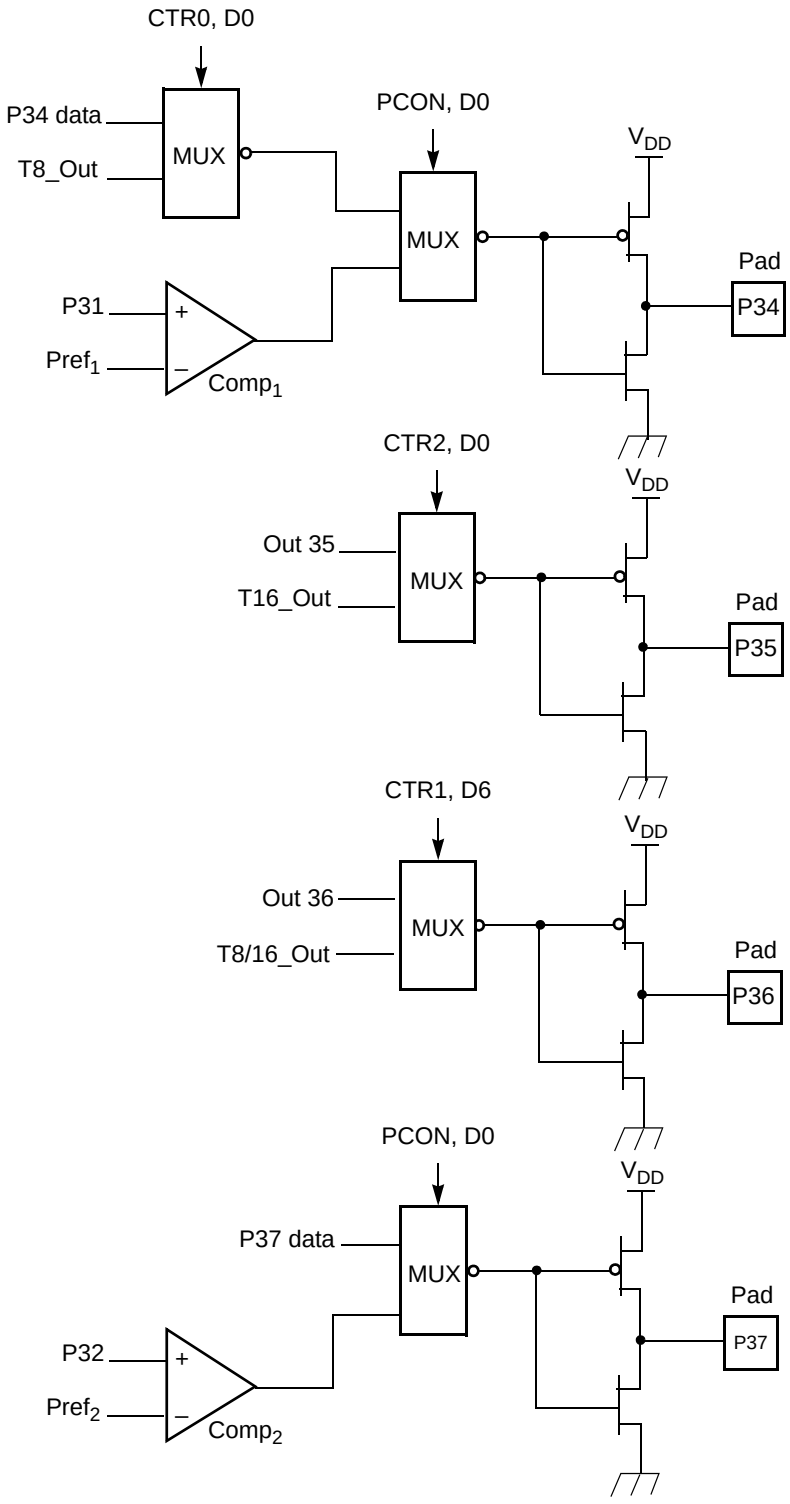


Figure 9. Port 3 Counter/Timer Output Configuration

Functional Description

The Z86L88 incorporates special functions to enhance the Z8's functionality in consumer and battery-operated applications.

Program Memory

The Z86L88 device addresses 16 KB of internal program memory. The first 12 bytes are reserved for interrupt vectors. These locations contain the five 16-bit vectors that correspond to the five available interrupts.

RAM

The Z86L88 device has 237 bytes of RAM that make up the register file.

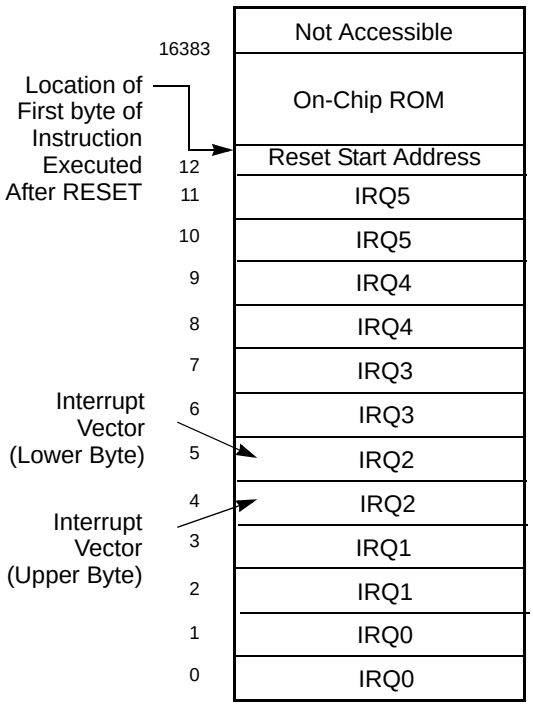


Figure 10. Program Memory Map (16K ROM)

Expanded Register File

The register file has been expanded to allow for additional system control registers and for mapping of additional peripheral devices into the register address area. The Z8 register address space R0 through R15 has been implemented as

16 banks with 16 registers per bank. These register groups are known as the Expanded Register File (ERF). Bits 7–4 of register RP select the working register group. Bits 3–0 of register RP select the expanded register file bank.

Note: An expanded register bank is also referred to as an expanded register group (see Figure 11).

The upper nibble of the register pointer (Figure 12 on page 22) selects which working register group is accessed of 16 bytes in the register file, out of the possible 256. The lower nibble selects the expanded register file bank and, in the case of the Z86L88 device, banks 0, F, and D are implemented. A 0h in the lower nibble allows the normal register file (bank 0) to be addressed, but any other value from 1h to Fh exchanges the lower 16 registers to an expanded register bank. For example, for the Z86L88 (see Figure 11):

```
R253 RP = 00h
     R0 = Port 0
     R1 = Port 1
     R2 = Port 2
     R3 = Port 3
```

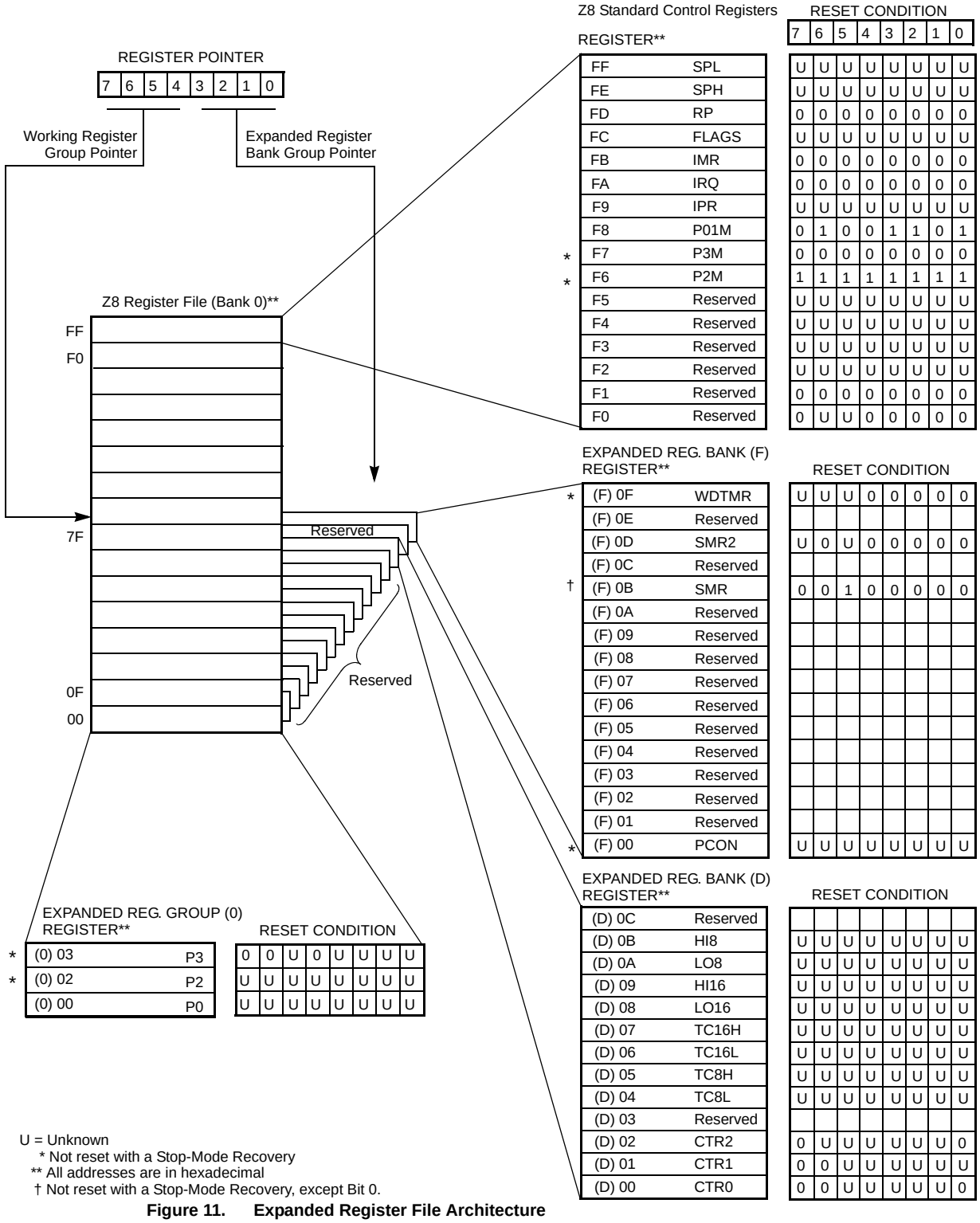
But if:

```
R253 RP = 0Dh
     R0 = CTRL0
     R1 = CTRL1
     R2 = CTRL2
     R3 = Reserved
```

The counter/timers are mapped into ERF group D. Access is easily performed using the following:

```
LD          RP, #0Dh    ; Select ERF D for access to bank D
                        ; (working register group 0)
LD          R0,#xx      ; load CTRL0
LD          1, #xx      ; load CTRL1
LD          R1, 2       ; CTRL2→CTRL1

LD          RP, #0Dh    ; Select ERF D for access to bank D
                        ; (working register group 0)
LD          RP, #7Dh    ; Select expanded register bank D
                        ; working register group 7 of bank 0
                        ; for access.
LD          71h, 2      ; CTRL2→register 71h
LD          R1, 2       ; CTRL2→register 71h
```



U = Unknown
* Not reset with a Stop-Mode Recovery
** All addresses are in hexadecimal
† Not reset with a Stop-Mode Recovery, except Bit 0.

Figure 11. Expanded Register File Architecture

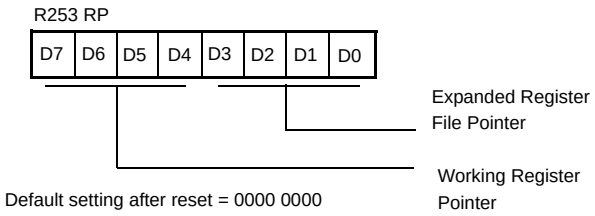


Figure 12. Register Pointer Register

Expanded Register File Control Registers (0D)

Figure 13, Figure 14, and Figure 15 show the expanded register file control registers (0D).

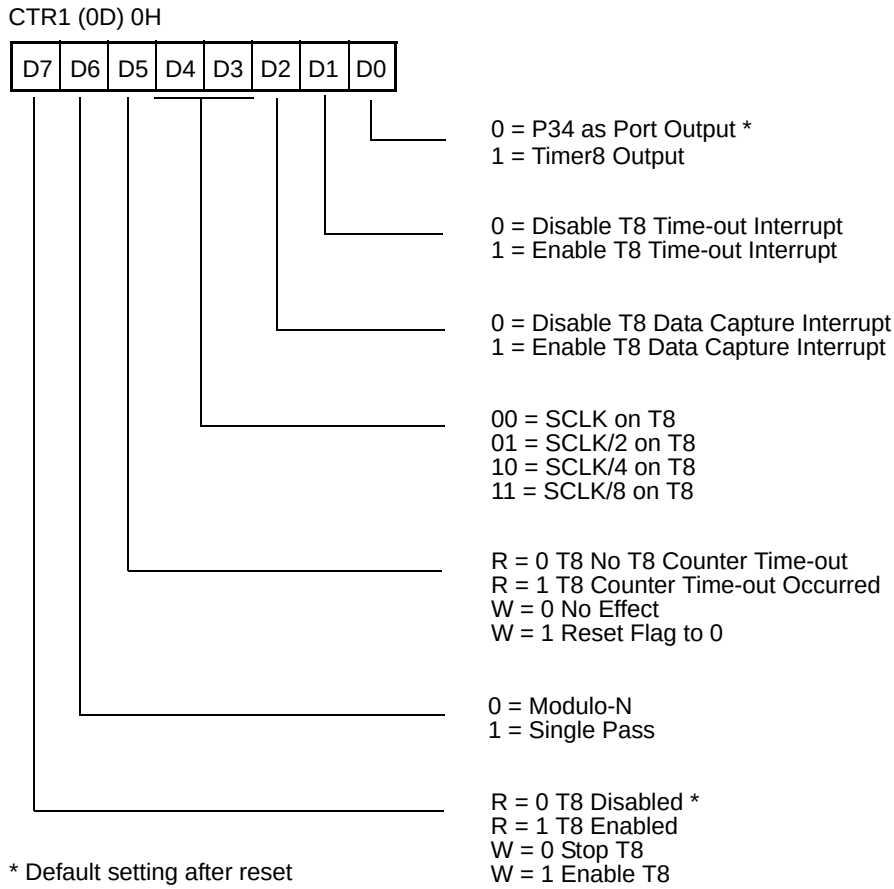


Figure 13. TC8 Control Register—(0D) OH: Read/Write Except Where Noted

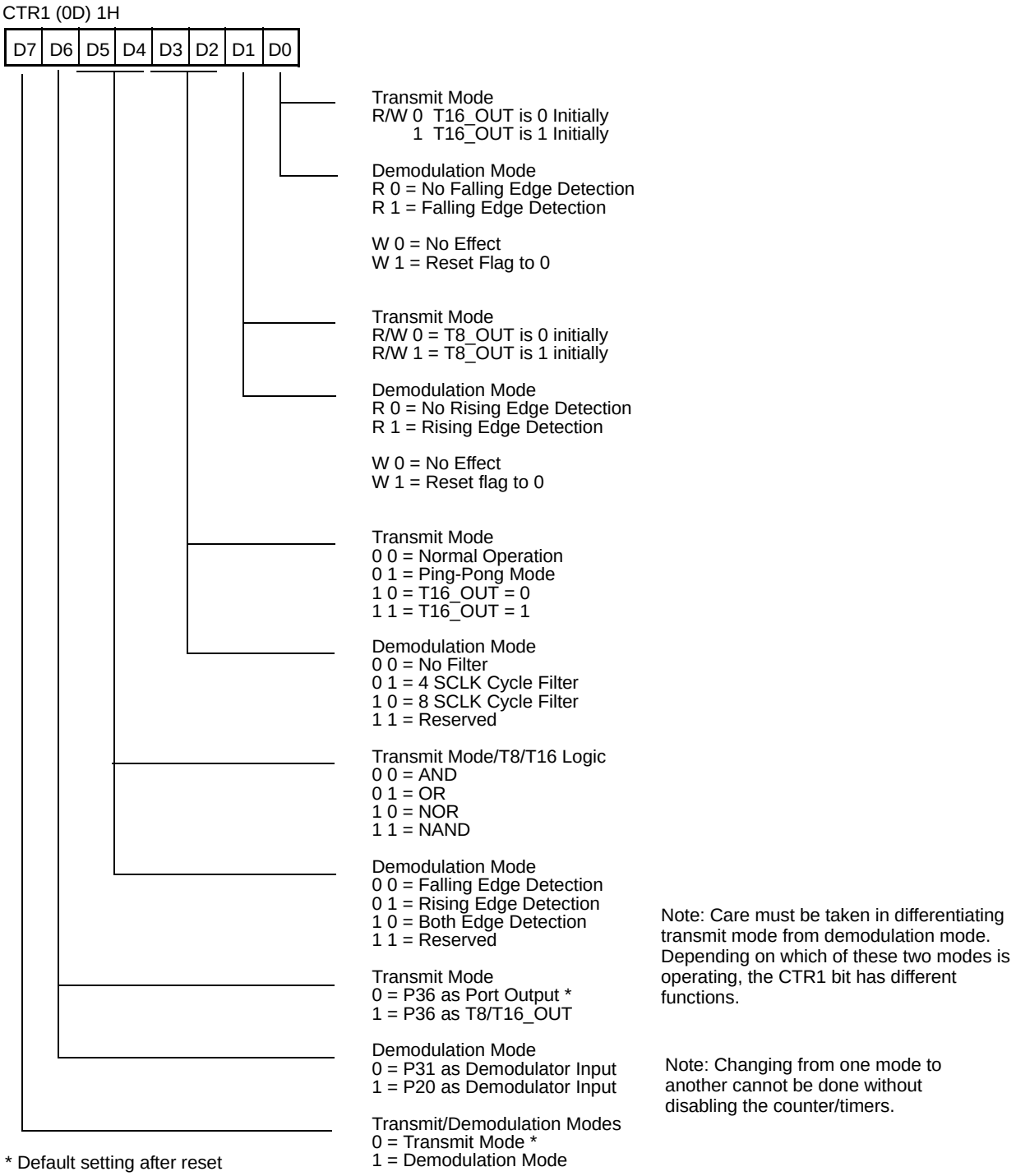


Figure 14. T8 and T16 Common Control Functions—(0D) 1H: Read/Write

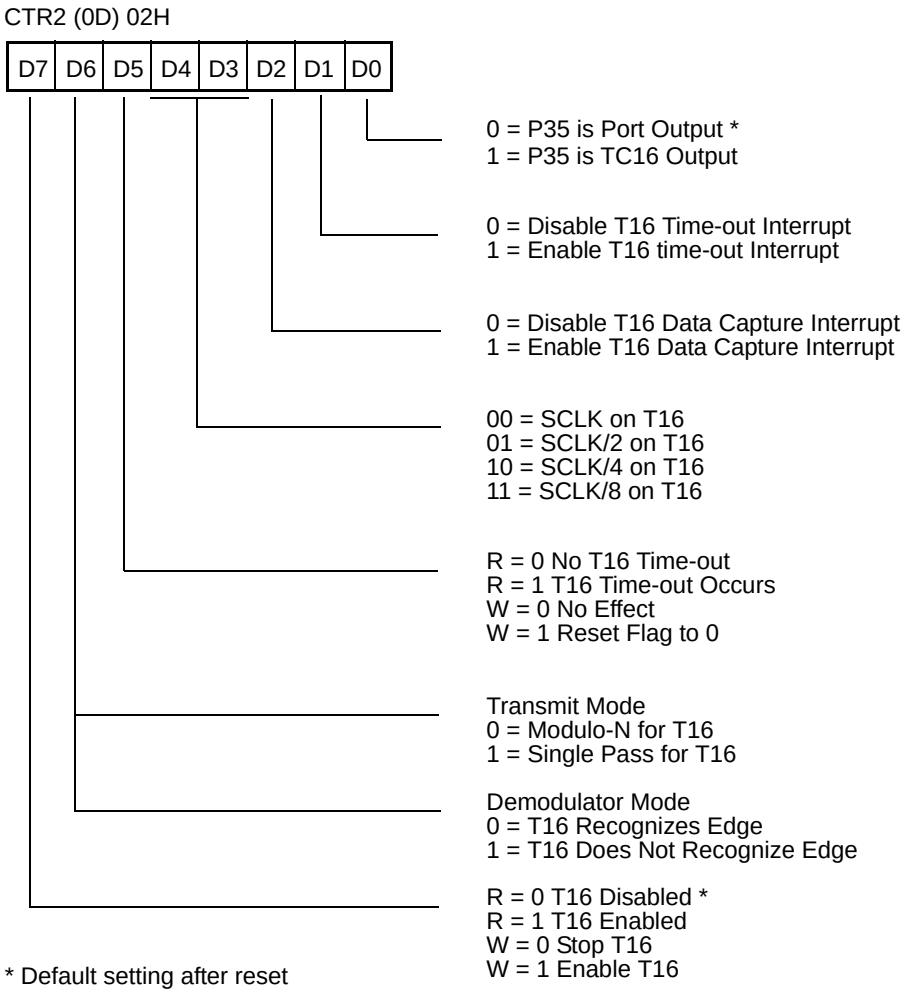
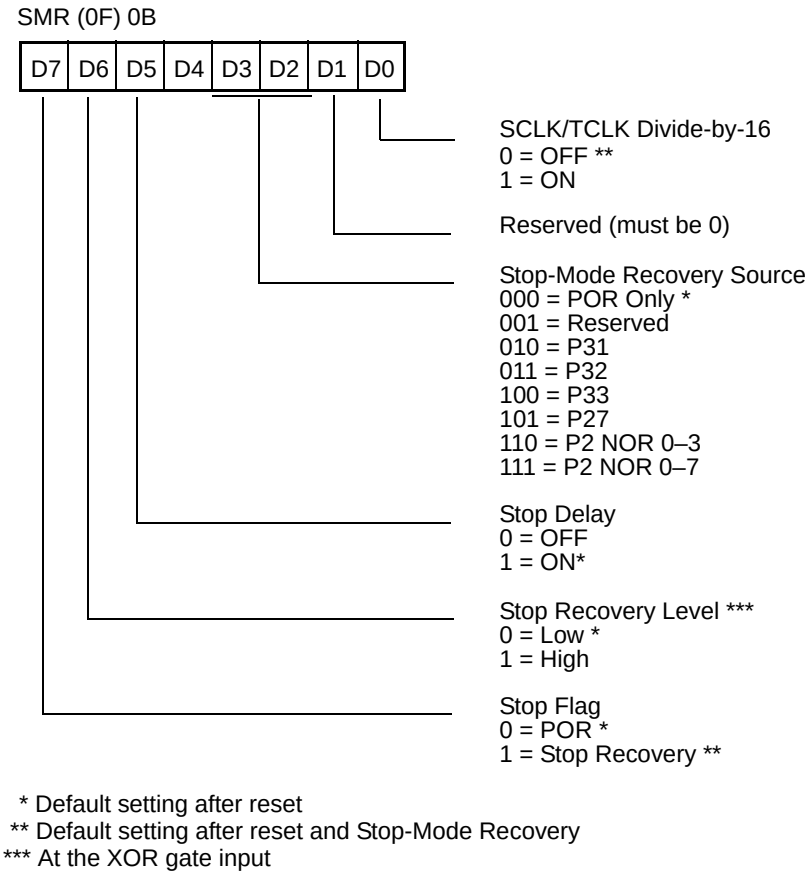


Figure 15. T16 Control Register—(0D) 2H: Read/Write Except Where Noted

Expanded Register File Control Registers (0F)

Figure 16 through Figure 29 show the expanded register file control registers (0F).



* Default setting after reset
** Default setting after reset and Stop-Mode Recovery
*** At the XOR gate input

Figure 16. Stop-Mode Recovery Register—(0F) 0BH: D6–D0 = Write Only, D7 = Read Only

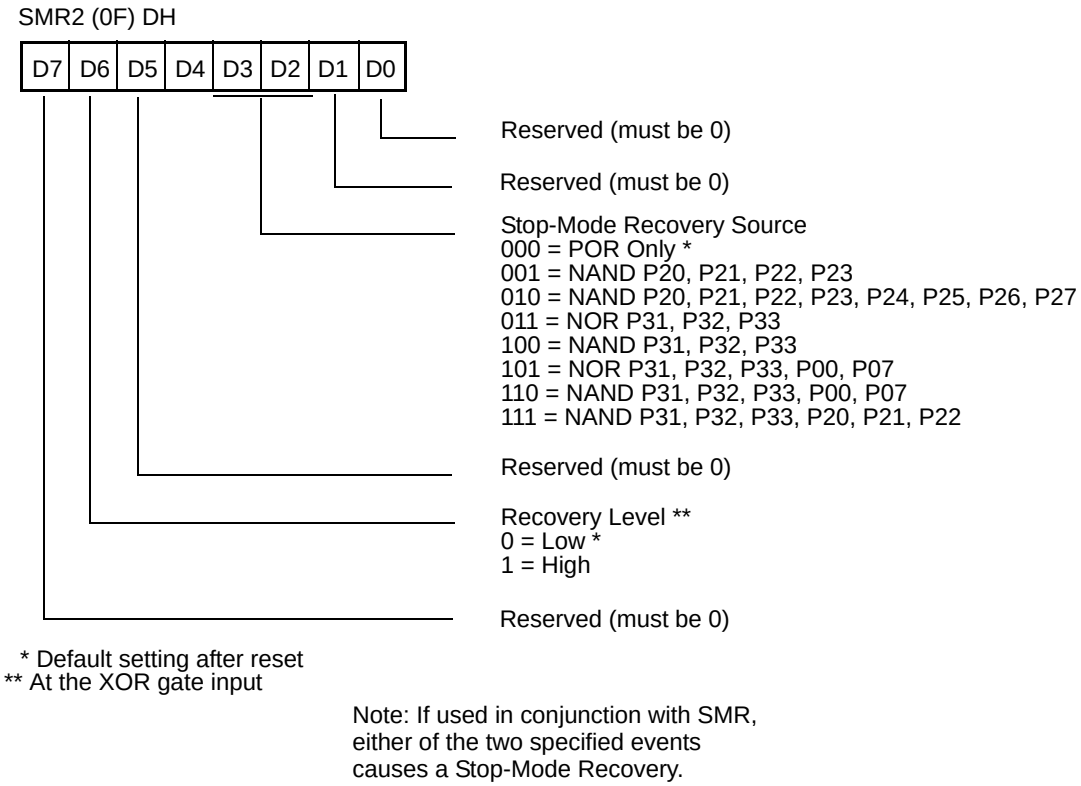
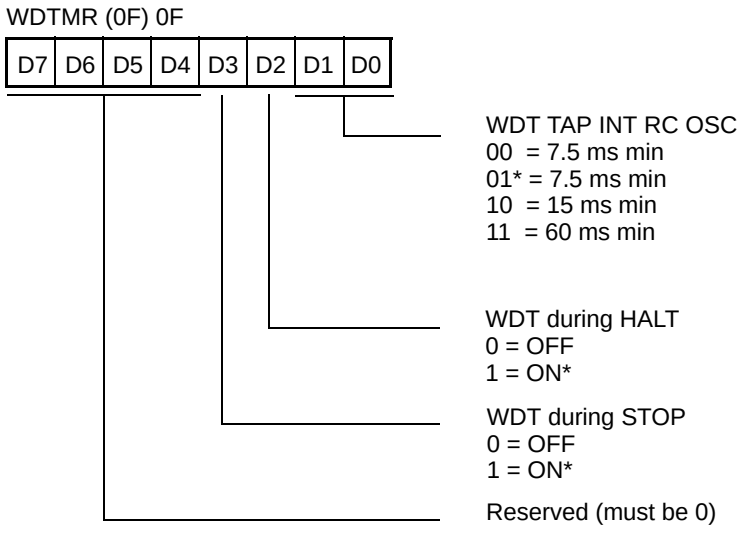
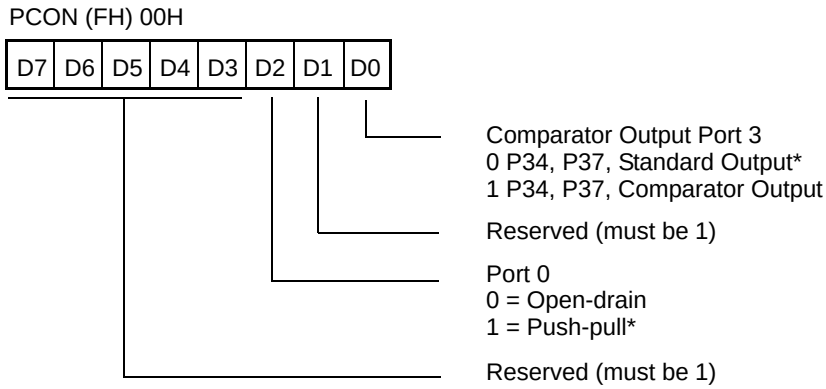


Figure 17. Stop-Mode Recovery Register 2—(0F) 0DH: D2–D4, D6 Write Only



* Default setting after reset

Figure 18. Watch-Dog Timer Register—(0F) 0FH: Write Only



*Default setting after reset

Figure 19. Port Configuration Register (PCON)—(0F) 0H: Write Only

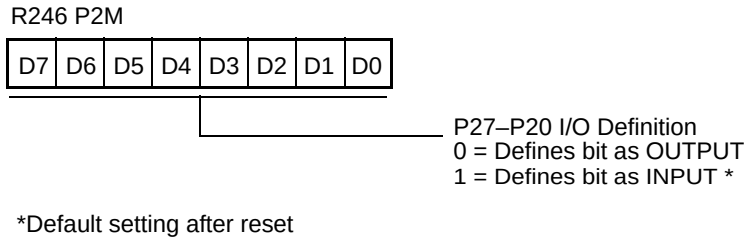


Figure 20. Port 2 Mode Register—F6H: Write Only

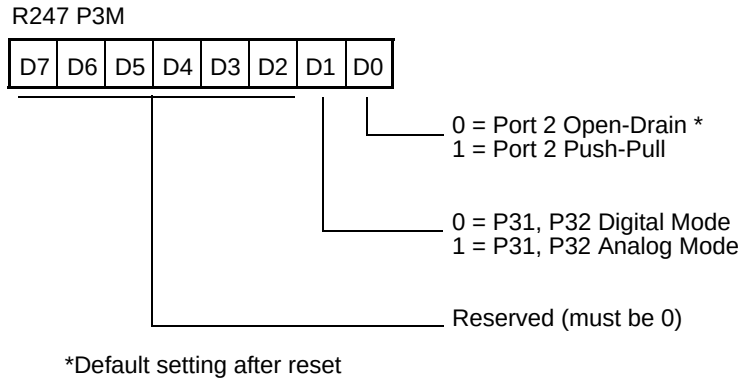
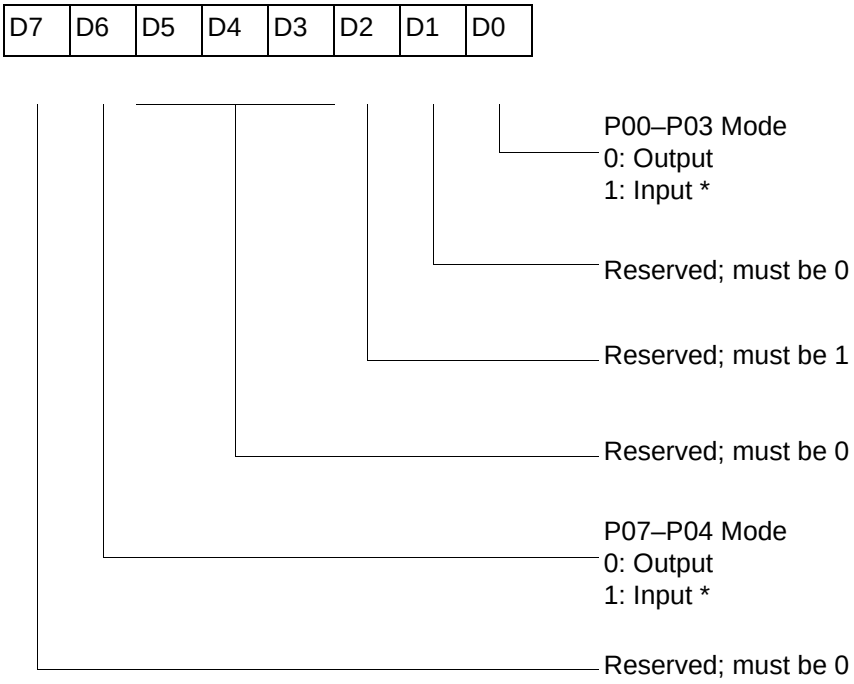


Figure 21. Port 3 Mode Register—F7H: Write Only

R248 P01M



* Default setting after reset

Figure 22. Port 0 and 1 Mode Register (F8h: Write Only)

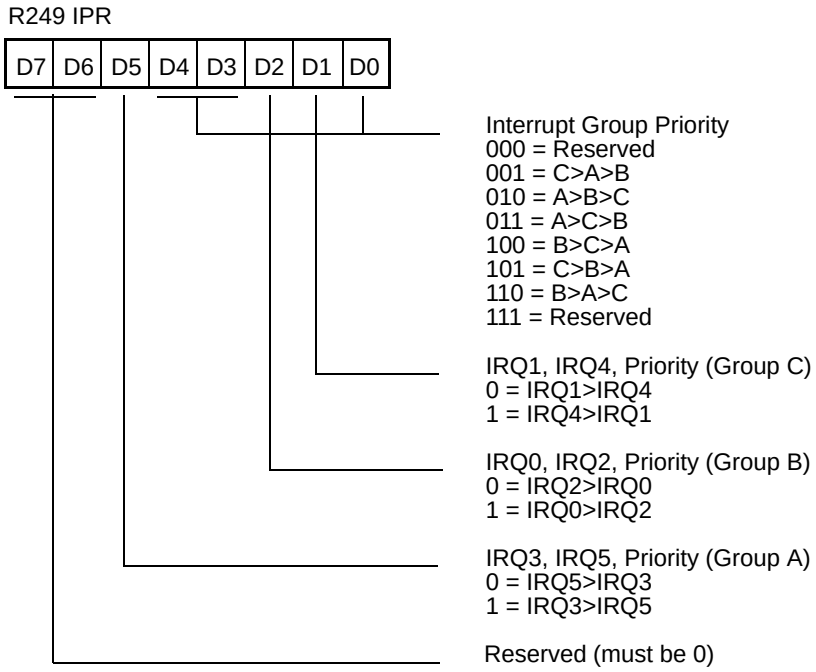


Figure 23. Interrupt Priority Register—F9H: Write Only

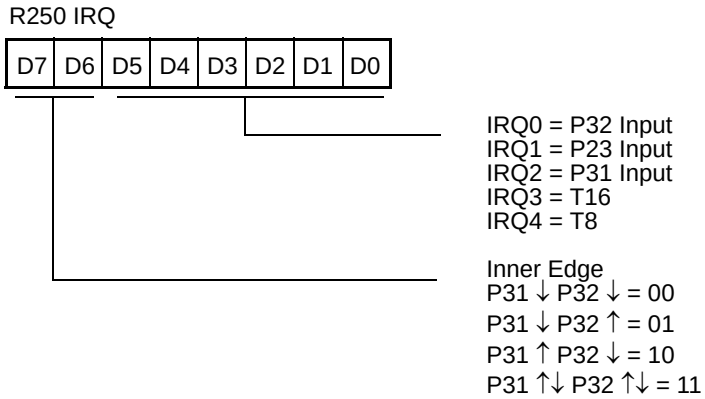
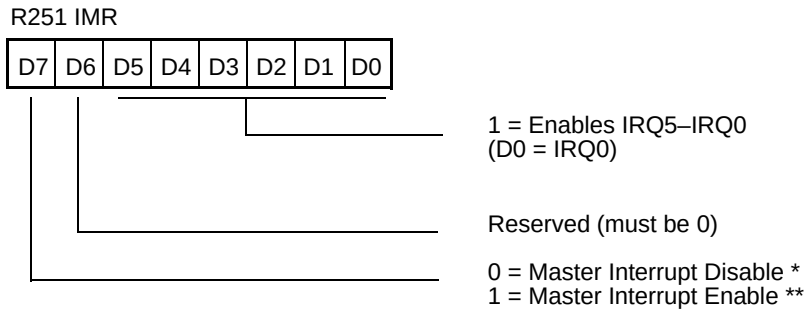


Figure 24. Interrupt Request Register—FAH: Read/Write



* Default setting after reset
** Only by using E1, D1 instruction. D1 is required before changing the IMR register.

Figure 25. Interrupt Mask Register—FBH: Read/Write

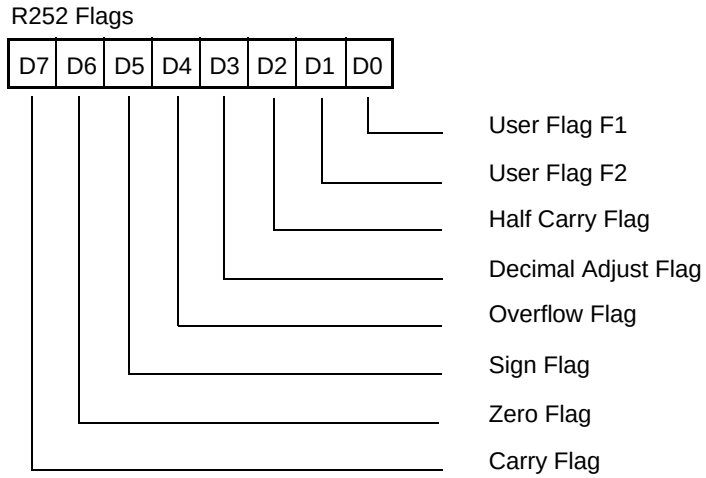


Figure 26. Flag Register—FCH: Read/Write

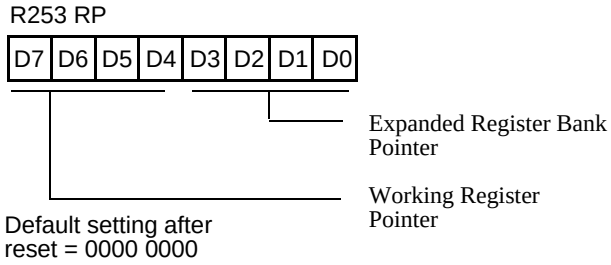


Figure 27. Register Pointer—FDH: Read/Write

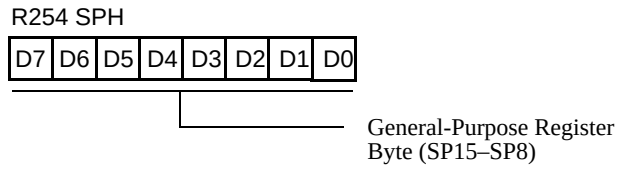


Figure 28. Stack Pointer High—FEH: Read/Write

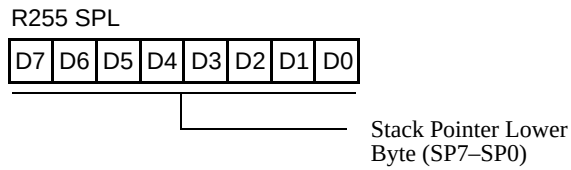


Figure 29. Stack Pointer Low—FFH: Read/Write

Register File

The register file (bank 0) consists of 4 I/O port registers, 237 general-purpose registers, and 16 control and status registers (R0–R3, R4–R239, and R240–255, respectively). Additionally, there are two expanded registers groups in Banks D and F. Instructions can access registers directly or indirectly through an 8-bit address field, thereby allowing a short, 4-bit register address to use the Register Pointer (Figure 30). In the 4-bit mode, the register file is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working register group.

Note: Working register group E0–EF can only be accessed through working registers and indirect addressing modes.

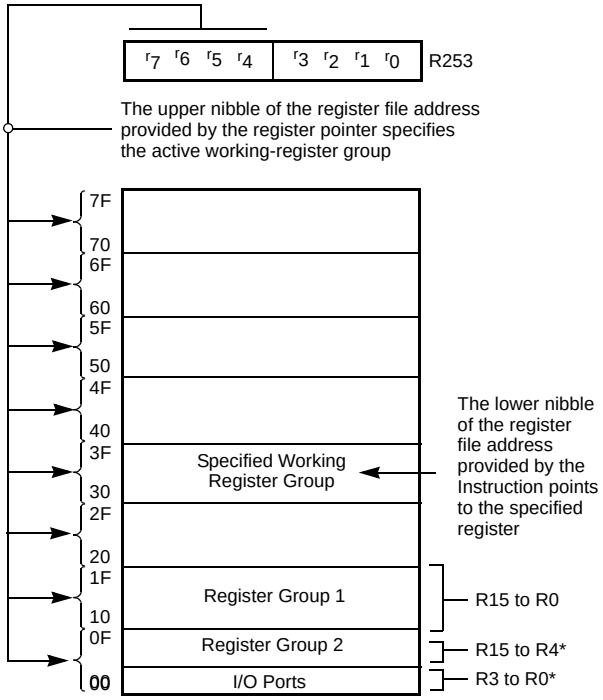


Figure 30. Register Pointer

Stack

The Z86L88 internal register file is used for the stack. An 8-bit Stack Pointer (R255) is used for the internal stack that resides in the general-purpose registers (R4–R239). SPH is used as a general-purpose register only when using internal stacks.

Counter/Timer Registers

Table 9 describes the expanded register group D.

Table 9. Expanded Register Group D

(D)0Ch	LVD
(D)0Bh	HI8
(D)0Ah	LO8
(D)09h	HI16
(D)08h	LO16
(D)07h	TC16H
(D)06h	TC16L
(D)05h	TC8H
(D)04h	TC8L
(D)03h	Reserved
(D)02h	CTR2
(D)01h	CTR1
(D)00h	CTR0

HI8(D)0Bh

This register (Table 10) holds the captured data from the output of the 8-bit Counter/Timer0. This register is typically used to hold the number of counts when the input signal is 1.

Table 10. HI8(D)0Bh

Field	Bit Position		Description
T8_Capture_HI	76543210	R W	Captured Data No Effect

L08(D)0Ah

This register (Table 11) holds the captured data from the output of the 8-bit Counter/Timer0. This register is typically used to hold the number of counts when the input signal is 0HI16(D)09h.

Table 11. L08(D)0Ah

Field	Bit Position		Description
T8_Capture_L0	76543210	R W	Captured Data No Effect

HI16(D)09h

This register (Table 12) holds the captured data from the output of the 16-bit Counter/Timer16. This register also holds the MS-Byte of the data.

Table 12. HI16(D)09h

Field	Bit Position		Description
T16_Capture_HI	76543210	R W	Captured Data No Effect

L016(D)08h

This register (Table 13) holds the captured data from the output of the 16-bit Counter/Timer16. This register also holds the LS-Byte of the data.

Table 13. L016(D)08h

Field	Bit Position		Description
T16_Capture_LO	76543210	R W	Captured Data No Effect

TC16H(D)07h

Table 14 describes the Counter/Timer2 MS-Byte Hold Register.

Table 14. TC16H(D)07h

Field	Bit Position		Description
T16_Data_HI	76543210	R/W	Data

TC16L(D)06h

Table 15 describes the Counter/Timer2 LS-Byte Hold Register.

Table 15. TC16L(D)06h

Field	Bit Position		Description
T16_Data_LO	76543210	R/W	Data

TC8H(D)05h

Table 16 describes the Counter/Timer8 High Hold Register.

Table 16. TC8H(D)05h

Field	Bit Position		Description
T8_Level_HI	76543210	R/W	Data

TC8L(D)04h

Table 17 describes the Counter/Timer8 Low Hold Register.

Table 17. TC8L(D)04h

Field	Bit Position		Description
T8_Level_LO	76543210	R/W	Data

CTR0 Counter/Timer8 Control Register

Table 18 describes the CTR0 (D)00 Counter/Timer8 Control Register.

Table 18. CTR0 (D)00 Counter/Timer8 Control Register

Field	Bit Position		Value	Description
T8_Enable	7-------	R	0*	Counter Disabled
			1	Counter Enabled
		W	0	Stop Counter
			1	Enable Counter
Single/Modulo-N	-6-------	R/W	0	Modulo-N
			1	Single Pass
Time_Out	--5------	R	0	No Counter Time-Out
			1	Counter Time-Out Occurred
		W	0	No Effect
			1	Reset Flag to 0
T8 _Clock	---43---	R/W	0 0	SCLK
			0 1	SCLK/2
			1 0	SCLK/4
			1 1	SCLK/8
Capture_INT_MASK	-----2--	R/W	0	Disable Data Capture Int.
			1	Enable Data Capture Int.
Counter_INT_Mask	------1-	R/W	0	Disable Time-Out Int.
			1	Enable Time-Out Int.
P34_Out	-------0	R/W	0*	P34 as Port Output
			1	T8 Output on P34

Note:
* Indicates the value upon Power-On Reset.

T8 Enable

This field enables T8 when set (written) to 1.

Single/Modulo-N

When set to 0 (modulo-n), the counter reloads the initial value when the terminal count is reached. When set to 1 (single pass), the counter stops when the terminal count is reached.

Time-Out

This bit is set when T8 times out (terminal count reached). To reset this bit, a 1 must be written to this location.

Caution: Writing a 1 is the only way to reset the Terminal Count status condition. Therefore, you must reset this bit before using/enabling the counter/timers.

The first clock of T8 might not exhibit complete clock width and can occur anytime when enabled.

Note: Care must be taken when using the OR or AND commands to manipulate CTR0, bit 5 and CTR1, bits 0 and 1 (demodulation mode). These instructions use a Read-Modify-Write sequence in which the current status from the CTR0 and CTR1 registers is ORed or ANDed with the designated value and then written back into the registers.

For example, when the status of bit 5 is 1, a timer reset condition occurs.

T8 Clock

This bit defines the frequency of the input signal to T8.

Capture_INT_Mask

Set this bit to allow an interrupt when data is captured into either LO8 or HI8 upon a positive or negative edge detection in demodulation mode.

Counter_INT_Mask

Set this bit to allow an interrupt when T8 has a time-out.

P34_Out

This bit defines whether P34 is used as a normal output pin or the T8 output.

Common Control Register to Counter/Timer T8 and T16

This register controls the functions in common with the T8 and T16. See Table 19.

Table 19. CTR1(D)01h Register

Field	Bit Position		Value	Description
Mode	7-------	R/W	0*	Transmit Mode
				Demodulation Mode
P36_Out/Demodulator_Input	-6------	R/W		Transmit Mode
			0*	Port Output
			1	T8/T16 Output
				Demodulation Mode
			0	P31
			1	P20
T8/T16_Logic/Edge _Detect	--54----	R/W		Transmit Mode
			00	AND
			01	OR
			10	NOR
			11	NAND
				Demodulation Mode
			00	Falling Edge
			01	Rising Edge
			10	Both Edges
			11	Reserved
Transmit_Submode/Glitch_Filter	----32--	R/W		Transmit Mode
			00	Normal Operation
			01	Ping-Pong Mode
			10	T16_Out = 0
			11	T16_Out = 1
				Demodulation Mode
			00	No Filter
			01	4 SCLK Cycle
			10	8 SCLK Cycle
			11	Reserved

Table 19. CTR1(D)01h Register (Continued)

Field	Bit Position		Value	Description
Initial_T8_Out/Rising_Edge	------1-			Transmit Mode
		R/W	0	T8_OUT is 0 Initially
			1	T8_OUT is 1 Initially
				Demodulation Mode
		R	0	No Rising Edge
			1	Rising Edge Detected
		W	0	No Effect
			1	Reset Flag to 0
Initial_T16_Out/Falling_Edge	-------0			Transmit Mode
		R/W	0	T16_OUT is 0 Initially
			1	T16_OUT is 1 Initially
				Demodulation Mode
		R	0	No Falling Edge
			1	Falling Edge Detected
		W	0	No Effect
			1	Reset Flag to 0

Note:
*Default upon Power-On Reset

Mode

If it is 0, the counter/timers are in the transmit mode; otherwise, they are in the demodulation mode.

P36_Out/Demodulator_Input

In transmit mode, this bit defines whether P36 is used as a normal output pin or the combined output of T8 and T16.

In demodulation mode, this bit defines whether the input signal to the counter/timers is from P20 or P31.

T8/T16_Logic/Edge_Detect

In transmit mode, this field defines how the outputs of T8 and T16 are combined (AND, OR, NOR, NAND).

In demodulation mode, this field defines which edge needs to be detected by the edge detector.

Transmit_Submode/Glitch_Filter

In transmit mode, this field defines whether T8 and T16 are in the “Ping-Pong” mode or in independent normal operation mode. Setting this field to “Normal

Operation Mode" terminates the "Ping-Pong Mode" operation. When this field is set to 10, T16 is immediately forced to a 0; a setting of 11 forces T16 to output a 1.

In demodulation mode, this field defines the width of the glitch that needs to be filtered out.

Initial_T8_Out/Rising_Edge

In transmit mode, if 0, the output of T8 is set to 0 when it starts to count. If 1, the output of T8 is set to 1 when it starts to count. When the counter is not enabled and this bit is set to 1 or 0, T8_OUT is set to the opposite state of this bit. This measure ensures that when the clock is enabled, a transition occurs to the initial state set by CTR1, D1.

In demodulation mode, this bit is set to 1 when a rising edge is detected in the input signal. In order to reset it, a 1 must be written to this location.

Initial_T16 Out/Falling_Edge

In transmit mode, if it is 0, the output of T16 is set to 0 when it starts to count. If it is 1, the output of T16 is set to 1 when it starts to count. This bit is effective only in Normal or Ping-Pong Mode (CTR1, D3, D2). When the counter is not enabled and this bit is set, T16_OUT is set to the opposite state of this bit. This measure ensures that when the clock is enabled, a transition occurs to the initial state set by CTR1, D0.

In demodulation mode, this bit is set to 1 when a falling edge is detected in the input signal. In order to reset it, a 1 must be written to this location.

Note: Modifying CTR1 (D1 or D0) while the counters are enabled causes unpredictable output from T8/16_OUT.

CTR2 Counter/Timer16 Control Register

Table 20 describes the contents of the CTR2 register.

Table 20. CTR2 (D)02h: Counter/Timer16 Control Register

Field	Bit Position		Value	Description
T16_Enable	7-------	R	0*	Counter Disabled
			1	Counter Enabled
		W	0	Stop Counter
			1	Enable Counter
Single/Modulo-N	-6------	R/W		Transmit Mode
			0	Modulo-N
			1	Single Pass
				Demodulation Mode
			0	T16 Recognizes Edge
			1	T16 Does Not Recognize Edge
Time_Out	--5-----	R	0	No Counter Time-Out
			1	Counter Time-Out Occurred
		W	0	No Effect
			1	Reset Flag to 0
T16 _Clock	---43---	R/W	00	SCLK
			01	SCLK/2
			10	SCLK/4
			11	SCLK/8
Capture_INT_Mask	-----2--	R/W	0	Disable Data Capture Int.
			1	Enable Data Capture Int.
Counter_INT_Mask	------1-	R/W	0	Disable Time-Out Int.
				Enable Time-Out Int.
P35_OUT	-------0	R/W	0*	P35 as Port Output
			1	T16 Output on P35

Note:
* Indicates the value upon Power-On Reset.

T16_Enable

This field enables T16 when set to 1.

Single/Modulo-N

In transmit mode, when this bit is set to 0, the counter reloads the initial value when the terminal count is reached. When this bit is set to 1, the counter stops when the terminal count is reached.

In demodulation mode, when this bit is set to 0, T16 captures and reloads on detection of all the edges. When this bit is set to 1, T16 captures and detects on the first edge but ignores the subsequent edges. For details, see “T16 Demodulation Mode” on page 51.

Time_Out

This bit is set when T16 times out (terminal count reached). To reset this bit, a 1 must be written to this location.

T16_Clock

This bit defines the frequency of the input signal to Counter/Timer16.

Capture_INT_Mask

This bit is set to allow an interrupt when data is captured into LO16 and HI16.

Counter_INT_Mask

This bit is set to allow an interrupt when T16 times out.

P35_Out

This bit defines whether P35 is used as a normal output pin or T16 output.

Counter/Timer Functional Blocks

The following are the counter/timer functional blocks:

- Input circuit
- Eight-bit counter/timer circuits (page 44)
- Sixteen-bit counter/timer circuits (page 50)
- Output circuit (page 54)

Input Circuit

The edge detector monitors the input signal on P31 or P20. Based on CTR1 D5–D4, a pulse is generated at the Pos Edge or Neg Edge line when an edge is detected. Glitches in the input signal that have a width less than specified (CTR1 D3, D2) are filtered out (see Figure 31).

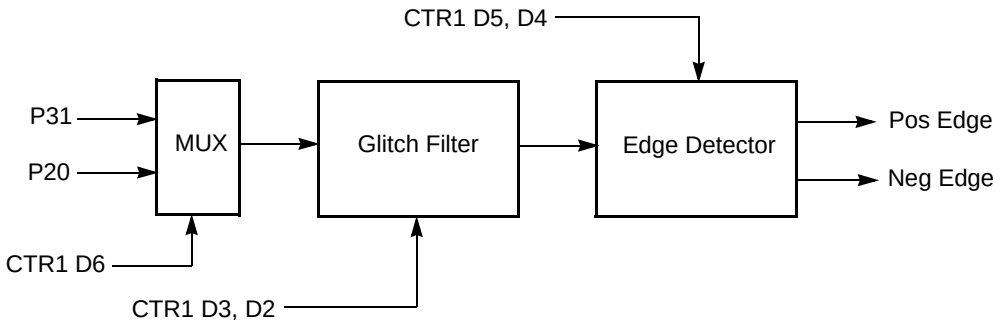


Figure 31. Glitch Filter Circuitry

Eight-Bit Counter/Timer Circuits

Figure 32 shows the 8-bit counter/timer circuits.

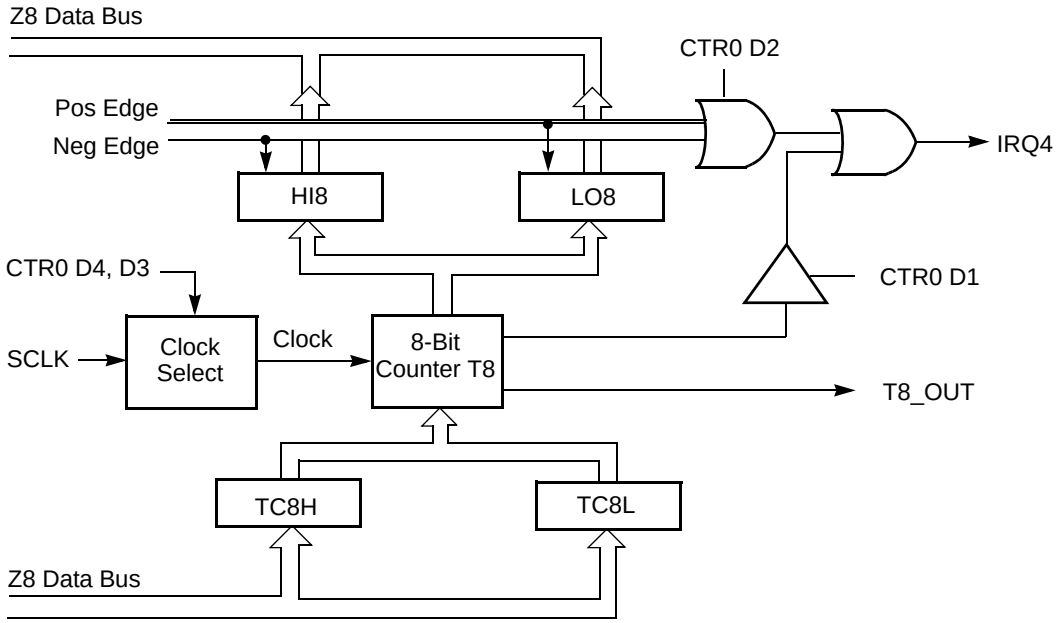


Figure 32. 8-Bit Counter/Timer Circuits

T8 Transmit Mode

Before T8 is enabled, the output of T8 depends on CTR1, D1. If it is 0, T8_OUT is 1. If it is 1, T8_OUT is 0.

When T8 is enabled, the output T8_OUT switches to the initial value (CTR1 D1). If the initial value (CTR1 D1) is 0, TC8L is loaded; otherwise, TC8H is loaded into the counter (see Figure 33). In Single-Pass Mode (CTR0 D6), T8 counts down to 0 and stops, T8_OUT toggles, and the time-out status bit (CTR0 D5) is set. A time-out interrupt can be generated if it is enabled (CTR0 D1). See Figure 34. In Modulo-N Mode, upon reaching the terminal count, T8_OUT is toggled, but no interrupt is generated. From that point, T8 loads a new count (if the T8_OUT level now is 0), TC8L is loaded; if it is 1, TC8H is loaded. T8 counts down to 0, toggles T8_OUT, sets the time-out status bit (CTR0 D5), and generates an interrupt if enabled (CTR0 D1). One cycle is thus completed. T8 then loads from TC8H or TC8L according to the T8_OUT level and repeats the cycle. See Figure 35.

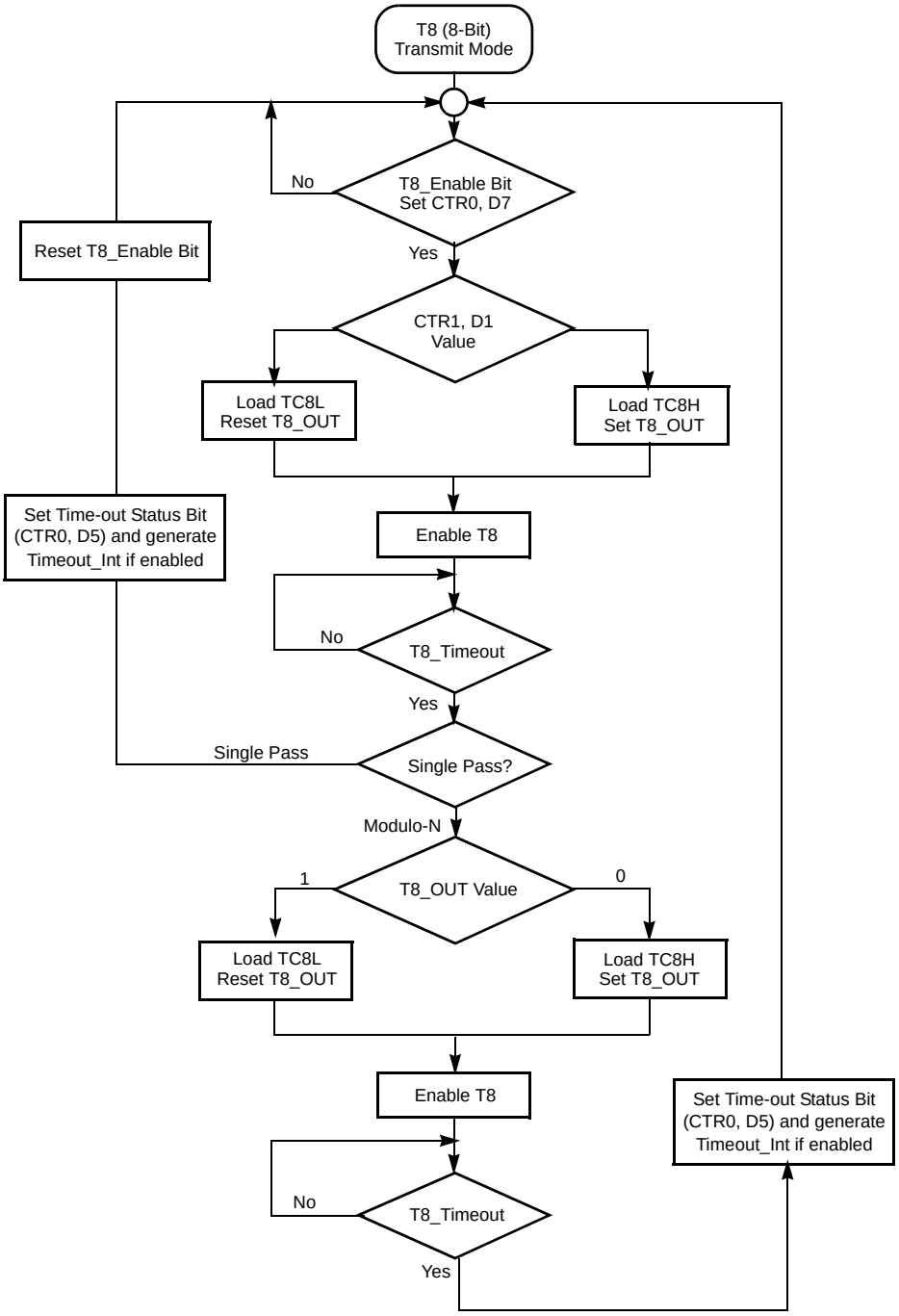


Figure 33. Transmit Mode Flowchart

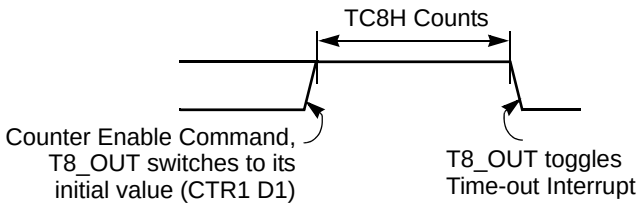


Figure 34. T8_OUT in Single-Pass Mode

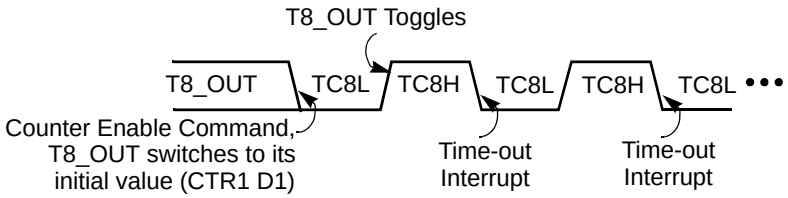


Figure 35. T8_OUT in Modulo-N Mode

You can modify the values in TC8H or TC8L at any time. The new values take effect when they are loaded. To ensure known operation, do not write these registers at the time the values are to be loaded into the counter/timer. *An initial count of 1 is not allowed (a nonfunction occurs).* An initial count of 0 causes TC8 to count from 0 to FFh to FEh.

Note: "h" is used for hexadecimal values.

Transition from 0 to FFh is not a time-out condition.

Caution: Do not use the same instructions for stopping the counter/timers and setting the status bits.

Two successive commands are necessary. First, the counter/timers must be stopped. Second, the status bits must be reset. These commands are required because it takes one counter/timer clock interval for the initiated event to actually occur.

T8 Demodulation Mode

You need to program TC8L and TC8H to FFh. After T8 is enabled, when the first edge (rising, falling, or both, depending on CTR1 D5, D4) is detected, it starts to count down. When a subsequent edge (rising, falling, or both depending on CTR1 D5, D4) is detected during counting, the current value of T8 is complemented and put into one of the capture registers. If it is a positive edge, data is put into LO8; if

it is a negative edge, HI8. From that point, an edge-detect status bits (CTR1 D1, D0) is set, and an interrupt can be generated if enabled (CTR0 D2). Meanwhile, T8 is loaded with FFh and starts counting again. If T8 reaches 0, the time-out status bit (CTR0 D5) is set, an interrupt can be generated if enabled (CTR0 D1), and T8 continues counting from FFh (see Figure 36 and Figure 37).

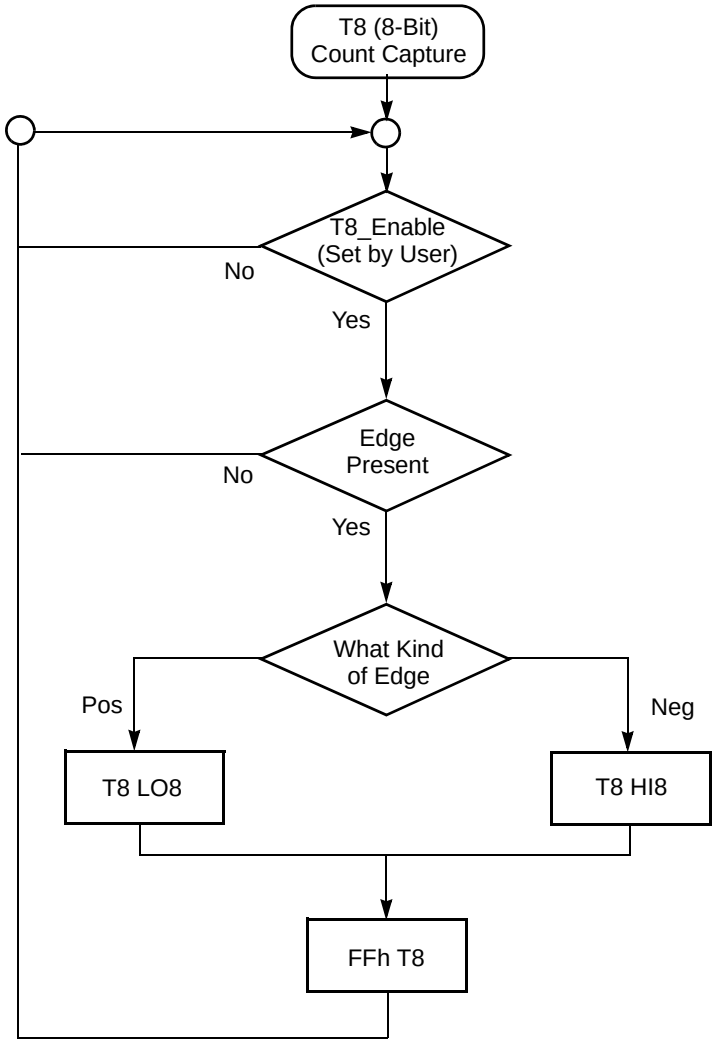


Figure 36. Demodulation Mode Count Capture Flowchart

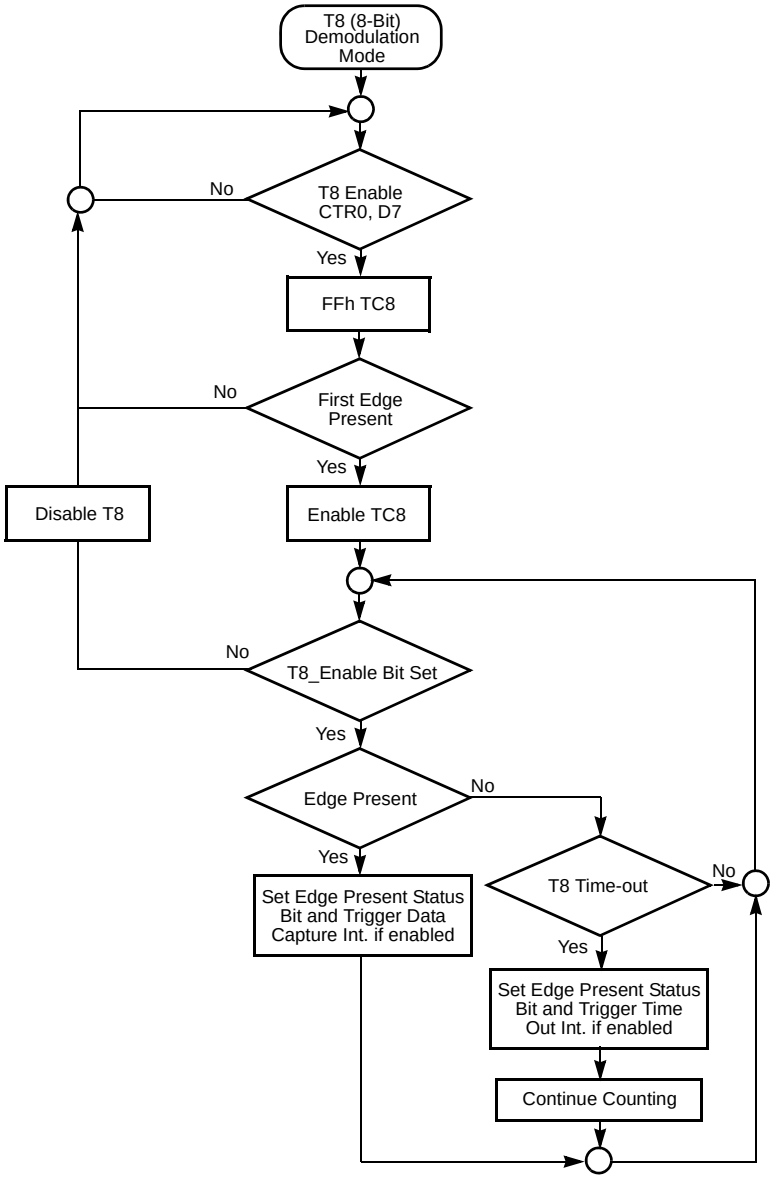


Figure 37. Demodulation Mode Flowchart

Sixteen-Bit Counter/Timer Circuits

Figure 38 shows the 16-bit counter/timer circuits.

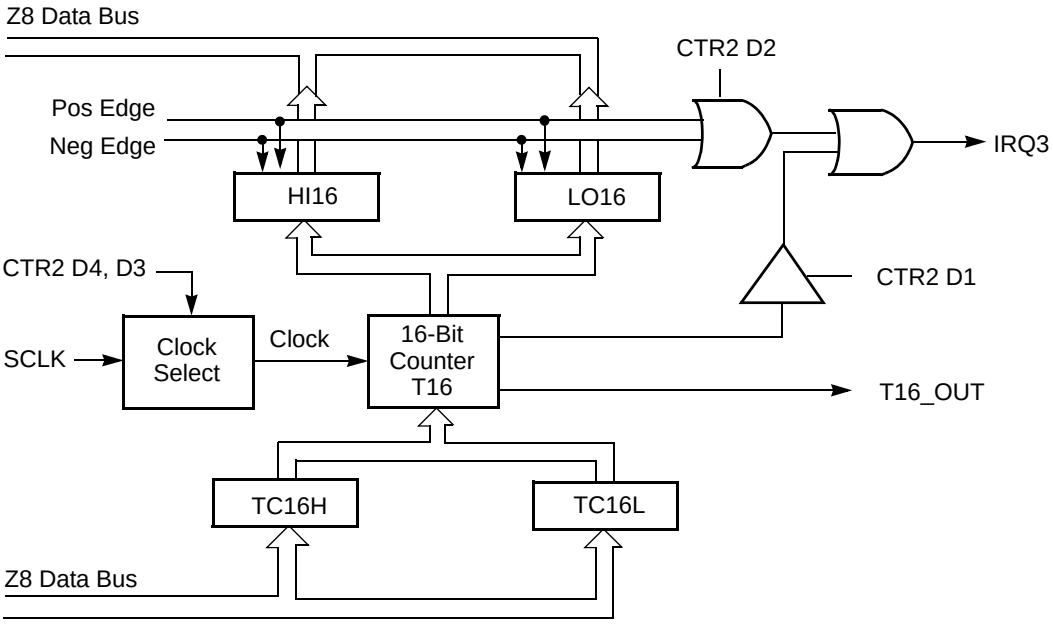


Figure 38. 16-Bit Counter/Timer Circuits

T16 Transmit Mode

In Normal or Ping-Pong Mode, the output of T16, when not enabled, is dependent on CTR1, D0. If the result is a 0, T16_OUT is a 1; if it is a 1, T16_OUT is 0. You can force the output of T16 to either a 0 or 1 whether it is enabled or not by programming CTR1 D3, D2 to a 10 or 11.

When T16 is enabled, TC16H * 256 + TC16L is loaded, and T16_OUT is switched to its initial value (CTR1 D0). When T16 counts down to 0, T16_OUT is toggled (in Normal or Ping-Pong Mode), an interrupt is generated if enabled (CTR2 D1), and a status bit (CTR2 D5) is set.

Note: Global interrupts override this function as described in “Interrupts” on page 54.

If T16 is in Single-Pass Mode, T16 is stopped at this point (see Figure 39). If T16 is in Modulo-N Mode, T16 is loaded with TC16H * 256 + TC16L and the counting continues (see Figure 40).

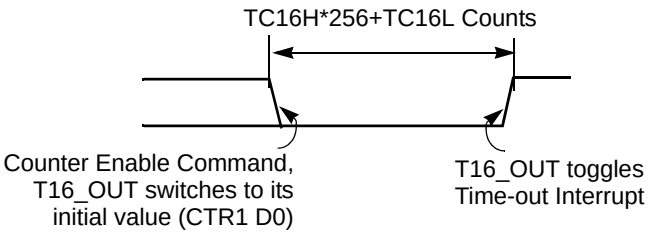


Figure 39. T16_OUT in Single-Pass Mode

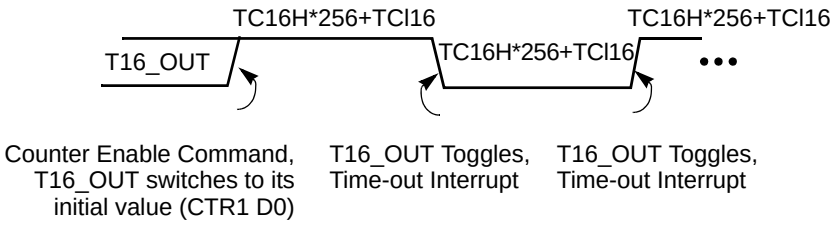


Figure 40. T16_OUT in Modulo-N Mode

You can modify the values in TC16H and TC16L at any time. The new values take effect when they are loaded. To ensure known operation, do not load these registers at the time the values are to be loaded into the counter/timer. An initial count of 1 is not allowed. An initial count of 0 causes T16 to count from 0 to FFFFh to FFFEh. Transition from 0 to FFFFh is not a time-out condition.

T16 Demodulation Mode

You need to program TC16L and TC16H to FFh. After T16 is enabled and the first edge (rising, falling, or both, depending on CTR1 D5, D4) is detected, T16 captures HI16 and LO16, reloads, and begins counting.

If D6 of CTR2 Is 0

When a subsequent edge (rising, falling, or both, depending on CTR1 D5, D4) is detected during counting, the current count in T16 is one's complemented and put into HI16 and LO16. When data is captured, one of the edge-detect status bits (CTR1 D1, D0) is set, and an interrupt is generated if enabled (CTR2 D2). From that point, T16 is loaded with FFFFh and starts again.

This T16 mode is generally used to measure space time, the length of time between bursts of carrier signal (marks).

If D6 of CTR2 Is 1

T16 ignores the subsequent edges in the input signal and continues counting down. A time-out of T8 causes T16 to capture its current value and generate an interrupt if enabled (CTR2, D2). In this case, T16 does not reload and continues counting. If the D6 bit of CTR2 is toggled (by writing a 0 and then a 1 to it), T16 captures and reloads on the next edge (rising, falling, or both, depending on CTR1 D5, D4) but continues to ignore subsequent edges.

This T16 mode is generally used to measure mark times, the length of active carrier signal bursts.

When T16 reaches 0, it continues counting from FFFFh. Meanwhile, a status bit (CTR2 D5) is set, and an interrupt time-out can be generated if enabled (CTR2 D1).

Ping-Pong Mode

This operation mode (see Figure 41) is only valid in transmit mode. T8 and T16 must be programmed in Single-Pass Mode (CTR0 D6, CTR2 D6), and Ping-Pong Mode must be programmed in CTR1 D3 and D2. You can begin the operation by enabling either T8 or T16 (CTR0 D7 or CTR2 D7). For example, if T8 is enabled, T8_OUT is set to this initial value (CTR1 D1). According to T8_OUT's level, TC8H or TC8L is loaded into T8. After the terminal count is reached, T8 is disabled, and T16 is enabled. T16_OUT switches to its initial value (CTR1 D0), data from TC16H and TC16L is loaded, and T16 starts to count. After T16 reaches the terminal count, it stops, T8 is enabled again, and the whole cycle repeats. Interrupts can be allowed when T8 or T16 reaches terminal control (CTR0 D1, CTR2 D1). To stop the Ping-Pong operation, write 00 to bits D3 and D2 of CTR1.

Note: Enabling Ping-Pong operation while the counter/timers are running might cause intermittent counter/timer function. Disable the counter/timers and then reset the status flags before instituting this operation.

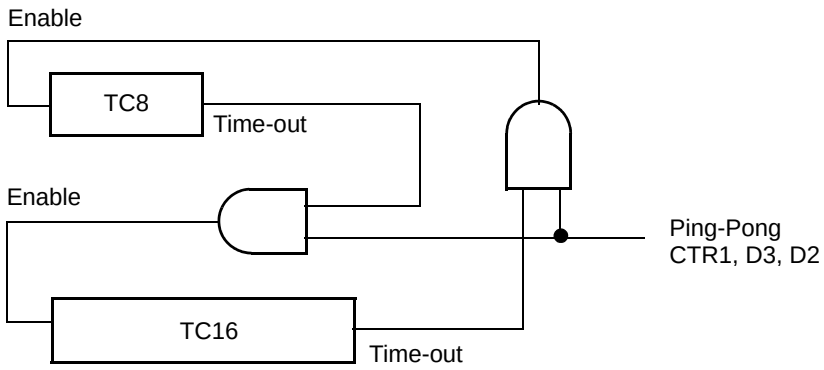


Figure 41. Ping-Pong Mode

Starting Ping-Pong Mode

First, make sure both counter/timers are not running. Then set T8 into Single-Pass Mode (CTR0 D6), set T16 into Single-Pass Mode (CTR2 D6), and set the Ping-Pong Mode (CTR1 D2, D3). These instructions do not have to be in any particular order. Finally, start Ping-Pong Mode by enabling either T8 (CTR0 D7) or T16 (CTR2 D7).

During Ping-Pong Mode

The enable bits of T8 and T16 (CTR0 D7, CTR2 D7) are set and cleared alternately by hardware. The time-out bits (CTR0 D5, CTR2 D5) are set every time the counter/timers reach the terminal count.

Output Circuit

Figure 42 shows the output circuit.

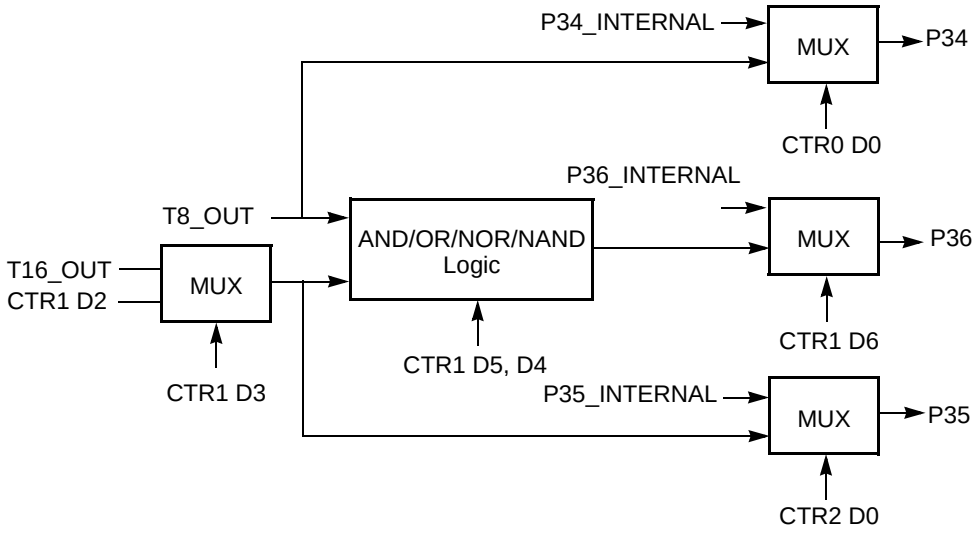


Figure 42. Output Circuit

Interrupts

The Z86L88 features five different interrupts. The interrupts are maskable and prioritized, as shown in Figure 43. The five sources are divided as follows: three sources are claimed by Port 3 lines P33–P31and two by the counter/timers (see Table 21). The Interrupt Mask Register, globally or individually, enables or disables the five interrupt requests.

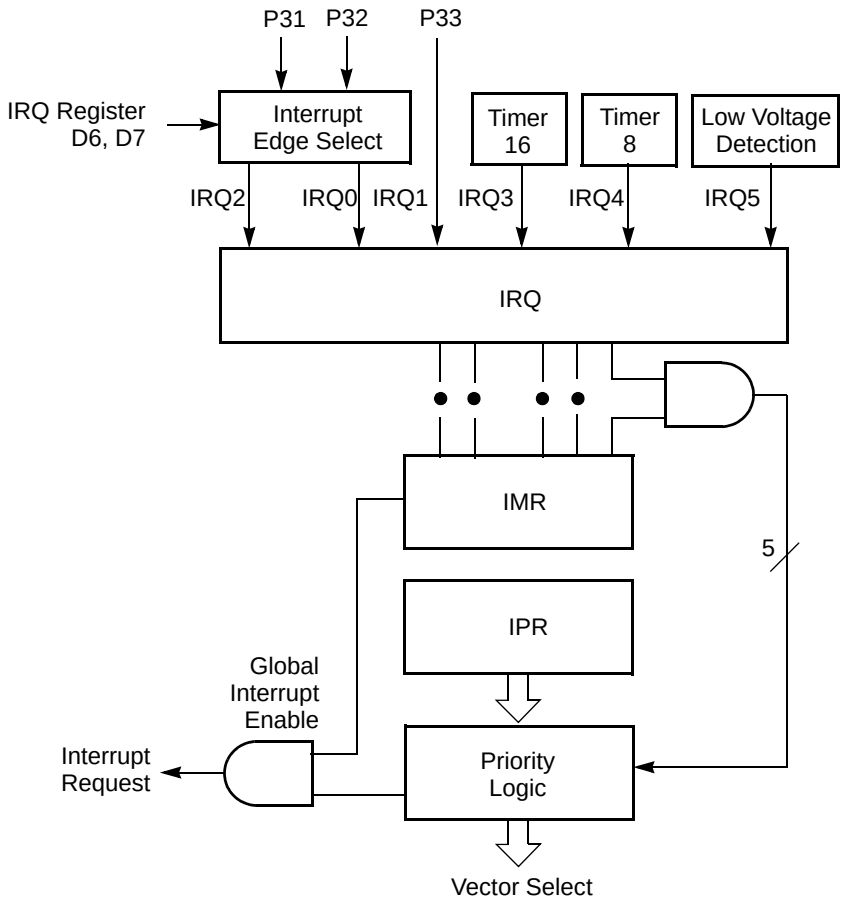


Figure 43. Interrupt Block Diagram

Table 21. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	P32	0,1	External (P32), Rising Falling Edge Triggered
IRQ1	P33	2,3	External (P33), Falling Edge Triggered
IRQ2	P31, T_{IN}	4,5	External (P31), Rising Falling Edge Triggered
IRQ3	T16	6,7	Internal
IRQ4	T8	8,9	Internal

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder controlled by the Interrupt Priority register. An interrupt machine cycle is activated when an interrupt request is granted. As a result, all subsequent interrupt are disabled, and the Program Counter and Status Flags are saved. The cycle then branches to the program memory vector location reserved for that interrupt. All Z86L88 interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request. To accommodate polled interrupt systems, interrupt inputs are masked, and the Interrupt Request register is polled to determine which of the interrupt requests require service.

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 can be rising, falling, or both edge triggered; all are programmable by the user. The software can poll to identify the state of the pin.

Programming bits for the Interrupt Edge Select are located in the IRQ Register (R250), bits D7 and D6. The configuration is indicated in Table 22.

Table 22. IRQ Register *

IRQ		Interrupt Edge	
D7	**D6**	**IRQ2 (P31)**	**IRQ0 (P32)**
0	0	F	F
0	1	F	R
1	0	R	F
1	1	R/F	R/F

Notes:
F = Falling Edge
R = Rising Edge
*In stop mode, the comparators are turned off.

Clock

The Z86L88 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, LC, ceramic resonator, or any suitable external clock source (XTAL1 = Input; XTAL2 = Output). The crystal must be AT cut, 1 MHz to 8 MHz maximum, with a series resistance (RS) less than or equal to 100 Ohms. The Z86L88 on-chip oscillator can be driven with a low-cost RC network or other suitable external clock source.

For 32-kHz crystal operation, an external feedback resistor (Rf) and a serial resistor (Rd) are required. See Figure 44.

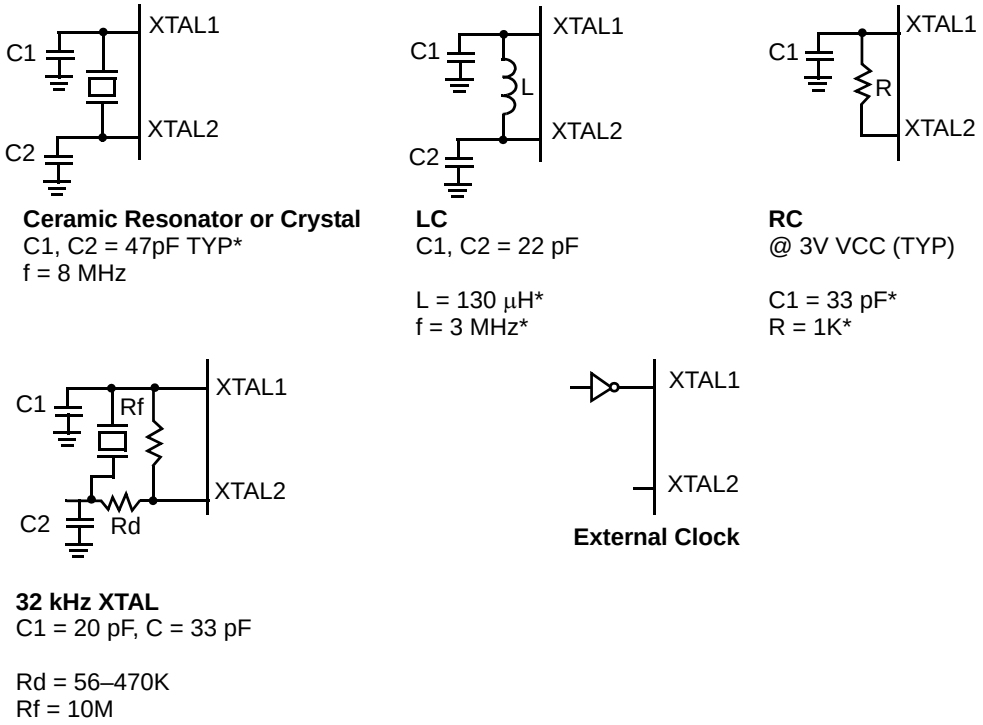


Figure 44. Oscillator Configuration

The crystal needs to be connected across XTAL1 and XTAL2 using the recommended capacitors (capacitance greater than or equal to 22 pF) from each pin to ground. The RC oscillator configuration is an external resistor connected from XTAL1 to XTAL2, with a frequency-setting capacitor from XTAL1 to ground (see Figure 44).

Power-On Reset (POR)

A timer circuit clocked by a dedicated on-board RC oscillator is used for the Power-On Reset (POR) timer function. The POR time allows V_{CC} and the oscillator circuit to stabilize before instruction execution begins.

The POR timer circuit is a one-shot timer triggered by one of three conditions:

- Power Fail to Power OK status including Waking up from V_{BO} Standby
- Stop-Mode Recovery (if D5 of SMR = 1)
- WDT Time-Out

The POR time is a nominal 5 ms. Bit 5 of the Stop-Mode Register determines whether the POR timer is bypassed after Stop-Mode Recovery (typical for external clock, RC, and LC oscillators).

HALT

HALT turns off the internal CPU clock, but not the XTAL oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2, IRQ3, and IRQ4 remain active. The devices are recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT Mode. After the interrupt service routine, the program continues from the instruction after the HALT.

STOP

This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 10 μA or less. STOP Mode is terminated only by a reset (such as WDT time-out), POR, SMR, or external reset. This termination causes the processor to restart the application program at address 000CH. To enter STOP (or HALT) mode, you need to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To execute this action, you must execute a NOP (op code = FFH) immediately before the appropriate sleep instruction. For example:

```
FF      NOP         ; clear the pipeline
6F      STOP        ; enter STOP Mode
```

or

```
FF      NOP         ; clear the pipeline
7F      HALT        ; enter HALT Mode
```

Port Configuration Register (PCON)

The PCON register configures the comparator output on Port 3. It is located in the expanded register 2 at Bank F, location 00, as shown in Figure 45.

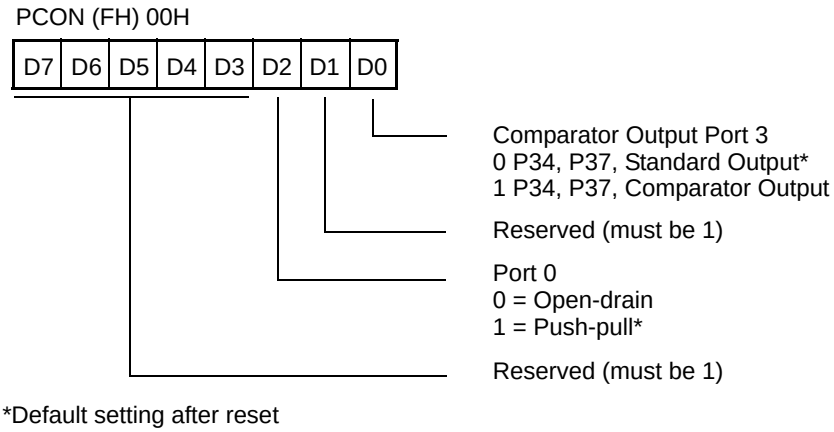


Figure 45. Port Configuration Register (PCON)—Write Only

Comparator Output Port 3 (D0)

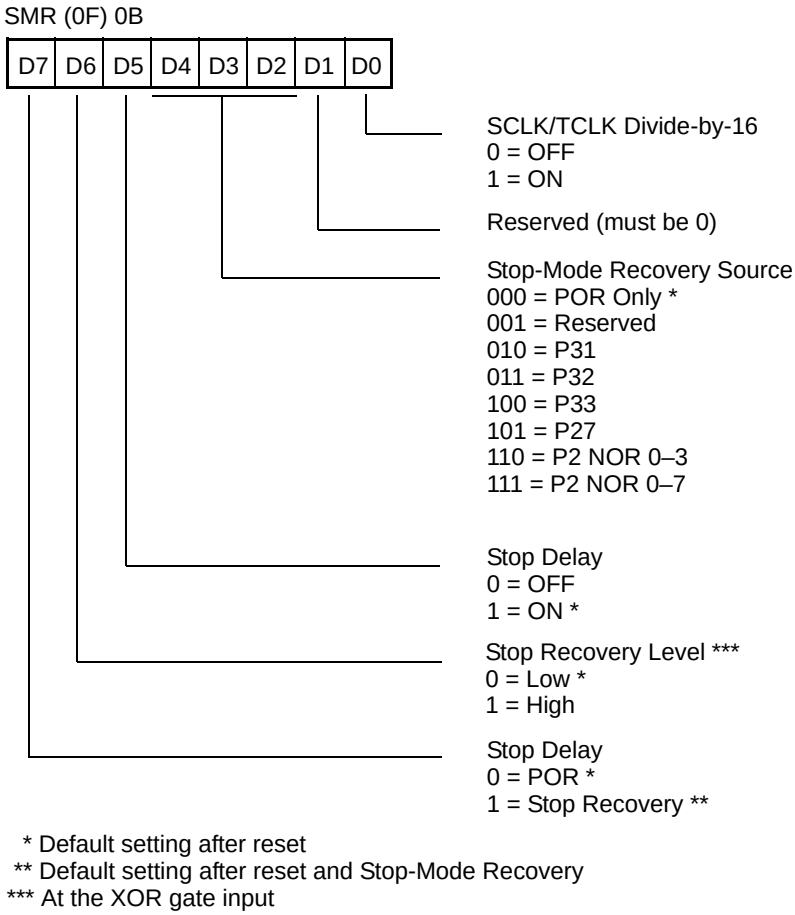
Bit 0 controls the comparator used in Port 3. A 1 in this location brings the comparator outputs to P34 and P37, and a 0 releases the port to its standard (/O configuration.

Port 0 Output Mode (D2)

Bit 2 controls the output mode of Port 0. A 1 in this location set the output to push-pull, and a 0 sets the output to open-drain.

Stop-Mode Recovery Register (SMR)

This register selects the clock divide value and determines the mode of Stop-Mode Recovery (Figure 46). All bits are write only except bit 7, which is read only. Bit 7 is a flag bit that is hardware set on the condition of STOP recovery and reset by a power-on cycle. Bit 6 controls whether a low level or a high level at the XOR-gate input is required from the recovery source. Bit 5 controls the reset delay after recovery. Bits D2, D3, and D4, or the SMR register specify the source of the Stop-Mode Recovery signal. Bit D0 determines if SCLK/TCLK (shown in Figure 47) are divided by 16 or not. The SMR is located in Bank F of the Expanded Register Group at address 0BH.



* Default setting after reset
** Default setting after reset and Stop-Mode Recovery
*** At the XOR gate input

Figure 46. Stop-Mode Recovery Register

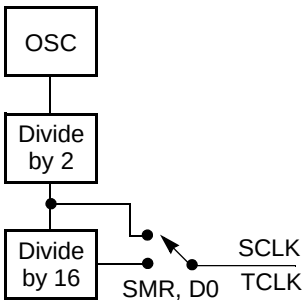


Figure 47. SCLK Circuit

SCLK/TCLK Divide-by-16 Select (D0)

D0 of the SMR controls a Divide-by-16 prescaler of SCLK/TCLK. The purpose of this control is to selectively reduce device power consumption during normal processor execution (SCLK control) and/or HALT Mode (where TCLK sources interrupt logic). After Stop-Mode Recovery, this bit is set to a 0.

Stop-Mode Recovery Source (D2, D3, and D4)

These three bits of the SMR specify the wake-up source of the STOP recovery (Figure 48 and Table 23 on page 63).

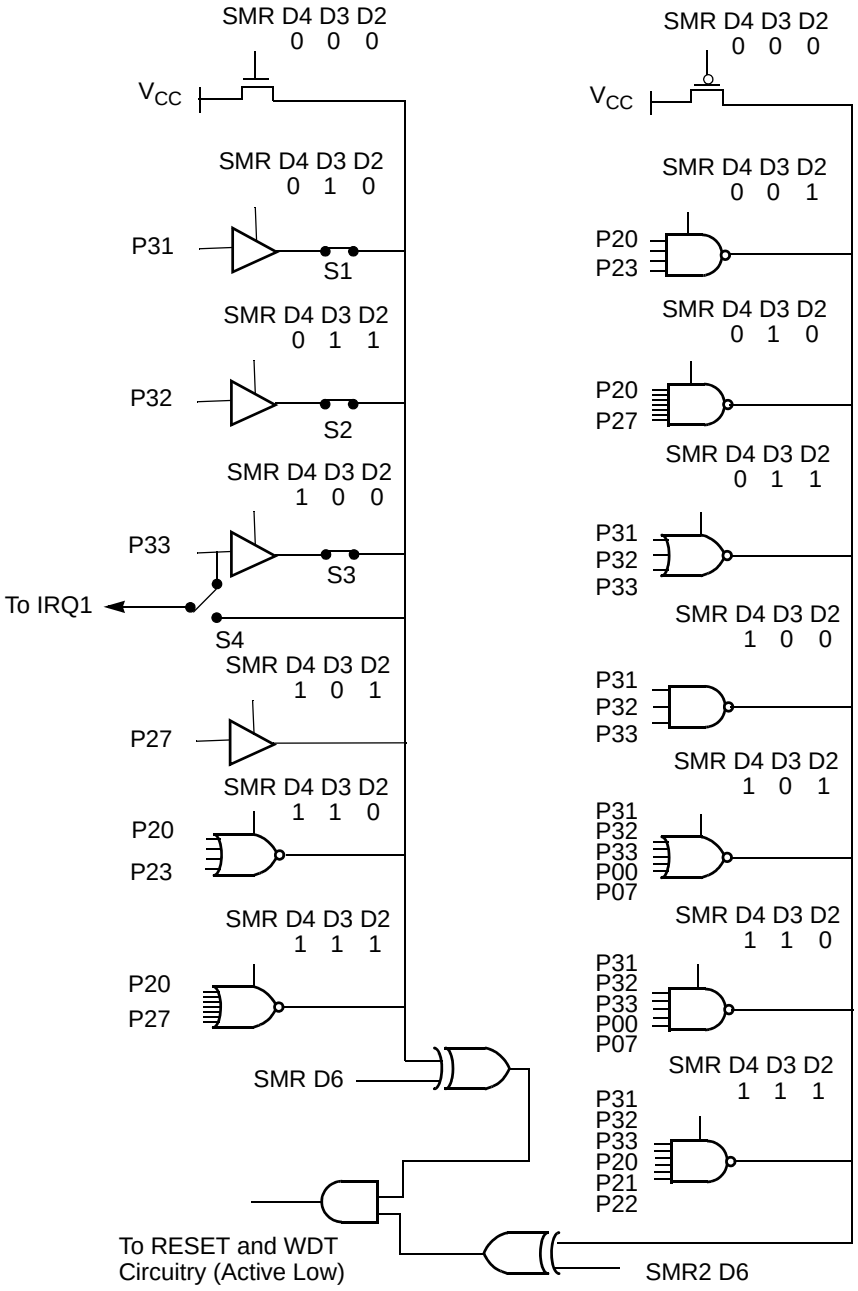


Figure 48. Stop-Mode Recovery Source

Table 23. Stop-Mode Recovery Source

SMR:432			Operation
D4	D3	D2	Description of Action
0	0	0	POR and/or external reset recovery
0	0	1	Reserved
0	1	0	P31 transition
0	1	1	P32 transition
1	0	0	P33 transition
1	0	1	P27 transition
1	1	0	Logical NOR of P20 through P23
1	1	1	Logical NOR of P20 through P27

Note: Any Port 2 bit defined as an output drives the corresponding input to the default state to allow the remaining inputs to control the AND/OR function. Refer to “Stop-Mode Recovery Register 2 (SMR2)” on page 64 for other recover sources.

Stop-Mode Recovery Delay Select (D5)

This bit, if low, disables the 5-ms $\overline{\text{RESET}}$ delay after Stop-Mode Recovery. The default configuration of this bit is 1. If the “fast” wake up is selected, the Stop-Mode Recovery source must be kept active for at least 5TpC.

Stop-Mode Recovery Edge Select (D6)

A 1 in this bit position indicates that a High level on any one of the recovery sources wakes the Z86L88 from STOP Mode. A 0 indicates Low level recovery. The default is 0 on POR.

Cold or Warm Start (D7)

This bit is read only. It is set to 1 when the device is recovered from Stop Mode. The bit is set to 0 when the device is reset other than Stop-Mode Recovery (SMR).

Stop-Mode Recovery Register 2 (SMR2)

This register determines the mode of Stop-Mode Recovery for SMR2 (see Figure 49).

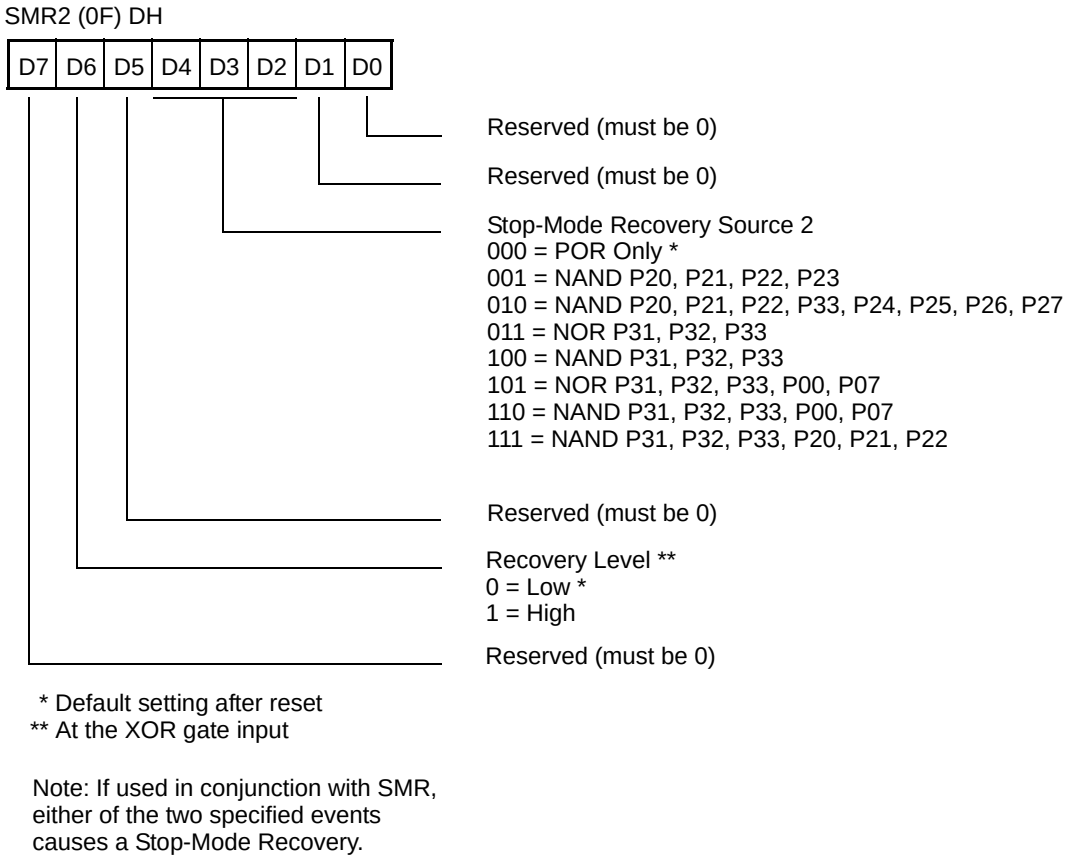


Figure 49. Stop-Mode Recovery Register 2—(0F) DH:D2–D4, D6 Write Only

If SMR2 is used in conjunction with SMR, either of the specified events causes a Stop-Mode Recovery.

Note: Port pins configured as outputs are ignored as a SMR or SMR2 recovery source. For example, if the NAND or P23–P20 is selected as the recovery source and P20 is configured as an output, the remaining SMR pins (P23–P21) form the NAND equation.

Table 24 describes the contents of the Stop-Mode Recovery register 2.

Table 24. SMR2(F)0Dh: Stop-Mode Recovery Register 2

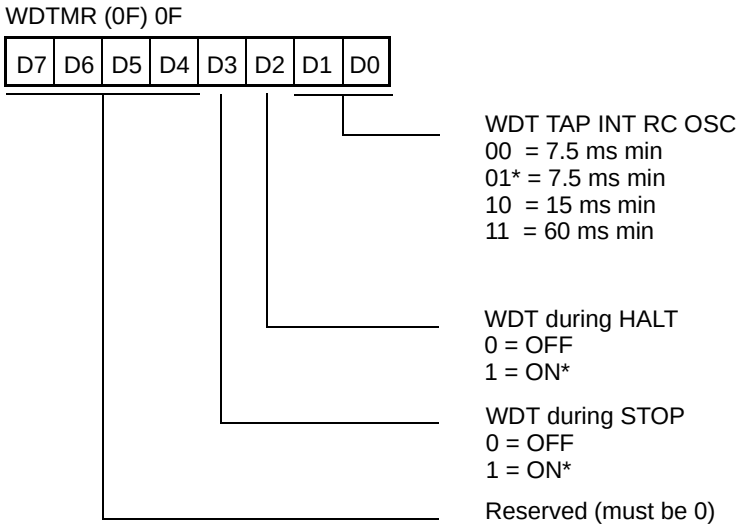
Field	Bit Position		Value	Description
Reserved	7-------		0	Reserved (Must be 0)
Recovery Level	-6------	W	0* 1	Low High
Reserved	--5-----		0	Reserved (Must be 0)
Source	---432--	W	000* 001 010 011 100 101 110 111	A. POR Only B. NAND of P23–P20 C. NAND or P27–P20 D. NOR of P33–P31 E. NAND of P33–P31 F. NOR of P33–P31, P00, P07 G. NAND of P33–P31, P00, P07 H. NAND of P33–P31, P22–P20
Reserved	------10		00	Reserved (Must be 0)

Notes:
*Indicates the value upon Power-On Reset
Port pins configured as outputs are ignored as a SMR recovery source.

Watch-Dog Timer Mode Register (WDTMR)

The WDT is a retriggerable, one-shot timer that resets the Z8 if it reaches its terminal count. The WDT must initially be enabled by executing the WDT instruction and refreshed on subsequent executions of the WDT instruction. The WDT circuit is driven by an on-board RC oscillator or external oscillator from the XTAL1 pin. The WDT instruction affects the Zero (Z), Sign (S), and Overflow (V) flags.

The POR clock source is selected with bit 4 of the WDT register. Bits 0 and 1 control a tap circuit that determines the minimum time-out period. Bit 2 determines whether the WDT is active during HALT, and Bit 3 determines WDT activity during STOP. Bits 5 through 7 are reserved (Figure 50). This register is accessible only during the first 61 processor cycles (122 XTAL clocks) from the execution of the first instruction after Power-On-Reset, Watch-Dog Reset, or a Stop-Mode Recovery (Figure 50). After this point, the register cannot be modified by any means, intentional or otherwise. The WDTMR cannot be read. The register is located in Bank F of the Expanded Register Group at address location 0FH. The WDTMR is organized as shown in Figure 50.



* Default setting after reset

Figure 50. Watch-Dog Timer Mode Register—Write Only

WDT Time Select (D0, D1)

This bit selects the WDT time period. It is configured as indicated in Table 25.

Table 25. WDT Time Select*

D1	D0	Time-Out of Internal RC OSC
0	0	7.5 ms min
0	1	7.5 ms min
1	0	15 ms min
1	1	60 ms min

Notes:
*TpC = XTAL clock cycle.
The default on reset is 10 ms.

WDTMR During HALT (D2)

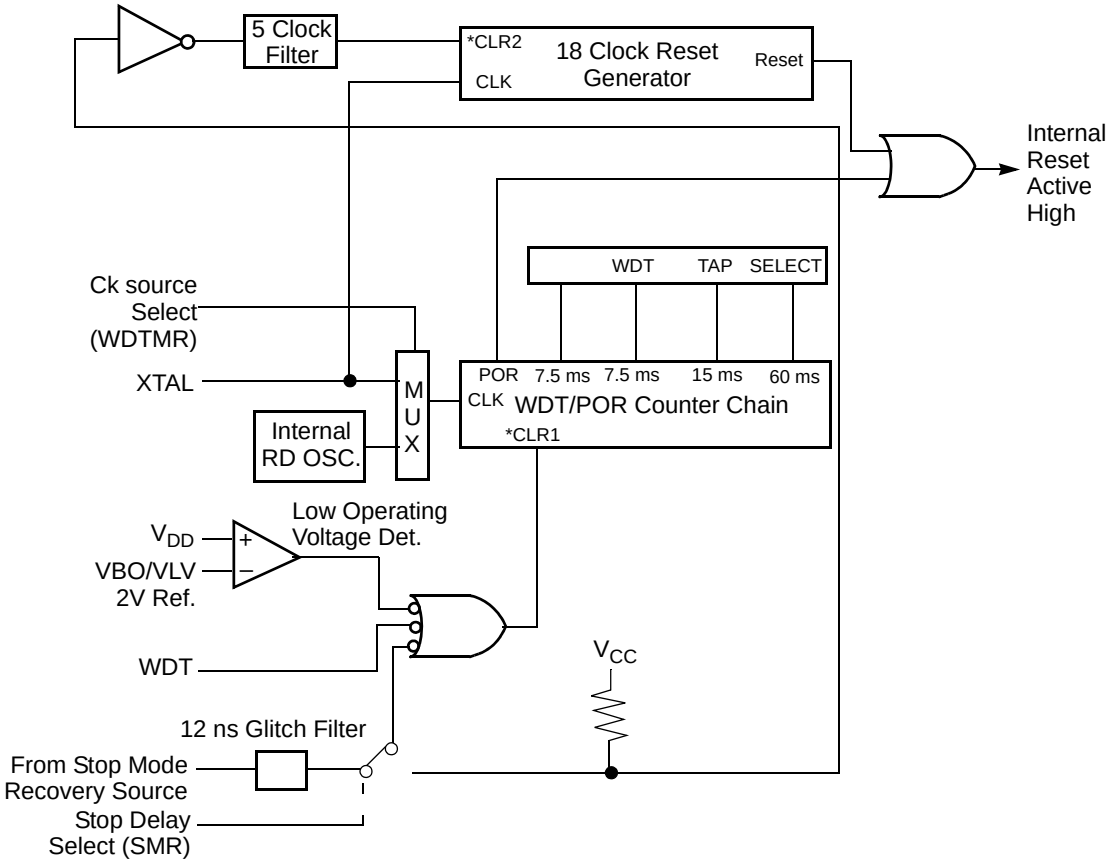
This bit determines whether or not the WDT is active during HALT Mode. A 1 indicates active during HALT. The default is 1.

WDTMR During STOP (D3)

This bit determines whether or not the WDT is active during STOP Mode. Since the XTAL clock is stopped during STOP Mode, the on-board RC has to be selected as the clock source to the WDT/POR counter. A 1 indicates active during STOP. The default is 1.

Clock Source for WDT (D4)

This bit determines which oscillator source is used to clock the internal POR and WDT counter chain. If the bit is a 1, the internal RC oscillator is bypassed, and the POR and WDT clock source is driven from the external pin, XTAL1. The default configuration of this bit is 0, which selects the RC oscillator. See Figure 51.



*$\overline{\text{CLR1}}$ and $\overline{\text{CLR2}}$ enable the WDT/POR and 18 Clock Reset timers upon a Low-to-High input translation.

Figure 51. Resets and WDT

Mask Selectable Options

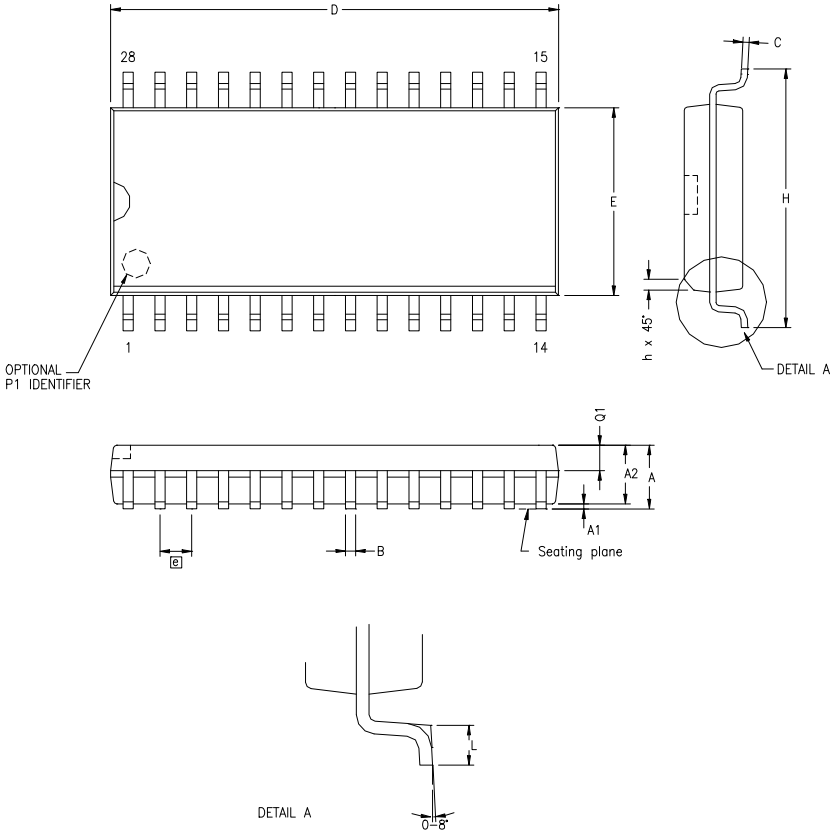
There are seven Mask Selectable Options to choose from based on ROM code requirements. These are listed in Table 26.

Table 26. Mask Selectable Options

RC/Other	RC/XTAL
32 kHz XTAL	On/Off
Port 0: 0–3 pull-ups	On/Off
Port 0: 4–7 pull-ups	On/Off
Port 2: 2–7 pull-ups	On/Off
Port 3: pull-ups	On/Off
Port 0: 0–3 Mouse Mode 0.4 V_{DD} Trip	On/Off

Ordering Information

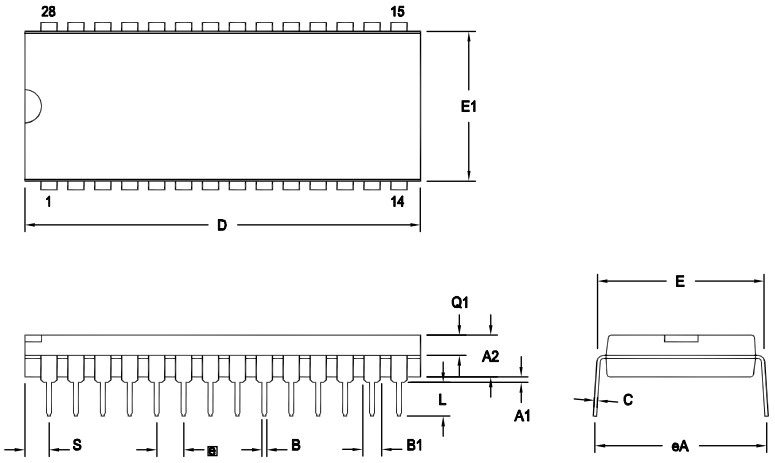
Figure 52 shows the 28-pin SOIC package diagram. Figure 53 shows the 28-pin DIP package diagram. Figure 54 shows the 28-pin SSOP package diagram.



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.64	.094	.104
A1	0.10	0.30	.004	.012
A2	2.24	2.44	.088	.096
B	0.36	0.46	.014	.018
C	0.23	0.30	.009	.012
D	17.78	18.00	.700	.710
E	7.40	7.60	.291	.299
e	1.27 BSC		.050 BSC	
H	10.00	10.65	.394	.419
h	0.30	0.71	.012	.028
L	0.61	1.00	.024	.039
Q1	0.97	1.09	.038	.043

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

Figure 52. 28-Pin SOIC Package Diagram



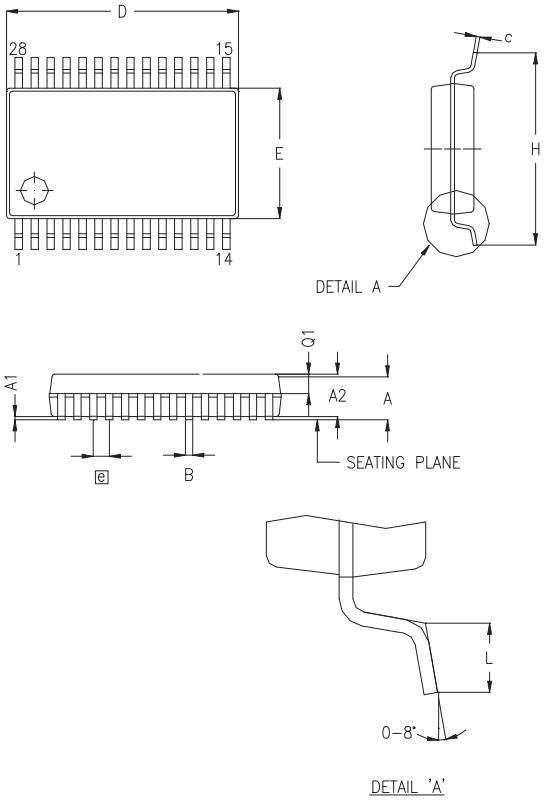
SYMBOL	OPT #	MILLIMETER		INCH	
		MIN	MAX	MIN	MAX
A1		0.38	1.02	.015	.040
A2		3.18	4.19	.125	.165
B		0.38	0.53	.015	.021
B1	01	1.40	1.65	.055	.065
	02	1.14	1.40	.045	.055
C		0.23	0.38	.009	.015
D	01	36.58	37.34	1.440	1.470
	02	35.31	35.94	1.390	1.415
E		15.24	15.75	.600	.620
E1	01	13.59	14.10	.535	.555
	02	12.83	13.08	.505	.515
e		2.54 TYP		.100 BSC	
eA		15.49	16.76	.610	.660
L		3.05	3.81	.120	.150
Q1	01	1.40	1.91	.055	.075
	02	1.40	1.78	.055	.070
S	01	1.52	2.29	.060	.090
	02	1.02	1.52	.040	.060

CONTROLLING DIMENSIONS : INCH

OPTION TABLE	
OPTION #	PACKAGE
01	STANDARD
02	IDF

Note: ZILOG supplies both options for production. Component layout PCB design should cover bigger option 01.

Figure 53. 28-Pin DIP Package Diagram



SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.73	1.86	1.99	0.068	0.073	0.078
A1	0.05	0.13	0.21	0.002	0.005	0.008
A2	1.68	1.73	1.78	0.066	0.068	0.070
B	0.25		0.38	0.010		0.015
C	0.09	–	0.20	0.004	0.006	0.008
D	10.07	10.20	10.33	0.397	0.402	0.407
E	5.20	5.30	5.38	0.205	0.209	0.212
e	0.65 TYP			0.0256 TYP		
H	7.65	7.80	7.90	0.301	0.307	0.311
L	0.63	0.75	0.95	0.025	0.030	0.037

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

Figure 54. 28-Pin SSOP Package Diagram

Z86L88

8.0 MHz 28-Pin DIP

Z86L8808PSC

Z86L8808PSG

28-Pin SOIC

Z86L8808SSC

Z86L8808SSG

Note: For the die form, please contact Maxim.

For fast results, contact your local Maxim sales office for assistance in ordering the part desired.

Codes

Figure 55 shows an example of what the ordering codes represent.

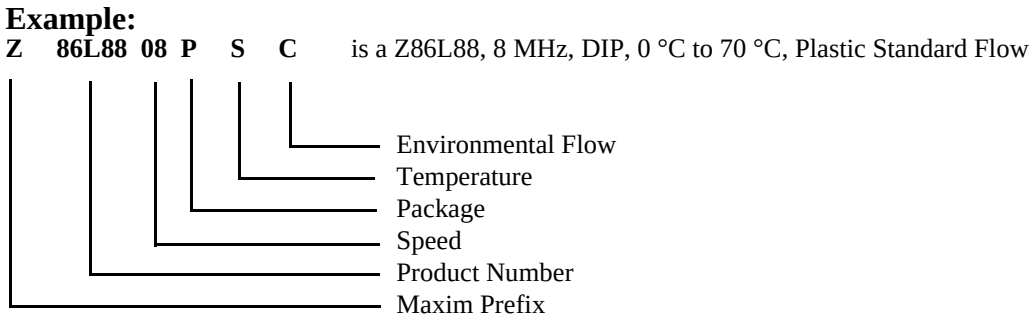


Figure 55. Ordering Codes Example

Package

P = Plastic DIP
S = SOIC (Small Outline Integrated Circuit)

Temperature

S = 0 °C to +70 °C

Speed

8 = 8.0 MHz

Environmental

C = Plastic Standard

G = Lead free

Customer Feedback

For any comments, detail technical questions, or reporting problems, please visit Maxim's Technical Support at https://support.maxim-ic.com/micro.