

# 74LVC2G00-Q100

Dual 2-input NAND gate

Rev. 3 — 20 June 2022

Product data sheet

## 1. General description

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The 74LVC2G00-Q100 is a dual 2-input NAND gate. Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V environments.

Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times.

This device is fully specified for partial power down applications using  $I_{OFF}$ . The  $I_{OFF}$  circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

## 2. Features and benefits

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- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Wide supply voltage range from 1.65 V to 5.5 V
- 5 V tolerant outputs for interfacing with 5 V logic
- High noise immunity
- $\pm 24$  mA output drive ( $V_{CC} = 3.0$  V)
- CMOS low power dissipation
- $I_{OFF}$  circuitry provides partial Power-down mode operation
- Complies with JEDEC standard:
  - JESD8-7 (1.65 V to 1.95 V)
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8-B/JESD36 (2.7 V to 3.6 V)
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Overvoltage tolerant inputs to 5.5 V
- ESD protection:
  - MIL-STD-883, method 3015 exceeds 2000 V
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V ( $C = 200$  pF,  $R = 0$   $\Omega$ )

### 3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
<a href="#">74LVC2G00DC-Q100</a>	-40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	<a href="#">SOT765-1</a>

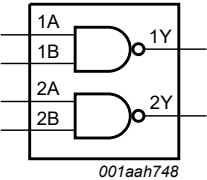
### 4. Marking

Table 2. Marking codes

Type number	Marking code[1]
74LVC2G00DC-Q100	V00

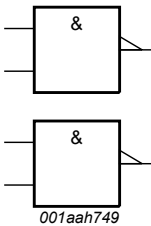
[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

### 5. Functional diagram



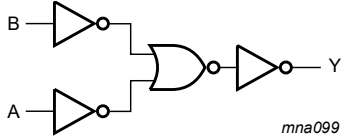
001aah748

**Fig. 1. Logic symbol**



001aah749

**Fig. 2. IEC logic symbol**



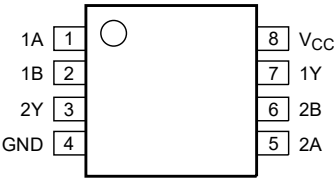
mna099

**Fig. 3. Logic diagram (one gate)**

### 6. Pinning information

#### 6.1. Pinning

**74LVC2G00**



001aab736

**Fig. 4. Pin configuration SOT765-1 (VSSOP8)**

## 6.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
1A, 2A	1, 5	data input
1B, 2B	2, 6	data input
GND	4	ground (0 V)
1Y, 2Y	7, 3	data output
V <sub>CC</sub>	8	supply voltage

## 7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level.

Input		Output
nA	nB	nY
L	L	H
L	H	H
H	L	H
H	H	L

## 8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+6.5	V
V <sub>I</sub>	input voltage		-0.5	+6.5	V
V <sub>O</sub>	output voltage	Active mode	-0.5	V <sub>CC</sub> + 0.5	V
		Power-down mode; V <sub>CC</sub> = 0 V	-0.5	+6.5	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < 0 V	-50	-	mA
I <sub>OK</sub>	output clamping current	V <sub>O</sub> < 0 V or V <sub>O</sub> > V <sub>CC</sub>	-	±50	mA
I <sub>O</sub>	output current	V <sub>O</sub> = 0 V to V <sub>CC</sub>	-	±50	mA
I <sub>CC</sub>	supply current		-	100	mA
I <sub>GND</sub>	ground current		-100	-	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 °C to +125 °C	-	250	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT765-1 (VSSOP8) package: P<sub>tot</sub> derates linearly with 4.9 mW/K above 99 °C.

## 9. Recommended operating conditions

Table 6. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		1.65	5.5	V
$V_I$	input voltage		0	5.5	V
$V_O$	output voltage	Active mode	0	$V_{CC}$	V
		Power-down mode; $V_{CC} = 0$ V	0	5.5	V
$T_{amb}$	ambient temperature		-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.65$ V to 2.7 V	-	20	ns/V
		$V_{CC} = 2.7$ V to 5.5 V	-	10	ns/V

## 10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
<b><math>T_{amb} = -40</math> °C to <math>+85</math> °C</b>						
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	$0.65 \times V_{CC}$	-	-	V
		$V_{CC} = 2.3$ V to 2.7 V	1.7	-	-	V
		$V_{CC} = 2.7$ V to 3.6 V	2.0	-	-	V
		$V_{CC} = 4.5$ V to 5.5 V	$0.7 \times V_{CC}$	-	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	-	-	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3$ V to 2.7 V	-	-	0.7	V
		$V_{CC} = 2.7$ V to 3.6 V	-	-	0.8	V
		$V_{CC} = 4.5$ V to 5.5 V	-	-	$0.3 \times V_{CC}$	V
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$				
		$I_O = -100$ $\mu$ A; $V_{CC} = 1.65$ V to 5.5 V	$V_{CC} - 0.1$	-	-	V
		$I_O = -4$ mA; $V_{CC} = 1.65$ V	1.2	1.53	-	V
		$I_O = -8$ mA; $V_{CC} = 2.3$ V	1.9	2.13	-	V
		$I_O = -12$ mA; $V_{CC} = 2.7$ V	2.2	2.50	-	V
		$I_O = -24$ mA; $V_{CC} = 3.0$ V	2.3	2.60	-	V
		$I_O = -32$ mA; $V_{CC} = 4.5$ V	3.8	4.10	-	V
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$				
		$I_O = 100$ $\mu$ A; $V_{CC} = 1.65$ V to 5.5 V	-	-	0.1	V
		$I_O = 4$ mA; $V_{CC} = 1.65$ V	-	0.08	0.45	V
		$I_O = 8$ mA; $V_{CC} = 2.3$ V	-	0.14	0.3	V
		$I_O = 12$ mA; $V_{CC} = 2.7$ V	-	0.19	0.4	V
		$I_O = 24$ mA; $V_{CC} = 3.0$ V	-	0.37	0.55	V
$I_O = 32$ mA; $V_{CC} = 4.5$ V	-	0.43	0.55	V		
$I_I$	input leakage current	$V_I = 5.5$ V or GND; $V_{CC} = 0$ V to 5.5 V	-	$\pm 0.1$	$\pm 1$	$\mu$ A
$I_{OFF}$	power-off leakage current	$V_I$ or $V_O = 5.5$ V; $V_{CC} = 0$ V	-	$\pm 0.1$	$\pm 2$	$\mu$ A
$I_{CC}$	supply current	$V_I = 5.5$ V or GND; $V_{CC} = 1.65$ V to 5.5 V; $I_O = 0$ A	-	0.1	4	$\mu$ A

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
$\Delta I_{CC}$	additional supply current	per pin; $V_I = V_{CC} - 0.6 \text{ V}$ ; $V_{CC} = 2.3 \text{ V to } 5.5 \text{ V}$ ; $I_O = 0 \text{ A}$	-	5	500	$\mu\text{A}$
$C_I$	input capacitance		-	2.5	-	$\text{pF}$
<b><math>T_{\text{amb}} = -40 \text{ }^\circ\text{C to } +125 \text{ }^\circ\text{C}</math></b>						
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	$0.65 \times V_{CC}$	-	-	$\text{V}$
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7	-	-	$\text{V}$
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2.0	-	-	$\text{V}$
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	$0.7 \times V_{CC}$	-	-	$\text{V}$
$V_{IL}$	LOW-level input voltage	$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	-	-	$0.35 \times V_{CC}$	$\text{V}$
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	-	-	0.7	$\text{V}$
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	-	-	0.8	$\text{V}$
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	-	-	$0.3 \times V_{CC}$	$\text{V}$
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH} \text{ or } V_{IL}$				
		$I_O = -100 \mu\text{A}$ ; $V_{CC} = 1.65 \text{ V to } 5.5 \text{ V}$	$V_{CC} - 0.1$	-	-	$\text{V}$
		$I_O = -4 \text{ mA}$ ; $V_{CC} = 1.65 \text{ V}$	0.95	-	-	$\text{V}$
		$I_O = -8 \text{ mA}$ ; $V_{CC} = 2.3 \text{ V}$	1.7	-	-	$\text{V}$
		$I_O = -12 \text{ mA}$ ; $V_{CC} = 2.7 \text{ V}$	1.9	-	-	$\text{V}$
		$I_O = -24 \text{ mA}$ ; $V_{CC} = 3.0 \text{ V}$	2.0	-	-	$\text{V}$
		$I_O = -32 \text{ mA}$ ; $V_{CC} = 4.5 \text{ V}$	3.4	-	-	$\text{V}$
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH} \text{ or } V_{IL}$				
		$I_O = 100 \mu\text{A}$ ; $V_{CC} = 1.65 \text{ V to } 5.5 \text{ V}$	-	-	0.1	$\text{V}$
		$I_O = 4 \text{ mA}$ ; $V_{CC} = 1.65 \text{ V}$	-	-	0.70	$\text{V}$
		$I_O = 8 \text{ mA}$ ; $V_{CC} = 2.3 \text{ V}$	-	-	0.45	$\text{V}$
		$I_O = 12 \text{ mA}$ ; $V_{CC} = 2.7 \text{ V}$	-	-	0.60	$\text{V}$
		$I_O = 24 \text{ mA}$ ; $V_{CC} = 3.0 \text{ V}$	-	-	0.80	$\text{V}$
		$I_O = 32 \text{ mA}$ ; $V_{CC} = 4.5 \text{ V}$	-	-	0.80	$\text{V}$
$I_I$	input leakage current	$V_I = 5.5 \text{ V or GND}$ ; $V_{CC} = 0 \text{ V to } 5.5 \text{ V}$	-	-	$\pm 1$	$\mu\text{A}$
$I_{OFF}$	power-off leakage current	$V_I \text{ or } V_O = 5.5 \text{ V}$ ; $V_{CC} = 0 \text{ V}$	-	-	$\pm 2$	$\mu\text{A}$
$I_{CC}$	supply current	$V_I = 5.5 \text{ V or GND}$ ; $V_{CC} = 1.65 \text{ V to } 5.5 \text{ V}$ ; $I_O = 0 \text{ A}$	-	-	4	$\mu\text{A}$
$\Delta I_{CC}$	additional supply current	per pin; $V_I = V_{CC} - 0.6 \text{ V}$ ; $V_{CC} = 2.3 \text{ V to } 5.5 \text{ V}$ ; $I_O = 0 \text{ A}$	-	-	500	$\mu\text{A}$

[1] All typical values are measured at  $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$ .

## 11. Dynamic characteristics

**Table 8. Dynamic characteristics**

Voltages are referenced to GND (ground 0 V); for test circuit see Fig. 6.

Symbol	Parameter	Conditions	T <sub>amb</sub> = -40 °C to +85 °C			T <sub>amb</sub> = -40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t <sub>pd</sub>	propagation delay	nA, nB to nY; see Fig. 5 [2]						
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.2	3.5	8.6	1.2	10.8	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	0.7	2.3	4.8	0.7	6.0	ns
		V <sub>CC</sub> = 2.7 V	0.7	3.0	5.6	0.7	7.0	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	0.7	2.2	4.3	0.7	5.4	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V	0.5	1.8	3.3	0.5	4.2	ns
C <sub>PD</sub>	power dissipation capacitance	per gate; V <sub>I</sub> = GND to V <sub>CC</sub> [3]	-	14	-	-	-	pF

[1] Typical values are measured at nominal V<sub>CC</sub> and at T<sub>amb</sub> = 25 °C.

[2] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.

[3] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz;

f<sub>o</sub> = output frequency in MHz;

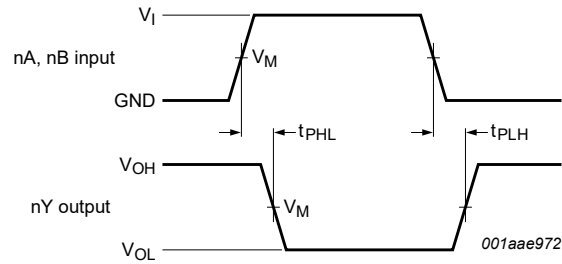
C<sub>L</sub> = output load capacitance in pF;

V<sub>CC</sub> = supply voltage in V;

N = number of inputs switching;

∑(C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs.

### 11.1. Waveforms and test circuit



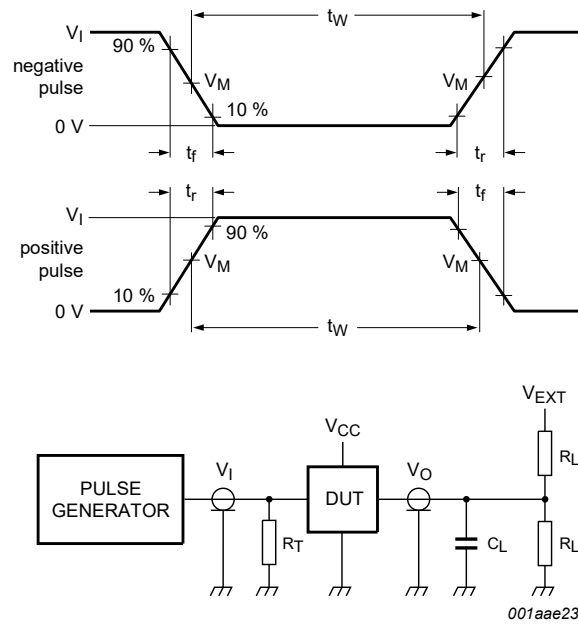
Measurement points are given in [Table 9](#).

$V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig. 5. Input (nA, nB) to output (nY) propagation delays**

**Table 9. Measurement points**

Supply voltage	Input	Output
$V_{CC}$	$V_M$	$V_M$
1.65 V to 1.95 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.3 V to 2.7 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.7 V	1.5 V	1.5 V
3.0 V to 3.6 V	1.5 V	1.5 V
4.5 V to 5.5 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$



Test data is given in [Table 10](#).

Definitions for test circuit:

$R_L$  = Load resistance;

$C_L$  = Load capacitance including jig and probe capacitance;

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator;

$V_{EXT}$  = Test voltage for switching times.

Fig. 6. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Input		Load		$V_{EXT}$
$V_{CC}$	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PLH}, t_{PHL}$
1.65 V to 1.95 V	$V_{CC}$	$\leq 2.0$ ns	30 pF	1 k $\Omega$	open
2.3 V to 2.7 V	$V_{CC}$	$\leq 2.0$ ns	30 pF	500 $\Omega$	open
2.7 V	2.7 V	$\leq 2.5$ ns	50 pF	500 $\Omega$	open
3.0 V to 3.6 V	2.7 V	$\leq 2.5$ ns	50 pF	500 $\Omega$	open
4.5 V to 5.5 V	$V_{CC}$	$\leq 2.5$ ns	50 pF	500 $\Omega$	open



12. Package outline

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1

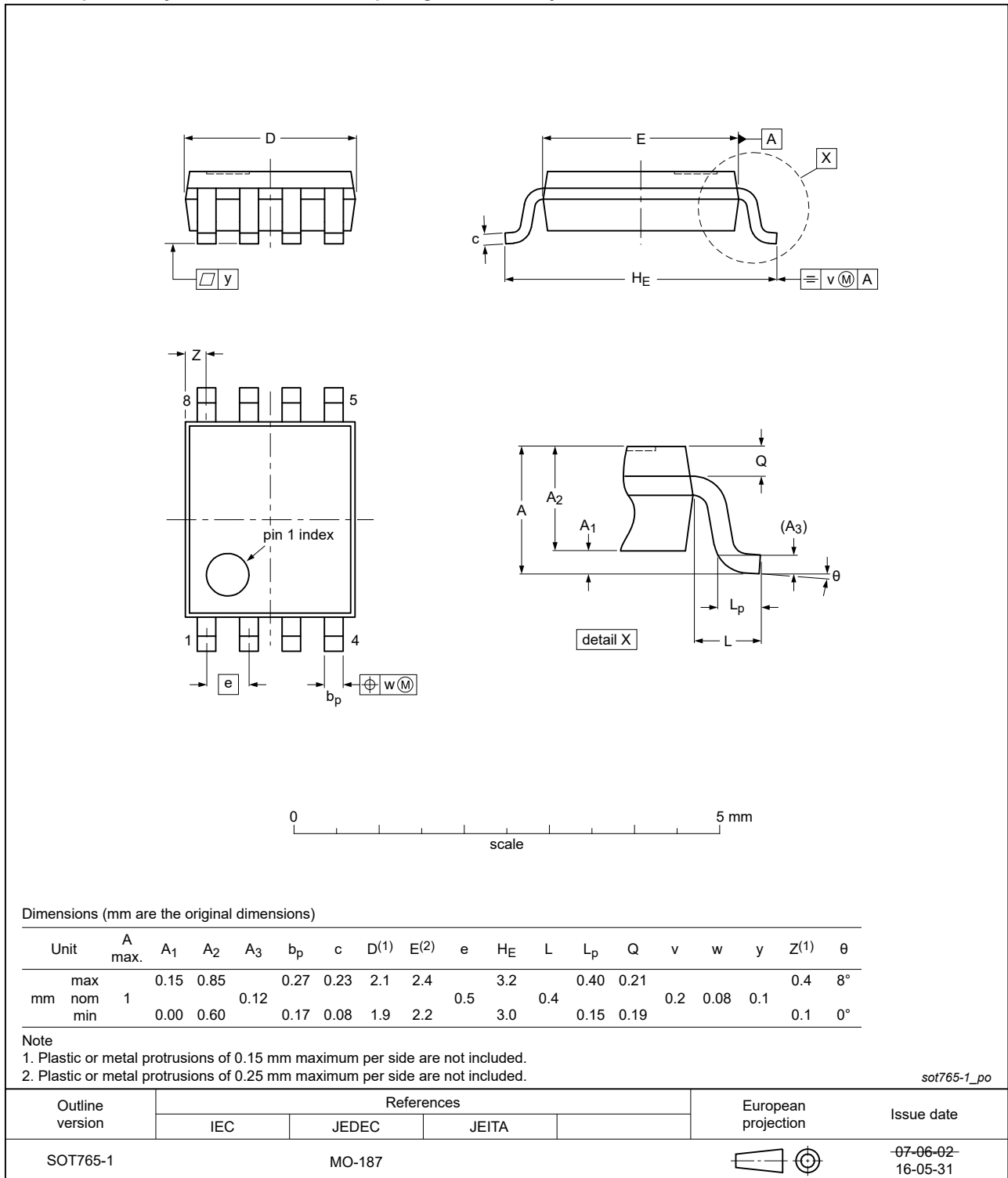


Fig. 7. Package outline SOT765-1 (VSSOP8)

## 13. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MIL	Military
MM	Machine Model
TTL	Transistor-Transistor Logic

## 14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC2G00_Q100 v.3	20220620	Product data sheet	-	74LVC2G00_Q100 v.2
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li><a href="#">Table 5</a>: P<sub>tot</sub> total power dissipation and derating values have been updated.</li> <li><a href="#">Section 1</a> and <a href="#">Section 2</a> updated.</li> </ul>			
74LVC2G00_Q100 v.2	20161213	Product data sheet	-	74LVC2G00_Q100 v.1
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Table 7</a>: The maximum limits for leakage current and supply current have changed.</li> </ul>			
74LVC2G00_Q100 v.1	20150903	Product data sheet	-	-

## 15. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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Date of release: 20 June 2022