74LVC3G06

Triple inverter with open-drain output

Rev. 15 — 20 April 2021

Product data sheet

1. General description

The 74LVC3G06 is a triple inverter with open-drain outputs. Inputs can be driven from either 3.3~V or 5~V devices. This feature allows the use of these devices as translators in mixed 3.3~V and 5~V environments.

Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times.

This device is fully specified for partial power down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

2. Features and benefits

- Wide supply voltage range from 1.65 V to 5.5 V
- Overvoltage tolerant inputs to 5.5 V
- · High noise immunity
- Complies with JEDEC standard:
 - JESD8-7 (1.65 V to 1.95 V)
 - JESD8-5 (2.3 V to 2.7 V)
 - JESD8-B/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V
- -24 mA output drive (V_{CC} = 3.0 V)
- CMOS low power consumption
- Latch-up performance exceeds 250 mA
- · Direct interface with TTL levels
- I_{OFF} circuitry provides partial Power-down mode operation
- · Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C



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3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC3G06DP	-40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	SOT505-2
74LVC3G06DC	-40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1
74LVC3G06GT	-40 °C to +125 °C	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body 1 × 1.95 × 0.5 mm	SOT833-1
74LVC3G06GN	-40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.2 × 1.0 × 0.35 mm	SOT1116
74LVC3G06GS	-40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.35 × 1.0 × 0.35 mm	SOT1203

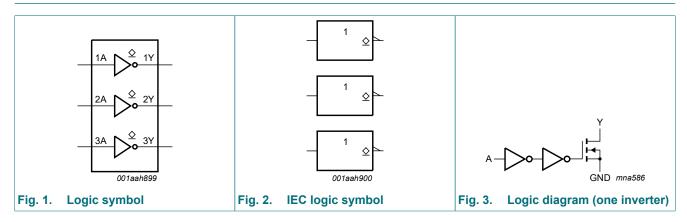
4. Marking

Table 2. Marking codes

able 1 marking deade		
Type number	Marking code [1]	
74LVC3G06DP	V06	
74LVC3G06DC	V06	
74LVC3G06GT	V06	
74LVC3G06GN	V6	
74LVC3G06GS	V6	

^[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram



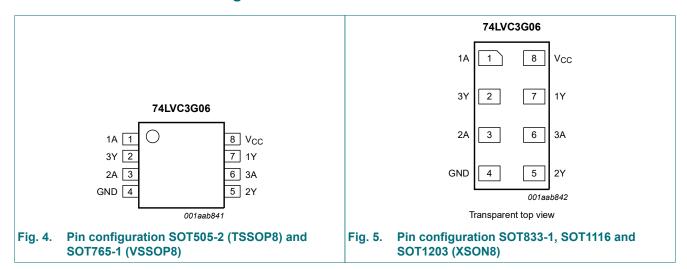
Product data sheet

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6. Pinning information

6.1. Pinning



6.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
1A, 2A, 3A	1, 3, 6	data input
1Y, 2Y, 3Y	7, 5, 2	data output
GND	4	ground (0 V)
Vcc	8	supply voltage

7. Functional description

Table 4. Function table

 $H = HIGH \ voltage \ level; \ L = LOW \ voltage \ level; \ Z = high-impedance \ OFF-state.$

Input nA	Output nY
L	Z
Н	L

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8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+6.5	V
I _{IK}	input clamping current	V _I < 0 V	-50	-	mA
VI	input voltage	[1]	-0.5	+6.5	V
I _{OK}	output clamping current	V _O < 0 V	-50	-	mA
Vo	output voltage	Active mode [1]	-0.5	+6.5	V
		Power-down mode; V _{CC} = 0 V [1]	-0.5	+6.5	V
Io	output current	V _O = 0 V to 6.5 V	-	50	mA
I _{CC}	supply current		-	100	mA
I _{GND}	ground current		-100	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C [2]	-	250	mW

^[1] The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed.

9. Recommended operating conditions

Table 6. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		1.65	5.5	V
VI	input voltage		0	5.5	V
Vo	output voltage	Active mode	0	5.5	V
		Power-down mode; V _{CC} = 0 V	0	5.5	V
T _{amb}	ambient temperature		-40	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 1.65 V to 2.7 V	-	20	ns/V
		V _{CC} = 2.7 V to 5.5 V	-	10	ns/V

^[2] For SOT505-2 (TSSOP8) package: Ptot derates linearly with 4.6 mW/K above 96 °C.

For SOT765-1 (VSSOP8) package: Ptot derates linearly with 4.9 mW/K above 99 °C.

For SOT833-1 (XSON8) package: Ptot derates linearly with 3.1 mW/K above 68 °C.

For SOT1116 (XSON8) package: P_{tot} derates linearly with 4.2 mW/K above 90 °C.

For SOT1203 (XSON8) package: Ptot derates linearly with 3.6 mW/K above 81 °C.

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10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
T _{amb} = -	40 °C to +85 °C				1	
V _{IH}	HIGH-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65V _{CC}	-	-	V
		V _{CC} = 2.3 V to 2.7 V	1.7	-	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	V
		V _{CC} = 4.5 V to 5.5 V	0.7V _{CC}	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 1.65 V to 1.95 V	-	-	0.35V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	V
		V _{CC} = 4.5 V to 5.5 V	-	-	0.3V _{CC}	V
V_{OL}	LOW-level output	$V_I = V_{IH}$ or V_{IL}				
	voltage	I _O = 100 μA; V _{CC} = 1.65 V to 5.5 V	-	-	0.10	V
		I _O = 4 mA; V _{CC} = 1.65 V	-	-	0.45	V
		I _O = 8 mA; V _{CC} = 2.3 V	-	-	0.30	V
	I _O = 12 mA; V _{CC} = 2.7 V	-	-	0.40	V	
		I _O = 24 mA; V _{CC} = 3.0 V	-	-	0.55	V
		$I_O = 32 \text{ mA}; V_{CC} = 4.5 \text{ V}$	-	-	0.55	V
l _l	input leakage current	$V_I = 5.5 \text{ V or GND}; V_{CC} = 0 \text{ V to } 5.5 \text{ V}$ [2]	-	±0.1	±1	μΑ
l _{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL} ; $V_O = V_{CC}$ or GND; $V_{CC} = 5.5 \text{ V}$	-	±0.1	±2	μA
I _{OFF}	power-off leakage current	$V_1 \text{ or } V_0 = 5.5 \text{ V}; V_{CC} = 0 \text{ V}$	-	±0.1	±2	μΑ
I _{CC}	supply current	V _I = 5.5 V or GND; I _O = 0 A; V _{CC} = 1.65 V to 5.5 V	-	0.1	4	μΑ
ΔI _{CC}	additional supply current	per pin; $V_1 = V_{CC} - 0.6 \text{ V}$; $I_0 = 0 \text{ A}$; [2] $V_{CC} = 2.3 \text{ V}$ to 5.5 V	-	5	500	μΑ
Cı	input capacitance		-	2.5	-	pF
T _{amb} = -	40 °C to +125 °C					
V _{IH}	HIGH-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65V _{CC}	-	-	V
		V _{CC} = 2.3 V to 2.7 V	1.7	-	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	V
		V _{CC} = 4.5 V to 5.5 V	0.7V _{CC}	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 1.65 V to 1.95 V	-	-	0.35V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	V
		V _{CC} = 4.5 V to 5.5 V	-	-	0.3V _{CC}	V

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Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
V _{OL}	LOW-level output	$V_I = V_{IH}$ or V_{IL}				
	voltage	$I_O = 100 \ \mu A; \ V_{CC} = 1.65 \ V \ to \ 5.5 \ V$	-	-	0.10	V
		I _O = 4 mA; V _{CC} = 1.65 V	-	-	0.70	V
		I _O = 8 mA; V _{CC} = 2.3 V	-	-	0.45	V
		I _O = 12 mA; V _{CC} = 2.7 V	-	-	0.60	V
		I _O = 24 mA; V _{CC} = 3.0 V	-	-	0.80	V
		I _O = 32 mA; V _{CC} = 4.5 V	-	-	0.80	V
Iį	input leakage current	V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V	-	-	±1	μΑ
I _{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL} ; $V_O = V_{CC}$ or GND; $V_{CC} = 5.5 \text{ V}$	-	-	±2	μΑ
I _{OFF}	power-off leakage current	V_{I} or $V_{O} = 5.5 \text{ V}$; $V_{CC} = 0 \text{ V}$	-	-	±2	μΑ
I _{CC}	supply current	V _I = 5.5 V or GND; I _O = 0 A; V _{CC} = 1.65 V to 5.5 V	-	-	4	μΑ
ΔI _{CC}	additional supply current	per pin; $V_I = V_{CC}$ - 0.6 V; $I_O = 0$ A; $V_{CC} = 2.3$ V to 5.5 V	-	-	500	μΑ

All typical values are measured at T_{amb} = 25 °C.

11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 7.

Symbol	Parameter	Conditions	-40	°C to +85	°C	-40 °C to	+125 °C	Unit
			Min	Typ [1]	Max	Min	Max	
t _{pd}	propagation delay	nA to nY; see Fig. 6 [2]						
		V _{CC} = 1.65 V to 1.95 V	1.0	2.6	6.5	1.0	8.2	ns
		V _{CC} = 2.3 V to 2.7 V	0.5	1.6	3.9	0.5	4.9	ns
		V _{CC} = 2.7 V	1.0	2.2	4.2	1.0	5.3	ns
		V _{CC} = 3.0 V to 3.6 V	0.5	2.0	3.4	0.5	4.3	ns
		V _{CC} = 4.5 V to 5.5 V	0.5	1.4	2.9	0.5	3.7	ns
C _{PD}	power dissipation capacitance	V_I = GND to V_{CC} ; V_{CC} = 3.3 V [3]	-	5.9	-	-	-	pF

^[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.8 V, 2.5 V, 2.7 V, 3.3 V and 5.0 V respectively.

 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:

 f_i = input frequency in MHz;

 f_o = output frequency in MHz;

C_L = output load capacitance in pF;

 V_{CC} = supply voltage in V;

N = number of inputs switching;

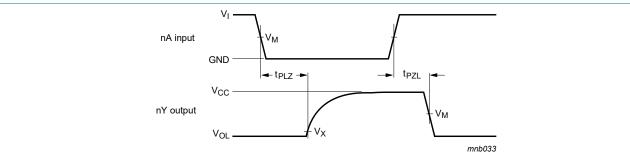
 $\Sigma(C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs.}$

These typical values are measured at V_{CC} = 3.3 V.

 t_{pd} is the same as t_{PLZ} and t_{PZL} . C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

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11.1. Waveforms and test circuit



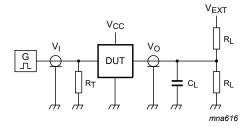
Measurement points are given in Table 9.

V_{OL} is the typical output voltage level that occurs with the output load.

Fig. 6. The input (nA) to output (nY) propagation delays

Table 9. Measurement points

Supply voltage	Input	Output	
V _{CC}	V _M	V _M	V _X
1.65 V to 1.95 V	0.5 × V _{CC}	0.5 × V _{CC}	V _{OL} + 0.15 V
2.3 V to 2.7 V	0.5 × V _{CC}	0.5 × V _{CC}	V _{OL} + 0.15 V
2.7 V	1.5 V	1.5 V	V _{OL} + 0.3 V
3.0 V to 3.6 V	1.5 V	1.5 V	V _{OL} + 0.3 V
4.5 V to 5.5 V	0.5 × V _{CC}	0.5 × V _{CC}	V _{OL} + 0.3 V



Test data is given in <u>Table 10</u>.

Definitions for test circuit:

 R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

 R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

 V_{EXT} = External voltage for measuring switching times.

Fig. 7. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Input		Load		V _{EXT}
V _{CC}	V _I	t _r , t _f	CL	R _L	t _{PZL} , t _{PLZ}
1.65 V to 1.95 V	V _{CC}	≤ 2.0 ns	30 pF	1 kΩ	2 × V _{CC}
2.3 V to 2.7 V	V _{CC}	≤ 2.0 ns	30 pF	500 Ω	2 × V _{CC}
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	6 V
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	6 V
4.5 V to 5.5 V	V _{CC}	≤ 2.5 ns	50 pF	500 Ω	2 × V _{CC}

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12. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2

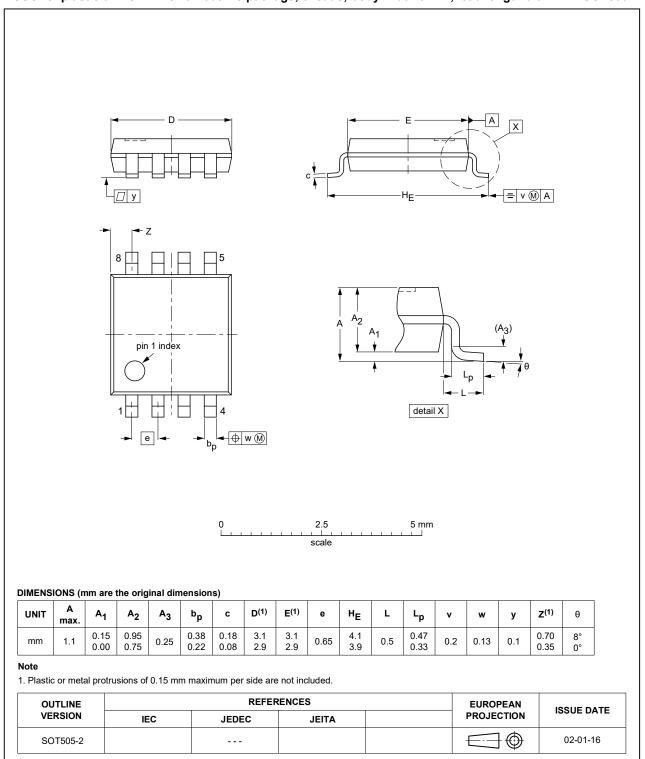


Fig. 8. Package outline SOT505-2 (TSSOP8)

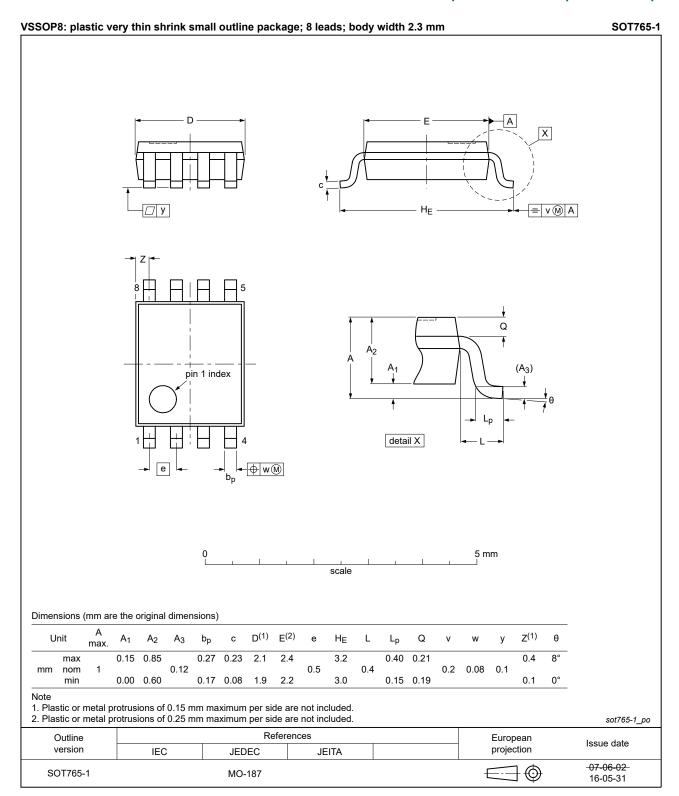


Fig. 9. Package outline SOT765-1 (VSSOP8)

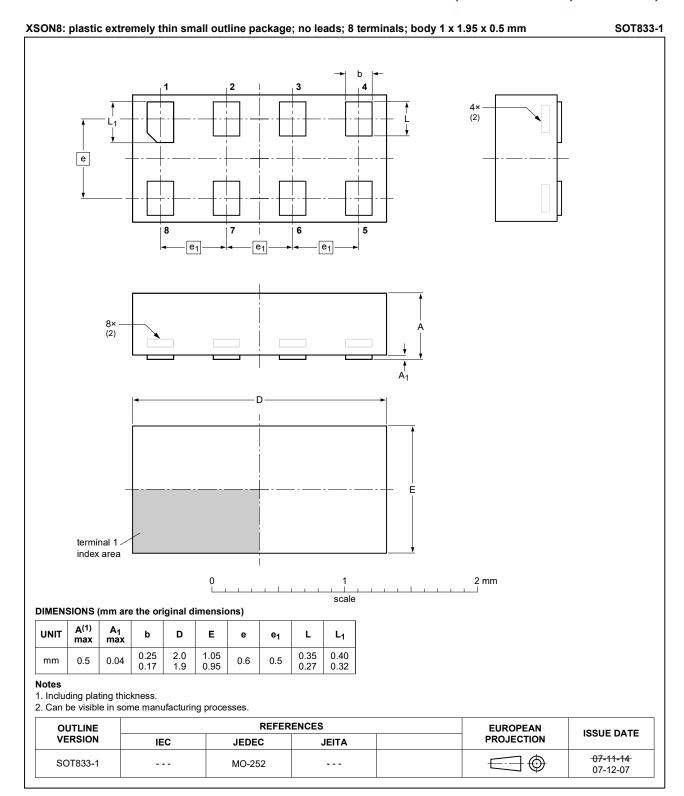


Fig. 10. Package outline SOT833-1 (XSON8)

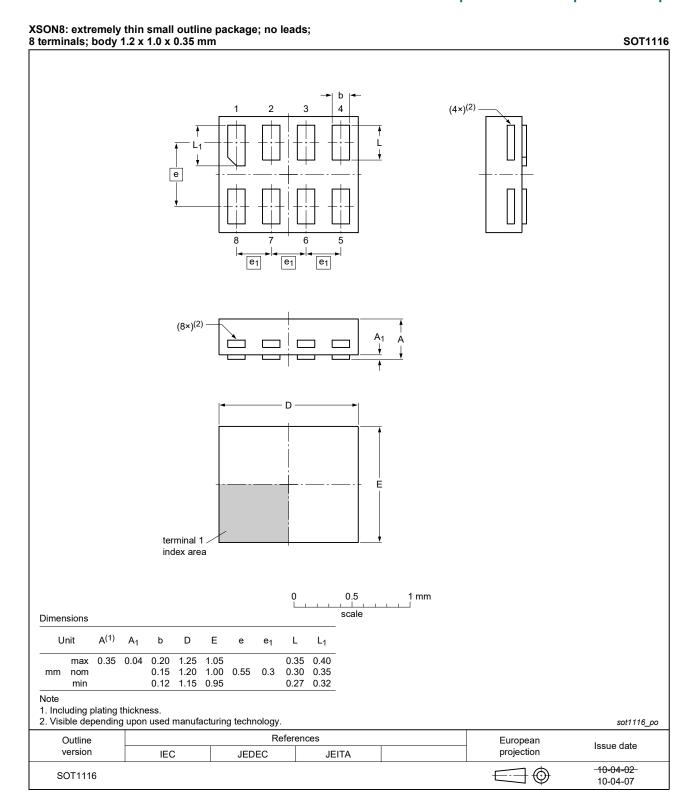


Fig. 11. Package outline SOT1116 (XSON8)

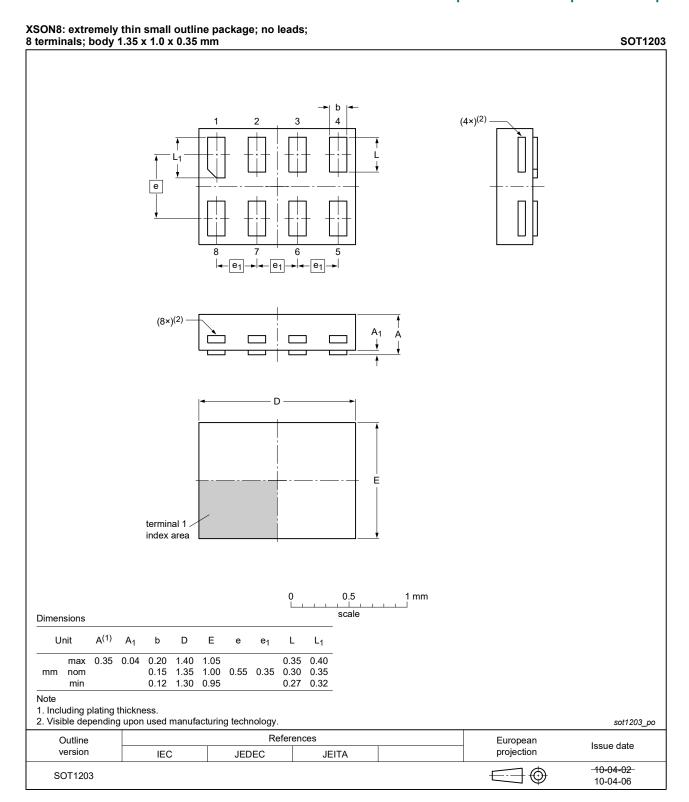


Fig. 12. Package outline SOT1203 (XSON8)

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13. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes	
74LVC3G06 v.15	20210420	Product data sheet	-	74LVC3G06 v.14	
Modifications:	 <u>Section 1</u> and <u>Section 2</u> updated. Type number 74LVC3G06GF (SOT1089 / XSON8) removed. 				
74LVC3G06 v.14	20190731	Product data sheet	-	74LVC3G06 v.13	
Modifications:	 Type number 74LVC3G06GM (SOT902-2) removed. Table 5: Derating values for P_{tot} total power dissipation updated. 				
74LVC3G06 v.13	20190206	Product data sheet	-	74LVC3G06 v.12	
Modifications:	 The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Type number 74LVC3G06GD (SOT996-2) removed. 				
74LVC3G06 v.12	20161215	Product data sheet	-	74LVC3G06 v.11	
Modifications:	• <u>Table 7</u> : The	e maximum limits for leak	kage current and su	pply current have changed.	
74LVC3G06 v.11	20130328	Product data sheet	-	74LVC3G06 v.10	
Modifications:	For type number 74LVC3G06GD XSON8U has changed to XSON8.				
74LVC3G06 v.10	20120627	Product data sheet	-	74LVC3G06 v.9	
Modifications:	For type number 74LVC3G06GM the SOT code has changed to SOT902-2.				
74LVC3G06 v.9	20111123	Product data sheet	-	74LVC3G06 v.8	
Modifications:	Legal pages	s updated.		1	
74LVC3G06 v.8	20100809	Product data sheet	-	74LVC3G06 v.7	
74LVC3G06 v.7	20090312	Product data sheet	-	74LVC3G06 v.6	
74LVC3G06 v.6	20080403	Product data sheet	-	74LVC3G06 v.5	
74LVC3G06 v.5	20070521	Product data sheet	-	74LVC3G06 v.4	
74LVC3G06 v.4	20060302	Product data sheet	-	74LVC3G06 v.3	
74LVC3G06 v.3	20050201	Product data sheet	-	74LVC3G06 v.2	
74LVC3G06 v.2	20041021	Product data sheet	-	74LVC3G06 v.1	
74LVC3G06 v.1	20040607	Product data sheet	-	-	

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15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- Please consult the most recently issued document before initiating or completing a design.
- 2] The term 'short data sheet' is explained in section "Definitions".
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