# HEF4013B-Q100

Dual D-type flip-flop

Rev. 4 — 23 November 2021

**Product data sheet** 

### 1. General description

The HEF4013B-Q100 is a dual D-type flip-flop with set and reset; positive-edge trigger. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of  $V_{DD}$ .

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

#### 2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Wide supply voltage range from 3.0 V to 15.0 V
- CMOS low power dissipation
- High noise immunity
- Tolerant of slow clock rise and fall times
- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- ESD protection:
  - MIL-STD-883, method 3015 exceeds 2000 V
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V (C = 200 pF, R = 0 Ω)
- Complies with JEDEC standard JESD 13-B

### 3. Applications

- · Counters and dividers
- Registers
- Toggle flip-flops

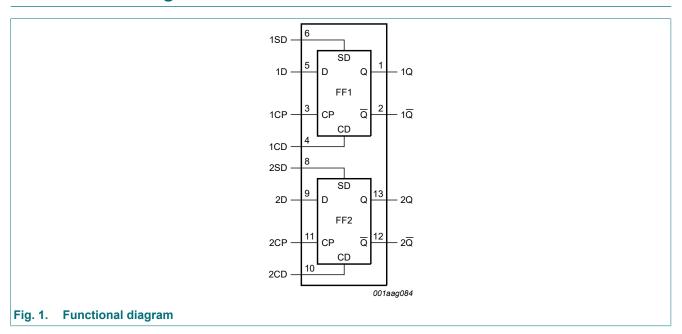
# 4. Ordering information

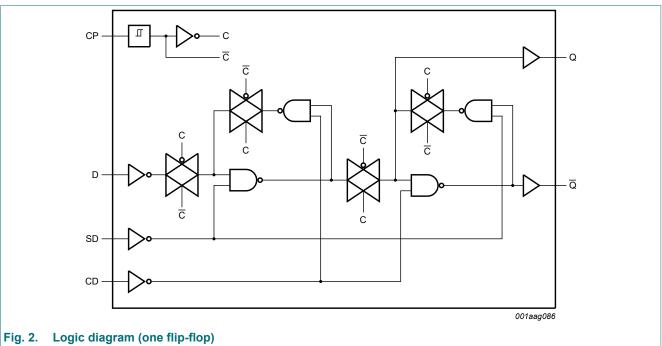
#### **Table 1. Ordering information**

Type number	Package	Package										
	Temperature range	Name	Description	Version								
HEF4013BT-Q100	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1								
HEF4013BTT-Q100	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1								



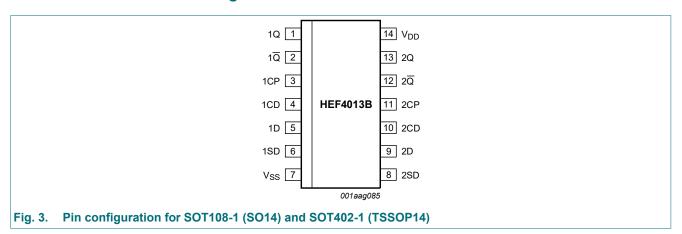
# 5. Functional diagram





# 6. Pinning information

### 6.1. Pinning



### 6.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1Q, 2Q	1, 13	true output
1Q, 2Q	2, 12	complement output
1CP, 2CP	3, 11	clock input (LOW to HIGH edge-triggered)
1CD, 2CD	4, 10	asynchronous clear-direct input (active HIGH)
1D, 2D	5, 9	data input
1SD, 2SD	6, 8	asynchronous set-direct input (active HIGH)
V <sub>SS</sub>	7	ground (0 V)
$V_{DD}$	14	supply voltage

# 7. Functional description

#### Table 3. Function table

 $H = HIGH \ voltage \ level; \ L = LOW \ voltage \ level; \ X = don't \ care; \ \uparrow = LOW-to-HIGH \ clock \ transition.$ 

Control			Input	Output	
nSD	nCD	nCP	nD	nQ	nQ
Н	L	Х	Х	Н	L
L	Н	Х	X	L	Н
Н	Н	Х	Х	Н	Н
L	L	<b>↑</b>	L	L	Н
L	L	1	Н	Н	L

# 8. Limiting values

#### **Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to  $V_{SS} = 0 \text{ V}$  (ground).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DD}$	supply voltage			-0.5	+18	V
I <sub>IK</sub>	input clamping current	$V_{I} < -0.5 \text{ V or } V_{I} > V_{DD} + 0.5 \text{ V}$		-	±10	mA
VI	input voltage			-0.5	V <sub>DD</sub> + 0.5	V
I <sub>OK</sub>	output clamping current	$V_{O}$ < -0.5 V or $V_{O}$ > $V_{DD}$ + 0.5 V		-	±10	mA
I <sub>I/O</sub>	input/output current			-	±10	mA
I <sub>DD</sub>	supply current			-	50	mA
T <sub>stg</sub>	storage temperature			-65	+150	°C
T <sub>amb</sub>	ambient temperature			-40	+125	°C
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 °C to +125 °C	[1]	-	500	mW
Р	power dissipation	per output		-	100	mW

<sup>[1]</sup> For SOT108-1 (SO14) package:  $P_{tot}$  derates linearly with 10.1 mW/K above 100 °C. For SOT402-1 (TSSOP14) package:  $P_{tot}$  derates linearly with 7.3 mW/K above 81 °C.

# 9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD}$	supply voltage		3	15	V
VI	input voltage		0	$V_{DD}$	V
T <sub>amb</sub>	ambient temperature		-40	+125	°C
Δt/ΔV	input transition rise and fall rate	V <sub>DD</sub> = 5 V	-	3.75	μs/V
		V <sub>DD</sub> = 10 V	-	0.5	μs/V
		V <sub>DD</sub> = 15 V	-	0.08	μs/V

## 10. Static characteristics

#### **Table 6. Static characteristics**

 $V_{SS} = 0 \ V$ ;  $V_{I} = V_{SS} \ or \ V_{DD}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	$V_{DD}$	T <sub>amb</sub> =	-40 °C	T <sub>amb</sub> =	+25 °C	T <sub>amb</sub> =	+85 °C	T <sub>amb</sub> = -	+125 °C	Unit
				Min	Max	Min	Max	Min	Max	Min	Max	1
V <sub>IH</sub>	HIGH-level	I <sub>O</sub>   < 1 µA	5 V	3.5	-	3.5	-	3.5	-	3.5	-	V
	input voltage		10 V	7.0	-	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	11.0	-	V
	LOW-level	I <sub>O</sub>   < 1 μA	5 V	-	1.5	-	1.5	-	1.5	-	1.5	V
	input voltage		10 V	-	3.0	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	-	4.0	V
V <sub>OH</sub>	HIGH-level	I <sub>O</sub>   < 1 μA	5 V	4.95	-	4.95	-	4.95	-	4.95	-	V
	output voltage		10 V	9.95	-	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	14.95	-	V
V <sub>OL</sub>	LOW-level	I <sub>O</sub>   < 1 μA	5 V	-	0.05	-	0.05	-	0.05	-	0.05	V
	output voltage		10 V	-	0.05	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	-	0.05	V
I <sub>OH</sub>	HIGH-level output current	V <sub>O</sub> = 2.5 V	5 V	-	-1.7	-	-1.4	-	-1.1	-	-1.1	mA
		V <sub>O</sub> = 4.6 V	5 V	-	-0.64	-	-0.5	-	-0.36	-	-0.36	mA
		V <sub>O</sub> = 9.5 V	10 V	-	-1.6	-	-1.3	-	-0.9	-	-0.9	mA
		V <sub>O</sub> = 13.5 V	15 V	-	-4.2	-	-3.4	-	-2.4	-	-2.4	mA
I <sub>OL</sub>	LOW-level	V <sub>O</sub> = 0.4 V	5 V	0.64	-	0.5	-	0.36	-	0.36	-	mA
	output current	V <sub>O</sub> = 0.5 V	10 V	1.6	-	1.3	-	0.9	-	0.9	-	mA
		V <sub>O</sub> = 1.5 V	15 V	4.2	-	3.4	-	2.4	-	2.4	-	mA
l <sub>l</sub>	input leakage current		15 V	-	±0.1	-	±0.1	-	±1.0	-	±1.0	μΑ
I <sub>DD</sub>	supply current	all valid input	5 V	-	1.0	-	1.0	-	30	-	30	μA
		combinations;	10 V	-	2.0	-	2.0	-	60	-	60	μA
		$ I_O  = 0 A$	15 V	-	4.0	-	4.0	-	120	-	120	μΑ
C <sub>I</sub>	input capacitance		-	-	-	-	7.5	-	-	-	-	pF

# 11. Dynamic characteristics

#### **Table 7. Dynamic characteristics**

 $T_{amb}$  = 25 °C, unless otherwise specified. For test circuit see Fig. 6.

Symbol	Parameter	Conditions	V <sub>DD</sub>	Extrapolation formula	Min	Тур	Max	Unit
t <sub>PHL</sub>	HIGH to LOW	nCP to nQ, nQ;	5 V [1]	83 + 0.55 × C <sub>L</sub>	-	110	220	ns
	propagation delay	see Fig. 4	10 V	34 + 0.23 × C <sub>L</sub>	-	45	90	ns
			15 V	22 + 0.16 × C <sub>L</sub>	-	30	60	ns
		nSD to nQ	5 V [1]	73 + 0.55 × C <sub>L</sub>	-	100	200	ns
			10 V	29 + 0.23 × C <sub>L</sub>	-	40	80	ns
			15 V	22 + 0.16 × C <sub>L</sub>	-	30	60	ns
		nCD to nQ	5 V [1]	73 + 0.55 × C <sub>L</sub>	-	100	200	ns
			10 V	29 + 0.23 × C <sub>L</sub>	-	40	80	ns
			15 V	22 + 0.16 × C <sub>L</sub>	-	30	60	ns
t <sub>PLH</sub>	LOW to HIGH	nCP to nQ, $n\overline{Q}$ ;	5 V [1]	68 + 0.55 × C <sub>L</sub>	-	95	190	ns
	propagation delay	see Fig. 4	10 V	29 + 0.23 × C <sub>L</sub>	-	40	80	ns
			15 V	22 + 0.16 × C <sub>L</sub>	-	30	60	ns
		nSD to nQ	5 V [1]	48 + 0.55 × C <sub>L</sub>	-	75	150	ns
			10 V	24 + 0.23 × C <sub>L</sub>	-	35	70	ns
			15 V	17 + 0.16 × C <sub>L</sub>	-	25	50	ns
		nCD to nQ	5 V [1]	33 + 0.55 × C <sub>L</sub>	-	60	120	ns
			10 V	19 + 0.23 × C <sub>L</sub>	-	30	60	ns
			15 V	12 + 0.16 × C <sub>L</sub>	-	20	40	ns
t <sub>t</sub>	transition time	see Fig. 4	5 V [1]	10 + 1.00 × C <sub>L</sub>	-	60	120	ns
			10 V	9 + 0.42 × C <sub>L</sub>	-	30	60	ns
			15 V	6 + 0.28 × C <sub>L</sub>	-	20	40	ns
t <sub>su</sub>	set-up time	nD to nCP; see Fig. 4	5 V		40	20	-	ns
			10 V		25	10	-	ns
			15 V		15	5	-	ns
t <sub>h</sub>	hold time	nD to nCP; see Fig. 4	5 V		20	0	-	ns
			10 V		20	0	-	ns
			15 V		15	0	-	ns
t <sub>W</sub>	pulse width	nCP input LOW;	5 V		60	30	-	ns
		see Fig. 4	10 V		30	15	-	ns
			15 V		20	10	-	ns
		nSD input HIGH;	5 V		50	25	-	ns
		see <u>Fig. 5</u>	10 V		24	12	-	ns
			15 V		20	10	-	ns
		nCD input HIGH;	5 V		50	25	-	ns
		see <u>Fig. 5</u>	10 V		24	12	-	ns
			15 V		20	10	-	ns

Symbol	Parameter	Conditions	V <sub>DD</sub>	Extrapolation formula	Min	Тур	Max	Unit
t <sub>rec</sub>	recovery time	nSD input; see Fig. 5	5 V		+15	-5	-	ns
			10 V		15	0	-	ns
			15 V		15	0	-	ns
		nCD input; see Fig. 5	5 V		40	25	-	ns
			10 V		25	10	-	ns
			15 V		25	10	-	ns
f <sub>clk(max)</sub>	maximum clock	see Fig. 4	5 V		7	14	-	MHz
frequency		10 V		14	28	-	MHz	
			15 V		20	40	-	MHz

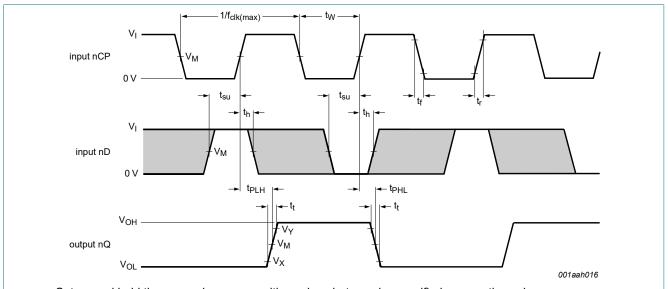
[1] Typical values of the propagation delays and output transition times can be calculated with the extrapolation formulas (C<sub>L</sub> in pF).

#### Table 8. Dynamic power dissipation

 $V_{SS} = 0 \ V; \ t_r = t_f \le 20 \ ns; \ T_{amb} = 25 \ ^{\circ}C.$ 

Symbol	Parameter	$V_{DD}$	Typical formula	Where
$P_D$	dynamic power dissipation	5 V	1 (0 1)	$f_i$ = input frequency in MHz;
		10 V		f <sub>o</sub> = output frequency in MHz; C <sub>L</sub> = output load capacitance in pF;
		15 V		$\Sigma(f_0 \times C_L)$ = sum of the outputs;
				$V_{DD}$ = supply voltage in V.

### 11.1. Waveforms and test circuit

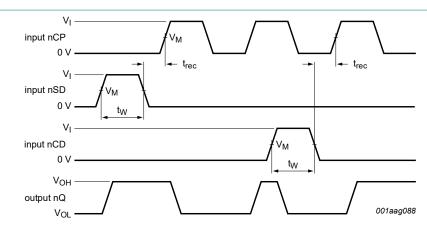


Set-up and hold times are shown as positive values but may be specified as negative values.

The shaded areas indicate when the input is permitted to change for predictable output performance.

Logic levels:  $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load. Measurement points are given in <u>Table 9</u>.

Fig. 4. Set-up time, hold time, minimum clock pulse width, propagation delays and transition times

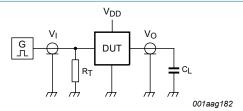


Recovery times are shown as positive values but may be specified as negative values. Logic levels:  $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load. Measurement points are given in <u>Table 9</u>.

Fig. 5. nSD, nCD recovery time and pulse width

#### **Table 9. Measurement points**

Supply voltage	Input	Output	Output								
V <sub>DD</sub>	V <sub>M</sub>	V <sub>M</sub>	V <sub>X</sub>	V <sub>Y</sub>							
5 V to 15 V	0.5V <sub>DD</sub>	0.5V <sub>DD</sub>	0.1V <sub>DD</sub>	0.9V <sub>DD</sub>							



Test and measurement data is given in Table 10;

Definitions test circuit:

 $R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

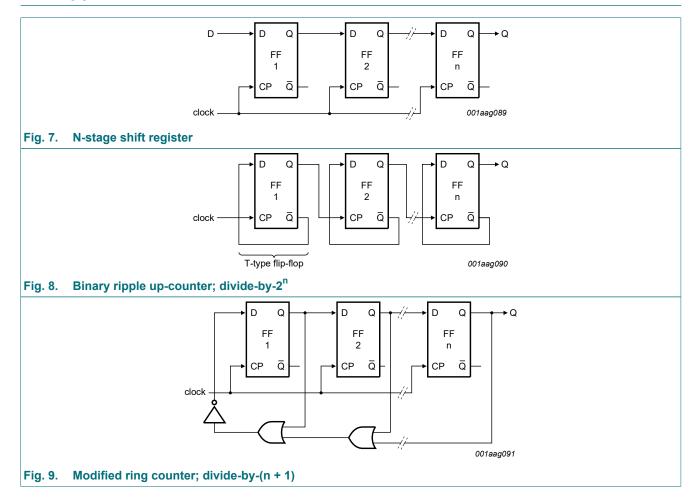
C<sub>L</sub> = Load capacitance including jig and probe capacitance.

Fig. 6. Test circuit for measuring switching times

#### Table 10. Test data

Supply voltage	Input	Load			
$V_{DD}$	V <sub>I</sub>	t <sub>r</sub> , t <sub>f</sub>	C <sub>L</sub>		
5 V to 15 V	V <sub>SS</sub> or V <sub>DD</sub>	≤ 20 ns	50 pF		

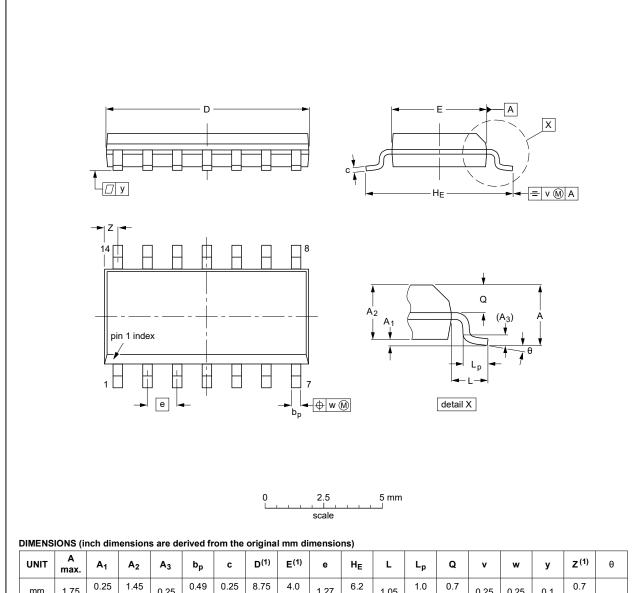
# 12. Application information



# 13. Package outline

#### SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	bp	С	D <sup>(1)</sup>	E <sup>(1)</sup>	е	HE	L	Lp	Q	v	w	у	Z <sup>(1)</sup>	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8°
inches	0.069	0.010 0.004	0.057 0.049	0.01	I	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	0°

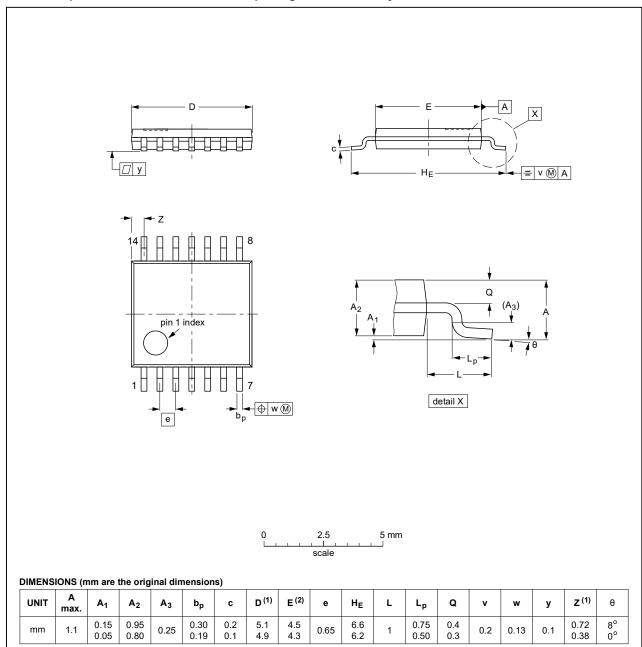
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE	REFERENCES				EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
SOT108-1	076E06	MS-012				<del>99-12-27</del> 03-02-19

Fig. 10. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



#### Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE	REFERENCES				EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
SOT402-1		MO-153				<del>99-12-27</del> 03-02-18

Fig. 11. Package outline SOT402-1 (TSSOP14)

### 14. Abbreviations

#### **Table 11. Abbreviations**

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model
MIL	Military
MM	Machine Model

# 15. Revision history

#### **Table 12. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4013B_Q100 v.4	20211123	Product data sheet	-	HEF4013B_Q100 v.3
Modifications:	<ul> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Section 1 and Section 2 updated.</li> <li>Table 4: Derating values for Ptot total power dissipation updated.</li> </ul>			
HEF4013B_Q100 v.3	20151215	Product data sheet	-	HEF4013B_Q100 v.2
Modifications:	Type number HEF4013BP-Q100 (SOT27-1) removed.			
HEF4013B_Q100 v.2	20130220	Product data sheet	-	HEF4013B_Q100 v.1
Modifications:	• HEF4013BP-Q100 (DIP14) added.			
HEF4013B_Q100 v.1	20120807	Product data sheet	-	-

### 16. Legal information

#### **Data sheet status**

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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