



# PESD5V0V1BLS

Very low capacitance bidirectional ESD protection diode

3 February 2021

Product data sheet

## 1. General description

Very low capacitance bidirectional ElectroStatic Discharge (ESD) protection diode designed to protect one signal line from the damage caused by ESD and other transients. The device is housed in a leadless ultra small DFN1006BD-2 (SOD882BD) Surface-Mounted Device (SMD) plastic package with side-wettable flanks (SWF).

## 2. Features and benefits

- Bidirectional ESD protection of one line
- Ultra small SMD plastic package
- Side wettable flanks
- Very low diode capacitance:  $C_d = 11$  pF
- Low clamping voltage:  $V_{CL} = 12.5$  V
- Ultra low leakage current:  $I_{RM}$  typ.  $< 1$  nA
- ESD protection up to 30 kV
- IEC 61000-4-2; level 4 (ESD)
- IEC 61000-4-5 (surge);  $I_{PPM} = 4.8$  A
- AEC-Q101 qualified

## 3. Applications

- Computers and peripherals
- Audio and video equipment
- Cellular handsets and accessories
- SIM card protection
- Communication systems
- Portable electronics

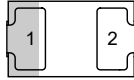
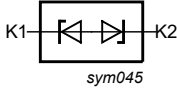
## 4. Quick reference data

Table 1. Quick reference data

| Symbol    | Parameter                | Conditions                                  | Min | Typ | Max | Unit |
|-----------|--------------------------|---|-----|-----|-----|------|
| $C_d$     | diode capacitance        | $f = 1$ MHz; $V_R = 0$ V; $T_{amb} = 25$ °C | -   | 11  | 13  | pF   |
| $V_{RWM}$ | reverse standoff voltage | $T_{amb} = 25$ °C                           | -   | -   | 5   | V    |

## 5. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description            | Simplified outline   | Graphic symbol   |
|-----|--------|------------------------|--|--|
| 1   | K      | cathode <sup>[1]</sup> |  <p>Transparent<br/>top view</p> <p><b>DFN1006BD-2 (SOD882BD)</b></p> |  <p><i>sym045</i></p> |
| 2   | K2     | cathode 2              |  |  |

[1] The marking bar indicates pin 1.

## 6. Ordering information

Table 3. Ordering information

| Type number  | Package     |  |          |
|--------------|-------------|--|----------|
|              | Name        | Description  | Version  |
| PESD5V0V1BLS | DFN1006BD-2 | Leadless ultra small plastic package with side-wettable flanks (SWF); 2 terminals; 0.65 mm pitch; 1 mm x 0.6 mm x 0.47 mm body | SOD882BD |

## 7. Marking

Table 4. Marking codes

| Type number  | Marking code |
|--------------|--------------|
| PESD5V0V1BLS | 3Q           |

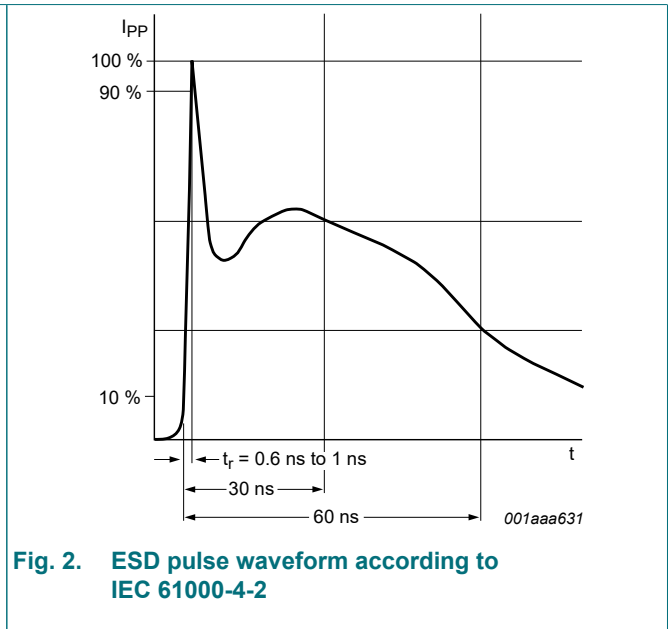
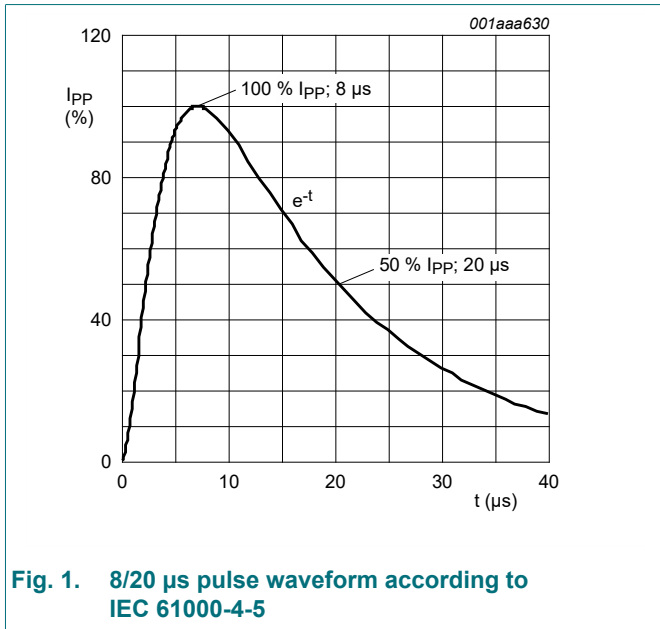
## 8. Limiting values

**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol                     | Parameter                       | Conditions                        |     | Min | Max | Unit |
|----------------------------|---------------------------------|-----------------------------------|-----|-----|-----|------|
| $I_{PPM}$                  | rated peak pulse current        | $t_p = 8/20 \mu s$                | [1] | -   | 4.8 | A    |
| $T_j$                      | junction temperature            |                                   |     | -   | 150 | °C   |
| $T_{amb}$                  | ambient temperature             |                                   |     | -55 | 150 | °C   |
| $T_{stg}$                  | storage temperature             |                                   |     | -65 | 150 | °C   |
| <b>ESD maximum ratings</b> |                                 |                                   |     |     |     |      |
| $V_{ESD}$                  | electrostatic discharge voltage | IEC 61000-4-2 (contact discharge) | [2] | -   | 30  | kV   |

- [1] Non-repetitive current pulse 8/20  $\mu s$  exponential decay waveform according to IEC 61000-4-5.
- [2] Device stressed with ten non-repetitive ESD pulses.



## 9. Characteristics

Table 6. Characteristics

| Symbol    | Parameter                | Conditions   | Min | Typ | Max  | Unit     |
|-----------|--------------------------|--|-----|-----|------|----------|
| $V_{RWM}$ | reverse standoff voltage | $T_{amb} = 25\text{ °C}$                                     | -   | -   | 5    | V        |
| $V_{BR}$  | breakdown voltage        | $I_R = 5\text{ mA}; T_{amb} = 25\text{ °C}$                  | 5.8 | 6.8 | 7.8  | V        |
| $I_{RM}$  | reverse leakage current  | $V_{RWM} = 5\text{ V}; T_{amb} = 25\text{ °C}$               | -   | 1   | 10   | nA       |
| $C_d$     | diode capacitance        | $f = 1\text{ MHz}; V_R = 0\text{ V}; T_{amb} = 25\text{ °C}$ | -   | 11  | 13   | pF       |
| $V_{CL}$  | clamping voltage         | $I_{PP} = 4.8\text{ A}; T_{amb} = 25\text{ °C}$              | [1] | -   | 12.5 | V        |
| $R_{dyn}$ | dynamic resistance       | $I_R = 10\text{ A}; T_{amb} = 25\text{ °C}$                  | [2] | 0.2 | -    | $\Omega$ |

[1] Non-repetitive current pulse 8/20  $\mu$ s exponential decay waveform according to IEC 61000-4-5.

[2] Non-repetitive current pulse, Transmission Line Pulse (TLP)  $t_p = 100\text{ ns}$ ; square pulse; ANSI/ESD STM5.5.1-20088.

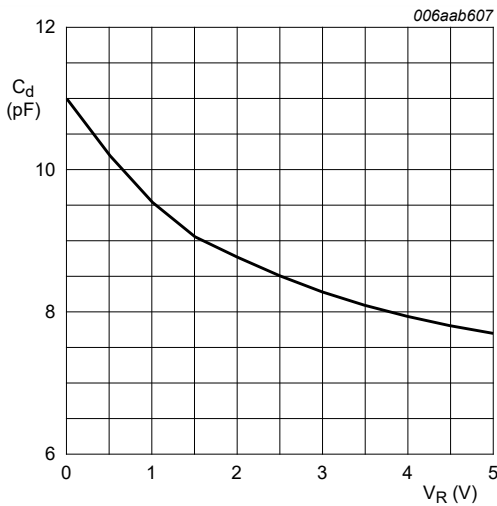


Fig. 3. Diode capacitance as a function of reverse voltage; typical values

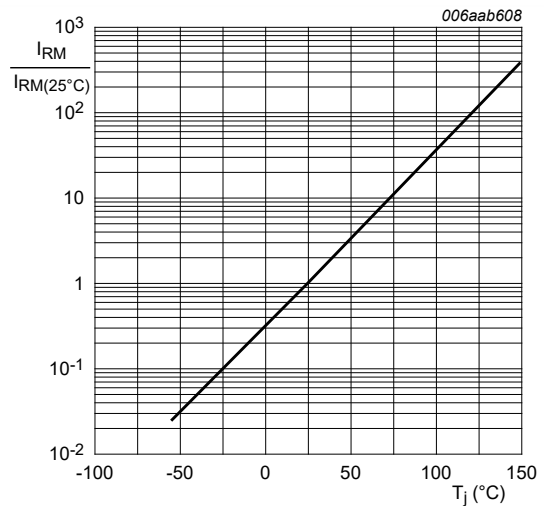


Fig. 4. Relative variation of reverse leakage current as a function of junction temperature; typical values

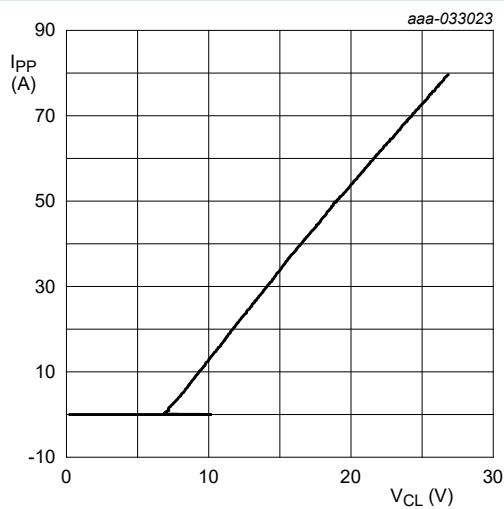


Fig. 5. Dynamic resistance with positive clamping; typical values

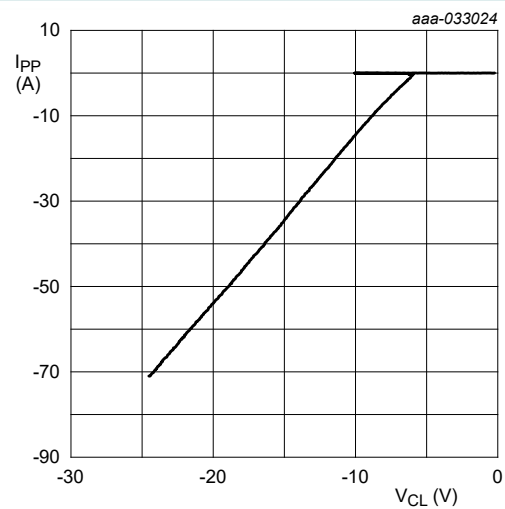
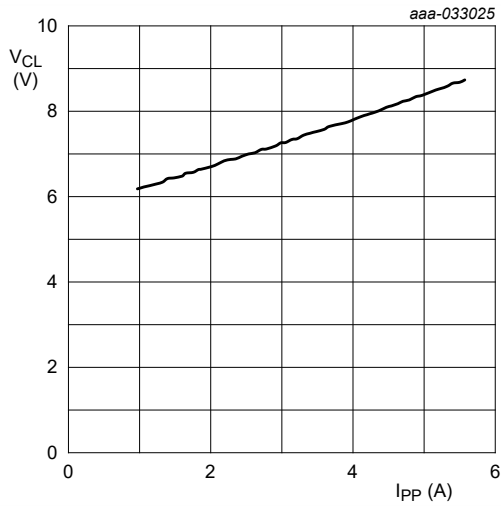
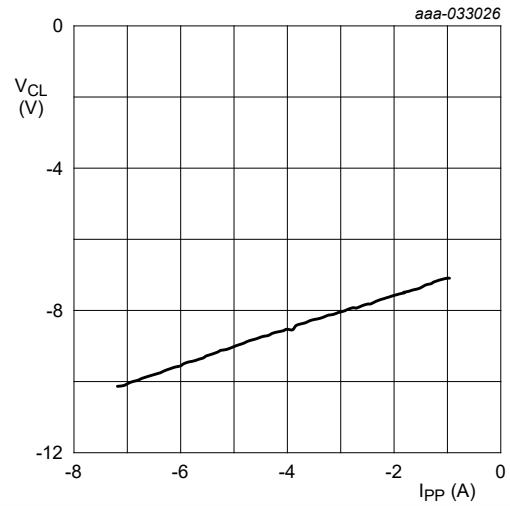


Fig. 6. Dynamic resistance with negative clamping; typical values



IEC 61000-4-5;  $t_p = 8/20 \mu s$ ; positive pulse

**Fig. 7. Dynamic resistance with positive clamping; typical values**



IEC 61000-4-5;  $t_p = 8/20 \mu s$ ; negative pulse

**Fig. 8. Dynamic resistance with negative clamping; typical values**

## 10. Application information

The device is designed for the protection of one bidirectional data of signal line from the damage caused by ESD and surge pulses. The device may be used on lines where the signal polarities are both, positive or negative with respect to ground.

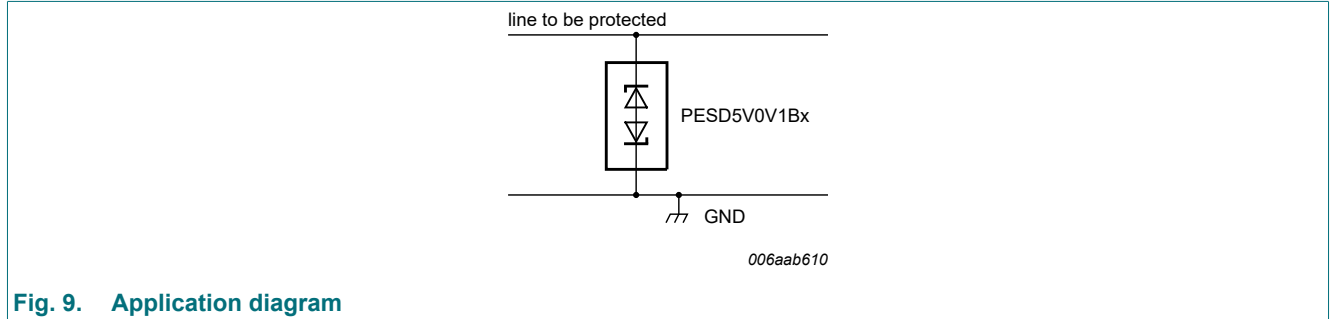


Fig. 9. Application diagram

### Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the device as close to the input terminal or connector as possible.
2. Minimize the path length between the device and the protected line.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

## 11. Test information

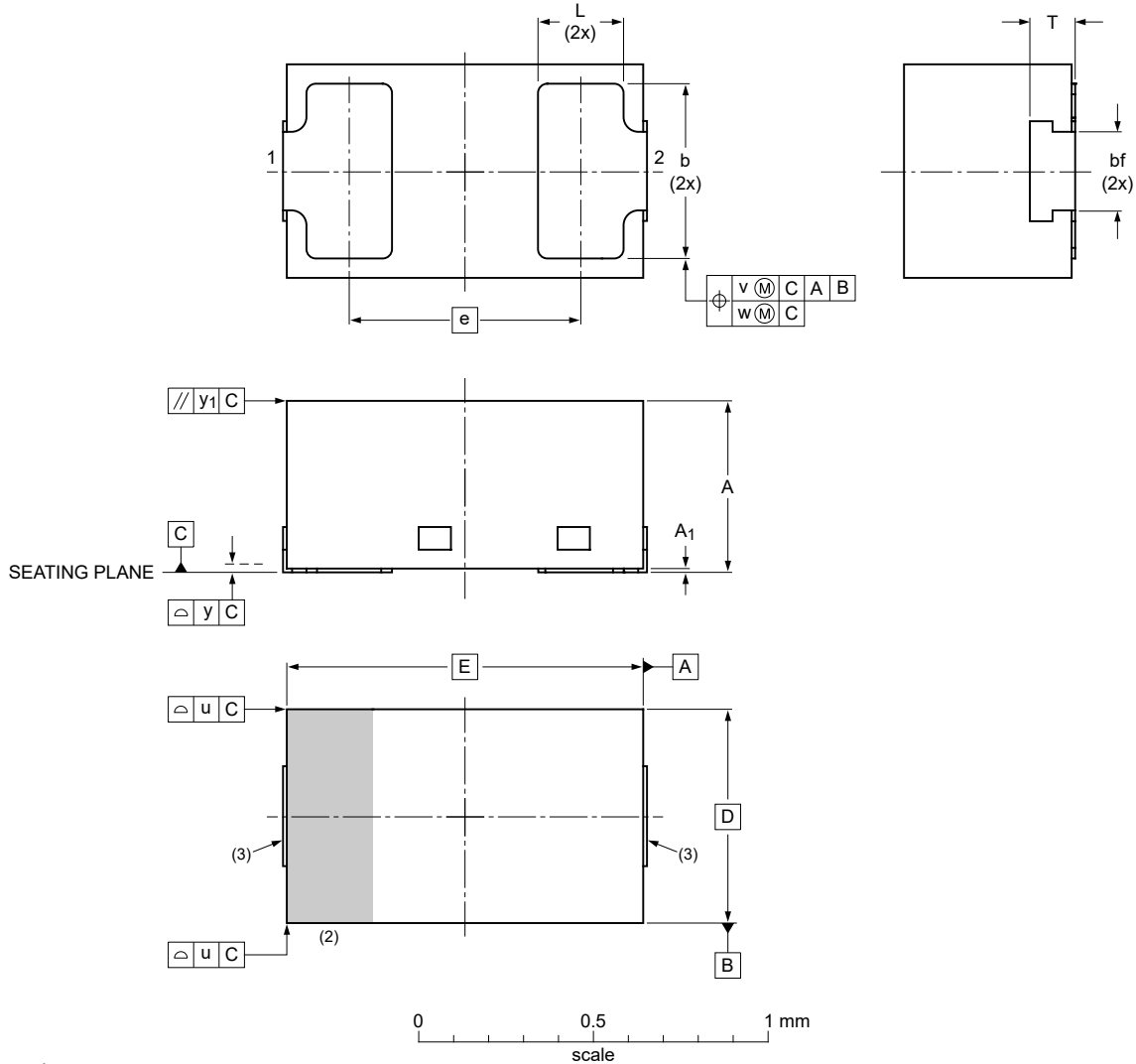
### Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

## 12. Package outline

**DFN1006BD-2** Leadless ultra small plastic package with side-wettable flanks (SWF); 2 terminals;  
0.65 mm pitch; 1 mm x 0.6 mm x 0.47 mm body

**SOD882BD**



Dimensions

| Unit   | A <sup>(1)</sup> | A <sub>1</sub> | bf <sup>(1)</sup> | b    | D    | E    | e    | L    | T <sup>(1)</sup> | u    | v    | w    | y    | y <sub>1</sub> |
|--------|------------------|----------------|-------------------|------|------|------|------|------|------------------|------|------|------|------|----------------|
| max    | 0.50             | 0.04           |                   | 0.55 |      |      |      | 0.30 | 0.22             |      |      |      |      |                |
| mm nom | 0.47             |                |                   | 0.50 | 0.60 | 1.00 | 0.65 | 0.25 | 0.16             | 0.05 | 0.10 | 0.05 | 0.05 | 0.05           |
| min    | 0.44             |                | 0.20              | 0.45 |      |      |      | 0.22 | 0.10             |      |      |      |      |                |

Note

1. Dimension including plating thickness.
2. The marking bar indicates the cathode.
3. Solderable lead end, protrusion max. 0.02 mm.

sod882bd\_po

| Outline version | References |          |       |  | European projection | Issue date           |
|-----------------|------------|----------|-------|--|---------------------|----------------------|
|                 | IEC        | JEDEC    | JEITA |  |                     |                      |
| SOD882BD        |            | MO-343AA |       |  |                     | 20-06-22<br>20-06-23 |

**Fig. 10. Package outline DFN1006BD-2 (SOD882BD)**

### 13. Soldering

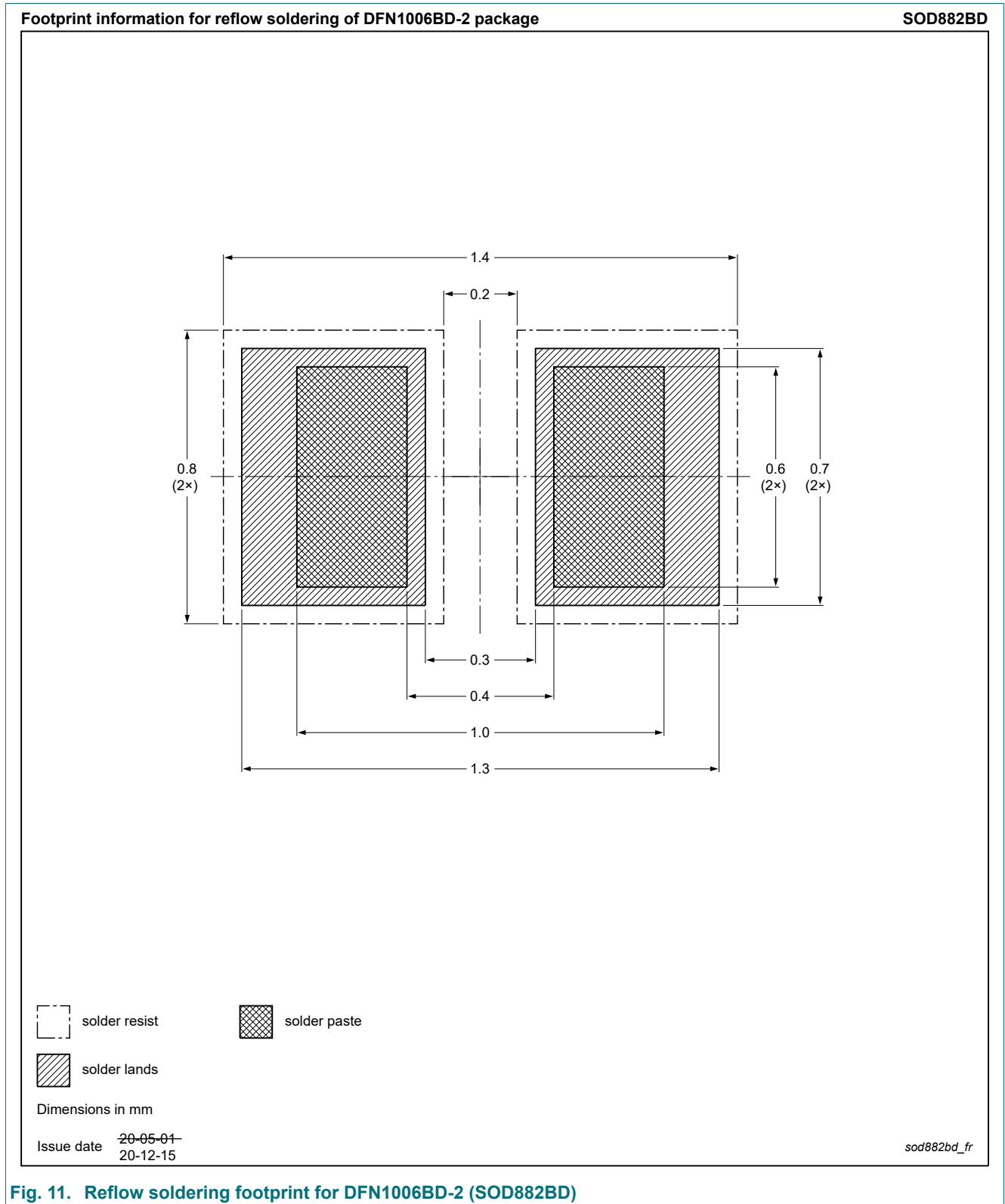


Fig. 11. Reflow soldering footprint for DFN1006BD-2 (SOD882BD)



## 14. Revision history

Table 7. Revision history

| Data sheet ID    | Release date | Data sheet status  | Change notice | Supersedes |
|------------------|--------------|--------------------|---------------|------------|
| PESD5V0V1BLS v.1 | 20210203     | Product data sheet | -             | -          |

## 15. Legal information

### Data sheet status

| Document status [1][2]         | Product status [3] | Definition  |
|--------------------------------|--------------------|---|
| Objective [short] data sheet   | Development        | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification      | This document contains data from the preliminary specification.                       |
| Product [short] data sheet     | Production         | This document contains the product specification.                                     |

- [1] Please consult the most recently issued document before initiating or completing a design.
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