Product data sheet

1. General description

Unidirectional ElectroStatic Discharge (ESD) protection diode designed to protect one signal line from the damage caused by ESD and other transients. The device is housed in a SOD882D leadless ultra small Surface-Mounted Device (SMD) plastic package with visible and solderable side pads.

2. Features and benefits

- Unidirectional ESD protection of one line
- Very high surge robustness; IPP = 16 A for 8/20 s pulse; averaged measured
- · ESD protection up to 30 kV
- Ultra small plastic package 1.0 x 0.6 x 0.37 mm
- AEC-Q101 qualified

3. Applications

· ESD and surge protection for interface lines

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V_{RWM}	reverse standoff voltage	T _{amb} = 25 °C		-	-	8	V
V _{CL}	clamping voltage	$I_{PPM} = 13 \text{ A}; t_p = 8/20 \mu\text{s}; T_{amb} = 25 ^{\circ}\text{C}$	[1]	-	18.5	22	V

[1] Device stressed with 8/20 µs exponential decay waveform according to IEC 61000-4-5.



5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K	cathode[1]		K [4] A
2	A	anode	Transparent top view DFN1006D-2 (SOD882D)	006aaa152

[1] The marking bar indicates the cathode.

6. Ordering information

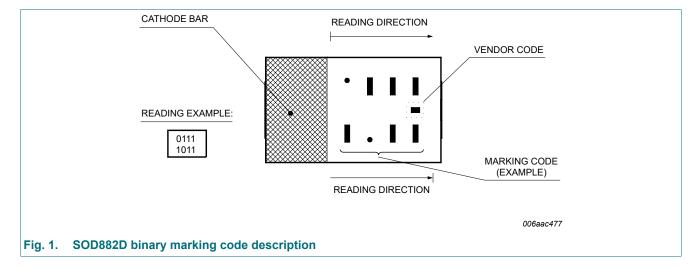
Table 3. Ordering information

Type number	Package			
	Name	Description	Version	
PESD8V0S1ULD		leadless ultra small plastic package with side-wettable flanks (SWF); 2 terminals; 0.65 mm pitch; 1 mm x 0.6 mm x 0.4 mm body	SOD882D	

7. Marking

Table 4. Marking codes

Type number	Marking code
PESD8V0S1ULD	1111
	1000



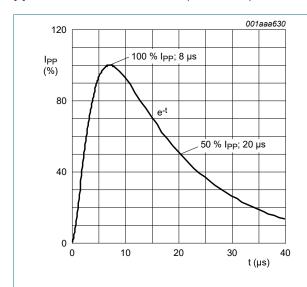
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
P _{PPM}	rated peak pulse power	t _p = 8/20 μs	[1]	-	286	W
I _{PPM}	rated peak pulse current		[1]	-	13	Α
T _j	junction temperature			-	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C
ESD maxim	num ratings		•			'
V _{ESD}	electrostatic discharge	IEC 61000-4-2 (contact discharge)	[2]	-	30	kV
	voltage	ISO 10605; contact discharge; C = 330 pF, R = 330 Ω		-	30	kV

- Non-repetitive current pulse $8/20~\mu s$ exponential decay waveform according to IEC 61000-4-5. Device stressed with ten non-repetitive ESD pulses.



8/20 µs pulse waveform according to Fig. 2. IEC 61000-4-5

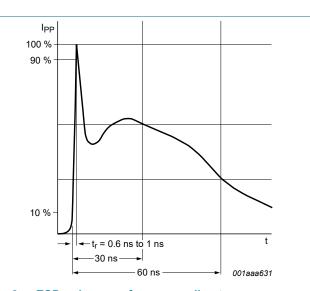


Fig. 3. ESD pulse waveform according to IEC 61000-4-2

9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V_{RWM}	reverse standoff voltage	T _{amb} = 25 °C		-	-	8	V
V_{BR}	breakdown voltage	I _R = 1 mA; T _{amb} = 25 °C		8.65	9.1	9.56	V
I _{RM}	reverse leakage current	V _{RWM} = 8 V; T _{amb} = 25 °C		-	5	500	nA
C _d	diode capacitance	f = 1 MHz; V _R = 0 V; T _{amb} = 25 °C		-	70	90	pF
V _{CL}	clamping voltage	I _{PP} = 1 A; t _p = 8/20 μs; T _{amb} = 25 °C	[1]	-	9.5	11.5	V
		I_{PPM} = 13 A; t_p = 8/20 µs; T_{amb} = 25 °C	[1]	-	18.5	22	V
		I _{PP} = 16 A; t _p = TLP; T _{amb} = 25 °C	[2]	-	15.5	-	V
R _{dyn}	dynamic resistance	I _R = 10 A; T _{amb} = 25 °C	[2]	-	0.4	-	Ω

- [1] Device stressed with 8/20 µs exponential decay waveform according to IEC 61000-4-5.
- [2] Non-repetitive current pulse; Transmission Line Pulse (TLP) t_p = 100 ns; square pulse; ANSI / ESD STM5.5.1-2008.

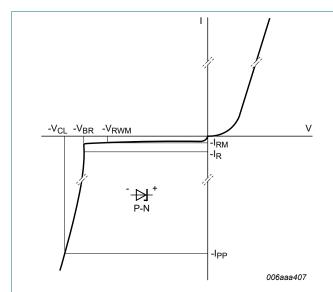


Fig. 4. V-I characteristics for a unidirectional ESD protection diode

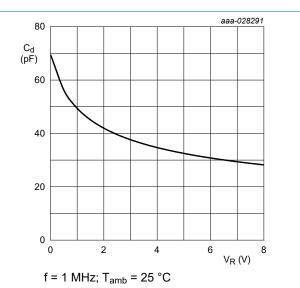


Fig. 5. Diode capacitance as a function of reverse voltage; typical values

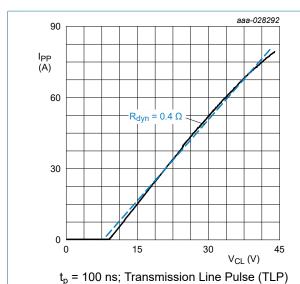


Fig. 6. Positive clamping voltage (TLP); typical values

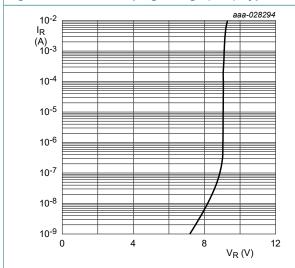
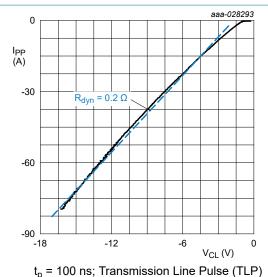


Fig. 8. Reverse current as a function of reverse voltage; typical values



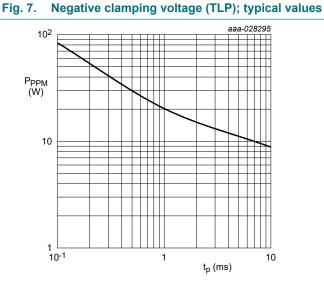
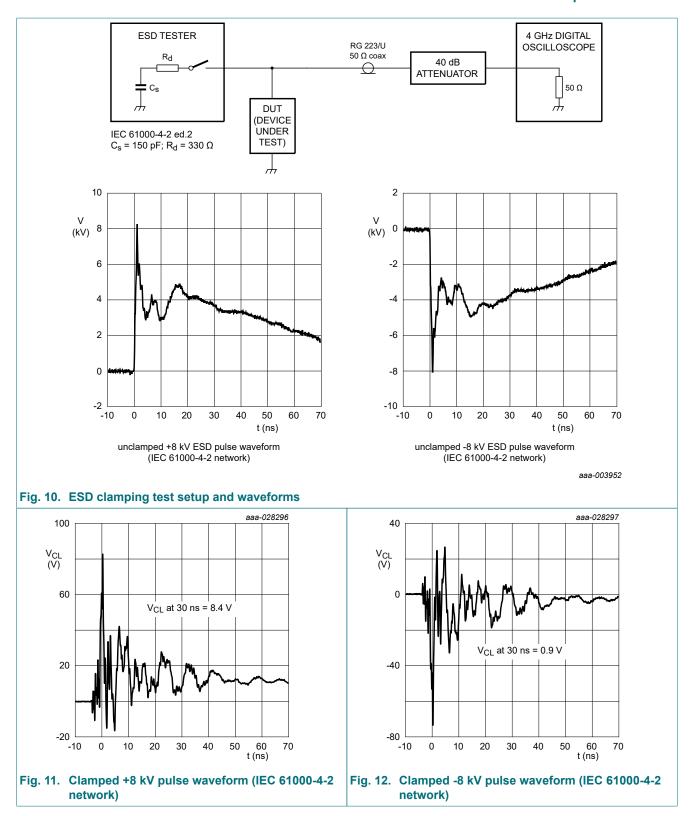
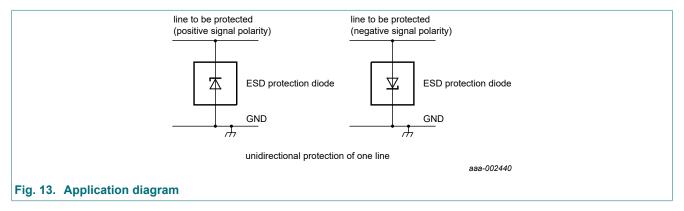


Fig. 9. Peak pulse power as a function of exponential pulse duration; typical values



10. Application information

The device is designed for protection of one unidirectional data or signal line from surge pulses and ESD damage. The device is suitable on lines where the signal polarities are either positive or negative with respect to ground.



Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

- 1. Place the device as close to the input terminal or connector as possible.
- 2. Minimize the path length between the device and the protected line.
- 3. Keep parallel signal paths to a minimum.
- 4. Avoid running protected conductors in parallel with unprotected conductors.
- 5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
- **6.** Minimize the length of the transient return path to ground.
- 7. Avoid using shared transient return paths to a common ground point.
- 8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

11. Test information

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

12. Package outline

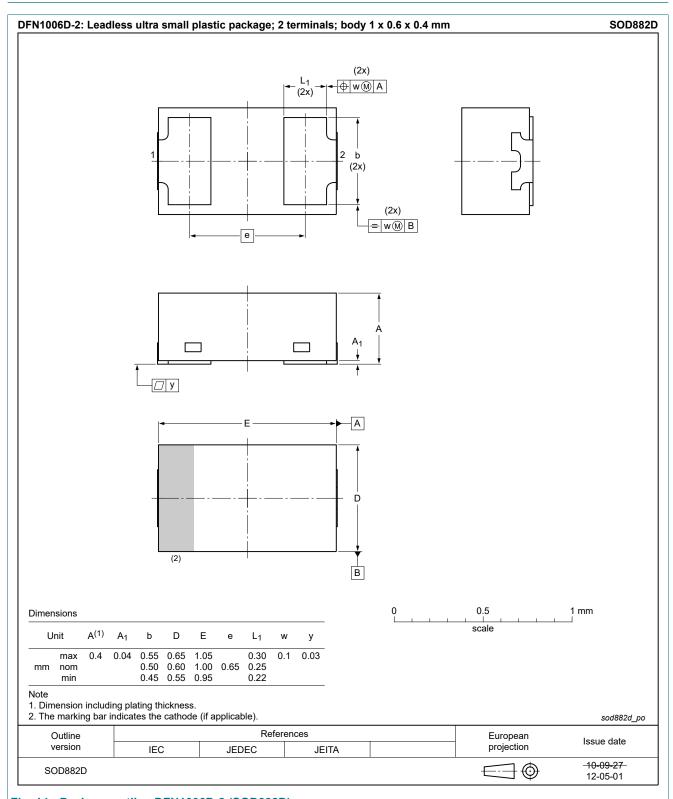
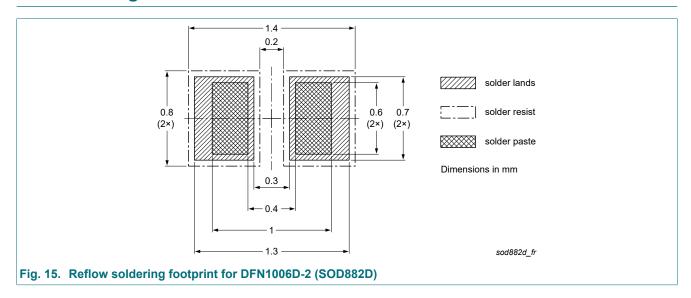


Fig. 14. Package outline DFN1006D-2 (SOD882D)

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13. Soldering



14. Revision history

Table 7. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes			
PESD8V0S1ULD v.2	20210423	Product data sheet	-	PESD8V0S1ULD v.1			
Modifications:	Chapter "Marking": typo correction at marking code						
PESD8V0S1ULD v.1	20180411	Product data sheet	-	-			

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- Please consult the most recently issued document before initiating or completing a design.
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