



PSMN015-100YSF

NextPower 100 V, 15.3 mOhm N-channel MOSFET in LFPAK56 package

16 March 2022

Preliminary data sheet

1. General description

NextPower 100 V, standard level gate drive MOSFET. Qualified to 175 °C and recommended for industrial and consumer applications.

2. Features and benefits

- Low Q_{rr} for higher efficiency and lower spiking
- Low $Q_G \times R_{DSon}$ FOM for high efficiency switching applications
- Strong avalanche energy rating (E_{AS})
- Avalanche rated and 100% tested
- Ha-free and RoHS compliant LFPAK56 package
- Wave-solderable LFPAK56 package

3. Applications

- Synchronous rectifier in AC-DC and DC-DC
- Primary side switch in 48 V DC-DC
- BLDC motor control
- USB-PD and mobile fast-charge adapters
- Flyback and resonant topologies

4. Quick reference data

Table 1. Quick reference data

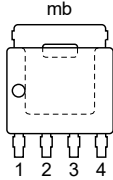
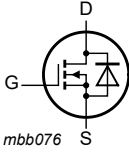
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	100	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	-	-	55	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1	-	-	105	W
T_j	junction temperature		-55	-	175	°C
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 15\text{ A}$; $T_j = 25\text{ °C}$; Fig. 12	-	11.6	15.3	mΩ
		$V_{GS} = 10\text{ V}$; $I_D = 15\text{ A}$; $T_j = 100\text{ °C}$; Fig. 13	-	18	24.4	mΩ
Dynamic characteristics						
Q_{GD}	gate-drain charge	$I_D = 15\text{ A}$; $V_{DS} = 50\text{ V}$; $V_{GS} = 10\text{ V}$; $T_j = 25\text{ °C}$; Fig. 14 ; Fig. 15	1.4	4.7	10.7	nC
$Q_{G(tot)}$	total gate charge		11	22	33	nC
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 23.2\text{ A}$; $V_{sup} \leq 100\text{ V}$; $R_{GS} = 50\text{ Ω}$; $V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ °C}$; unclamped; $t_p = 43\text{ μs}$; Fig. 4	[1]	-	65.2	mJ

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
Q_r	recovered charge	$I_S = 20\text{ A}$; $di_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$; $V_{DS} = 50\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 18	-	21	-	nC

[1] Protected by 100% test

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p>LFLPAK56; Power-SO8 (SOT669)</p>	 <p>mbb076</p>
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN015-100YSF	LFLPAK56; Power-SO8	plastic, single-ended surface-mounted package; 4 terminals	SOT669

7. Limiting values

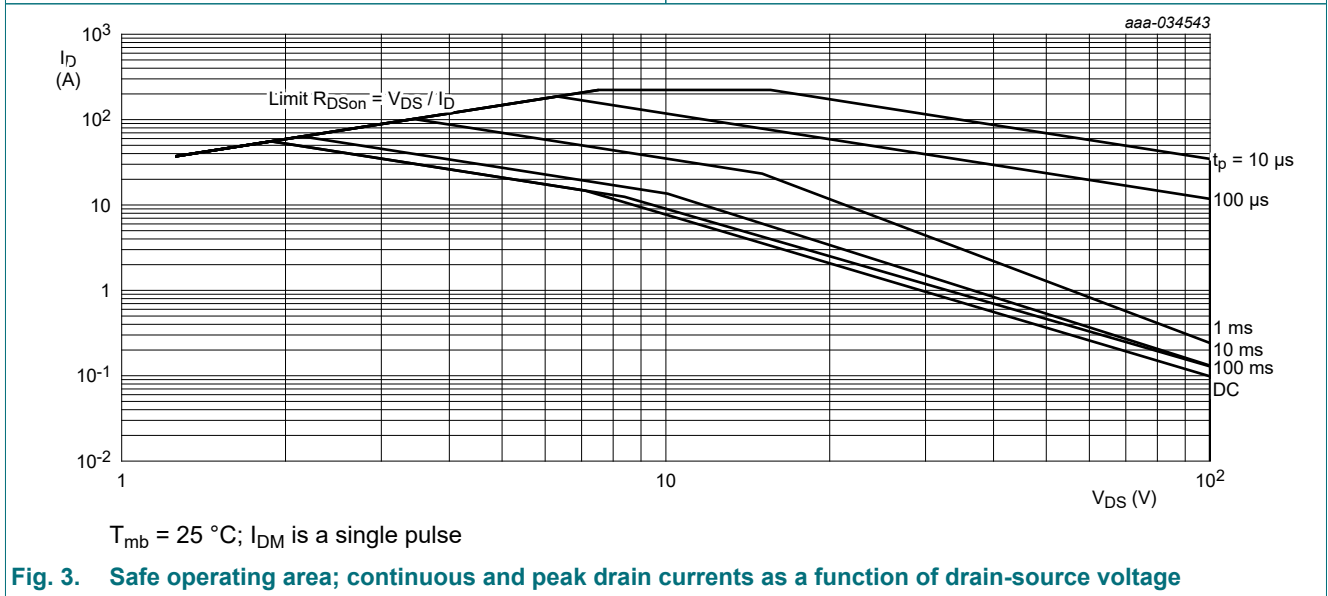
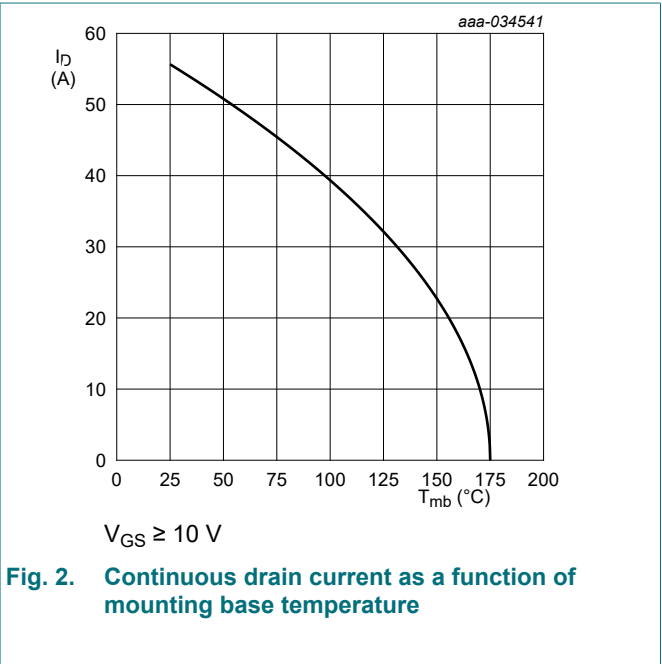
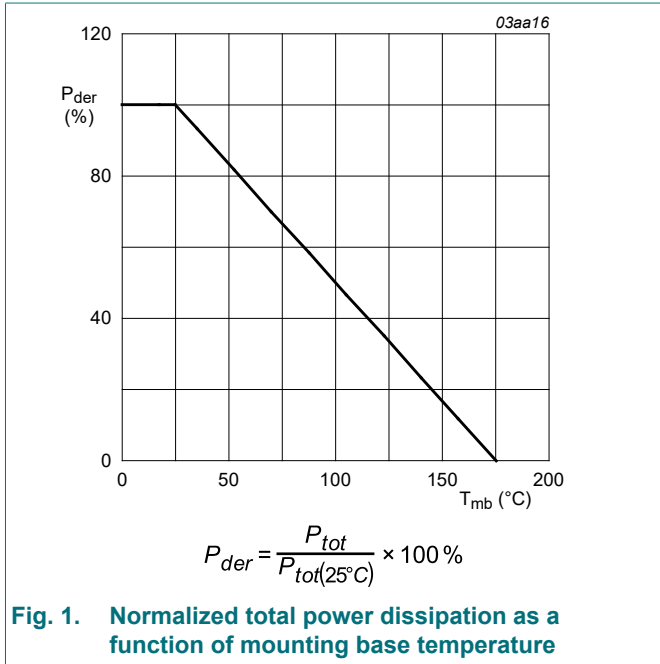
Table 4. Limiting values

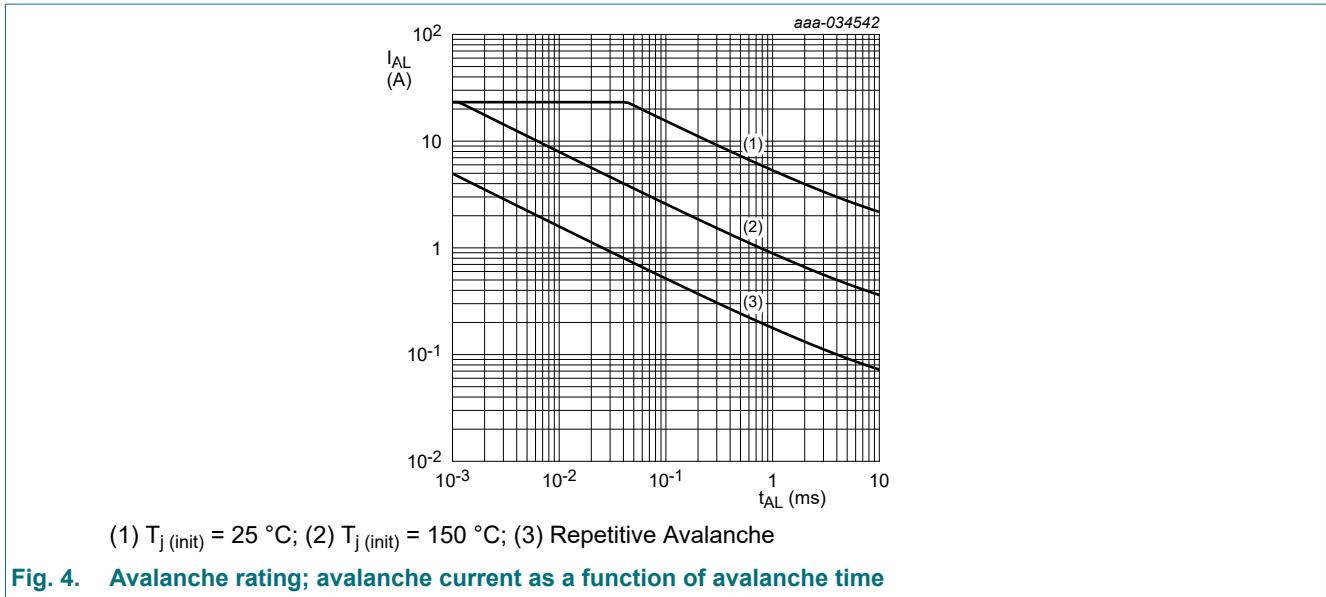
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ }^\circ\text{C} \leq T_j \leq 175\text{ }^\circ\text{C}$	-	100	V
V_{DGR}	drain-gate voltage	$25\text{ }^\circ\text{C} \leq T_j \leq 175\text{ }^\circ\text{C}$; $R_{GS} = 20\text{ k}\Omega$	-	100	V
V_{GS}	gate-source voltage		-20	20	V
P_{tot}	total power dissipation	$T_{mb} = 25\text{ }^\circ\text{C}$; Fig. 1	-	105	W
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ }^\circ\text{C}$; Fig. 2	-	55	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ }^\circ\text{C}$; Fig. 2	-	39	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ }^\circ\text{C}$; Fig. 3	-	218	A
T_{stg}	storage temperature		-55	175	$^\circ\text{C}$
T_j	junction temperature		-55	175	$^\circ\text{C}$
$T_{sld(M)}$	peak soldering temperature		-	260	$^\circ\text{C}$
Source-drain diode					
I_S	source current	$T_{mb} = 25\text{ }^\circ\text{C}$	-	55	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ }^\circ\text{C}$	-	218	A

Symbol	Parameter	Conditions	Min	Max	Unit	
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 23.2 \text{ A}$; $V_{sup} \leq 100 \text{ V}$; $R_{GS} = 50 \Omega$; $V_{GS} = 10 \text{ V}$; $T_{j(\text{init})} = 25 \text{ }^\circ\text{C}$; unclamped; $t_p = 43 \mu\text{s}$; Fig. 4	[1]	-	65.2	mJ
I_{AS}	non-repetitive avalanche current	$V_{sup} = 100 \text{ V}$; $V_{GS} = 10 \text{ V}$; $T_{j(\text{init})} = 25 \text{ }^\circ\text{C}$; $R_{GS} = 50 \Omega$; Fig. 4	[1]	-	23.2	A

[1] Protected by 100% test

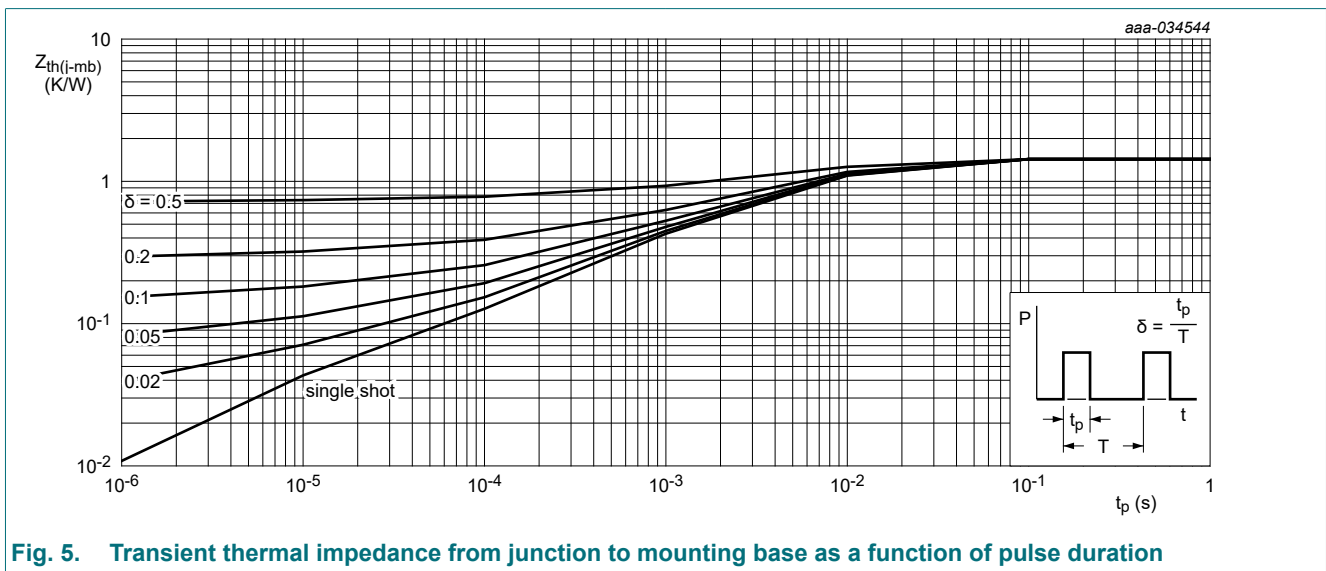


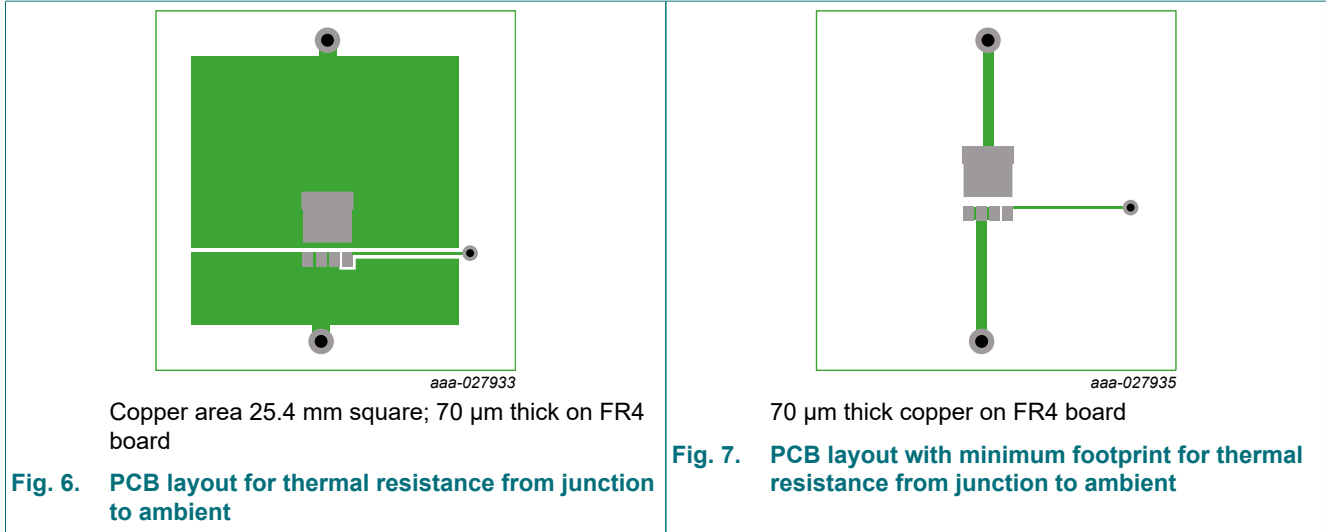


8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	1.3	1.43	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Fig. 6	-	42	-	K/W
		Fig. 7	-	85	-	K/W



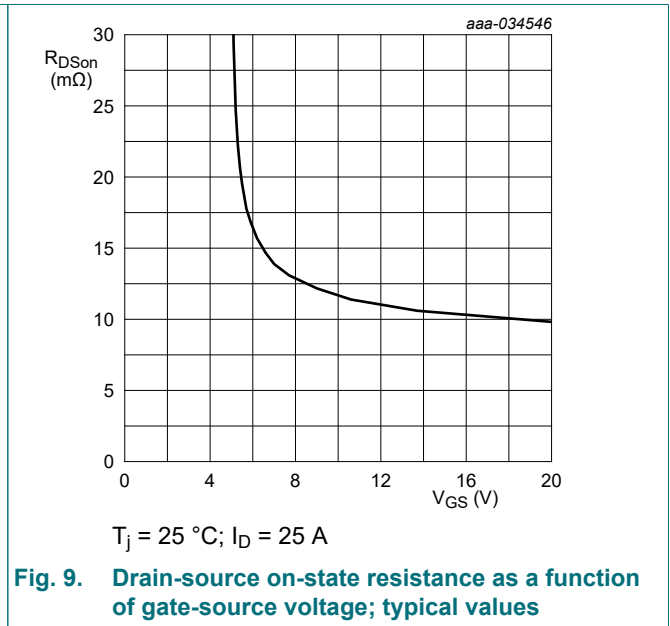
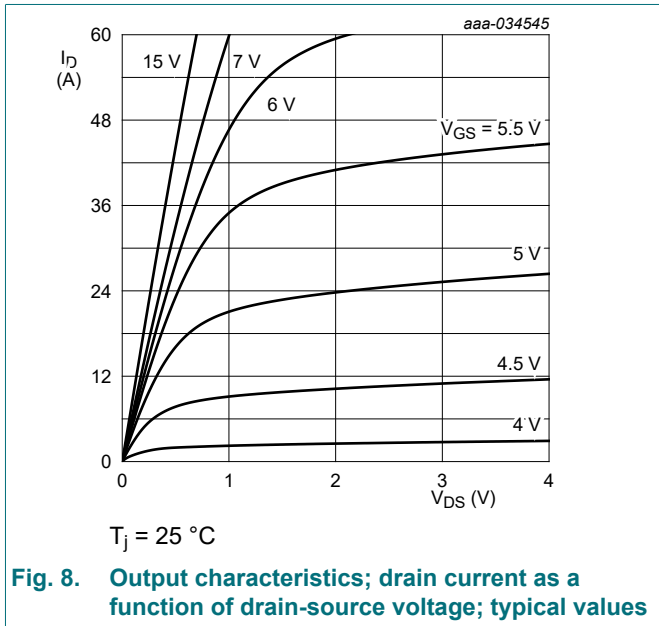


9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	100	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	90	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 25 \text{ }^\circ C; \text{ Fig. 11}$	2	3	4	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 175 \text{ }^\circ C$	-	1.9	-	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = -55 \text{ }^\circ C$	-	3.4	-	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	$25 \text{ }^\circ C \leq T_j \leq 150 \text{ }^\circ C$	-	-7	-	mV/K
I_{DSS}	drain leakage current	$V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	0.01	1	μA
		$V_{DS} = 100 V; V_{GS} = 0 V; T_j = 125 \text{ }^\circ C$	-	3.2	100	μA
I_{GSS}	gate leakage current	$V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	2	100	nA
		$V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 V; I_D = 15 A; T_j = 25 \text{ }^\circ C; \text{ Fig. 12}$	-	11.6	15.3	m Ω
		$V_{GS} = 7 V; I_D = 15 A; T_j = 25 \text{ }^\circ C$	-	14	23	m Ω
		$V_{GS} = 10 V; I_D = 15 A; T_j = 100 \text{ }^\circ C; \text{ Fig. 13}$	-	18	24.4	m Ω
		$V_{GS} = 10 V; I_D = 15 A; T_j = 175 \text{ }^\circ C; \text{ Fig. 13}$	-	25.7	34.7	m Ω
R_G	gate resistance	$f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ C$	0.8	1.5	3	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 15 A; V_{DS} = 50 V; V_{GS} = 10 V; T_j = 25 \text{ }^\circ C; \text{ Fig. 14}; \text{ Fig. 15}$	11	22	33	nC
		$I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V; T_j = 25 \text{ }^\circ C$	-	11	-	nC

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Q_{GS}	gate-source charge	$I_D = 15\text{ A}; V_{DS} = 50\text{ V}; V_{GS} = 10\text{ V};$ $T_j = 25\text{ }^\circ\text{C};$ Fig. 14 ; Fig. 15	4	6.7	9.4	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	4.3	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	2.4	-	nC
Q_{GD}	gate-drain charge		1.4	4.7	10.7	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 15\text{ A}; V_{DS} = 50\text{ V}; T_j = 25\text{ }^\circ\text{C};$ Fig. 14 ; Fig. 15	-	4.6	-	V
C_{iss}	input capacitance	$V_{DS} = 50\text{ V}; V_{GS} = 0\text{ V}; f = 1\text{ MHz};$ $T_j = 25\text{ }^\circ\text{C};$ Fig. 16	871	1451	2031	pF
C_{oss}	output capacitance		250	418	668	pF
C_{rss}	reverse transfer capacitance		2	19	48	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 50\text{ V}; R_L = 3.3\text{ }\Omega; V_{GS} = 10\text{ V};$ $R_{G(ext)} = 5\text{ }\Omega; T_j = 25\text{ }^\circ\text{C}$	-	7	-	ns
t_r	rise time		-	6	-	ns
$t_{d(off)}$	turn-off delay time		-	14	-	ns
t_f	fall time		-	8	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 15\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C};$ Fig. 17	-	0.87	1	V
t_{rr}	reverse recovery time	$I_S = 20\text{ A}; di_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V};$ $V_{DS} = 50\text{ V}; T_j = 25\text{ }^\circ\text{C};$ Fig. 18	-	30	-	ns
Q_r	recovered charge		-	21	-	nC



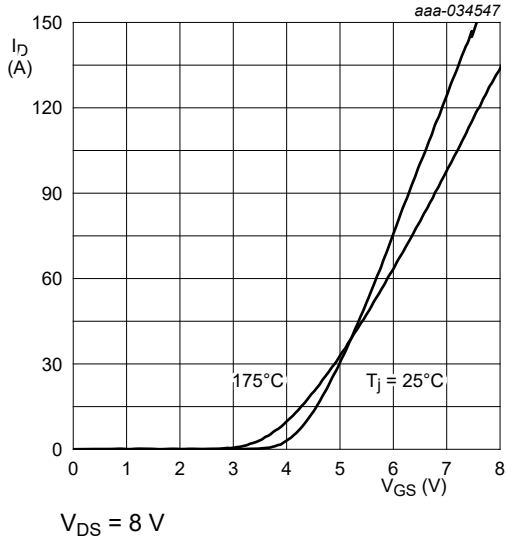


Fig. 10. Transfer characteristics; drain current as a function of gate-source voltage; typical values

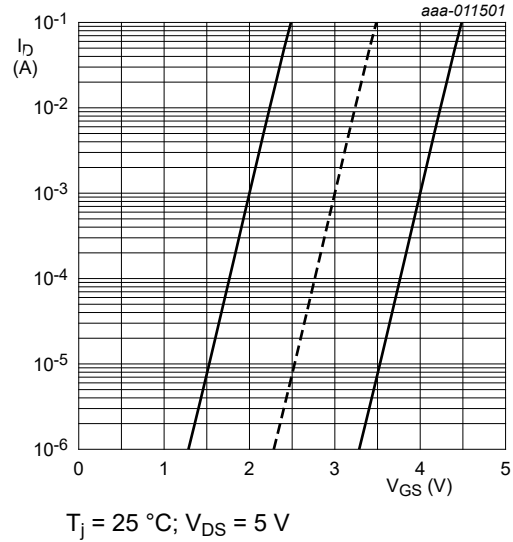


Fig. 11. Sub-threshold drain current as a function of gate-source voltage

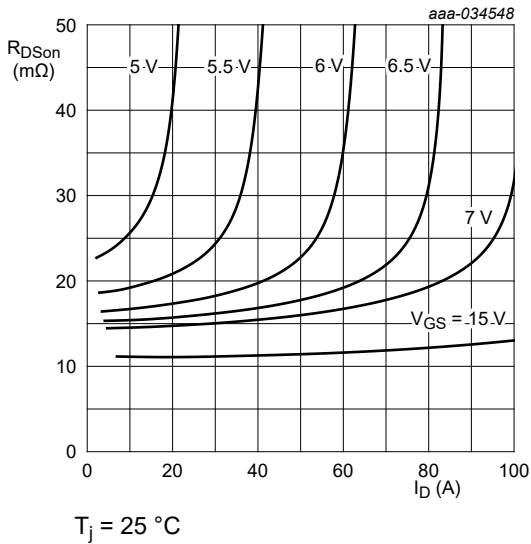


Fig. 12. Drain-source on-state resistance as a function of drain current; typical values

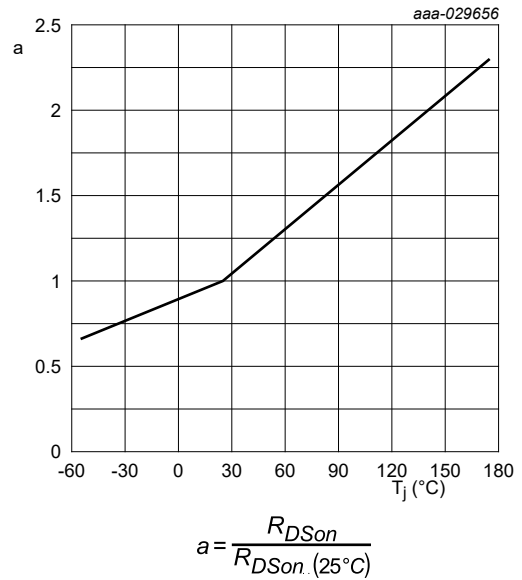


Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature

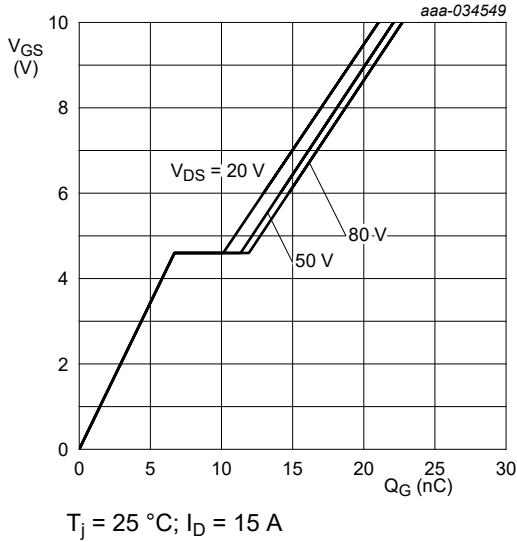


Fig. 14. Gate-source voltage as a function of gate charge; typical values

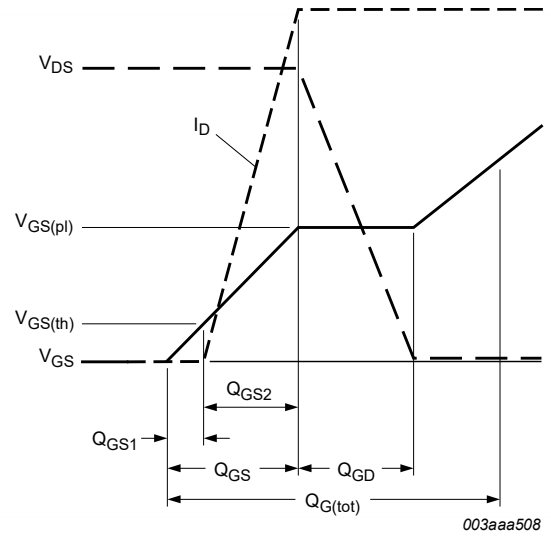


Fig. 15. Gate charge waveform definitions

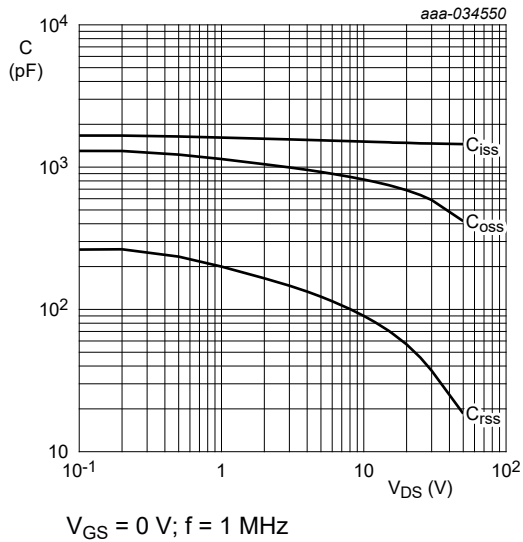


Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

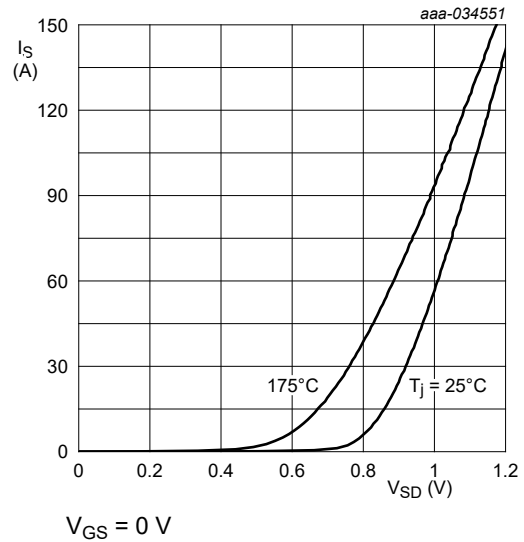


Fig. 17. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

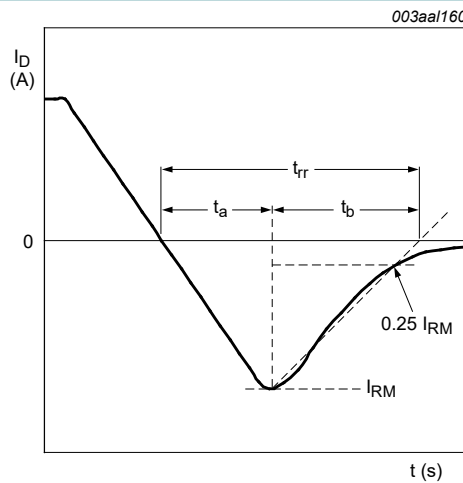


Fig. 18. Reverse recovery timing definition

10. Package outline

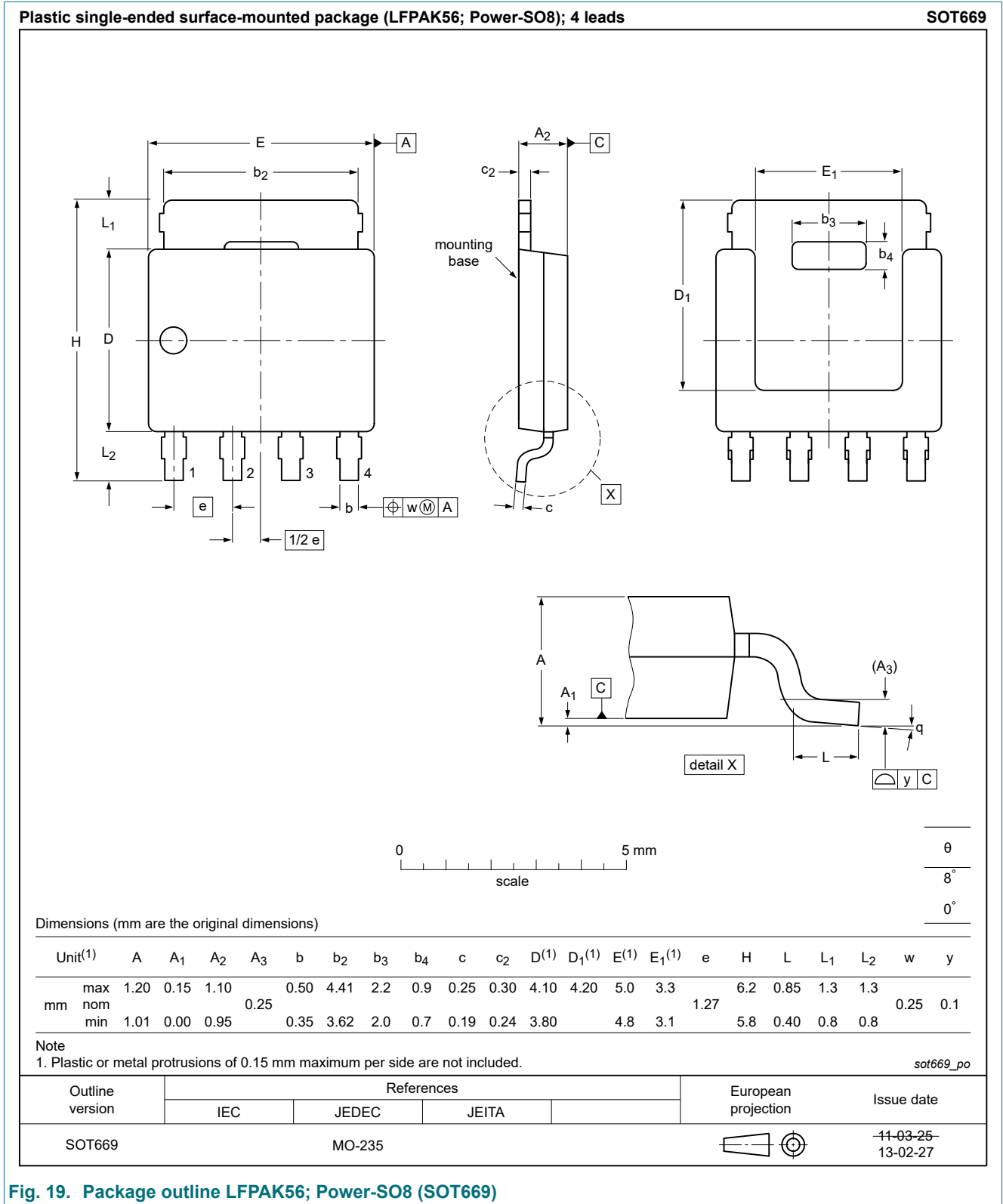


Fig. 19. Package outline LPAK56; Power-SO8 (SOT669)

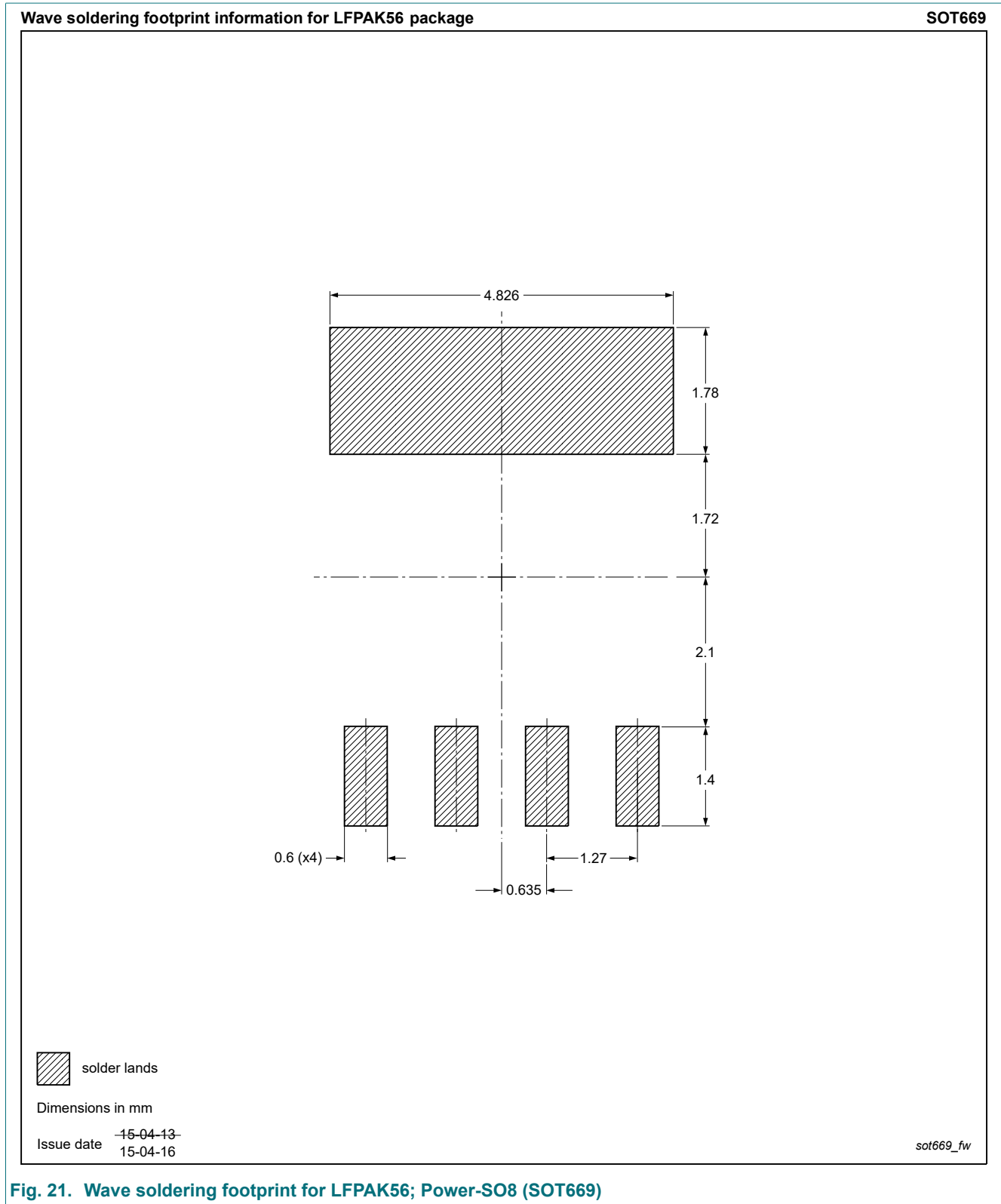


Fig. 21. Wave soldering footprint for LFPAK56; Power-SO8 (SOT669)

12. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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