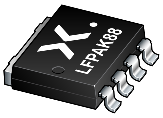


PSMN1R1-50SLH

N-channel 50 V, 1.18 mOhm, 280 A logic level MOSFET in LFPAK88 using NextPower-S3 Schottky-Plus technology

8 January 2021 **Objective data sheet**

1. General description

280 Amp, logic level gate drive N-channel enhancement mode MOSFET in 175 °C LFPAK88 package using advanced TrenchMOS Superjunction technology. This product has been designed and qualified for high performance industrial applications.

2. Features and benefits

- 280 Amp continuous current capability
- LFPAK88 (8 x 8 mm) LFPAK-style low-stress exposed lead-frame for ultimate reliability, optimum soldering and easy solder-joint inspection
- Copper-clip and solder die attach for low package inductance and resistance, and high $I_{D(max)}$ rating
- Ideal replacement for D2PAK and 10 x 12 mm leadless package types
- Qualified to 175 °C
- Avalanche rated, 100 % tested
- Low Q_G, Q_{GD} and Q_{OSS} for high efficiency, especially at higher switching frequencies
- Superfast switching with soft body-diode recovery for low-spiking and ringing, recommended for low EMI designs
- Unique “SchottkyPlus” technology for Schottky-like switching performance and low I_{DSS} leakage
- Narrow $V_{GS(th)}$ rating for easy paralleling and improved current sharing
- Very strong linear-mode / safe operating area characteristics for safe and reliable switching at high-current conditions

3. Applications

- Brushless DC motor control
- Synchronous rectifier in high-power AC-to-DC applications, e.g. server power supplies
- Battery protection and Battery Management Systems (BMS)
- Load switch
- 10 cell lithium-ion battery applications (36 V – 42 V)

4. Quick reference data

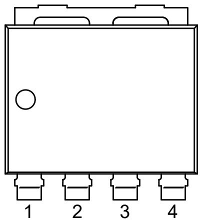
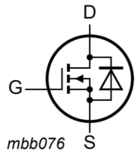
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	-	50	V
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C		-	-	280	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	-	375	W
T_j	junction temperature			-55	-	175	°C
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C		-	0.97	1.18	mΩ
		V_{GS} = 4.5 V; I_D = 25 A; T_j = 25 °C		-	[tbd]	[tbd]	mΩ

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Dynamic characteristics							
Q_{GD}	gate-drain charge	I_D = 25 A; V_{DS} = 25 V; V_{GS} = 4.5 V; Fig. 4		-	20	[tbd]	nC
$Q_{G(tot)}$	total gate charge			-	86	[tbd]	nC

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 LFPAK88 (SOT1235)	
2	S	source		
3	S	source		
4	S	source		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN1R1-50SLH	LFPAK88	plastic, single-ended surface-mounted package (LFPAK88); 4 leads; 2 mm pitch; 8 mm x 8 mm x 1.6 mm body	SOT1235

7. Limiting values

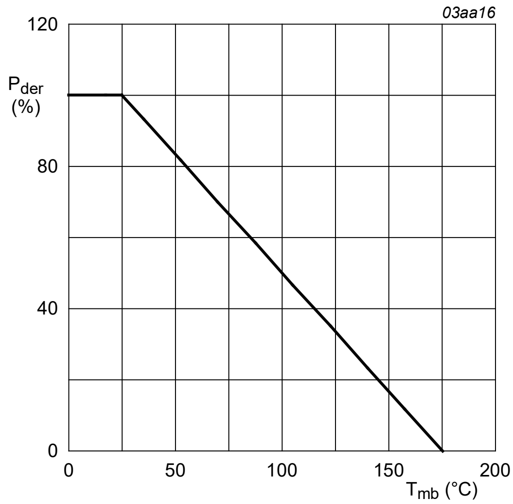
Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	50	V
V_{DGR}	drain-gate voltage	25 °C ≤ T_j ≤ 175 °C; R_{GS} = 20 kΩ		-	50	V
V_{GS}	gate-source voltage			-20	20	V
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	375	W
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C		-	280	A
		V_{GS} = 10 V; T_{mb} = 100 °C		-	269	A
I_{DM}	peak drain current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C		-	1524	A
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C
Source-drain diode						
I_S	source current	T_{mb} = 25 °C		-	280	A
I_{SM}	peak source current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C		-	1524	A

Symbol	Parameter	Conditions		Min	Max	Unit
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 25 A; V_{sup} ≤ 50 V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped; t_p = 6.1 ms	[1]	-	4.9	J
I_{AS}	non-repetitive avalanche current	V_{sup} ≤ 50 V; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; R_{GS} = 50 Ω	[1]	-	[tbd]	A

[1] Protected by 100% test



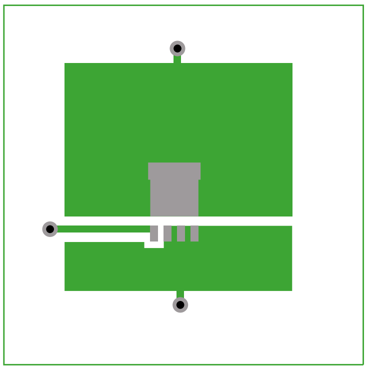
$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

Fig. 1. Normalized total power dissipation as a function of mounting base temperature

8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base			-	0.35	0.4	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Fig. 2		-	35	-	K/W
		Fig. 3		-	70	-	K/W



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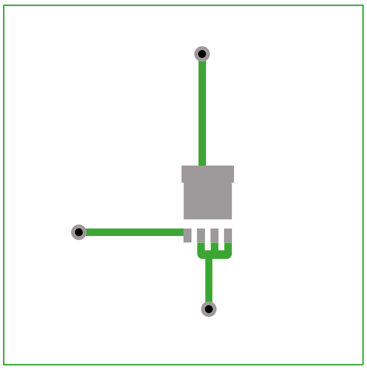
Copper square 25.4 mm x 25.4 mm; 70 µm thick on FR4 board

Fig. 2. PCB layout for resistance from junction to ambient



aaa-029384

70 µm thick copper on FR4 board

Fig. 3. PCB layout with minimum footprint for thermal resistance from junction to ambient

9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C		50	-	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C		45	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS}=V_{GS}; T_j = 25 °C		1.2	1.78	2.2	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	25 °C ≤ T_j ≤ 150 °C		-	[tbd]	-	mV/K
I_{DSS}	drain leakage current	V_{DS} = 40 V; V_{GS} = 0 V; T_j = 25 °C		-	-	1	µA
		V_{DS} = 40 V; V_{GS} = 0 V; T_j = 125 °C		-	[tbd]	-	µA
I_{GSS}	gate leakage current	V_{GS} = 16 V; V_{DS} = 0 V; T_j = 25 °C		-	-	100	nA
		V_{GS} = -16 V; V_{DS} = 0 V; T_j = 25 °C		-	-	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C		-	0.97	1.18	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 150 °C		-	-	[tbd]	mΩ
		V_{GS} = 4.5 V; I_D = 25 A; T_j = 25 °C		-	[tbd]	[tbd]	mΩ
		V_{GS} = 4.5 V; I_D = 25 A; T_j = 150 °C		-	-	[tbd]	mΩ
R_G	gate resistance	f = 1 MHz; T_j = 25 °C		[tbd]	[tbd]	[tbd]	Ω
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	I_D = 25 A; V_{DS} = 25 V; V_{GS} = 4.5 V; Fig. 4		-	86	[tbd]	nC
		I_D = 25 A; V_{DS} = 25 V; V_{GS} = 10 V; Fig. 4		-	190	[tbd]	nC
		I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V		-	101	-	nC
Q_{GS}	gate-source charge	I_D = 25 A; V_{DS} = 25 V; V_{GS} = 4.5 V; Fig. 4		-	28	[tbd]	nC
$Q_{GS(th)}$	pre-threshold gate-source charge			-	19	[tbd]	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge			-	9	[tbd]	nC
Q_{GD}	gate-drain charge			-	20	[tbd]	nC

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{GS(pl)}$	gate-source plateau voltage	I_D = 25 A; V_{DS} = 25 V; Fig. 4		-	[tbd]	-	V
C_{iss}	input capacitance	V_{DS} = 25 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C		-	13338	[tbd]	pF
C_{oss}	output capacitance			-	1276	[tbd]	pF
C_{rss}	reverse transfer capacitance			-	337	[tbd]	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 25 V; R_L = 1 Ω; V_{GS} = 4.5 V; $R_{G(ext)}$ = 5 Ω		-	[tbd]	-	ns
t_r	rise time			-	[tbd]	-	ns
$t_{d(off)}$	turn-off delay time			-	[tbd]	-	ns
t_f	fall time			-	[tbd]	-	ns
Q_{oss}	output charge	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz; T_j = 25 °C		-	68	-	nC
Source-drain diode							
V_{SD}	source-drain voltage	I_S = 25 A; V_{GS} = 0 V; T_j = 25 °C		-	0.75	1	V
t_{rr}	reverse recovery time	I_S = 25 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 25 V; Fig. 5		-	[tbd]	-	ns
Q_r	recovered charge		[1]	-	[tbd]	-	nC
t_a	reverse recovery rise time			-	[tbd]	-	ns
t_b	reverse recovery fall time			-	[tbd]	-	ns

[1] includes capacitive recovery

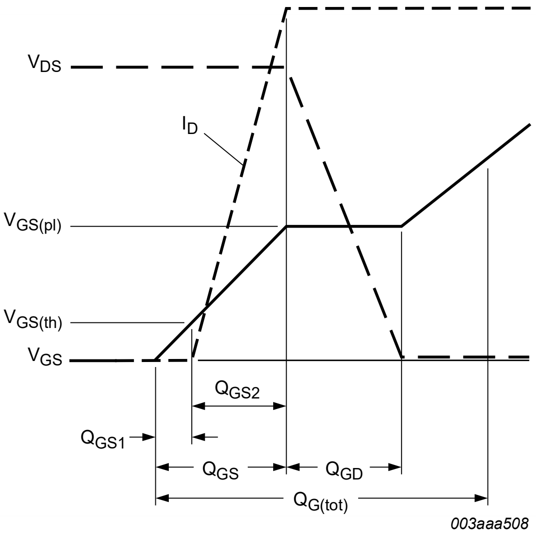


Fig. 4. Gate charge waveform definitions

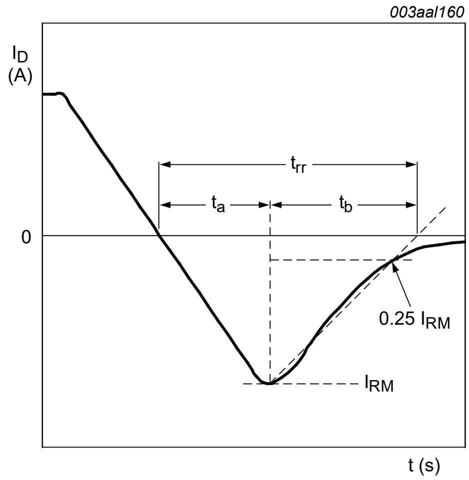
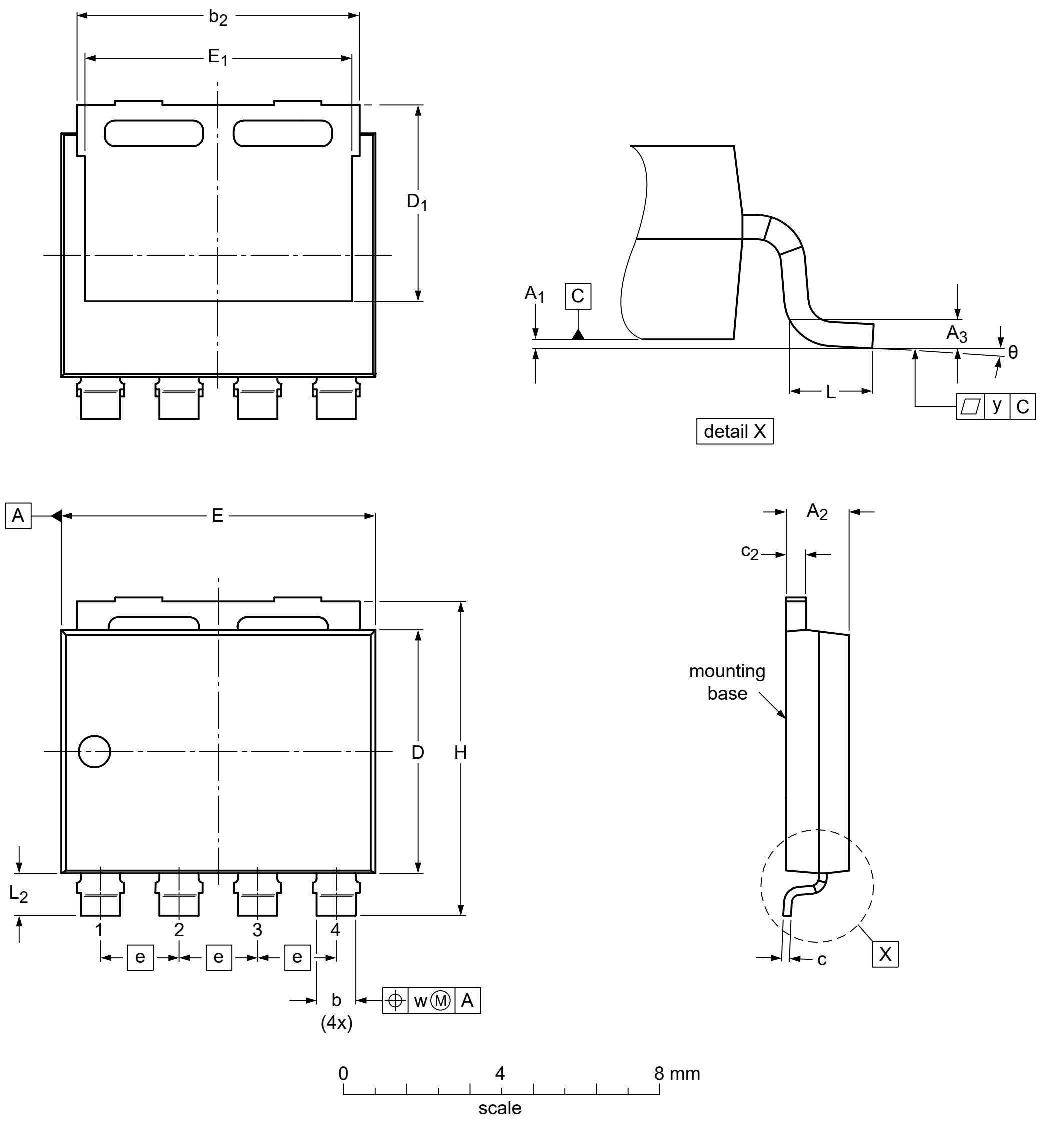


Fig. 5. Reverse recovery timing definition

10. Package outline

Plastic single-ended surface-mounted package (LFPAK88); 4 leads **SOT1235**



Dimensions (mm are the original dimensions)

Unit		A_1	A_2	A_3	b	b_2	c	c_2	$D^{(1)}$	$D_1^{(1)}$	$E^{(1)}$	$E_1^{(1)}$	e	$H^{(1)}$	L	L_2	w	y	θ
mm	max	0.15	1.7		1.1	7.3	0.24	0.55	6.3	5.1	8.1	6.9		8.1	0.8	1.3			8°
	nom			0.25									2.0				0.25	0.10	
	min	0.00	1.5		0.9	7.1	0.18	0.45	6.1	4.9	7.9	6.7		7.8	0.6	0.9			0°

Note
1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

sot1235_po

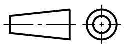
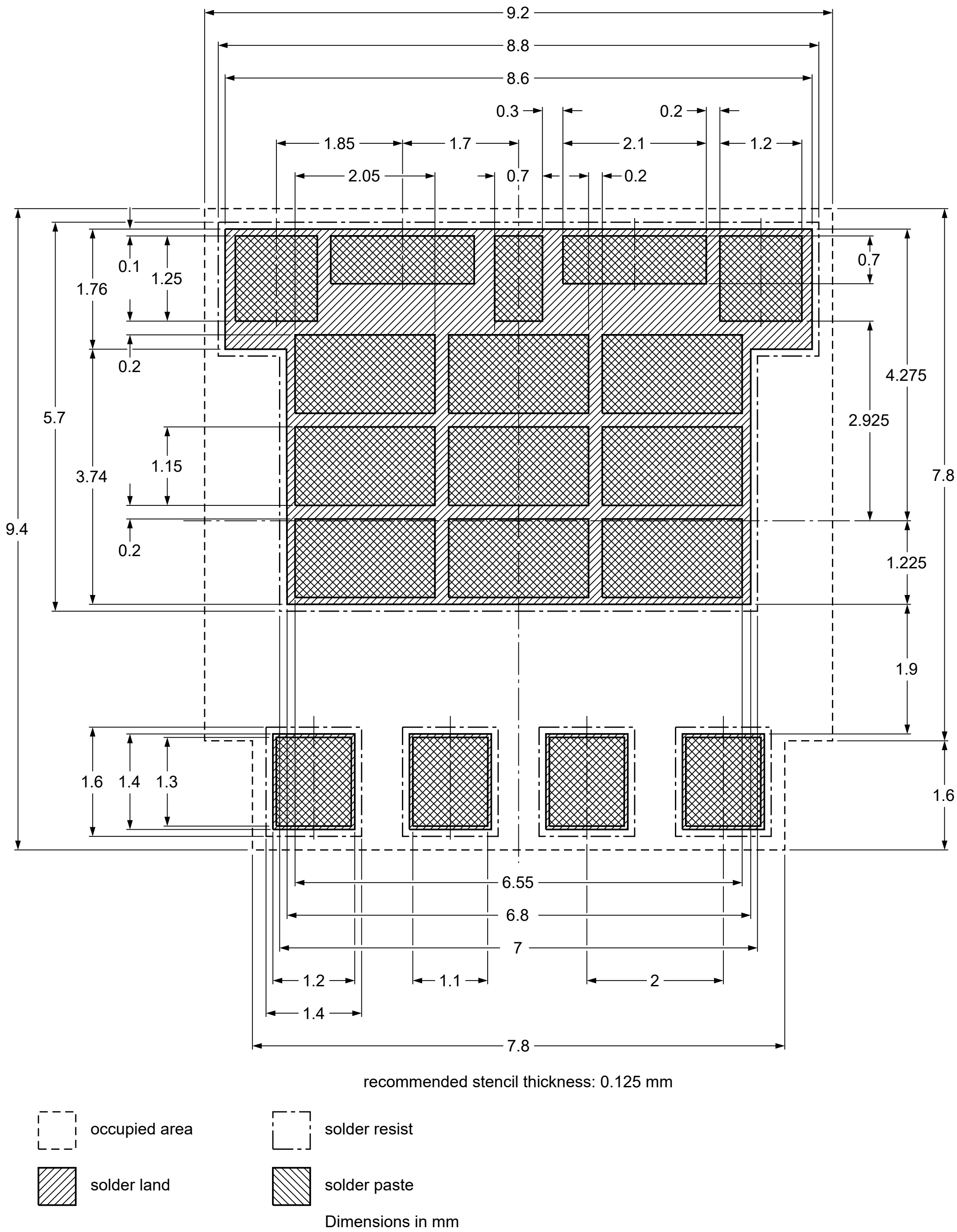
Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1235						~~17-08-02~~ 17-08-07

Fig. 6. Package outline LFPAK88 (SOT1235)

11. Soldering

Footprint information for reflow soldering of LFPAK88 package **SOT1235**



Issue date ~~18-12-12~~ 18-12-13 *sot1235_fr*

Fig. 7. Reflow soldering footprint for LFPAK88 (SOT1235)

12. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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