MOTOROLA
Semiconductor Technical Data

Advance Information

DSP56654/D
Rev. 1, 10/00

DSP56654 Integrated Cellular Baseband Processor Data Sheet

Part 1 Introduction

Motorola designed the DSP56654 to support the rigorous demands of the cellular subscriber market. Optimized for GSM, the high level of on-chip integration in the DSP56654 minimizes application system design complexity and component count, resulting in very compact implementations.

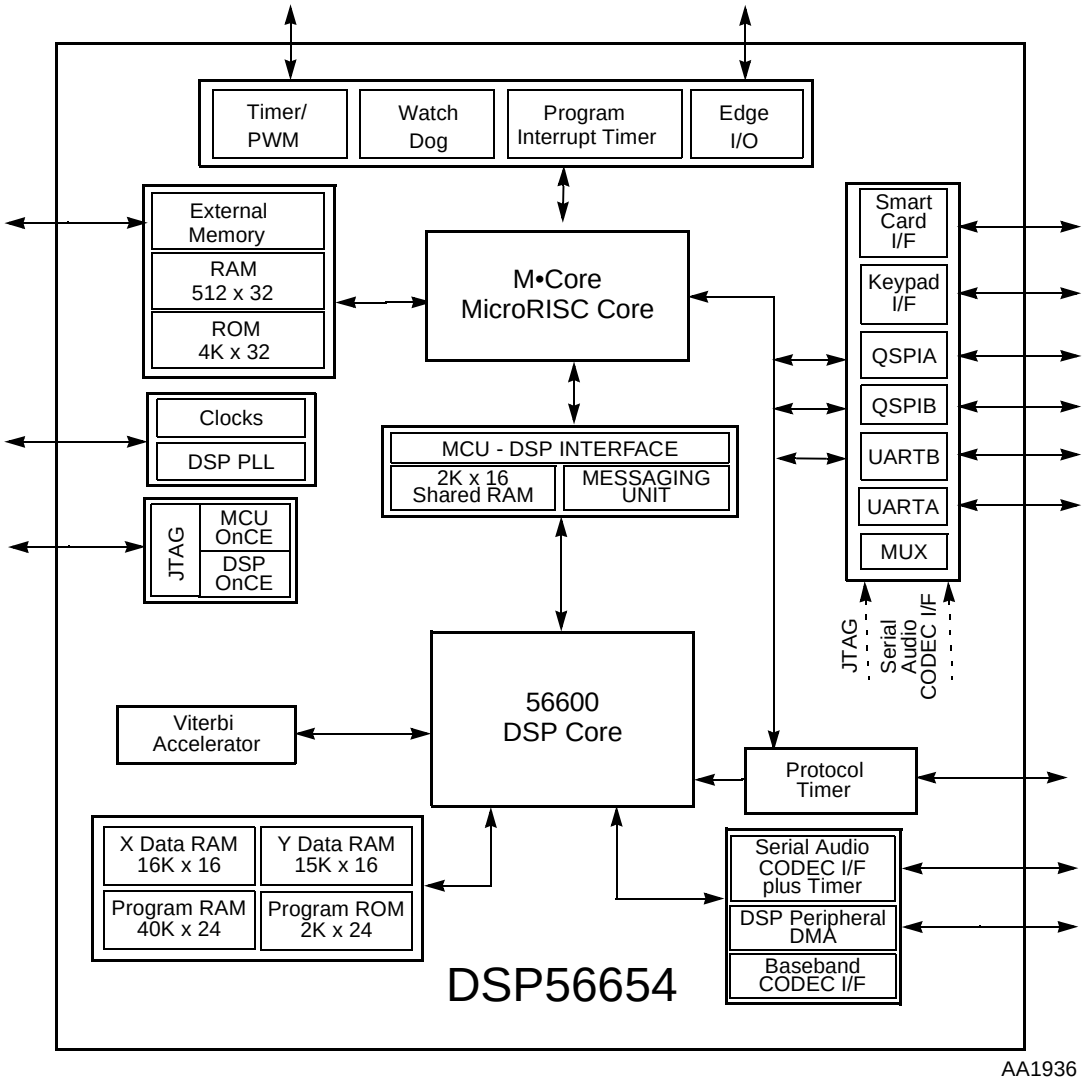


Figure 1-1. DSP56654 System Block Diagram

This integration also yields very low power consumption and cost-effective system performance. The DSP56654 combines the power of Motorola's 32-bit M•CORE ™ MicroRISC Engine (MCU) and the DSP56600 digital signal processor (DSP) core with on-chip memory, protocol timer, and custom peripherals to provide a single-chip cellular base-band processor. Figure 1-1 shows the basic block diagram of the DSP56654.

1.1 Introduction to the DSP56654

Refer to Section 1.2 for information on this data sheet and on the DSP56654.

1.2 Content Organization

This section outlines the information contained in this document.

1.3 Data Conventions

This data sheet uses the following conventions:

- The overbar (e.g., “$\overline{\text{OVERBAR}}$”) is used to indicate a signal that is active when pulled low (e.g., “$\overline{\text{RESET}}$”).
- “Asserted” means that a high true signal (i.e., an active high) is high or that a low true signal (i.e., an active low) is low.
- “Deasserted” means that a high true signal is low or that a low true signal is high.

Please refer to the examples in Table 1-1.

Table 1-1. Data Conventions

Signal/Symbol	Logic State	Signal State	Voltage
$\overline{\text{PIN}}$	True	Asserted	V_{IL}/V_{OL}
$\overline{\text{PIN}}$	False	Deasserted	V_{IH}/V_{OH}
PIN	True	Asserted	V_{IH}/V_{OH}
PIN	False	Deasserted	V_{IL}/V_{OL}

1.4 Features

The DSP56654 offers the following suite of features.

- RISC M•CORE MCU
  - 32-bit load/store RISC architecture
  - Fixed 16-bit instruction length
  - 16-entry 32-bit general-purpose register file
  - 32-bit internal address and data buses
  - Efficient four-stage, fully interlocked execution pipeline
  - Special branch, byte, and bit manipulation instructions
  - Support for byte, half-word, and word memory accesses
  - Fast interrupt support via vectoring/auto-vectoring and a 16-entry dedicated alternate register file
- High-performance DSP56600 core
  - 1 × engine (e.g., 70 MHz = 70 MIPS)
  - Fully pipelined 16 × 16-bit parallel multiplier-accumulator (MAC)
  - Two 40-bit accumulators including extension bits
  - 40-bit parallel barrel shifter
  - Highly parallel instruction set with unique DSP addressing modes
  - Position-independent code support
  - Nested hardware DO loops
  - Fast auto-return interrupts
  - On-chip support for software patching and enhancements
  - Realtime trace capability via external address bus
- On-chip memories
  - 4K × 32-bit MCU ROM
  - 512 × 32-bit MCU RAM
  - 40K × 24-bit DSP Program RAM
  - 2K × 24-bit DSP Program ROM
  - 31K × 16-bit DSP data RAM, split into 16K × 16-bit X data RAM and 15K × 16-bit Y data RAM spaces
  - 2K × 16 DSP/MCU Interface, dual port RAM (part of the 16K ×16 X data RAM
- On-chip peripherals
  - Fully programmable phase-locked loop (PLL) for DSP clock generation
  - External interface module (EIM) for glueless system integration
  - External 22-bit address and 16-bit data MCU buses
  - Thirty-two source MCU interrupt controller
  - Intelligent MCU/DSP interface (MDI) dual 2K × 16-bit dual port RAM (shares 2K DSP X data RAM) with messaging status and control
  - Viterbi accelerator for GSM equalizer and channel decoder

  - Serial audio codec port
  - Serial baseband codec port
  - One DMA channel connected to selectable peripherals
  - Protocol timer frees the MCU from radio channel timing events
  - Two queued serial peripheral interface (QSPI) communicate with external peripherals
  - Keypad port capable of scanning up to an 8 × 8 matrix keypad
  - Software watchdog timer, DSP timer, O/S programmable interrupt timer, and MCU general purpose timers
  - Pulse width modulation (PWM) output
  - Two universal asynchronous receiver/transmitter (UARTs) with FIFO
  - IEEE 1149.1-compliant boundary scan Joint Test Action Group (JTAG) test access port (TAP)
  - Integrated DSP/M•CORE On-Chip Emulation (OnCE™) module
  - DSP address bus visibility and DSP data bus visibility modes for system development
  - ISO 7816-compatible SmartCard port
- Operating features
  - Comprehensive static and dynamic power management
  - M•CORE operating frequency: dc to 16.8 MHz at 1.8 V
  - DSP operating frequency: dc to 58.8 MHz at 1.8 V
  - Internal operating voltage range: 1.8–2.5 V with 3.3 V-tolerant input/output (I/O)
  - Operating temperature: –40° to 85°C ambient
  - 256-pin 17 × 17mm plastic ball grid array (PBGA) package

1.5 Target Applications

The DSP56654 is intended for use in cellular subscriber applications, primarily GSM, and other applications needing both DSP and control processing.

1.6 Product Documentation

The four manuals listed in Table 1-2 are required for a complete description of the DSP56654 and are necessary to design with the part properly. Documentation is available from a local Motorola distributor, a Motorola semiconductor sales office, a Motorola Literature Distribution Center, or the World Wide Web.

Table 1-2. DSP56654 Documentation

Document Name	Description of Contents	Order Number
DSP56600 Family Manual	Detailed description of the DSP56600 family core processor architecture and instruction set	DSP56600FM/AD
M•CORE Reference Manual	Detailed description of the M•CORE MCU and instruction set	MCORERM/AD

Table 1-2. DSP56654 Documentation (Continued)

DSP56654 User's Manual	Detailed description of DSP56654 memory, peripherals, and interfaces	DSP56654UM/D
DSP56654 Technical Data	DSP56654 pin and package descriptions; electrical and timing specifications	DSP56654/D

1.7 Ordering Information

Table 1-3 lists the pertinent information needed to place an order. Consult a Motorola Semiconductor sales office or authorized distributor to determine availability and to order parts.

Table 1-3. DSP56654 Ordering Information

Part	Supply Voltage	Package Type	Pin Count	Order Number
DSP56654	3 V	Plastic ball grid array (PBGA)	256	Customer Specific
DSP56654	3 V	Map ball grid array (MBGA)	256	Customer Specific

Part 2 Signal/Connection Descriptions

The pins and signals of the DSP56654 are described in the following sections. Figure 2-1 and Figure 2-2 are top and bottom views of the package, respectively, showing the pin-outs. Subsequent tables list the pins by number and signal name. Figure 2-3 on page 2-12 is a representational pin-out of the chip grouping the signals by their function. Subsequent tables identify the signals of each group.

2.1 DSP56654 Pin Description

The following section provides information about the available packages for this product, including diagrams of the package pinouts and tables describing how the signals of the DSP56654 are allocated for the 256-pin PBGA/MBGA packages. Top and bottom views of the PBGA/MBGA package are shown in Figure 2-1 and Figure 2-2 with their pin-outs, while Table 2-1 on page 2-4 identifies the signal associated with each pin.

2.2 PBGA/MBGA Package Description

Top View

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	XY A6	XY A5	XY A4	XY A0	TOUT 0	TOUT 5	HGND	TOUT 11	QSCKA	SPICS 3B	HGND	SCKB2	SC1B	STDB	SC2A	SC1A
B	LV_{DD}	XYA3	XYA2	XYST	XYSEL	TOUT4	TOUT9	TOUT10	MISOA	SPICS 2B	HV_{DD}	SRDB2	SCOB	SRDB	EV_{DD}	SCOA
	LGND	XYA7	XYA8	XYRW	TOUT1	TOUT3	TOUT8	HV_{DD}	MOSIA	SPICS 1B	MISOB	$\overline{DSP\_IRQ}$	SCKB	SC2B	SCKA	EGND
	XYA9	XYA10	XYA11	XYA1	TOUT2	TOUT6	TOUT7	TOUT 12	SPICS 0A	SPICS 0B	QSCKB	MOSIB	SRDA	PSTAT2	PSTAT3	STDA
E	XYA13	XYA12	XYA14	XYA15	A15	TOUT 13	TOUT 14	TOUT 15	SPICS 3A	SPICS 2A	SPICS 1A	SPICS 4B	PSTAT 0	KGND	PSTAT 1	KV_{DD}
F	A19	A20	A21	A18	A10	GND SUBSTRATE	SPICS 4A	QV_{CC}	QV_{CCH}	QGND	GND SUBSTRATE	TDO	$\overline{CTSA}$	SIZ1	SIZ0	MUX_CTL
	AV_{DD}	AGND	A16	A17	A9	A7	GND SUBSTRATE	GND SUBSTRATE	GND SUBSTRATE	GND SUBSTRATE	$\overline{DSP\_DE}$	TDI	$\overline{RTSA}$	RXA	TXA	TEST
	A12	A13	A14	A11	A8	A6	GND SUBSTRATE	GND SUBSTRATE	GND SUBSTRATE	GND SUBSTRATE	$\overline{MCU\_DE}$	TMS	TCK	$\overline{TRST}$	GGND	GV_{DD}
J	A1	A0	$\overline{EB1}$	A2	AV_{DD}	A5	GND SUBSTRATE	GND SUBSTRATE	GND SUBSTRATE	GND SUBSTRATE	QV_{CCH}	RXB	ROW7/ RIA/SCKA/ TCK	ROW4	ROW5/ IC2B	ROW6/ DCDA/SC2A/ DSP_DE
K	$\overline{EB0}$	CKIL	QV_{CCH}	CKIH	AGND	A4	GND SUBSTRATE	GND SUBSTRATE	GND SUBSTRATE	GND SUBSTRATE	TXB	$\overline{RTSB}$	ROW1	ROW2	ROW3	GGND
L	QGND	CKOH	FGND	QV_{CC}	A3	GND SUBSTRATE	QGND	MV_{DD}	MGND	XYD8	GND SUBSTRATE	$\overline{CTSB}$	QV_{CC}	INT7/DTRA /SCLKA/ SRDA/TMS	ROW0	QGND
	$\overline{OE}$	$\overline{R/W}$	CKO	FV_{DD}	XYD2	XYD7	QV_{CC}	QV_{CCH}	XYD9	XYD10	XYD11	GV_{DD}	INT6/ $\overline{DSRA}$ /STDA/ TRST	INT5	INT3	INT4
	CV_{DD}	$\overline{CS1}$	$\overline{CS0}$	CGND	D9	D13	D14	XYD6	XYD12	P1GND	SMCLK	SIM DATA	COL0	INT2	INT1	INT0
P	$\overline{CS4}$	$\overline{CS2}$	D4	D7	D8	D10	D15	XYD3	XYD15 /TXA	PGND	BGND	SENSE	$\overline{RESET\_OUT}$	COL7 /PWM	COL6 /OC1	COL5
	CS5	$\overline{CS3}$	D3	D6	DV_{DD}	D11	XYD0	XYD4	XYD14 /RXA	PCAP	BV_{DD}	MOD	$\overline{RESET\_IN}$	COL1	COL2	COL4
T	D0	D1	D2	D5	DGND	D12	XYD1	XYD5	XYD13	PV_{CC}	PWR _EN	$\overline{SIM\ RESET}$	ST0	COL3	GGND	GV_{DD}

Figure 2-1. DSP56654 PBGA Top View

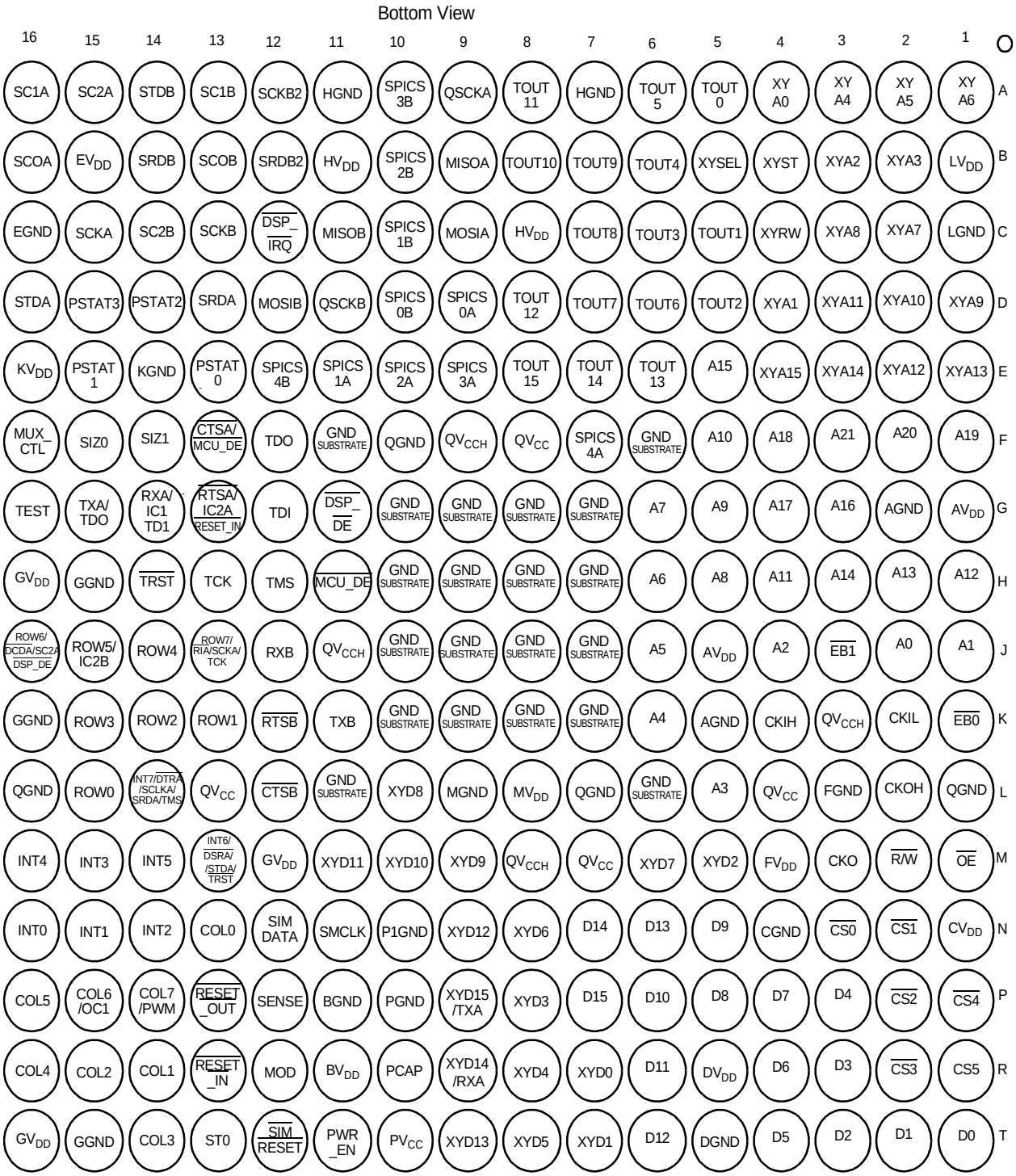


Figure 2-2. DSP56654 PBGA Bottom View

2.3 DSP56654 Signal/Pin Identification

Table 2-1. DSP56654 PBGA/MBGA Signal Identification by Pin Number

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
A1	XYA6	B11	HV_{DD}	D5	TOUT2
A2	XYA5	B12	SRDB2	D6	TOUT6
A3	XYA4	B13	SCOB	D7	TOUT7
A4	XYA0	B14	SRDB	D8	TOUT12
A5	TOUT0	B15	EV_{DD}	D9	SPICS0A
A6	TOUT5	B16	SCOA	D10	SPICS0B
A7	HGND	C1	LGND	D11	QSCKB
A8	TOUT11	C2	XYA7	D12	MOSIB
A9	QSCKA	C3	XYA8	D13	SRDA
A10	SPICS3B	C4	XYRW	D14	PSTAT2
A11	HGND	C5	TOUT1	D15	PSTAT3
A12	SCKB2	C6	TOUT3	D16	STDA
A13	SC1B	C7	TOUT8	E1	XYA13
A14	STDB	C8	HV_{DD}	E2	XYA12
A15	SC2A	C9	MOSIA	E3	XYA14
A16	SC1A	C10	SPICS1B	E4	XYA15
B1	LV_{DD}	C11	MISOB	E5	A15
B2	XYA3	C12	$\overline{\text{DSP\_IRQ}}$	E6	TOUT13
B3	XYA2	C13	SCKB	E7	TOUT14
B4	XYST	C14	SC2B	E8	TOUT15
B5	XYSEL	C15	SCKA	E9	SPICS3A
B6	TOUT4	C16	EGND	E10	SPICS2A
B7	TOUT9	D1	XYA9	E11	SPICS1A
B8	TOUT10	D2	XYA10	E12	SPICS4B
B9	MISOA	D3	XYA11	E13	PSTAT0
B10	SPICS2B	D4	XYA1	E14	KGND

Table 2-1. DSP56654 PBGA/MBGA Signal Identification by Pin Number (Continued)

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
E15	PSTAT1	G8	$GND_{SUBSTRATE}$	J2	A0
E16	KV_{DD}	G9	$GND_{SUBSTRATE}$	J3	$\overline{EB1}$
F1	A19	G10	$GND_{SUBSTRATE}$	J4	A2
F2	A20	G11	$\overline{DSP\_DE}$	J5	AV_{DD}
F3	A21	G12	TDI	J6	A5
F4	A18	G13	$\overline{RTSA/IC2A/RESET\_IN}$	J7	$GND_{SUBSTRATE}$
F5	A10	G14	RXA/IC1/TDI	J8	$GND_{SUBSTRATE}$
F6	$GND_{SUBSTRATE}$	G15	TXA/TDO	J9	$GND_{SUBSTRATE}$
F7	SPICS4A	G16	TEST	J10	$GND_{SUBSTRATE}$
F8	QV_{CC}	H1	A12	J11	QV_{CCH}
F9	QV_{CCH}	H2	A13	J12	RXB
F10	QGND	H3	A14	J13	ROW7/$\overline{RIA}$/SCKA/TCK
F11	$GND_{SUBSTRATE}$	H4	A11	J14	ROW4
F12	TDO	H5	A8	J15	ROW5/IC2B
F13	$\overline{CTSA}$/ $\overline{MCU\_DE}$	H6	A6	J16	ROW6/$\overline{DCDA}$/SC2A/ $\overline{DSP\_DE}$
		H7	$GND_{SUBSTRATE}$		
F14	SIZ1	H8	$GND_{SUBSTRATE}$	K1	$\overline{EB0}$
F15	SIZ0	H9	$GND_{SUBSTRATE}$	K2	CKIL
F16	MUX_CTL	H10	$GND_{SUBSTRATE}$	K3	QV_{CCH}
G1	AV_{DD}	H11	$\overline{MCU\_DE}$	K4	CKIH
G2	AGND	H12	TMS	K5	AGND
G3	A16	H13	TCK	K6	A4
G4	A17	H14	$\overline{TRST}$	K7	$GND_{SUBSTRATE}$
G5	A9	H15	GGND	K8	$GND_{SUBSTRATE}$
G6	A7	H16	GV_{DD}	K9	$GND_{SUBSTRATE}$
G7	$GND_{SUBSTRATE}$	J1	A1	K10	$GND_{SUBSTRATE}$

Table 2-1. DSP56654 PBGA/MBGA Signal Identification by Pin Number (Continued)

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
K11	TXB	M5	XYD2	N16	INT0
K12	$\overline{\text{RTSB}}$	M6	XYD7	P1	$\overline{\text{CS4}}$
K13	ROW1	M7	QV_{CC}	P2	$\overline{\text{CS2}}$
K14	ROW2	M8	QV_{CCH}	P3	D4
K15	ROW3	M9	XYD9	P4	D7
K16	GGND	M10	XYD10	P6	D10
L1	QGND	M11	XYD11	P5	D8
L2	CKOH	M12	GV_{DD}	P7	D15
L3	FGND	M13	INT6/$\overline{\text{DSRA}}$/STDA/$\overline{\text{TRST}}$	P8	XYD3
L4	QV_{CC}	M14	INT5	P9	XYD15/TXA
L5	A3	M15	INT3	P10	PGND
L6	$GND_{SUBSTRATE}$	M16	INT4	P11	BGND
L7	QGND	N1	CV_{DD}	P12	SENSE
L8	MV_{DD}	N2	$\overline{\text{CS1}}$	P13	$\overline{\text{RESET\_OUT}}$
L9	MGND	N3	$\overline{\text{CS0}}$	P14	COL7/PWM
L10	XYD8	N4	CGND	P15	COL6/OC1
L11	$GND_{SUBSTRATE}$	N5	D9	P16	COL5
L12	$\overline{\text{CTSB}}$	N6	D13	R1	CS5
L13	QV_{CC}	N7	D14	R2	$\overline{\text{CS3}}$
L14	INT7/DTRA/SCLKA/SRDA/ TMS	N8	XYD6	R3	D3
		N9	XYD12	R4	D6
L15	ROW0	N10	P1GND	R5	DV_{DD}
L16	QGND	N11	SIMCLK	R6	D11
M1	$\overline{\text{OE}}$	N12	SIMDATA	R7	XYD0
M2	R/$\overline{\text{W}}$	N13	COL0	R8	XYD4
M3	CKO	N14	INT2	R9	XYD14/RXA
M4	FV_{DD}	N15	INT1	R10	PCAP

Table 2-1. DSP56654 PBGA/MBGA Signal Identification by Pin Number (Continued)

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
R11	BV_{DD}	T3	D2	T11	PWR_EN
R12	MOD	T4	D5	T12	$\overline{\text{SIMRESET}}$
R13	$\overline{\text{RESET\_IN}}$	T5	DGND	T13	ST0
R14	COL1	T6	D12	T14	COL3
R15	COL2	T7	XYD1	T15	GGND
R16	COL4	T8	XYD5	T16	GV_{DD}
T1	D0	T9	XYD13		
T2	D1	T10	PV_{CC}		

Table 2-2. DSP56654 PBGA/MBGA Signal Identification by Name

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
A0	J2	A17	G4	COL3	T14
A1	J1	A18	F4	COL4	R16
A2	J4	A19	F1	COL5	P16
A3	L5	A20	F2	COL6	P15
A4	K6	A21	F3	COL7	P14
A5	J6	AGND	G2, K5	$\overline{\text{CS0}}$	N3
A6	H6	AV_{DD}	G1, J5	$\overline{\text{CS1}}$	N2
A7	G6	BGND	P11	$\overline{\text{CS2}}$	P2
A8	H5	BV_{DD}	R11	$\overline{\text{CS3}}$	R2
A9	G5	CGND	N4	$\overline{\text{CS4}}$	P1
A10	F5	CKIH	K4	CS5	R1
A11	H4	CKIL	K2	$\overline{\text{CTSA}}$	F13
A12	H1	CKO	M3	$\overline{\text{CTSB}}$	L12
A13	H2	CKOH‘	L2	CV_{DD}	N1
A14	H3	COL0	N13	D0	T1
A15	E5	COL1	R14	D1	T2
A16	G3	COL2	R15	D2	T3

Table 2-2. DSP56654 PBGA/MBGA Signal Identification by Name (Continued)

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
D3	R3	GV_{DD}	H16,M12, T16	PSTAT1	E15
D4	P3			PSTAT2	D14
D5	T4	HGND	A7,A11	PSTAT3	D15
D6	R4	HV_{DD}	B11, C8	PV_{CC}	T10
D7	P4	INTO	N16	PWR_EN	T11
D8	P5	INT1	N15	QGND	F10, L1, L7, L16
D9	N5	INT2	N14		
D10	P6	INT3	M15	QSCKA	A9
D11	R6	INT4	M16	QSCKB	D11
D12	T6	INT5	M14	QV_{CC}	F8, L4, L13, M7
D13	N6	INT6	M13		
D14	N7	INT7	L14	QV_{CCH}	F9, J11, K3, M8
D15	P7	KGND	E14		
DGND	T5	KV_{DD}	E16	R6	INT0
$\overline{DSP\_DE}$	G11	LGND	C1	R/$\overline{W}$	M2
$\overline{DSP\_IRQ}$	C12	LV_{DD}	B1	$\overline{RESET\_IN}$	G13, R13
DV_{DD}	R5	MCU_DE	H11	$\overline{RESET\_OUT}$	P13
$\overline{EB0}$	K1	MISOA	B9	ROW0	L15
$\overline{EB1}$	J3	MISOB	C11	ROW1	K13
EGND	C16	MOD	R12	ROW2	K14
EV_{DD}	B15	MOSIA	C9	ROW3	K15
FGND	L3	MOSIB	D12	ROW4	J14
FV_{DD}	M4	MUX_CTL	F16	ROW5	J15
GGND	H15,K16, T15	$\overline{OE}$	M1	ROW6	J16
		P1GND	N10	ROW7	J13
$GND_{SUBSTRATE}$	F6,F11, G7-10, H7-10,J7-10,K7-10, L6,L11	PCAP	R10	$\overline{RTSA}$	G13
		PGND	P10	$\overline{RTSB}$	K12
		PSTAT0	E13	RXA	G14

Table 2-2. DSP56654 PBGA/MBGA Signal Identification by Name (Continued)

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
RXB	J12	SRDB2	B12	XYA0	A4
SC1A	A16	ST0	T13	XYA1	D4
SC1B	A13	STDA	D16	XYA2	B3
SC2A	A15	STDB	A14	XYA3	B2
SC2B	C14	TCK	H13	XYA4	A3
SCKA	C15	TD0	F12	XYA5	A2
SCKB	C13	TDI	G12	XYA6	A1
SCKB2	A12	TEST	G16	XYA7	C2
SCOA	B16	TMS	H12	XYA8	C3
SCOB	B13	$\overline{\text{TRST}}$	H14	XYA9	D1
SENSE	P12	TXA	G15	XYA10	D2
SIMCLK	N11	TXB	K11	XYA11	D3
SIMDATA	N12	TOUT0	A5	XYA12	E2
$\overline{\text{SIMRESET}}$	T12	TOUT1	C5	XYA13	E1
SIZ0	F15	TOUT2	D5	XYA14	E3
SIZ1	F14	TOUT3	C6	XYA15	E4
SPICS0A	D9	TOUT4	B6	XYD0	R7
SPICS0B	D10	TOUT5	A6	XYD1	T7
SPICS1A	E11	TOUT6	D6	XYD2	M5
SPICS1B	C10	TOUT7	D7	XYD3	P8
SPICS2A	E10	TOUT8	C7	XYD4	R8
SPICS2B	B10	TOUT9	B7	XYD5	T8
SPICS3A	E9	TOUT10	B8	XYD6	N8
SPICS3B	A10	TOUT11	A8	XYD7	M6
SPICS4A	F7	TOUT12	D8	XYD8	L10
SPICS4B	E12	TOUT13	E6	XYD9	M9
SRDA	D13	TOUT14	E7	XYD10	M10
SRDB	B14	TOUT15	E8	XYD11	M11

Table 2-2. DSP56654 PBGA/MBGA Signal Identification by Name (Continued)

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
XYD12	N9	XYD15	P9	XYST	B4
XYD13	T9	XYRW	C4		
XYD14	R9	XYSEL	B5		

2.4 DSP56654 Signal Description

DSP56654 signals are organized into 23 functional groups as summarized in Table 2-3. Figure 2-3 is a diagram of DSP56654 signals by functional group.

Table 2-3. Signal Functional Group Allocations

Functional Group		Number of Signals	Detailed Description
Power (V_{CCX})		24	Table 2-4
Ground (GND_X)		21	Table 2-5
Substrate ground (GND)		20	Table 2-6
PLL and Clock		5	Table 2-6
Address bus	External Interface Module (EIM)	22	Table 2-7
Data bus		16	Table 2-8
Bus control		4	Table 2-9
Chip selects		6	Table 2-11
Reset, mode, and multiplexer control		5	Table 2-12
External interrupts		9	Table 2-13
Protocol Timers		16	Table 2-14
Keypad Port		16	Table 2-15
Serial data port A (UARTA)		4	Table 2-16
Serial data port B (UARTB)		4	Table 2-17
Serial control port A (QSPIA)		8	Table 2-18
Serial control port B (QSPIB)		8	Table 2-19
SmartCard port (SIM)		5	Table 2-20
Serial audio codec port (SAP)		6	Table 2-21
Baseband codec port		8	Table 2-22

Table 2-3. Signal Functional Group Allocations (Continued)

Functional Group		Number of Signals	Detailed Description
Emulation port	Develop-ment and Test	6	Table 2-23
Debug control port		2	Table 2-24
JTAG test access port (TAP)		6	Table 2-25
DSP X-Y Visibility Port		35	Table 2-10

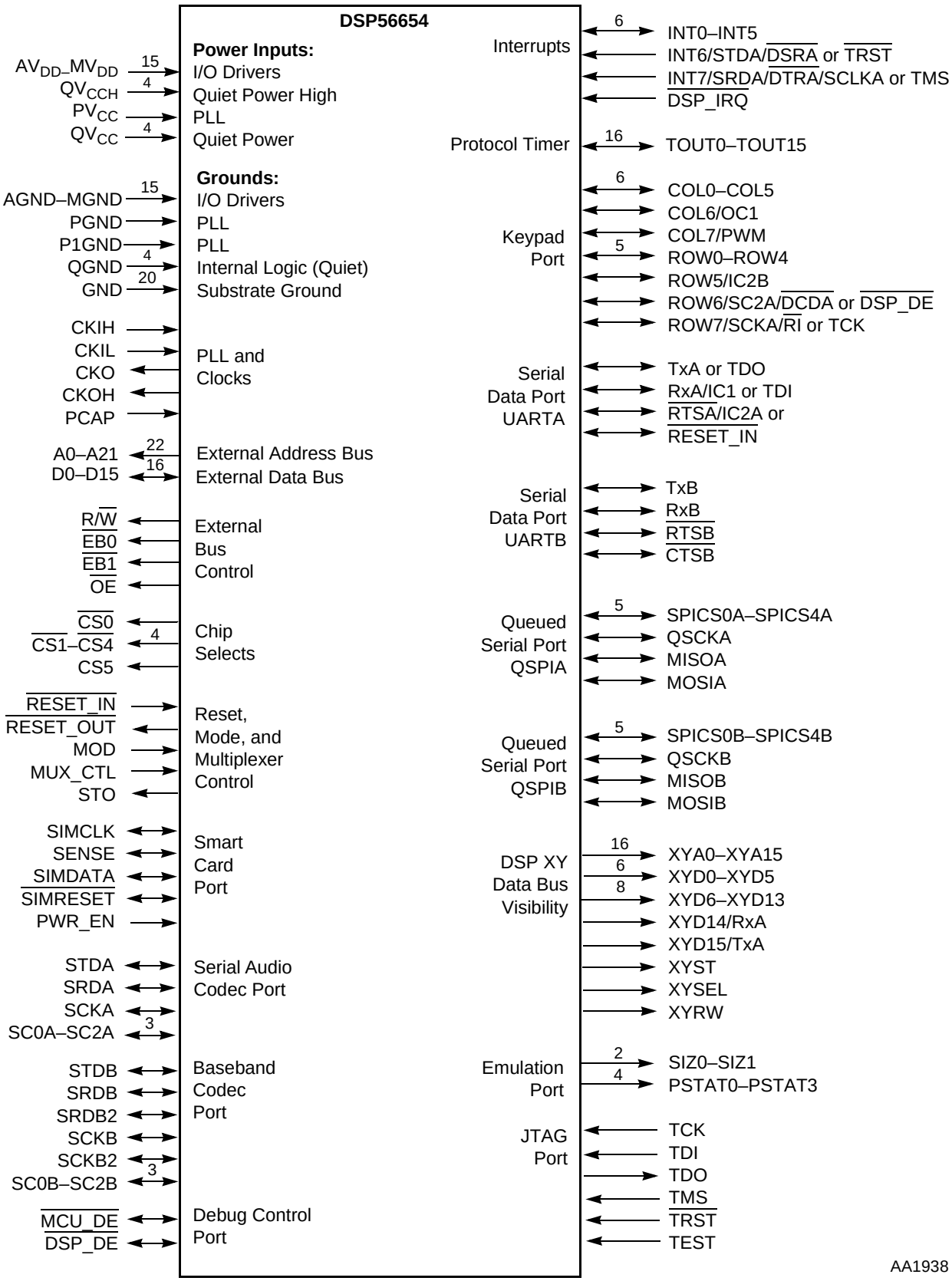


Figure 2-3. Signals Identified by Functional Group

2.5 Power

Table 2-4. Power

Power Names	Description
AV_{DD}	**Address bus power**—These lines supply power to the address bus.
BV_{DD}	**SmartCard interface power**—This line supplies isolated power for SmartCard interface I/O drivers.
CV_{DD}	**Bus control power**—This line supplies power to the bus control logic.
DV_{DD}	**Data bus power**—These lines supply power to the data bus.
EV_{DD}	**Audio codec port power**—This line supplies power to audio codec I/O drivers.
FV_{DD}	**Clock output power**—This line supplies a quiet power source for the CKOUT output. Ensure that the input voltage to this line is well-regulated and uses an extremely low impedance path to tie to the V_{CC} power rail. Use a 0.1 µF bypass capacitor located as close as possible to the chip package to connect between the FV_{DD} line and the FGND line.
GV_{DD}	**GPIO power**—This line supplies power to the GPIO, keypad, data port, interrupts, STO, and JTAG I/O drivers.
HV_{DD}	**Baseband codec and timer power**—This line supplies power to the baseband codec, timer and QSPI I/O drivers.
QV_{CCH}	**Quiet power high**—These lines supply a quiet power source to the pre-driver voltage converters. This value should be greater than or equal to the maximum value of the power supplies of the chip I/O drivers (i.e., the maximum of AV_{DD}, BV_{DD}, CV_{DD}, DV_{DD}, EV_{DD}, FV_{DD}, GV_{DD}, HV_{DD}, and KV_{DD}).
KV_{DD}	**Emulation port power**—This line supplies power to the emulation port I/O drivers.
MV_{DD}	**DSP Visibility Address and Port Control Power —** This line supplies power to the DSP Visibility Address and Port Control system.
PV_{CC}	**Analog PLL circuit power**—This line is dedicated to the analog PLL circuits and must remain noise-free to ensure stable PLL frequency and performance. Ensure that the input voltage to this line is well-regulated and uses an extremely low impedance path to tie to the V_{CC} power rail. Use a 0.1 µF capacitor and a 0.01 µF capacitor located as close as possible to the chip package to connect between the PV_{CC} line and the PGND and P1GND lines.
QV_{CC}	**Quiet power**—These lines supply a quiet power source to the internal logic circuits. Ensure that the input voltage to this line is well-regulated and uses an extremely low impedance path to tie to the V_{CC} power rail. Use a 0.1 µF bypass capacitor located as close as possible to the chip package to connect between the QV_{CC} lines and the QGND lines.

2.6 Ground

Table 2-5. Ground

Ground Names	Description
AGND	**Address bus ground**—These lines connect system ground to the address bus.
BGND	**SmartCard interface ground**—These lines connect system ground to the SmartCard bus.
CGND	**Bus control ground**—This line connects ground to the bus control logic.
DGND	**Data bus ground**—These lines connect system ground to the data bus.
EGND	**Audio codec port ground**—These lines connect system ground to the audio codec port.
FGND	**Clock output ground**—This line supplies a quiet ground connection for the clock output drivers. Ensure that this line connects through an extremely low impedance path to ground. Use a 0.1 µF bypass capacitor located as close as possible to the chip package to connect between the FV_{DD} line and the FGND line.
GGND	**GPIO ground**—These lines connect system ground to GPIO, keypad, data port, interrupts, STO, and JTAG I/O drivers.
HGND	**Baseband codec and timer ground**—These lines connect system ground to the baseband codec, timer and QSPI I/O drivers.
KGND	**Emulation port ground**—These lines connect system ground to the emulation port I/O drivers.
LGND	**DSP Visibility Address and Port Control Ground**—This line grounds the DSP Visibility Adress and Port Control system
MGND	**DSP Visibility Address Data/Data-Port Ground —** This line grounds the DSP Visibility Address and Data Port Control system.
PGND	**Analog PLL circuit ground**—This line supplies a dedicated quiet ground connection for the analog PLL circuits and must remain relatively noise-free to ensure stable PLL frequency and performance. Ensure that this line connects through an extremely low impedance path to ground. Use a 0.1 µF capacitor and a 0.01 µF capacitor located as close as possible to the chip package to connect between the PV_{CC} line and the PGND line.
P1GND	**Analog PLL circuit ground**—This line supplies a dedicated quiet ground connection for the analog PLL circuits and must remain relatively noise-free to ensure stable PLL frequency and performance. Ensure that this line connects through an extremely low impedance path to ground. Use a 0.1 µF capacitor and a 0.01 µF capacitor located as close as possible to the chip package to connect between the $P1V_{CC}$ line and the P1GND line.
QGND	**Quiet ground**—These lines supply a quiet ground connection for the internal logic circuits. Ensure that this line connects through an extremely low impedance path to ground. Use a 0.1 µF bypass capacitor located as close as possible to the chip package to connect between the QV_{CC} line and the QGND line.
$GND_{SUBSTRATE}$	**Substrate ground**—These lines must be tied to ground.

2.7 PLL and Clock

Table 2-6. PLL and Clock Signals

Signal Name	Signal Type	State during Reset	Signal Description
CKIH	Input	Input	**High frequency clock input**—This signal provides the high frequency input clock, a 13 to 16.8 MHz.300mVpp sine wave input. If the frequency needs to be higher, it must be driven at CMOS levels and the CKIHF bit of the CKCTL register must be set.
CKIL	Input	Input	**Low frequency clock input**—This signal provides the low frequency input clock and should be less than or equal to the frequency of CKIH. With a value of 32,768 Hz square wave, this is the default input clock after reset.
CKO	Output	Driven low	**DSP/MCU output clock**—This signal provides an output clock synchronized to the DSP or MCU core internal clock phases, according the selected programming option. The choices of clock source and enabling/disabling the output signal are software selectable.
CKOH	Output	Driven low	**High frequency clock output**—This signal provides an output clock derived from the CKIH input. This signal can be enabled or disabled by software and defaults to disabled logic-low at reset.
PCAP	Input/ Output	Indeter-minate	**PLL capacitor**—This signal is used to connect the required external filter capacitor to the PLL filter. Connect one end of the capacitor to PCAP and the other to V_{CCP}. The value of the capacitor can be found in Table 3-8 on page 3-5.

2.8 Address Bus

Table 2-7. Address Bus Signals

Signal Names	Signal Type	State during Reset	Signal Description
A0–21	Output	Driven low	**Address bus—**These signals specify the address for external memory accesses. If there is no external bus activity, A0–A21 remain at their previous values to reduce power consumption.

2.9 Data Bus

Table 2-8. Data Bus Signals

Signal Names	Signal Type	State during Reset	Signal Description
D0–D15	Input/ Output	Input	**Data bus**—These signals provide the bidirectional data bus for external memory accesses. D0–D15 are held at their last logic state when there is no external bus activity and during hardware reset. This is done with weak “keepers” inside the I/O buffers.

2.10 Bus Control

Table 2-9. Bus Control Signals

Signal Name	Signal Type	State during Reset	Signal Description
R/$\overline{W}$	Output	Driven high	**Read/write—**This signal indicates the bus access type. A high signal indicates a bus read. A low signal indicates a write to the bus. When accessing memory it can also be used as write enable ($\overline{WE}$) signal. When accessing a peripheral chip, the signal acts as a read/write. The signal is set to high during hardware reset.
$\overline{EB0}$	Output	Driven high	**Enable byte 0**—When driven low, this signal indicates access to data byte 0 (D8–D15) during a read or write cycle. This pin may also act as a write byte enable, if so programmed. This output is used when accessing 16-bit wide SRAM.
$\overline{EB1}$	Output	Driven high	**Enable byte 1**—When driven low, this signal indicates access to data byte 1 (D0–D7) during a read or write cycle. This pin may also act as a write byte enable, if so programmed. This output is used when accessing 16-bit wide SRAM.
$\overline{OE}$	Output	Driven high	**Bus select—**When driven low, this signal indicates that the current bus access is a read cycle and enables slave devices to drive the data bus with a read.

2.11 DSP X-Y Visibility Port (35 Pins)

Table 2-10. DSP X-Y Visibility Port Signals

Signal Name	Signal Type	State during Reset	Signal Description
XYA0-15	Output	N/C	DSP X or Y Address Bus Visibility - These signals reflect the value of the internal DSP Address lines XAB0-15 or YAB0-15, according to the XYSEL bit in the DSP operating mode register (OMR).

Table 2-10. DSP X-Y Visibility Port Signals (Continued)

Signal Name	Signal Type	State during Reset	Signal Description
XYD15 TXA GPIO	Output Output Input/ Output	GPI	DSP X or Y Data Bus Visibility - This signal can be programmed as an output signal, reflecting the value of the internal DSP Data lines XDB15 or YDB15, according to the XYSEL bit in the DSP OMR. UARTA Transmit - The UART A transmit pin. GPIO pin. The GPIO function can be controlled from two sets of registers: The emulation port registers, if the bit GPC9 in GPCR is cleared. The UART port control registers, if the bit GPC9 in GPCR is set. The default state at reset is general purpose input pin controlled from the emulation port registers.
XYD14 RXA GPIO	Output Input Input/ Output	GPI	DSP X or Y Data Bus Visibility - This signal can be programmed as an output signal, reflecting the value of the internal DSP Data line XDB14 or YDB14, according to the XYSEL bit in the DSP Operating Mode Register. UART A Receive - the UART A receive pin. GPIO pin. The GPIO function can be controlled from two sets of registers: • The emulation port registers, if the bit GPC9 in GPCR is cleared. • The UART port control registers, if the bit GPC9 in GPCR is set. The default state at reset is general purpose input pin controlled from the emulation port registers.
XYD13-6	Output Input/ Output	GPI	DSP X or Y Data Bus Visibility) - These signals can be programmed as output signals, reflecting the value of the internal DSP Data lines XDB13-6 or YDB13-6, according to the XYSEL bit in the DSP OMR. GPIO pins. The default state at reset is general purpose input pins.
XYD5-0	Output	N/C	DSP X or Y Data Bus Visibility - These signals reflect the value of the internal DSP Data lines XDB5-0 or YDB5-0, according to the XYSEL bit in the DSP OMR. The default state at reset is not connected.
XYST	Output	N/C	(DSP X or Y Strobe Visibility - When high, this signal indicates that a valid data transfer cycle is active over the internal DSP X or Y bus, according to the XYSEL bit in the DSP OMR. The default state at reset is not connected.
XYSEL	Output	N/C	DSP X or Y Select Visibility - When high, this signal indicates that the DSP X bus is selected for “visibility” in the DSP X-Y visibility port. When XYSEL is low, the DSP Y bus is selected for “visibility” in the DSP X-Y visibility port. This pin reflects the XYSEL bit in the DSP OMR. The default state at reset is not connected.
XYRW	Output	N/C	DSP X or Y Read/Write Visibility - This output signal indicates if the current cycle on the internal DSP X or Y bus, according to the XYSEL bit in the DSP OMR, is a read cycle (when XYRW is high) or a write cycle (when XYRW is low). The default state at reset is not connected.

2.12 Chip Selects

Table 2-11. Chip Select Signals

Signal Name	Signal Type	State during Reset	Signal Description
$\overline{\text{CS0}}$	Output	Chip-driven	**Chip select 0—**This signal is asserted low based on the decode of the internal address bus bits A[31:24] and is typically used as the external flash memory chip select. After reset, accesses using this CS have a default of 15 wait states.
$\overline{\text{CS1}}$–$\overline{\text{CS4}}$	Output	Driven high	**Chip select 1–chip select 4—**These signals are asserted low based on the decode of the internal address bus bits A[31:24] of the access address. When not selected as chip select signals, these signals become general purpose outputs (GPOs). After reset, these signals are GPOs that are driven high.
CS5	Output	Driven low	**Chip select 5—**This signal is asserted high based on the decode of the internal address bus bits A[31:24] of the access address. When not selected as a chip select signal, this signal becomes a GPO. After reset, this signal is a GPO that is driven low.

2.13 Reset, Mode, and Multiplexer Control

Table 2-12. Reset, Mode, and Multiplexer Control Signals

Signal Name	Signal Type	State during Reset	Signal Description
RESET_IN	Input	Input	**Reset input**—This signal is an active low Schmitt trigger input that provides a reset signal to the internal circuitry. The input is valid if it is asserted for at least three CKIL clock cycles. This pin has a 47kΩ pull-up resistor. **Note:** If MUX_CTL is held high, the $\overline{\text{RTS}}$ signal of the serial data port (UART) becomes the RESET_IN input line. Its input is valid if it is asserted for at least four CKIL clock cycles. (See Table 2-16 on page 2-24.)

Table 2-12. Reset, Mode, and Multiplexer Control Signals (Continued)

<table>
<tr><th>Signal Name</th><th>Signal Type</th><th>State during Reset</th><th>Signal Description</th></tr>
<tr><td>RESET_OUT</td><td>Output</td><td>Pulled low</td><td>Note: Reset output—This signal is asserted low for at least eight CKIL clock cycles under one of the following conditions:
• RESET_IN is pulled low for at least three CKIL clock cycles
• The alternate RESET_IN signal is enabled by MUX_CTL and is pulled low for at least four CKIL clock cycles
• The watchdog count expires
This signal is asserted immediately after the qualifier detects a valid RESET_IN signal, remains asserted during RESET_IN assertion, and is stretched for at least eight more CKIL clock cycles after RESET_IN is deasserted. Three CKIL clock cycles before RESET_OUT is deasserted. Four CKIL clock cycles before the RESET_OUT pin is negated, the MCU boot mode is latched from the MOD signal.</td></tr>
<tr><td>MOD</td><td>Input</td><td>Input</td><td>Mode select—This signal selects the MCU boot mode during hardware reset. If MOD is driven low at least four CKIL clock cycles before RESET_OUT is deasserted, then the internal MCU ROM ignores the first access and the M•CORE fetches the first word from the first location the external Flash memory. If MOD is driven high four CKIL clock cycles before RESET_OUT deassertion, then the internal MCU ROM is enabled and the M•CORE fetches the first word from the first location in the internal ROM.</td></tr>
<tr><td>MUX_CTL</td><td>Input</td><td>Input</td><td>Multiplexer control—This input allows the designer to select an alternate set of pins to be used for RESET_IN, the debug control port signals, and the JTAG signals as defined below:
<table>
<tr><th colspan="2">Normal (MUX_CTL low)</th><th>Alternate (MUX_CTL high)</th></tr>
<tr><td rowspan="2">Interrupt signals (See Table 2-13)</td><td>INT6/STDA/DSR</td><td>TRST</td></tr>
<tr><td>INT7/SRDA/DTR/SCLK</td><td>TMS</td></tr>
<tr><td rowspan="2">Keypad signals (See Table 2-15)</td><td>ROW6/SC2A/DCD</td><td>DSP_DE</td></tr>
<tr><td>ROW7/SCKA/RI</td><td>TCK</td></tr>
<tr><td rowspan="4">Serial Data Port (UART) signals (See Table 2-16)</td><td>TxD</td><td>TDO</td></tr>
<tr><td>RxD/IC1</td><td>TDI</td></tr>
<tr><td>RTS/IC2A</td><td>RESET_IN</td></tr>
<tr><td>CTS</td><td>MCU_DE</td></tr>
</table>
If MUX_CTL is driven low, the normal functions are selected. If MUX_CTL is driven high, the alternate functions are selected.
Note: The user is responsible to ensure that transition between normal and alternate functions are made smoothly. No provisions are made in the on-chip hardware to assure such a smooth switch. The external command converter used to drive this signal must ensure that critical pins (such as the JTAG TMS and TRST signals and RESET_IN) are driven with inactive values during and after the switch.
The MUX_CTL signal has an internal 100 kΩ pull-down resistor.</td></tr>
<tr><td>STO</td><td>Output</td><td>Chip driven</td><td>Soft turn off—This is a general purpose output pin. Its logic state is not affected by reset.</td></tr>
</table>

For Reset, mode, and MUX control signals equipped with resistors, all pull-ups and pull-downs are automatically disconnected when the pin is an output.

2.14 Interrupts

Table 2-13. Interrupt Signals

Signal Name	Signal Type	State during Reset	Signal Description
INT0–INT3	Input or Output	Input	**Interrupt 0–interrupt 3**—These signals can be programmed as interrupt inputs or GPIO signals. The signals have on-chip 100 kΩ pull-up resistors. As Schmitt trigger interrupt inputs the signals can be programmed to be level sensitive, positive edge-triggered, or negative edge-triggered. When edge-triggered, triggering occurs at a voltage level and is not directly related to the fall time of the interrupt signal; however, as signal fall time of the interrupt signal increases, the probability of generating multiple interrupts due to this noise also increases. The signals are GPIOs when not programmed as interrupts. After reset, the default state for these signals is general purpose input (GPI).
INT4–INT5	Input or Output	Input	**Interrupt 4–interrupt 5**—These signals can be programmed as interrupt inputs or GPIO signals, and have 10-27kΩ pull-up resistors. As Schmitt trigger interrupt inputs, the signals can be programmed to be level sensitive, positive edge-triggered, or negative edge-triggered. When edge-triggered, triggering occurs at a voltage level and is not directly related to the fall time of the interrupt signal; however, as signal fall time of the interrupt signal increases, the probability of generating multiple interrupts due to this noise also increases. The signals are GPIOs when not programmed as interrupts. After reset, the default state for these signals is GPI.
Normal:			**MUX_CTL driven low**
INT6	Input or Output	Input	**Interrupt 6**—When selected, this signal can be programmed as an interrupt input or a GPIO signal, and has a 47kΩ pull-up resistor. As a Schmitt trigger interrupt input, the signal can be programmed to be level sensitive, positive edge-triggered, or negative edge-triggered. When edge-triggered, triggering occurs at a voltage level and is not directly related to the fall time of the interrupt signal; however, as signal fall time of the interrupt signal increases, the probability of generating multiple interrupts due to this noise also increases.
STDA	Output		**Audio codec serial transmit data** (alternate)—When programmed as STDA, this signal transmits data from the serial transmit shift register in the serial audio codec port. **Note:** When this signal is used as STDA, the primary STDA signal is disabled. (See Table 2-21.)
$\overline{\text{DSRA}}$	Output		**Data set ready**—When programmed as GPIO output, this signal can be used as the $\overline{\text{DSR}}$ output for serial data port A. (See Table 2-16) The signal is a GPIO when not programmed as one of the above functions. After reset, the default state for this signal is GPI.

Table 2-13. Interrupt Signals (Continued)

Signal Name	Signal Type	State during Reset	Signal Description
Alternate:			**MUX_CTL driven high**
$\overline{\text{TRST}}$	Input	Input	**Test Reset**—When selected, this signal acts as the $\overline{\text{TRST}}$ input for the JTAG TAP controller. The signal is a Schmitt trigger input that asynchronously initializes the JTAG test controller when asserted. **Note:** When this signal is enabled, the primary $\overline{\text{TRST}}$ signal is disconnected from the TAP controller. (See Table 2-25.)
Normal:			**MUX_CTL driven low**
INT7	Input or Output	Input	**Interrupt 7**—When selected, this signal can be programmed as an interrupt input or a GPIO signal, and has a 47kΩ pull-up resistor. As a Schmitt trigger interrupt input, the signal can be programmed to be level sensitive, positive edge-triggered, or negative edge-triggered. When edge-triggered, triggering occurs at a voltage level and is not directly related to the fall time of the interrupt signal; however, as signal fall time of the interrupt signal increases, the probability of generating multiple interrupts due to this noise also increases.
SRDA	Input		**Audio codec serial receive data** (alternate)—When programmed as SRDA, this signal receives data into the serial receive shift register in the serial audio codec port. **Note:** When this signal is used as SRDA, the primary SRDA signal is disabled. (See Table 2-21.)
$\overline{\text{DTRA}}$	Input		**Data terminal ready**—When programmed as GPIO, this signal is used as the $\overline{\text{DTR}}$ positive and negative edge-triggered interrupt input for serial data port A. (See Table 2-16.)
SCLK	Input		**Serial clock**–When so programmed, this signal provides the input clock for the serial data port (UART). (See Table 2-16.) The signal is a GPIO when not programmed as one of the above functions. After reset, the default state for this signal is GPI.
Alternate:			**MUX_CTL driven high**
TMS	Input	Input	**Test Mode Select**—When selected, this signal acts as the TMS input for the JTAG TAP controller. The signal is used to sequence that TAP controller state machine. The TMS is sampled on the rising edge of TCK. **Note:** When this signal is enabled, the primary TMS signal is disconnected from the TAP controller. (See Table 2-25.)
DSP_IRQ	Input	Input	**DSP external interrupt request**—This active low Schmitt trigger input can be programmed as a level-sensitive or negative edge-triggered maskable interrupt request input during normal instruction processing. If the DSP is in the stop state and DSP_IRQ is asserted, the DSP exits the stop state. This signal has an on-chip 47 kΩ pull-up resistor.

For interrupt signals equipped with resistors, all pull-ups and pull-downs are automatically disconnected when the pin is an output.

2.15 Timers

Table 2-14. Timer Signals

Signal Name	Signal Type	State during Reset	Signal Description
TOUT0–TOUT15	Input or Output	Input	**Timer output 0–15—**These are Layer 1 Timer Output signals. **Note:** These signals are GPIOs when not used as timer outputs. After reset, the default state for these signals are GPIs.

2.16 Keypad Port

Table 2-15. Keypad Port Signals

Signal Name	Signal Type	State during Reset	Signal Description
COL0–COL5	Input or Output	Input	**Column strobe 0–5—**These signals function as keypad column strobes that can be programmed as regular or open-drain outputs. When not used as column strobe signals, these are GPIO signals. After reset, the default state is GPI.
COL6 OC1	Input or Output Output	Input	**Column strobe 6—**This signal functions as a keypad column strobe that can be programmed as a regular or open drain output. **MCU timer output compare** —When programmed as OC1, this is the MCU timer 1 output compare signal. When not programmed as OC1 and not used as a column strobe signal, this is a GPIO signal. After reset, the default state is GPI.
COL7 PWM	Input or Output Output	Input	**Column strobe 7—**This signal functions as a keypad column strobe that can be programmed as a regular or open-drain output. **Pulse width modulator output**—When so programmed, this is the pulse width modulator output. When not programmed as PWM and not used as a column strobe signal, this is a GPIO signal. After reset, the default state is GPI.
ROW0–ROW4	Input or Output	Input	**Row sense 0–4—**These signals function as keypad row senses. When not used as row sense signals, these are GPIO signals. After reset, the default state is GPI. These signals have on-chip 22 kΩ pull-up resistors.
ROW5 IC2B	Input or Output Input	Input	**Row sense 5—**This signal functions as a keypad row sense. **MCU input compare 2 timer**—When so programmed, this signal can be the input capture for the MCU input compare 2 timer. When not programmed as IC2B and not used as a row sense signal, this is a GPIO signal. After reset, the default state is GPI.
Normal:			**MUX_CTL driven low**

Table 2-15. Keypad Port Signals (Continued)

Signal Name	Signal Type	State during Reset	Signal Description
ROW6 SC2A $\overline{\text{DCDA}}$	Input or Output Input or Output Output	Input	**Row sense 6—**This signal functions as a keypad row sense and is equipped with an on-chip 100kΩ pull-up resistor. **Audio codec serial control 2** (alternate)—When programmed as SC2A, this signal provides I/O frame synchronization for the serial audio codec port. In synchronous mode, the signal provides the frame sync for both the transmitter and receiver. In asynchronous mode, the signal provides the frame sync for the transmitter only. As SC2A, this pin has a 100kΩ pull-down resistor. **Note:** When this signal is used as SC2A, the primary SC2A signal is disabled. (See Table 2-21.) **Data carrier detect**—When programmed as GPIO output, this signal can be used as the $\overline{\text{Carrier-Data-Detect}}$ for the Serial Data Port A. (See Table 2-16.) After reset, the default state is GPI.
Alternate:			**MUX_CTL driven high**
$\overline{\text{DSP\_DE}}$	Input Output	Input	**Digital signal processor debug event**—As an input signal, this signal provides a means to enter the debug mode of operation from an external command converter. An an output signal, it acknow-ledges that the DSP has entered the debug mode. When program-med as DSP_DE, this signal has an open-drain 100kΩ pull-up. When the DSP enters the debug mode due to a debug request or as the result of meeting a breakpoint condition, it asserts $\overline{\text{DSP\_DE}}$ as an output signal for three clock cycles. **Note:** When this signal is enabled, the primary $\overline{\text{DSP\_DE}}$ signal is disabled. (See Table 2-24.)
Normal:			**MUX_CTL driven low**
ROW7 SCKA $\overline{\text{RIA}}$	Input or Output Input Output	Input	**Row sense 7—**This signal functions as a keypad row sense. **Audio codec serial clock** (alternate)—When programmed as SCKA, this signal provides the serial bit rate clock for the serial audio codec port. In synchronous mode, the signal provides the clock input or output for both the transmitter and receiver. In asynchronous mode, the signal provides the clock for the transmitter only. **Note:** When this signal is used as SCKA, the primary SCKA signal is disabled. (See Table 2-21.) **Ring indicator**—When programmed as GPIO output, this signal can be used as the $\overline{\text{RI}}$ output for the serial data port. (See Table 2-16.) After reset, the default state is GPI
Alternate:			**MUX_CTL driven high**

Table 2-15. Keypad Port Signals (Continued)

Signal Name	Signal Type	State during Reset	Signal Description
TCK	Input	Input	**Test clock**—When selected, this signal provides the TCK input for the JTAG TAP controller. The signal is used to synchronize the JTAG test logic. This signal is equipped with a 47kΩ pull-up resistor. **Note:** When this signal is enabled, the primary TCK signal is disconnected from the TAP controller. (See Table 2-25.)

For keypad port signals equipped with resistors, all pull-ups and pull-downs are automatically disconnected when the pin is an output.

2.17 Serial Data Port A (UARTA)

Table 2-16. UARTA Signals

Signal Name	Signal Type	State during Reset	Signal Description
Normal:			**MUX_CTL driven low**
TXA	Input or Output	Input	**UART transmit—**This signal transmits data from UARTA. The signal is a GPIO when not programmed as the TXA signal. After reset, the default state for this signal is GPI.
Alternate:			**MUX_CTL driven high**
TDO	Output		**Test data output**—When selected, this signal provides the TDO serial output for test instructions and data from the JTAG TAP controller. TDO is a tri-state signal that is actively driven in the shift-IR and shift-DR controller states. **Note:** When this signal is enabled, the primary TDO signal is disconnected from the TAP controller. (See Table 2-25.)
Normal:			**MUX_CTL driven low**
RXA IC1	Input or Output Input	Input	**UART receive—**This signal receives data into UARTA. **Input compare 1**—When so programmed, the signal connects to an Input capture/output compare Timer used for autobaud mode support. The signal is a GPIO when not programmed as one of the above functions. This signal has an on-chip 47 kΩ pull-up resistor. After reset, the default state for this signal is GPI.
Alternate:			**MUX_CTL driven high**

Table 2-16. UARTA Signals (Continued)

Signal Name	Signal Type	State during Reset	Signal Description
TDI	Input	Input	**Test data in**—When selected, this signal provides the TDI serial input for test instructions and data for the JTAG TAP controller. TDI is sampled on the rising edge of TCK. **Note:** When this signal is enabled, the primary TDI signal is disconnected from the TAP controller. (See Table 2-25.)
Normal:			**MUX_CTL driven low**
$\overline{\text{RTSA}}$ IC2A	Input or Output Input	Input	**Request to send—**This signal functions as the UARTA $\overline{\text{RTS}}$ signal. **Input compare 2 A**—When so programmed, this signal connects to an Input Capture Timer channel. The signal is a GPIO when not programmed as one of the above functions. After reset, the default state for this signal is GPI.
Alternate:			**MUX_CTL driven high**
RESET_IN	Input	Input	**Reset input**—This signal is an active low Schmitt trigger input that provides a reset signal to the internal circuitry. The input is valid if it is asserted for at least three CKIL clock cycles. **Note:** When this signal is enabled, the primary $\overline{\text{RESET\_IN}}$ signal is disabled. (See Table 2-12.)
Normal:			**MUX_CTL driven low**
$\overline{\text{CTSA}}$	Input or Output	Input	**Clear to send—**This signal functions as the UARTA $\overline{\text{CTS}}$ signal, and is equipped with a 47kΩ pull-up. **Note:** The signal is a GPIO when not used as $\overline{\text{CTS}}$. After reset, the default state for this signal is GPI.
Alternate:			**MUX_CTL driven high**
$\overline{\text{MCU\_DE}}$	Input Output	Input	**Microcontroller debug event**—As an input signal, this signal provides a means to enter the debug mode of operation from an external command converter. An an output signal, it acknowledges that the MCU has entered the debug mode. The signal is equipped with an open-drain 100kΩ pull-up resistor. When the MCU enters the debug mode due to a debug request or as the result of meeting a breakpoint condition, it asserts $\overline{\text{MCU\_DE}}$ as an output signal for several clock cycles. **Note:** When this signal is enabled, the primary $\overline{\text{MCU\_DE}}$ signal is disabled. (See Table 2-24.)

Note: There are four additional signals that support UART operation, provided as follows:

- $\overline{\text{DSR}}$—data set ready. This is an alternate function for the INT6 signal. (See Table 2-13 on page 2-20.)
- $\overline{\text{DTR}}$—data terminal ready. This is an alternate function for the INT7 signal. (See Table 2-13 on page 2-20.)

- $\overline{\text{DCD}}$—data carrier detect. This is an alternate function for the ROW6 signal. (See Table 2-15 on page 2-22.)
- $\overline{\text{RI}}$—ring indicator. This is an alternate function for the ROW7 signal. (See Table 2-15 on page 2-22.)

For UARTA signals equipped with resistors, all pull-ups and pull-downs are automatically disconnected when the pin is an output.

2.18 Serial Data Port B (UARTB)

Table 2-17. UARTB Signals

Signal Name	Signal Type	State during Reset	Signal Description
TXB	Input or Output	Input	**UART transmit—**This signal transmits data from UARTB. The signal is a GPIO when not programmed as the TXB signal. After reset, the default state for this signal is GPI.
RXB	Input or Output	Input	**UART receive—**This signal receives data into UARTB, and is equipped with a 47kΩ pull-up. The signal is a GPIO when not programmed as the RXB signal. After reset, the default state for this signal is GPI.
$\overline{\text{RTSB}}$	Input or Output	Input	**Request to send—**This signal functions as the UARTB $\overline{\text{RTS}}$ signal. The signal is a GPIO when not programmed as one of the above functions. After reset, the default state for this signal is GPI.
$\overline{\text{CTSB}}$	Input or Output	Input	**Clear to send—**This signal functions as the UARTA $\overline{\text{CTS}}$ signal, and is equipped with a 47kΩ pull-up. The signal is a GPIO when not used as $\overline{\text{CTSA}}$. After reset, the default state for this signal is GPI.

2.19 Serial Control Port A (QSPIA)

Table 2-18. Serial Control Port A Signals

Signal Name	Signal Type	State during Reset	Signal Description
SPICS0A–SPICS3A	Output Input or Output	Input	Synchronous peripheral chip Select 0–3—The output signals provide chip select signals for Queued Serial Peripheral Interface A (QSPIA). The signals are programmable as active high or active low. Each signal has an on-chip 100 kΩ pull-up resistor. These are GPIO signals when the chip select functions are not being used. After reset, the default state for each signal is GPI.

Table 2-18. Serial Control Port A Signals (Continued)

Signal Name	Signal Type	State during Reset	Signal Description
SPICS4A	Output Input or Output	Input	Synchronous peripheral chip select 4—This output signal provides a chip select signal for QSPIA. This signal is programmable as active high or active low. This signal has an on-chip 100 kΩ pull-down resistor. This is a GPIO signal when the chip select function is not being used. After reset, the default state is GPI.
QSCKA	Output Input or Output	Input	**Serial clock** — This output signal provides the serial clock from QSPIA for the accessed peripherals. There is a programmable number of clock cycles delay between the assertion of the chip select signal and the first transmission of the serial clock. The polarity and phase of QSCKA are programmable. This is a GPIO signal when the SCK function is not being used. After reset, the default state is GPI.
MISOA	Input Input or Output	Input	**Synchronous master in slave out**—This input signal provides serial data input to QSPIA. Input data can be sampled on the rising or falling edge of QSCKA and received in QSPI RAM LSB first. This is a GPIO signal when the function is not being used. After reset, the default state is GPI.
MOSIA	Output Input or Output	Input	**Synchronous master out slave in**—This output signal provides serial data from QSPIA. Output data can be programmed to change state on the rising or falling edge of QSCKA and transmitted LSB first. This is a GPIO signal when the function is not being used. After reset, the default state is GPI.

For serial control port signals equipped with resistors, all pull-ups and pull-downs are automatically disconnected when the pin is an output.

2.20 Serial Control Port B(QSPIB)

Table 2-19. Serial Control Port B Signals

Signal Name	Signal Type	State during Reset	Signal Description
SPICS0B/1B/3B/4B	Output Input or Output	Input	Synchronous peripheral chip Selects—The output signals provide chip select signals for the Queued Serial Peripheral Interface B (QSPIB). The signals are programmable as active high or active low. Each signal has an on-chip 100 kΩ pull-up resistor. These are GPIO signals when the chip select functions are not being used. After reset, the default state for each signal is GPI.

Table 2-19. Serial Control Port B Signals (Continued)

Signal Name	Signal Type	State during Reset	Signal Description
SPICS2B	Output Input or Output	Input	Synchronous peripheral chip select —This output signal provides a chip select signal for QSPIB. This signal is programmable as active high or active low. This signal has an on-chip 100 kΩ pull-down resistor. This is a GPIO signal when the chip select function is not being used. After reset, the default state is GPI.
QSCKB	Output Input or Output	Input	**Serial clock** — This output signal provides the serial clock from QSPIB for the accessed peripherals. There is a programmable number of clock cycles delay between the assertion of the chip select signal and the first transmission of the serial clock. The polarity and phase of QSCKB are programmable. This is a GPIO signal when the QSCKB function is not being used. After reset, the default state is GPI.
MISOB	Input Input or Output	Input	**Synchronous master in slave out**—This input signal provides serial data input to QSPIB. Input data can be sampled on the rising or falling edge of QSCKB and received in QSPI RAM LSB first. This is a GPIO signal when the function is not being used. After reset, the default state is GPI.
MOSIB	Output Input or Output	Input	**Synchronous master out slave in**—This output signal provides serial data from QSPIB. Output data can be programmed to change state on the rising or falling edge of QSCKB and transmitted LSB first. This is a GPIO signal when the function is not being used. After reset, the default state is GPI.

For serial control port signals equipped with resistors, all pull-ups and pull-downs are automatically disconnected when the pin is an output.

2.21 SmartCard Port

After reset, the default state of all SmartCard port pins is GPI. For SmartCard port signals equipped with resistors, all pull-ups and pull-downs are automatically disconnected when the pin is an output.

Table 2-20. SmartCard Port Signals

Signal Name	Signal Type	State during Reset	Signal Description
SIMCLK	Output Input or Output	Input	**SIM clock—**This signal is an output clock from the SmartCard port to the SmartCard. This signal is a GPIO signal when the SmartCard port is not being used.

Table 2-20. SmartCard Port Signals (Continued)

Signal Name	Signal Type	State during Reset	Signal Description
SENSE	Input Input or Output	Input	**SIM sense—**This signal is a Schmitt trigger input that signals when a SmartCard is inserted or removed. This signal is a GPIO signal when the SmartCard port is not being used. The signal has an on-chip 100 kΩ pull-down resistor.
SIMDATA	Input/ Output Input or Output	Input	**SIM data—**This bidirectional signal is used to transmit data to and receive data from the SmartCard. In the output state, the signal is open drain. This signal is a GPIO signal when the SmartCard port is not being used. The signal has an on-chip 47 kΩ pull-up resistor.
$\overline{\text{SIMRESET}}$	Output Input or Output	Input	**SIM Reset—**This signal is an output reset signal from the SmartCard port to the SmartCard. The SmartCard port can activate the reset of an attached SmartCard by driving $\overline{\text{SIMRESET}}$ low. This signal is a GPIO signal when the SmartCard port is not being used.
PWR_EN	Output Input or Output	Input	**SIM power enable—**This active high output enables the external device that supplies V_{CC} to the SmartCard. If this pin is driven high, the external device supplies power to the SmartCard. Driving the signal low cuts off power to card. This permits effective power management and power sequencing for SmartCard enable/disable. This signal is a GPIO signal when the SmartCard port is not being used. This signal has an on-chip 100 kΩ pull-down resistor.

2.22 Serial Audio Codec Port

After reset, the default state of all serial audio codec pins is Hi-Z. For serial audio codec port signals equipped with resistors, all pull-ups and pull-downs are automatically disconnected when the pin is an output.

Table 2-21. Serial Audio Codec Port Signals

Signal Name	Signal Type	State during Reset	Signal Description
STDA	Input or Output	Input	**Audio codec transmit data**— This output signal transmits serial data from the audio codec serial transmitter shift register. It is equipped with a 100kΩ pull-up resistor. This is a GPIO signal when STDA is not being used. **Note:** This signal is disabled if the alternate STDA function on INT6 is selected. (See Table 2-13.)
SRDA	Input or Output	Input	**Audio codec receive data** — This input signal receives serial data and transfers the data to the audio codec receive shift register. It is equipped with a 100kΩ pull-down resistor. This is a GPIO signal when SRDA is not being used. **Note:** This signal is disabled if the alternate SRDA function on INT7 is selected. (See Table 2-13.)

Table 2-21. Serial Audio Codec Port Signals (Continued)

Signal Name	Signal Type	State during Reset	Signal Description
SCKA	Input or Output	Input	**Audio codec serial clock** — This bidirectional signal provides the serial bit rate clock when only one clock is being used or the TxD clock otherwise. It is equipped with a 100kΩ pull-down resistor. This is a GPIO signal when the serial audio codec port is not being used. **Note:** This signal is disabled if the alternate SCKA function on ROW7 is selected. (See Table 2-15.)
SC0A	Input or Output	Input	**Audio codec serial clock 0—**This signal's function is determined by the SCLK mode. • Synchronous mode—serial I/O flag 0 • Asynchronous mode—receive clock I/O This is a GPIO signal when SC0A is not being used.
SC1A	Input or Output	Input	**Audio codec serial clock 1—**This signal's function is determined by the SCLK mode. • Synchronous mode—serial I/O flag 0 • Asynchronous mode—receiver frame sync I/O This is a GPIO signal when SC1A is not being used.
SC2A	Input or Output	Input	**Audio codec serial clock 2—**This signal's function is determined by the SCLK mode. • Synchronous mode—transmitter and receiver frame sync I/O • Asynchronous mode—transmitter frame sync I/O It is equipped with a 100kΩ pull-down resistor. This is a GPIO signal when SC2A is not being used. **Note:** This signal is disabled if the alternate SC2A function on ROW6 is selected. (See Table 2-15.)

2.23 Baseband Codec Port

After reset, the default state of the baseband codec port pins is Hi-Z. For baseband codec port signals equipped with resistors, all pull-ups and pull-downs are automatically disconnected when the pin is an output.

Table 2-22. Baseband Codec Port Signals

Signal Name	Signal Type	State during Reset	Signal Description
STDB	Output Input or Output	Input	**Baseband codec transmit data**— This output signal transmits serial data from the baseband codec serial transmitter shift register. This signal is equipped with a 100 pull-up resistor. This is a GPIO signal when STDB is not being used.

Table 2-22. Baseband Codec Port Signals (Continued)

Signal Name	Signal Type	State during Reset	Signal Description
SRDB	Input Input or Output	Input	**Baseband codec receive data** — This input signal receives serial data and transfers the data to the baseband codec receive shift register. This signal is equipped with a 100kΩ pull-down resistor. This is a GPIO signal when SRDB is not being used.
SCKB	Input or Output	Input	**Baseband codec serial clock** — This bidirectional Schmitt trigger input signal providing the serial bit rate clock for the interface. The SCKB is a clock input or output used by both the transmitter and receiver in synchronous modes or by the transmitter in asynchro-nous modes. SCKB may be programmed as a general purpose I/O pin when the SCK function is not being used. If the bit MAGEN in the CKCTL Register is set, the SCK pin of the BBP is connected to the SCKB pin through the MAGIC interface logic and, therefore, if it is programmed as a general purpose input pin (in the BBP) it will not reflect the SCKB pin value, but the output value of the MAGIC interface logic. This pin is connected to the BBP SCK pin or left not connected, according to the value of the bit MAGIOEN in the CKCTL Register. This signal is equipped with an internal 100kW pull-down resistor. This is a GPIO signal when the port is not being used.
SC0B	Input or Output	Input	**Baseband codec serial clock 0—**This signal's function is determined by the SCLK mode. • Synchronous mode—serial I/O flag 0 • Asynchronous mode—receive clock I/O This signal is equipped with a 100kΩ pull-down resistor. This is a GPIO signal when SC0B is not being used.
SC1B	Input or Output	Input	**Baseband codec serial clock 1—**This signal's function is determined by the SCLK mode. • Synchronous mode—serial I/O flag 0 • Asynchronous mode—receiver frame sync I/O This signal is equipped with a 100KkΩ pull-down resistor. This is a GPIO signal when SC1B is not being used.
SC2B	Input or Output	Input	**Baseband codec serial clock 2—**This signal's function is determined by the SCLK mode. • Synchronous mode—transmitter and receiver frame sync I/O • Asynchronous mode—transmitter frame sync I/O This signal is equipped with a 100kΩ pull-down resistor. This is a GPIO signal when SC2B is not being used.
SRDB2	Input/ Output	GPI	Serial Receive Data Pin Multiplexed - receives serial data and transfers the data to the receive shift register. SRDB2 is input when data is being received. SRDB2 may be programmed as a general purpose I/O pin when the SRD function is not being used. This pin is connected to the BBP SRD pin or left not connected, according to the value of the bit MAGIOEN in the CKCTL Register. The SRDB2 pin has an internal 100kΩ pulldown resistor. The default state at reset is general purpose input.

Table 2-22. Baseband Codec Port Signals (Continued)

Signal Name	Signal Type	State during Reset	Signal Description
SCKB2	Input/ Output		Serial Clock Pin Multiplexed - is a bidirectional (Schmitt trigger input pin providing the serial bit rate clock for the interface. The SCKB2 is a clock input or output used by both the transmitter and receiver in synchronous modes or by the transmitter in asynchro-nous modes. SCKB2 may be programmed as a general purpose I/O pin when the SCK function is not being used. If the bit MAGEN in the CKCTL Register is set, the SCK pin of the BBP is connected to the SCKB2 pin through the MAGIC interface logic and, therefore, if it is programmed as a general purpose input pin (in the BBP) it will not reflect the SCKB2 pin value, but the output value of the MAGIC interface logic. This pin is connected to the BBP SCK pin or left not connected, according to the value of the bit MAGIOEN in the CKCTL Register. The SCKB pin has an internal 100kΩ pulldown resistor. The default state at reset is general purpose input.

2.24 Emulation Port

After reset, the default state for the emulation port pins is GPI.

Table 2-23. Emulation Port Signals

Signal Name	Signal Type	State during Reset	Signal Description
SIZ0–SIZ1	Input or Output	Input	**Data size 0–1—**These signals encode the data size for the current MCU access. When not programmed as data size signals, these are GPIO signals. The signals have on-chip 100 kΩ pull-up resistors.
PSTAT0–PSTAT3	Input or Output	Input	**Pipeline state 0–3—**These signals encode the internal MCU execution unit status. When not programmed as pipeline state signals, these are GPIO signals. The signals have on-chip 100 kΩ pull-up resistors.

2.25 Debug Control Port

If the MUX_CTL signal is driven high, the alternate $\overline{\text{MCU\_DE}}$ and $\overline{\text{DSP\_DE}}$ signal locations are selected, and this interface is disabled. For debug port control signals equipped with resistors, all pull-ups and pull-downs are automatically disconnected when the pin is an output.

Table 2-24. Debug Port Control Signals

Signal Name	Signal Type	State during Reset	Signal Description
$\overline{\text{MCU\_DE}}$	Input Output	Input	**Microcontroller debug event**—As an input signal, this signal provides a means to enter the debug mode of operation from an external command converter. An an output signal, it acknowledges that the MCU has entered the debug mode. This signal is equipped with an open-drain 47kΩ pull-up resistor. When the MCU enters the debug mode due to a debug request or as the result of meeting a breakpoint condition, it asserts $\overline{\text{MCU\_DE}}$ as an output signal for three clock cycles.
$\overline{\text{DSP\_DE}}$	Input Output	Input	**Digital signal processor debug event**—As an input signal, this signal provides a means to enter the debug mode of operation from an external command converter. An an output signal, it acknow-ledges that the DSP has entered the debug mode.This signal is equipped with an open-drain 4kΩ pull-up resistor. When the DSP enters the debug mode due to a debug request or as the result of meeting a breakpoint condition, it asserts $\overline{\text{DSP\_DE}}$ as an output signal for three clock cycles.

2.26 JTAG Port

When the bottom connector pins are selected as a debug port by holding the MUX_CTL pin at a logic high, the dedicated JTAG pins become inactive. That is, they are disconnected from the JTAG TAP controller. For JTAG signals equipped with resistors, all pull-ups and pull-downs are automatically disconnected when the pin is an output.

Table 2-25. JTAG Port Signals

Signal Name	Signal Type	State during Reset	Signal Description
TMS	Input	Input	**Test mode select**—TMS is an input signal used to sequence the test controller's state machine. TMS is sampled on the rising edge of TCK and has an internal 47 kΩ pull-up resistor. **MUX_CTL high**: INT7 is connected to the TAP controller and functions as TMS, see Table 2-13.)
TDI	Input	Input	**Test data input**—TDI is a serial test data input signal used for test instructions and data. TDI is sampled on the rising edge of TCK and has an internal 47 kΩ pull-up resistor. **MUX_CTL high**: RxD is connected to the TAP controller and functions as TDI, see Table 2-16.)

Table 2-25. JTAG Port Signals (Continued)

Signal Name	Signal Type	State during Reset	Signal Description
TDO	Output	Tri-stated	**Test data output**—TDO is a test data serial output signal used for test instructions and data. TDO is tri-statable and is actively driven in the shift-IR and shift-DR controller states. TDO changes on the falling edge of TCK. **MUX_CTL high**: TxD is connected to the TAP controller and functions as TDO, see Table 2-16.)
TCK	Input	Input	**Test clock**—TCK is a test clock input signal used to synchronize the JTAG test logic. It has an internal 47 kΩ pull-up resistor. **MUX_CTL high**: ROW7 is connected to the TAP controller and functions as TCK, see Table 2-15.)
$\overline{\text{TRST}}$	Input	Input	**Test Reset**—$\overline{\text{TRST}}$ is an active-low Schmitt-trigger input signal used to asynchronously initialize the test controller. $\overline{\text{TRST}}$ has an internal 47 kΩ pull-up resistor. **MUX_CTL high**: INT6 is connected to the TAP controller and functions as $\overline{\text{TRST}}$, see Table 2-13.)
TEST	Input	Input	**Factory test mode**—Selects factory test mode. Reserved. This pin has an internal 100kΩ pulldown resistor.

Part 3 Specifications

3.1 General Characteristics

The DSP56654 is fabricated in high-density CMOS. The DSP56654 specifications are preliminary and are from design simulations, and may not be fully tested or guaranteed at this early stage of the product life cycle. Finalized specifications will be published after full characterization and device qualifications are complete.

3.2 Maximum Ratings

CAUTION

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, normal precautions should be taken to avoid exceeding maximum voltage ratings. Reliability is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

Note: In the calculation of timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a “maximum” value for a specification will never occur in the same device that has a “minimum” value for another specification; adding a maximum to a minimum represents a condition that can never exist.

Table 3-1. Absolute Maximum Ratings (GND = 0 V)

Rating	Symbol	Value	Unit
Internal supply voltage	V_{CCI}	–0.3 to +2.75	V
External supply voltage	V_{DDE}	–0.3 to +3.6	V
Operating temperature range	T_A	–40 to +85	°C
Storage temperature	T_{STG}	–55 to +125	°C

3.3 Thermal Characteristics

Table 3-2. Thermal Characteristics

Characteristic	Symbol	BGA Value[1]	Unit
Junction-to-ambient thermal resistance[2]	$R_{\theta JA}$ or θ_{JA}	TBD	°C/W
Junction-to-case thermal resistance[3]	$R_{\theta JC}$ or θ_{JC}	TBD	°C/W
Thermal characterization parameter	Ψ_{JT}	TBD	°C/W

1. These are measured values; testing is not complete. Values were measured on a non-standard four-layer thermal test board (two internal planes) at one watt in a horizontal configuration.
2. Junction-to-ambient thermal resistance is based on measurements on a horizontal-single-sided printed circuit board per SEMI G38-87 in natural convection.(SEMI is Semiconductor Equipment and Materials International, 805 East Middlefield Rd., Mountain View, CA 94043, (415) 964-5111)
3. Junction-to-case thermal resistance is based on measurements using a cold plate per SEMI G30-88, with the exception that the cold plate temperature is used for the case temperature.

3.4 DC Electrical Characteristics

Table 3-3. DC Electrical Characteristics

Characteristics	Symbol	Min	Typ	Max	Units
Internal supply voltage	V_{CCI}	1.8	—	2.5	V
External supply voltage	V_{DDE}	V_{CCI}	—	3.4	V
I/O predriver supply voltage	V_{CCHQ}	V_{DDE}	—	3.4	V
Input high voltage	V_{IH}	$0.7 \times V_{DDE}$	—	V_{DDE}+ 0.2	V
Input low voltage	V_{IL}	–0.3	—	$0.2 \times V_{DDE}$	V
Input leakage current	I_{IN}	–10	—	10	µA
Output high voltage (I_{OH} = –400 µA)	V_{OH}	$0.9 \times V_{DDE}$	—	V_{DDE}	V
Output low voltage (I_{OL} = 800 µA)	V_{OL}	0	—	$0.1 \times V_{DDE}$	V
Total stop mode (DSP and MCU stopped, PLL powered down, timers disabled)	I_{CC_STOP}	—	60	—	µA
DSP run current at 58.8 MHz (MCU stopped, timers disabled, DSP running algorithm from internal memory, BBP and SAP active)	I_{CCDSP_RUN}	—	35	—	mA
PLL supply current (16.8 MHz input, DSP freq = 58.8 MHz, MCU clock = 16.8 MHz)	I_{CC_PLL}	—	1.6	—	mA
DSP wait current at 58.8 MHz (MCU stopped, timers disabled, BBP and SAP active)	$I_{CC\_DSP\_WAIT}$	—	4.5	—	mA

Table 3-3. DC Electrical Characteristics (Continued)

Characteristics	Symbol	Min	Typ	Max	Units
MCU run current at 16.8 MHz (DSP and DSP PLL stopped, timers disabled, MCU peripherals active)	$I_{CC\_MCU\_RUN}$	—	9	—	mA
MCU doze current at 16.8 MHz (DSP and DSP PLL stopped, timers disabled, MCU peripherals active)	$I_{CC\_MCU\_DOZE}$	—	3	—	mA
MCU wait current at 16.8 MHz (DSP and DSP PLL stopped, timers disabled, MCU peripherals active)	$I_{CC\_MCU\_WAIT}$	—	3	—	mA
Layer 1 Timer current (MCU and DSP stopped; 16.8 MHz to timer)	I_{CC_TIMER}	—	500	—	µA
Input capacitance per pin	C_{IN}	2	—	2.5	pF
Pull-up resistor value[1]	—	50%	100 %	180%	—

1. Applies to 22K and 47K resistors.

3.5 Clock Requirements

Table 3-4. Clock Requirements

Characteristics	Symbol	Min	Typ	Max	Units
CKIH input frequency	f_1	0	—	16.8	MHz
CKIL input frequency	f_2	0	32.768	f_1	kHz
MCU internal frequency	$f_{MCU-CLK}$	DC	—	16.8	MHz
DSP internal frequency	$f_{DSP-CLK}$	—	—	58.8	MHz
CKIH input voltage	V_{I-CKIH}	285	—	V_{IH}	mV_{PP}
CKIL input high voltage	$V_{IH-CKIL}$	1.8	—	2.77	V
CKIH input impedance	R_{I-CKIH}	TBD	—	TBD	MΩ

3.6 External Bus Interface Requirements

When the MCU is operating at 16.8 MHz, the bus interface can access 100 ns access time external memory with one wait state or 15 ns access time external memory with no wait states.

3.7 AC Electrical Characteristics

The characteristics listed in this section are given for V_{CCI} = 1.8 V and V_{DDE} = 3.3 V with a capacitive load of 50 pF.

3.8 Internal Clocks

For each occurrence of T_{DH}, T_{DL}, T_{DC}, or I_{DCYC}, substitute with the numbers in Table 3-6. DF, MF, and PDF are the DSP PLL division, multiplication, and pre-division factors set in registers.

Table 3-5. DSP Clocks

Characteristics	Symbol	Min	Max	Unit
Input frequency to the DSP PLL	EfD	0	16.8	MHz
DSP PLL input clock cycle time • • with PLL disabled • • with PLL enabled	ET_{DC}	 59.5 59.5	 ∞ 273100	 ns ns

Table 3-6. Internal DSP Clocks

Characteristics	Symbol	Expression
Internal DSP operation frequency with PLL enabled	fD	(EfD × MF) / (PDF × DF)
Internal DSP operation frequency with PLL disabled	fD	EfD/2
Internal DSP clock high period • with PLL disabled • with PLL enabled and MF ≤ 4 • with PLL enabled and MF > 4	T_{DH}	ET_{DC} (Min) 0.49 × ET_{DC} × PDF × DF/MF (Max) 0.51 × ET_{DC} × PDF × DF/MF (Min) 0.47 × ET_{DC} × PDF × DF/MF (Max) 0.53 × ET_{DC} × PDF × DF/MF
Internal clock low period • with PLL disabled • with PLL enabled and MF ≤ 4 • with PLL enabled and MF > 4	T_{DL}	ET_{DC} (Min) 0.49 × ET_{DC} × PDF × DF/MF (Max) 0.51 × ET_{DC} × PDF × DF/MF (Min) 0.47 × ET_{DC} × PDF × DF/MF (Max) 0.53 × ET_{DC} × PDF × DF/MF
Internal clock cycle time with PLL enabled	T_{DC}	ET_{DC} × PDF × DF/MF
Internal clock cycle time with PLL disabled	T_{DC}	2 × ET_{DC}
DSP Instruction cycle time	I_{DCYC}	T_{DC}

Table 3-7. MCU Clocks

Characteristics	Symbol	Min	Max	Unit
Frequency of the internal MCU-CLK clock	fM	0	16.8	MHz
Internal MCU-CLK clock cycle time	T_{MC}	59.5	∞	ns

3.9 PLL Characteristics

Table 3-8. PLL Characteristics

Characteristics	Expression	Min	Max	Unit
VCO frequency when PLL enabled[1]	MF × EfD × 2 / PDF	30	120	MHz
PLL external capacitor (PCAP pin to V_{CCP}) • MF ≤ 4 • MF > 4	C_{PCAP} [2]	 MF × 580– 100 MF × 830	 MF × 780– 140 MF × 1470	pF

1. The VCO output is further divided by 2 when PLL is enabled. If the division factor (DF) is 1, the operating frequency is $\frac{VCO}{2}$.
2. C_{PCAP} is the value of the PLL capacitor (connected between PCAP pin and V_{CCP}). (The recommended value for Cpcap is (680 ¥ MF – 120) pF for MF £ 4 and (1100 ¥ MF) pF for MF > 4.)

3.10 RESET, Mode Select, and Interrupt Timing

Table 3-9. Reset, Mode Select, and Interrupt Timing

Num	Characteristics	Expression	MCU @16.8 MHz DSP @58.8 MHz		Unit
			Min	Max	
1	$\overline{\text{RESET\_IN}}$ duration to guarantee reset	$3 \times T_{CKIL} + 0.05$	91.6	—	µs
2	Delay from $\overline{\text{RESET\_IN}}$ assertion to $\overline{\text{RESET\_OUT}}$ assertion	min: $4.5 \times T_{CKIL}$ max: $5.5 \times T_{CKIL}$	137.33	167.85	µs
3	Duration of $\overline{\text{RESET\_OUT}}$ assertion	$7 \times T_{CKIL}$	213.62	—	µs
4	Delay from $\overline{\text{RESET\_IN}}$ assertion to all pins at Reset value (periodically sampled and not 100% tested)	min: $4.5 \times T_{CKIL}$ max: $5.5 \times T_{CKIL}$	137.33	167.85	µs µs
5	MOD select setup time	$3.5 \times T_{CKIL} + 0.02$	107	—	µs
6	MOD select hold time	—	0	—	ns
7	Minimum edge-triggered $\overline{\text{DSP\_IRQ}}$ assertion width	—	15	—	ns
8	Minimum edge-triggered $\overline{\text{DSP\_IRQ}}$ deassertion width	—	15	—	ns
9	Minimum edge-triggered INTn width high	—	TBD	—	ns
10	Minimum edge-triggered INTn width low	—	TBD	—	ns

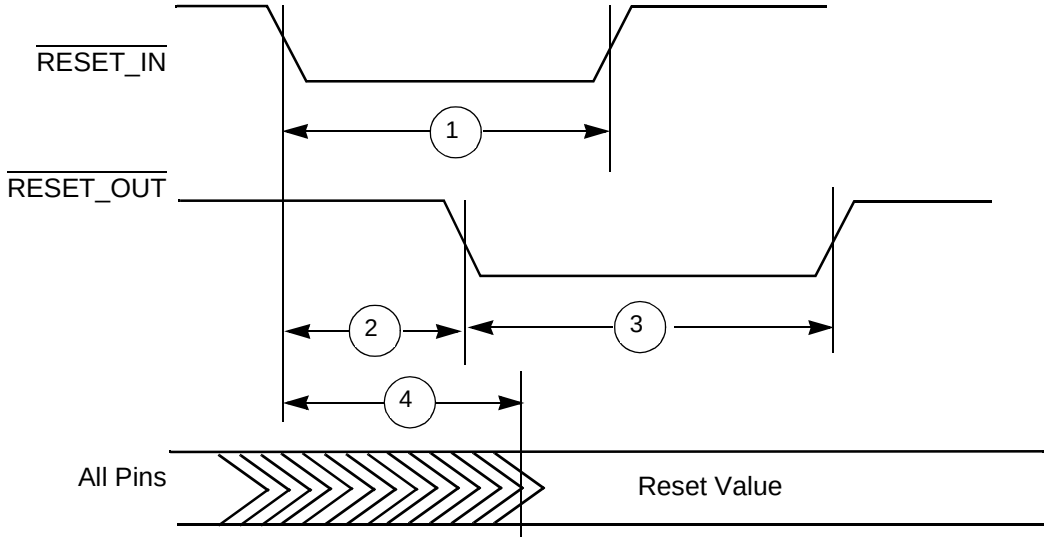


Figure 3-1. Reset Timing

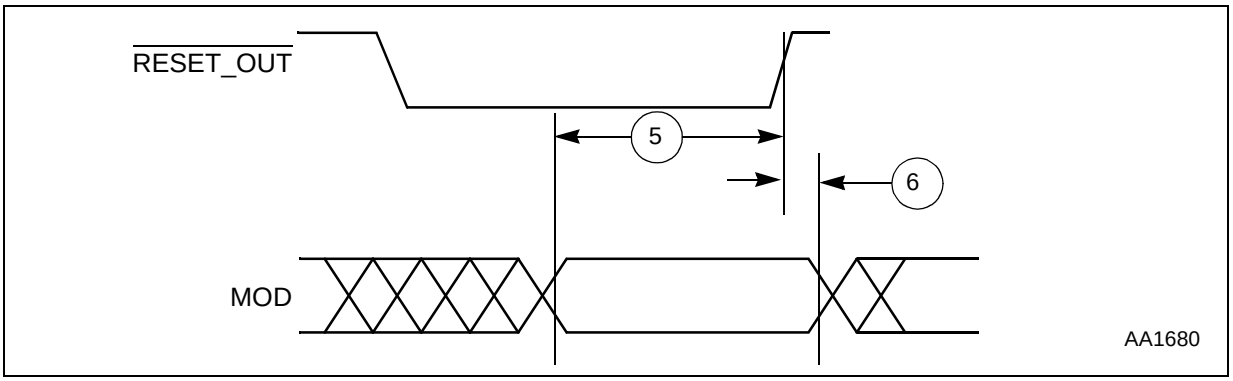


Figure 3-2. Operating Mode Select Timing

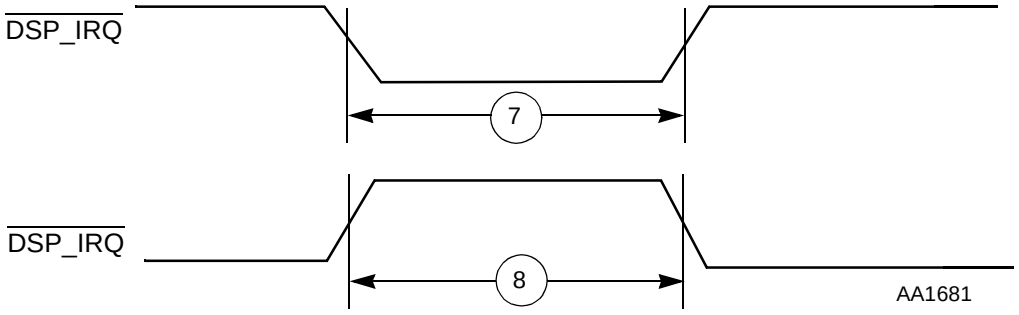


Figure 3-3. DSP External Interrupt Timing (Negative Edge-Triggered)

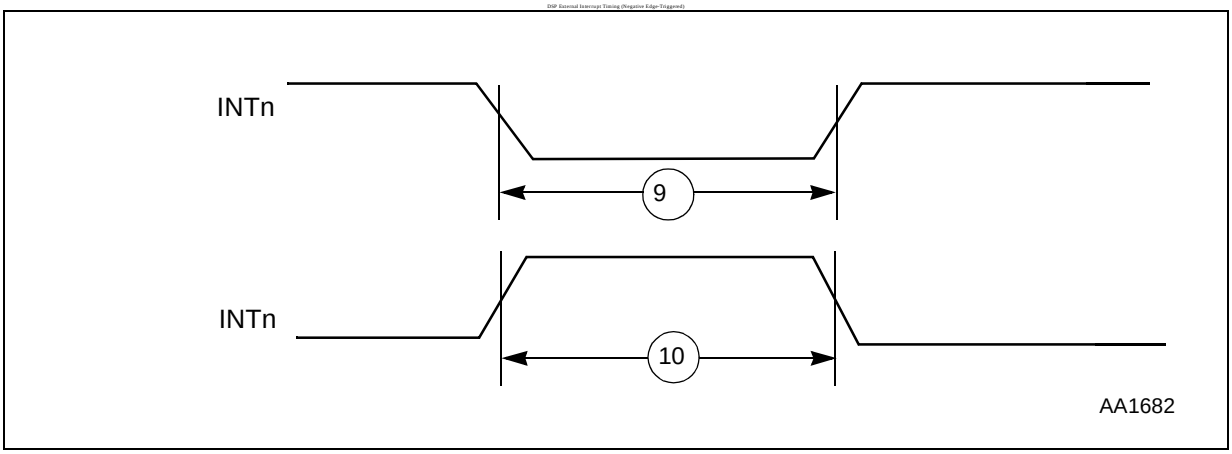


Figure 3-4. INT0–INT7 External Interrupt Timing

3.11 External Interface Module Timing

The EIM provides the bus interface between the DSP56654 and external memory and peripherals. It uses the external address bus, data bus, bus control signals, and the chip select signals.

Table 3-10. EIM External Bus Output AC Timing Specifications[1]

Num	Characteristics	MCU @16.8 MHz		Unit
		Min	Max	
11	CLK rise to address and R/$\overline{W}$ valid	0	15	ns
12	CLK rise to address and R/$\overline{W}$ invalid (output hold)	0	15	ns
13	CLK rise to CS asserted	0	15	ns
14	CLK rise to CS deasserted (output hold)	0	15	ns
15	CLK fall to $\overline{OE}$, $\overline{EB}$ asserted (read, OEA = 0), $\overline{EB}$ asserted (write)[2]	0	15	ns
16	CLK rise to $\overline{OE}$, $\overline{EB}$ asserted (read, OEA = 1)[2]	0	15	ns
17	CLK rise to $\overline{OE}$, $\overline{EB}$ deasserted (output hold) (read)[2]	0	15	ns
	CLK rise to $\overline{EB}$ deasserted (output hold) (write, WEN = 0)	0	15	ns
18	CLK fall to $\overline{EB}$ deasserted (output hold) (write, WEN = 1)	0	15	ns
19	CLK fall to $\overline{OE}$, $\overline{EB}$ asserted (WSC = 0)[2]	0	15	ns
20	CLK rise to $\overline{OE}$, $\overline{EB}$ deasserted (output hold) (WSC = 0)[2]	0	15	ns
21	Data-in valid to CLK rise (set-up)	3	—	ns

Table 3-10. EIM External Bus Output AC Timing Specifications[1]

Num	Characteristics	MCU @16.8 MHz		Unit
		Min	Max	
22	CLK rise to data–in invalid (hold)	7	—	ns
23	CLK rise to data-out valid	0	20	ns
24	CLK rise to data-out invalid (output hold)	0	20	ns
25	CLK rise to data-out high impedance	0	20	ns
26	CLK fall to data-out valid (WSC = 0)	0	20	ns
27	CLK rise to data-out invalid (output hold) (WSC = 0)	0	20	ns
28	CLK rise to data-out high impedance (WSC = 0)	0	20	ns

1. The following notes apply to this table:
   - Input and output timings are measured at the 50% point of the waveforms. The specifications assume a capacitive load of 50 pF.
   - These timings were measured with respect to the input clock edges.
2. EB outputs are asserted for reads if the EBC bit in the corresponding CS control register is clear.

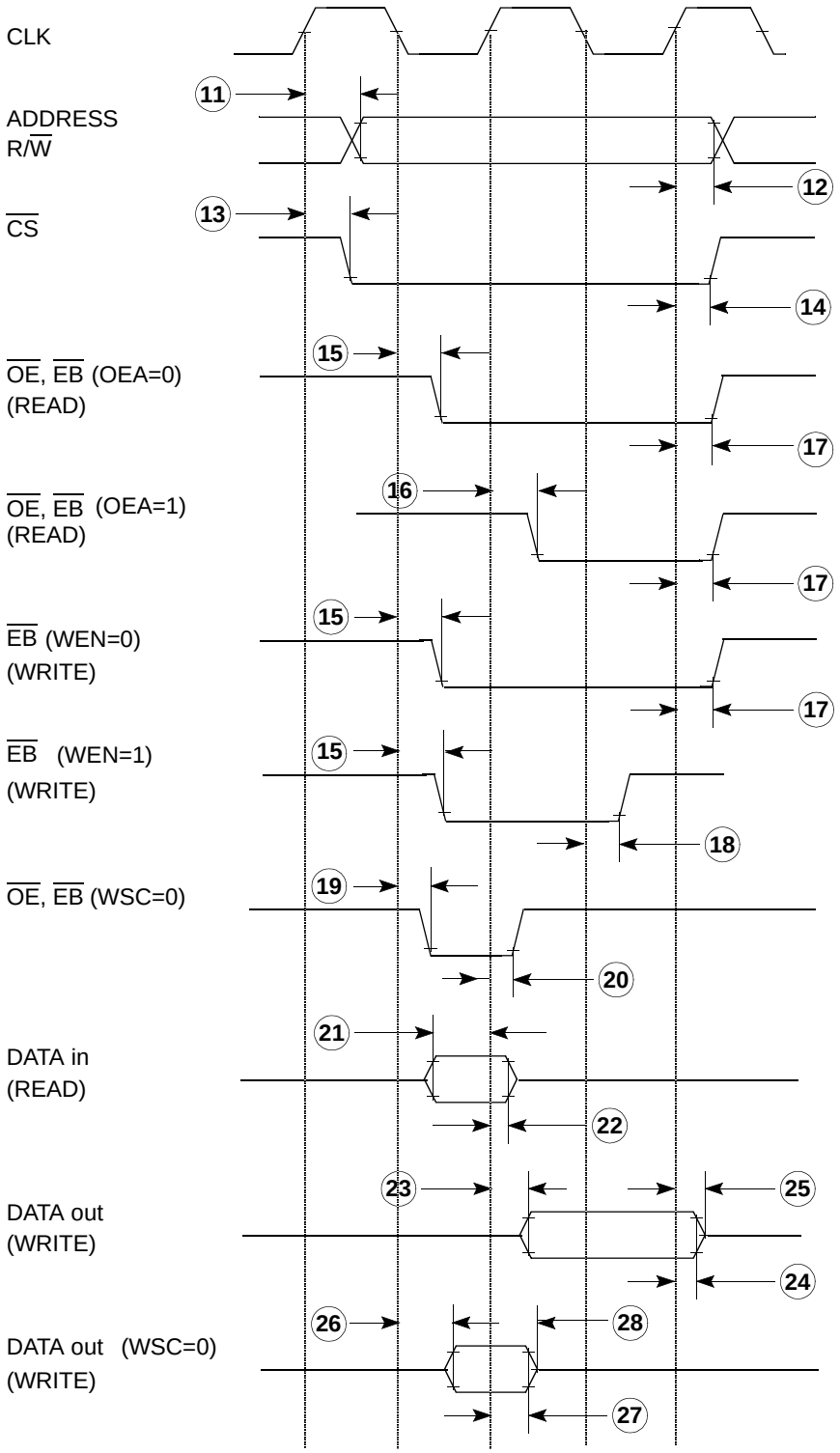


Figure 3-5. EIM Read/Write Timing

3.12 Emulation Port Timing

Table 3-11. Emulation Port AC Timing Specifications

Num	Characteristics	Expression	@16.8 MHz		Unit
			Min	Max	
11	CKO rise to SIZ Valid		—	TBD	ns
12	CKO rise to SIZ Invalid (output hold)		TBD	—	ns
13	CKO rise to PSTAT Valid		—	TBD	ns
14	CKO rise to PSTAT Invalid (output hold)		TBD	—	ns

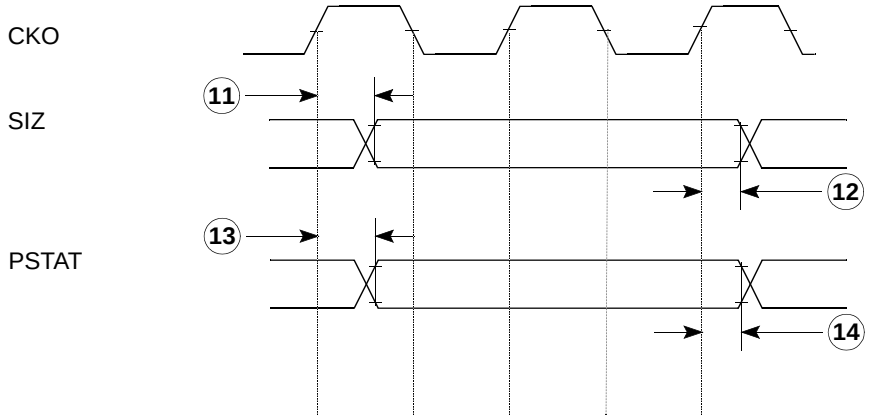


Figure 3-6. SIZ / PSTAT Timing

3.13 SmartCard Timing

Table 3-12. SmartCard Port to SmartCard AC Timing

Num	Characteristics	CKIH @ 16.8 MHz		Unit
		Min	Max	
31	$\overline{\text{SIMRESET}}$ low to SIMCLK low	1.18	200/f	µs
32	SIMCLK deactivated to SIMDATA tri-state to low	1.18	200/f	µs
33	SIMDATA low to PWR_EN low	1.18	200/f	µs
34	$\overline{\text{SIMRESET}}$ low	40000/f	—	ns
35	SENSE high to $\overline{\text{SIMRESET}}$ low	57	76	µs

Table 3-12. SmartCard Port to SmartCard AC Timing (Continued)

Num	Characteristics	CKIH @ 16.8 MHz		Unit
		Min	Max	

Note: "f" is CKIH/4 (for 5 V sims) or CKIH/5 (for 3 V sims), as programmed in the SmartCard port.

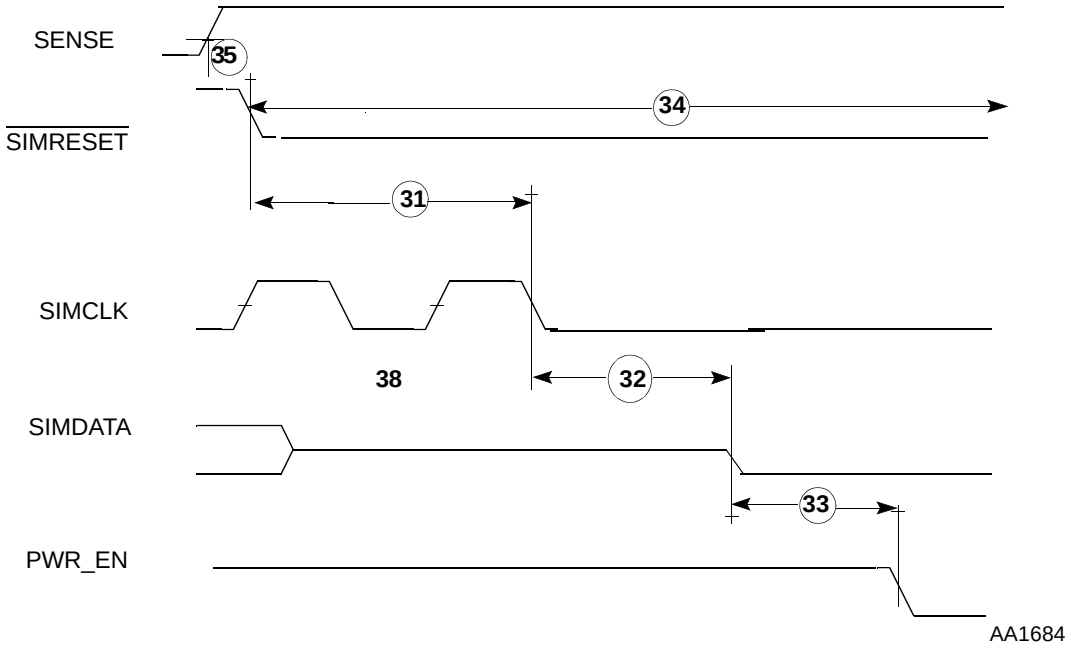


Figure 3-7. SmartCard Interface Power-Down AC Timing

3.14 QSPI Timing

The QSPI uses the signals in the serial control port to select individual serial peripherals (using the SPI chip select signals) and transfer data between peripherals and the DSP56654**.**

Table 3-13. QSPI Timing

Num	Characteristics	Symbol	Expression	MCU @ 16.8 MHz		Unit
				Min	Max	
301	Cycle time	T_{QCYC}	—	1	504	T_{MC}
302	Clock (SCK) high or low time	T_{SW}	—		252	T_{MC}
303	Chip-select lag time	T_{LAG}	—	1	∞	T_{QCYC}
304	Inter-queue transfer delay	T_{TD}	—	1	∞	T_{QCYC}
305	Chip-select lead time	T_{LEAD}	—	1	128	T_{QCYC}

Table 3-13. QSPI Timing (Continued)

Num	Characteristics	Symbol	Expression	MCU @ 16.8 MHz		Unit
				Min	Max	
306	Data setup time (inputs)	T_{SU}	—	0	—	nS
307	Data hold time (inputs)	T_{HI}	—	0.5	—	T_{QCYC}
308	Data valid (after SCK edge)	T_V	—	—	6	nS
309	Data hold time (outputs)	T_{HO}	—	–2	—	nS
310	Rise time	T_I	—	—	10	nS
311	Fall time	T_F	—	—	10	nS

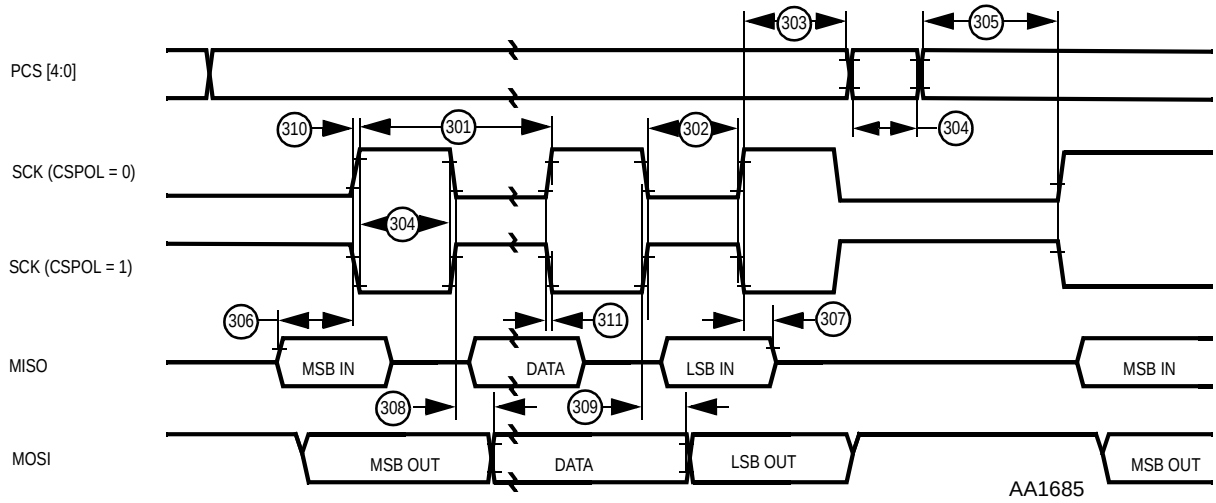


Figure 3-8. QSPI Timings for CPHA = 0

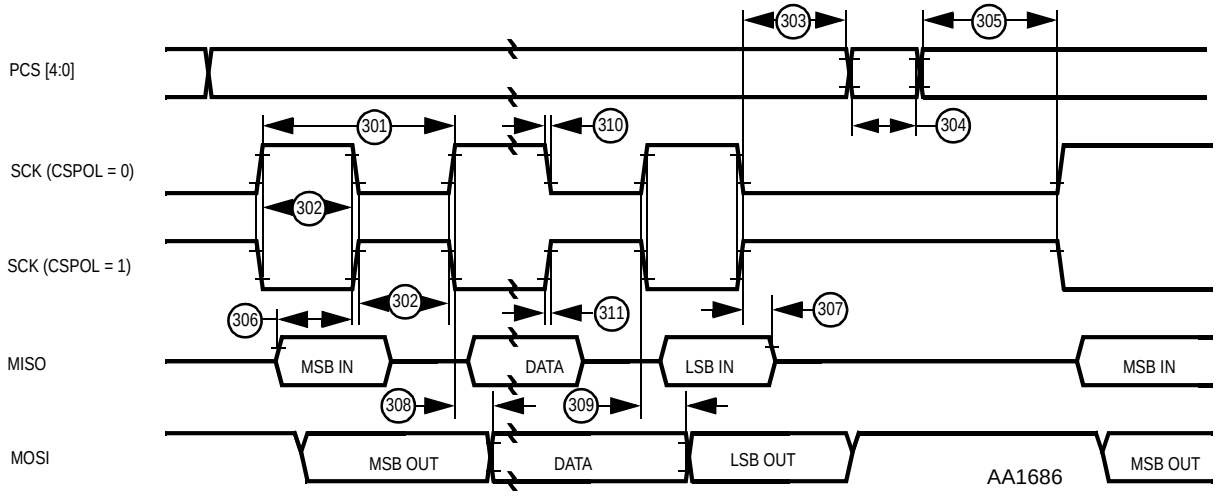


Figure 3-9. QSPI Timings for CPHA = 1

3.15 Audio Serial Codec and Baseband Serial Codec Timing

The audio serial codec port (also called the serial audio port or SAP) and the baseband serial codec port (also called the baseband port or BBP) have the same timing specifications. The timing table uses the following acronyms to describe the signal parameters:

- SSICC = BBP/SAP clock cycle time
- TXC (SCKA/SCKB Pin) = transmit clock
- RXC (SC0A/SC0B or SCKA/SCKB Pin) = receive clock
- FST (SC2A/SC2B Pin) = transmit frame sync
- FSR (SC1A/SC1B or SC2A/SC2B Pin) = receive frame sync
- i ck = internal clock
- x ck = external clock
- i ck a = internal clock, asynchronous mode (“asynchronous” implies that TXC and RXC are two different clocks)
- i ck s = internal clock, synchronous mode (“synchronous” implies that TXC and RXC are the same clock)
- bl = bit length
- wl = word length
- wr = word length relative

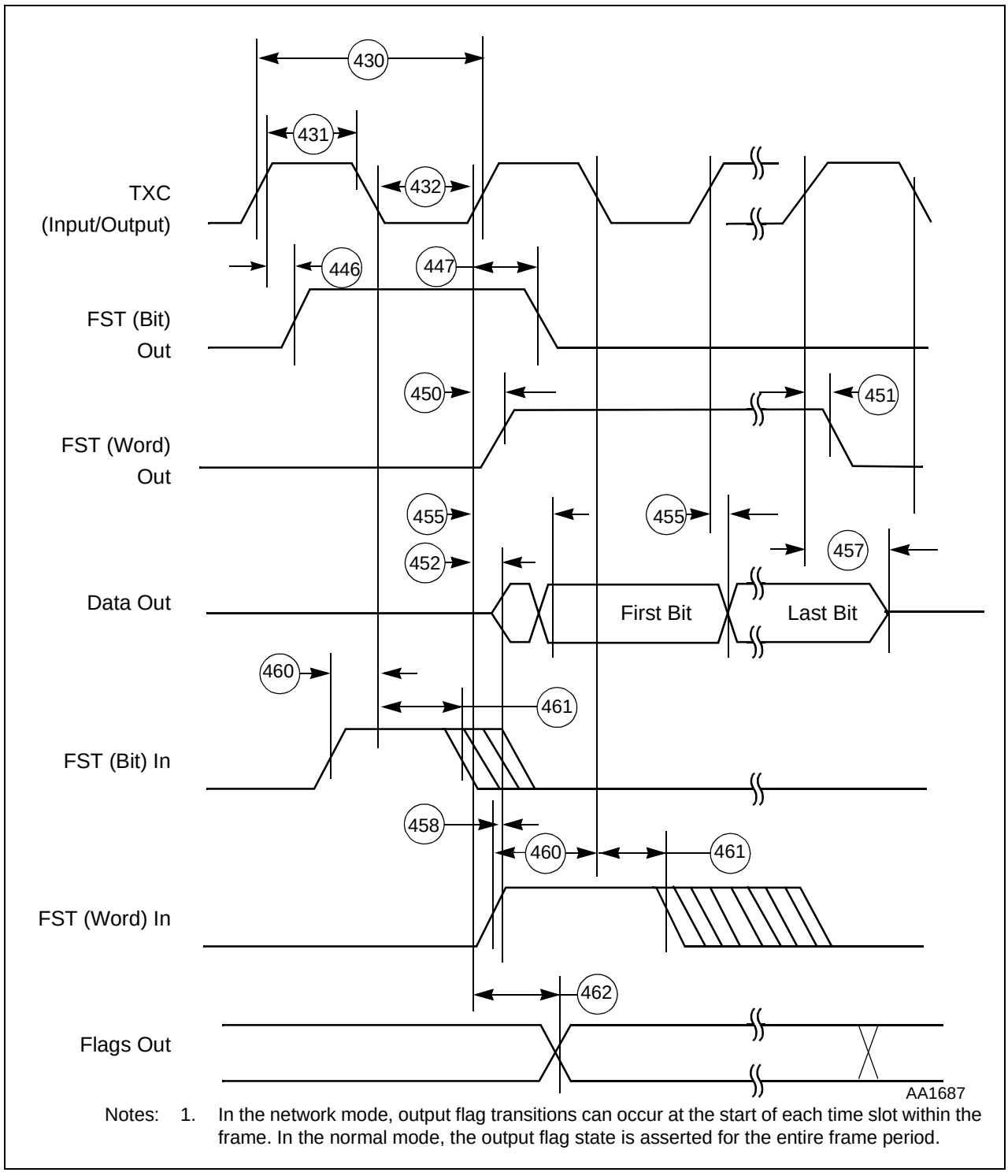
Table 3-14. SAP and BBP Timing

Num	Characteristics	Symbol	Expression	DSP_CLK @ 58.8 MHz		Case	Unit
				Min	Max		
430	Clock cycle[1]	t_{SSICC}	$4 \times T_{DC}$ $3 \times T_{DC}$	68 51	— —	i ck x ck	ns ns
431	Clock high period • for internal clock • for external clock	—	 $2 \times T_{DC} - 12.2$ $1.5 \times T_{DC}$	 21.8 25.5	 — —	 i ck x ck	 ns ns
432	Clock low period • for internal clock • for external clock	—	 $2 \times T_{DC} - 12.2$ $1.5 \times T_{DC}$	 21.8 25.5	 — —	 i ck x ck	 ns ns
433	RXC rising edge to FSR out (bl) high	—	—	— —	45.1 26.8	x ck i ck a	ns ns
434	RXC rising edge to FSR out (bl) low	—	—	— —	45.1 26.8	x ck i ck a	ns ns
435	RXC rising edge to FSR out (wr) high[2]	—	—	— —	47.6 29.3	x ck i ck a	ns ns
436	RXC rising edge to FSR out (wr) low[2]	—	—	— —	47.6 29.3	x ck i ck a	ns ns
437	RXC rising edge to FSR out (wl) high	—	—	— —	45.9 25.6	x ck i ck a	ns ns
438	RXC rising edge to FSR out (wl) low	—	—	— —	45.1 26.8	x ck i ck a	ns ns
439	Data in setup time before RXC (SCK in synchronous mode) falling edge	—	—	0.0 23.2	— —	x ck i ck	ns ns
440	Data in hold time after RXC falling edge	—	—	6.1 3.6	— —	x ck i ck	ns ns
441	FSR input (bl, wr) high before RXC falling edge[2]	—	—	1.2 28.0	— —	x ck i ck a	ns ns
442	FSR input (wl) high before RXC falling edge	—	—	1.2 28.0	— —	x ck i ck a	ns ns
443	FSR Input hold time after RXC falling edge	—	—	3.6 0.0	— —	x ck i ck a	ns ns
444	Flags input setup before RXC Falling edge	—	—	0.0 23.2	— —	x ck i ck s	ns ns
445	Flags input hold time after RXC falling edge	—	—	7.3 0.0	— —	x ck i ck s	ns ns
446	TXC rising edge to FST out (bl) high	—	—	— —	35.4 18.3	x ck i ck	ns ns
447	TXC rising edge to FST out (bl) low	—	—	— —	37.8 20.7	x ck i ck	ns ns

Table 3-14. SAP and BBP Timing (Continued)

Num	Characteristics	Symbol	Expression	DSP_CLK @ 58.8 MHz		Case	Unit
				Min	Max		
448	TXC rising edge to FST out (wr) high[2]	—	—	— —	37.8 20.7	x ck i ck	ns ns
449	TXC rising edge to FST out (wr) low[2]	—	—	— —	40.3 23.2	x ck i ck	ns ns
450	TXC rising edge to FST out (wl) high	—	—	— —	36.6 19.5	x ck i ck	ns ns
451	TXC rising edge to FST out (wl) low	—	—	— —	37.8 20.7	x ck i ck	ns ns
452	TXC rising edge to data out enable from high impedance	—	—	— —	37.8 20.7	x ck i ck	ns ns
454	TXC rising edge to data out valid	—	$35 + 0.5 \times T_{DC}$	— —	43.5 25.6	x ck i ck	ns ns
455	TXC rising edge to data out high impedance[3]	—	—	— —	37.8 19.5	x ck i ck	ns ns
457	FST input (bl, wr) set-up time before TXC falling edge[2]	—	—	2.0 21.0	— —	x ck i ck	ns ns
458	FST input (wl) to data out enable from high impedance[3]	—	—	—	32.9		ns
460	FST input (wl) setup time before TXC falling edge	—	—	2.0 21.0	— —	x ck i ck	ns ns
461	FST input hold time after TXC falling edge	—	—	4.0 0.0	— —	x ck i ck	ns ns
462	Flag output valid after TXC rising edge	—	—	— —	39.0 22.0	x ck i ck	ns ns

1. For internal clock, external clock cycle is defined by I_{CYC} and BBP/SAP control register.
2. Word relative frame sync signal wave form, relates to clock, as the bit length frame sync signal wave form, but spreads from one serial clock before first bit clock (same as bit length frame sync signal), until the one before last bit clock of the first word in frame.
3. Periodically sampled and not 100% tested.



Notes: 1. In the network mode, output flag transitions can occur at the start of each time slot within the frame. In the normal mode, the output flag state is asserted for the entire frame period.

Figure 3-10. BBP and SAP Transmitter Timing

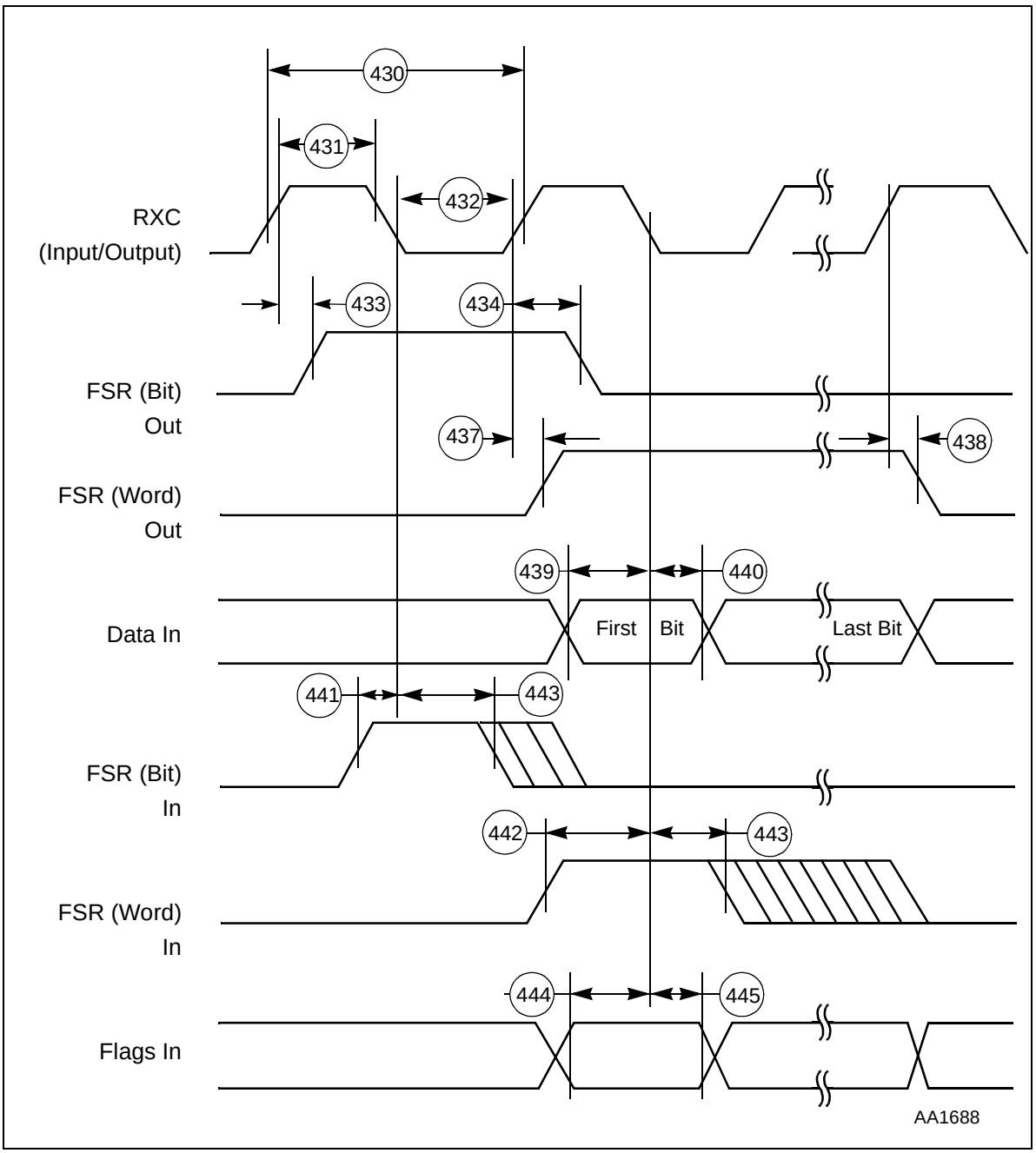


Figure 3-11. BBP and SAP Receiver Timing

3.16 JTAG Port Timing

Table 3-15. JTAG Timing

Num	Characteristics	Expression	DSP_CLK @ 58.8 MHz		Unit
			Min	Max	
500	TCK frequency of operation	$1/(3 \times T_{DC})$	0.0	19.6	MHz
501	TCK cycle time in crystal mode	—	45.0	—	ns
502	TCK clock pulse width measured at 1.5 V	—	20.0	—	ns
503	TCK rise and fall times	—	0.0	3.0	ns
504	Boundary scan input data setup time	—	5.0	—	ns
505	Boundary scan input data hold time	—	24.0	—	ns
506	TCK low to output data valid	—	0.0	40.0	ns
507	TCK low to output high impedance	—	0.0	40.0	ns
508	TMS, TDI data setup time	—	5.0	—	ns
509	TMS, TDI data hold time	—	25.0	—	ns
510	TCK low to TDO data valid	—	0.0	44.0	ns
511	TCK low to TDO high impedance	—	0.0	44.0	ns
512	TRST assert time	—	100.0	—	ns
513	TRST setup time to TCK low	—	40.0	—	ns

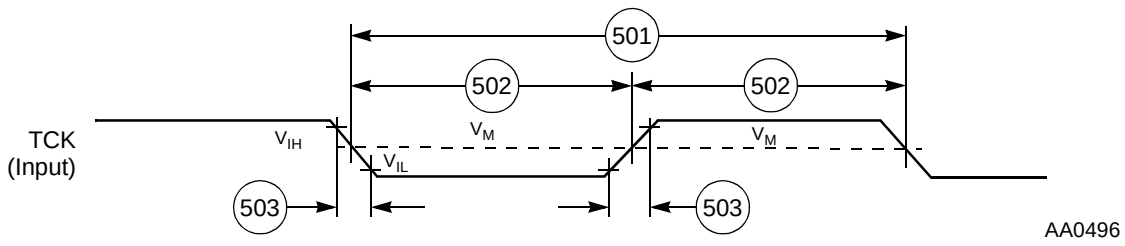


Figure 3-12. Test Clock Input Timing Diagram

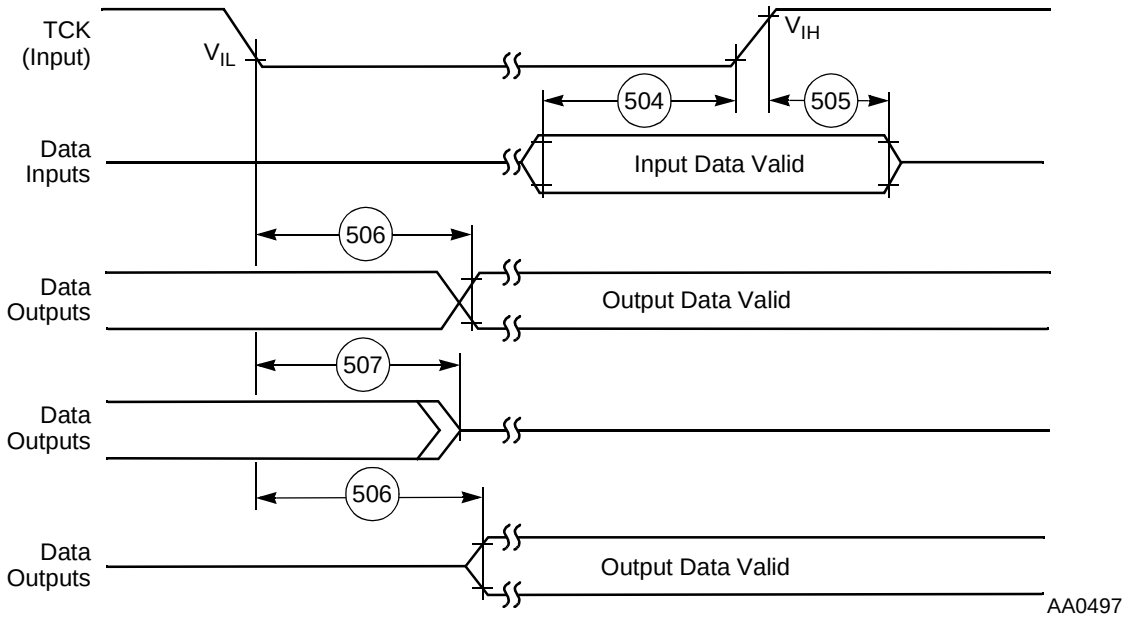


Figure 3-13. Boundary Scan (JTAG) Timing Diagram

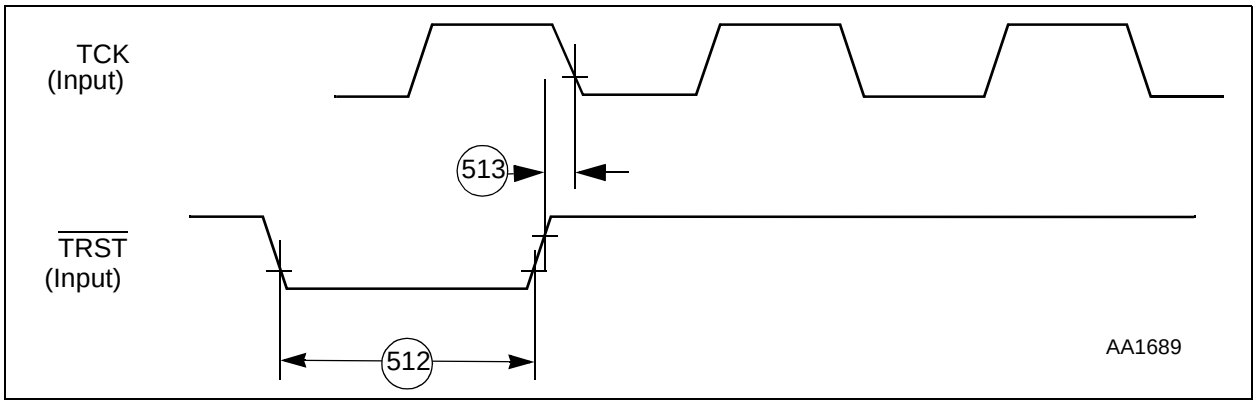


Figure 3-14. $\overline{\text{TRST}}$ Timing Diagram

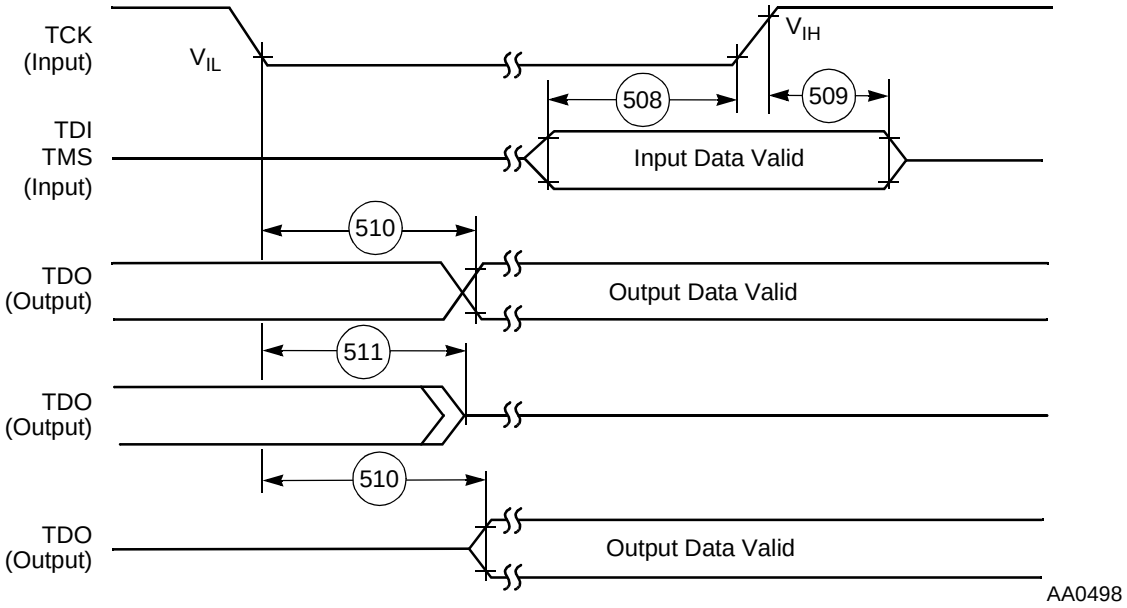


Figure 3-15. Test Access Port Timing Diagram

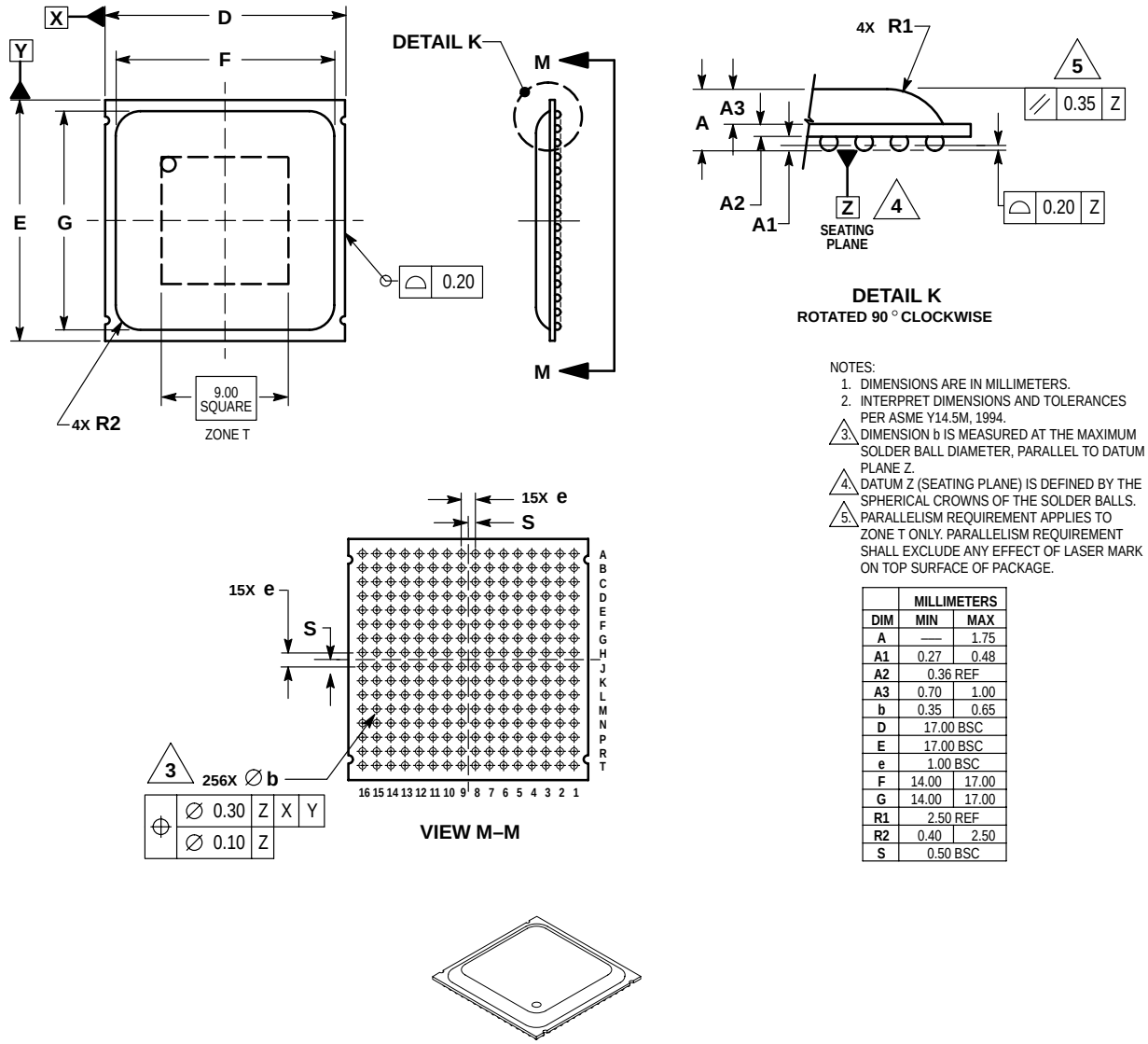
Part 4 Pin-Out and Package Information

This section provides information about the available packages for this product. The DSP56654 is available in a 256-pin PBGA and MBGA package.

4.1 256-Pin BGA Details

The DSP56654 is offered in the JEDEC-standard, 17-mm Plastic BGA and Map BGA with 1-mm-pitch solder balls. Refer to Section 4.1.1, "PBGA Package Mechanical Drawing," on page 4-1 and Section 4.1.2, "MBGA Package Mechanical Drawing," on page 4-2 for package drawing and dimensions, respectively.

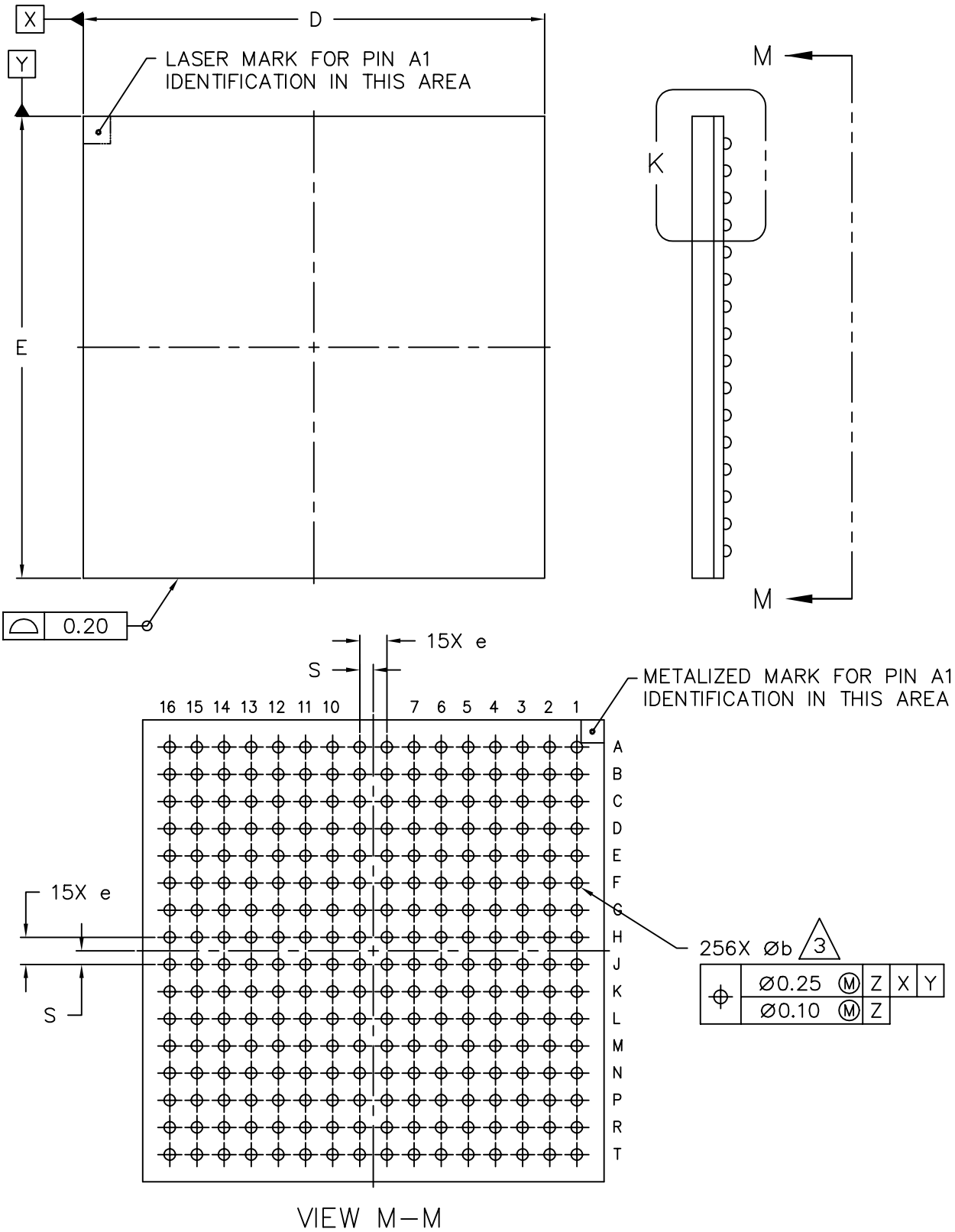
4.1.1 PBGA Package Mechanical Drawing

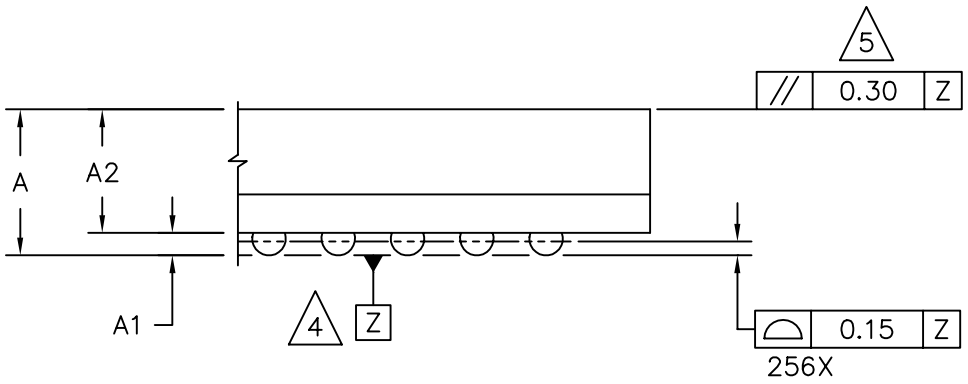


NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
4. DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM REQUIREMENT APPLIES TO ZONE T ONLY. PARALLELISM REQUIREMENT SHALL EXCLUDE ANY EFFECT OF LASER MARK ON TOP SURFACE OF PACKAGE.

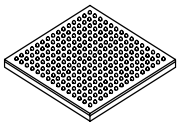
	MILLIMETERS	
DIM	MIN	MAX
A	—	1.75
A1	0.27	0.48
A2	0.36 REF	
A3	0.70	1.00
b	0.35	0.65
D	17.00 BSC	
E	17.00 BSC	
e	1.00 BSC	
F	14.00	17.00
G	14.00	17.00
R1	2.50 REF	
R2	0.40	2.50
S	0.50 BSC	

4.1.2 MBGA Package Mechanical Drawing





DETAIL K
ROTATED 90° CLOCKWISE



DIM	MIN	MAX
A	1.25	1.60
A1	0.27	0.47
A2	1.16 REF	
b	0.40	0.60
D	17.00 BSC	
E	17.00 BSC	
e	1.00 BSC	
S	0.50 BSC	

NOTES

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
4. DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

4.2 Ordering Drawings

Complete mechanical information regarding DSP56654 packaging is available by facsimile through Motorola's Mfax system. Call the following number to obtain information by facsimile:

(602) 244-6591

The Mfax automated system requests the following information:

- The receiving facsimile telephone number including area code or country code
- The caller's personal identification number (PIN)

Note: For first time callers, the system provides instructions for setting up a PIN, which requires entry of a name and telephone number.

- The type of information requested:
  - Instructions for using the system
  - A literature order form
  - Specific part technical information or data sheets
  - Other information described by the system messages

A total of three documents may be ordered per call.

The DSP56654 256-pin PBGA package mechanical drawing is referenced as Case 1216-02 Rev. A.
The DSP56654 256-pin MBGA package mechanical drawing is referenced as Case 1216-01 Rev. B.

Part 5 Design Considerations

5.1 Heat Dissipation

An estimation of the DSP56654 chip junction temperature, T_J, in °C can be obtained from the equation:

Equation 1: $T_J = T_A + (P_D \times R_{\theta JA})$

Where:

T_A = ambient temperature °C
$R_{\theta JA}$ = package junction-to-ambient thermal resistance °C/W
P_D = power dissipation in package

Historically, thermal resistance has been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

Equation 2: $R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$

Where:

$R_{\theta JA}$ = package junction-to-ambient thermal resistance °C/W
$R_{\theta JC}$ = package junction-to-case thermal resistance °C/W
$R_{\theta CA}$ = package case-to-ambient thermal resistance °C/W

$R_{\theta JC}$ is device-related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For example, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on the printed circuit board, or otherwise change the thermal dissipation capability of the area surrounding the device on a printed circuit board. This model is most useful for ceramic packages with heat sinks; ninety percent of the heat flow is dissipated through the case to the heat sink and out to the ambient environment. For ceramic packages, in situations where the heat flow is split between a path to the case and an alternate path through the printed circuit board, analysis of the device thermal performance may need the additional modeling capability of a system level thermal simulation tool.

The thermal performance of plastic packages is more dependent on the temperature of the printed circuit board to which the package is mounted. Again, if the estimations obtained from $R_{\theta JA}$ do not satisfactorily answer whether the thermal performance is adequate, a system level model may be appropriate.

A complicating factor is the existence of three common ways for determining the junction-to-case thermal resistance in plastic packages:

- To minimize temperature variation across the surface, the thermal resistance is measured from the junction to the outside surface of the package (case) closest to the chip mounting area when that surface has a proper heat sink.
- To define a value approximately equal to a junction-to-board thermal resistance, the thermal resistance is measured from the junction to where the leads are attached to the case.
- If the temperature of the package case (T_T) as determined by a thermocouple, the thermal resistance is computed using the value obtained by the equation $(T_J - T_T)/P_D$.

As noted above, the junction-to-case thermal resistances quoted in this data sheet are determined using the first definition. From a practical standpoint, this value is also suitable for determining the junction temperature from a case thermocouple reading in forced convection environments. In natural

convection, using the junction-to-case thermal resistance to estimate junction temperature from a thermocouple reading on the case of the package will estimate a junction temperature slightly hotter than actual temperature. Hence, the new thermal metric, thermal characterization parameter or Ψ_{JT}, has been defined to be $(T_J - T_T)/P_D$. This value gives a better estimate of the junction temperature in natural convection when using the surface temperature of the package. Remember that surface temperature readings of packages are subject to significant errors caused by inadequate attachment of the sensor to the surface and to errors caused by heat loss to the sensor. The recommended technique is to attach a 40-gauge thermocouple wire and bead to the top center of the package with thermally conductive epoxy.

Note: **Table 3-2 on page 3-2** of this document contains the package thermal values for this chip.

5.2 Electrical Design Considerations

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

Use the following list of recommendations to assure correct DSP operation:

- Provide a low-impedance path from the board power supply to each V_{CC} pin on the DSP and from the board ground to each GND pin.
- Use at least four 0.1 µF bypass capacitors positioned as close as possible to the four sides of the package to connect the V_{CC} power source to GND.
- Ensure that capacitor leads and associated printed circuit traces that connect to the chip V_{CC} and GND pins are less than 0.5 inch per capacitor lead.
- Use at least a four-layer printed circuit board (PCB) with two inner layers for V_{CC} and GND.
- Because the DSP output signals have fast rise and fall times, PCB trace lengths should be minimal. This recommendation particularly applies to the address and data buses as well as the R/$\overline{W}$, $\overline{DSP\_IRQ}$, and INT0–INT7 signals.
- Consider all device loads as well as parasitic capacitance due to PCB traces when calculating capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the V_{CC} and GND circuits.
- All inputs must be terminated (i.e., not allowed to float) using CMOS levels.
- Take special care to minimize noise levels on the PLL supply pins (both V_{CC} and GND).

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