HC05PE0GRS/D

68HC05PE0

SPECIFICATION

REV. 1.2

(General Release)

CSIC System Design Group
Austin, Texas

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SECTION 1 INTRODUCTION

1.1 GENERAL

The MC68HC05PE0 is a 28-pin device based on the MC68HC05P1. The memory map includes 2096 bytes of user ROM, 128 bytes of RAM, and 64 bits of Personality EPROM. The MCU has two 8-bit I/O ports A and C. Port B has three I/O pins and port D has two pins, one I/O and the other input only. MC68HC05PE0 includes an on-chip mask programmable Computer Operating Properly (COP) watchdog circuit.

1.2 FEATURES

- Low cost
- HC05 Core
- 28 pin package
- On-Chip Oscillator with RC or Crystal/Ceramic Resonator Mask Options
- 128 Bytes of On-Chip RAM
- 2096 Bytes of User ROM plus 16 user vector locations
- 64 Bits of CPU programmable Personality EPROM
- 16 Bit Timer
- 20 Bidirectional I/O Lines Including:
  - Mask programmable interrupts on 8 I/O pins (Keyboard Scan Feature)
  - High Current Sink and Source on one I/O pin
- Single-Chip Mode
- Self-Check Mode
- Test Mode
- Power Saving STOP and WAIT Modes
- Edge-Sensitive or Edge and Level-Sensitive Interrupt Trigger Mask Option
- Mask option selectable Watchdog Timer (COP)

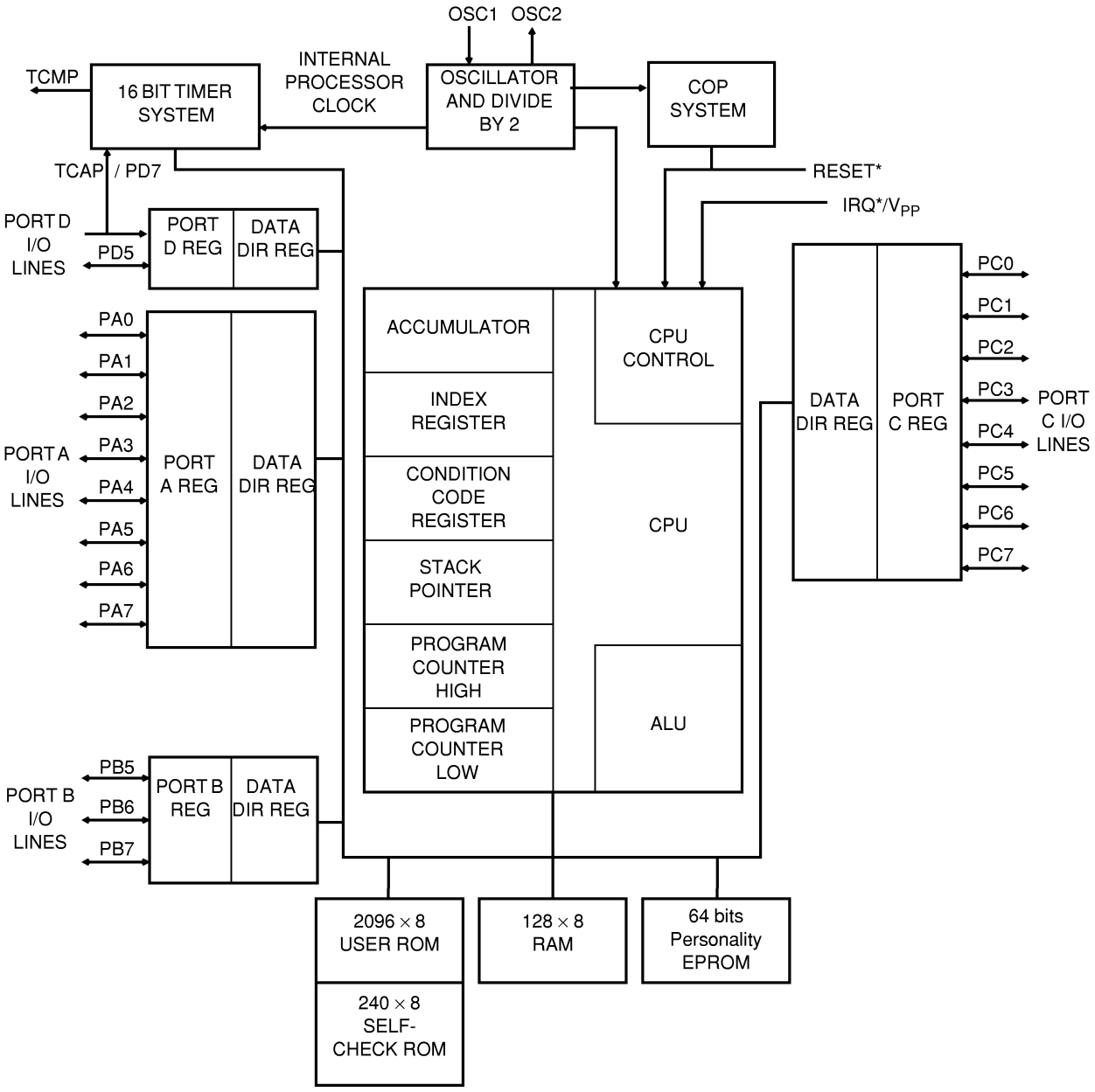


Figure 1-1: Block Diagram

1.3 MASK OPTIONS

There are eleven mask options on the MC68HC05PE0: CLOCK (RC or Crystal), IRQ* (edge-sensitive only or edge and level-sensitive), COP Watchdog Timer (enable/disable) and eight Port A interrupts and pulldowns (enable/disable). All mask options and the user ROM are programmed on the 01N layer in fabrication.

NOTE: Negative true signals like RESET* and IRQ* will be denoted with either an asterisk or an overline.

1.4 SIGNAL DESCRIPTION

1.4.1 V_{DD} AND V_{SS}

Power is supplied to the microcontroller using these two pins. V_{DD} is the positive supply, and V_{SS} is ground.

1.4.2 IRQ*/VPP

This pin has a mask option that provides two different choices of interrupt triggering sensitivity. The IRQ* pin contains an internal Schmitt trigger as part of its input to improve noise immunity. **See Section 4.5, INTERRUPTS for more detail.**

This pin is also used to provide high voltage for programming the personality EPROM. **See Section 8.2, PEPROM PROGRAMMING for more detail.**

1.4.3 OSC1, OSC2

These pins provide control input for an on-chip clock oscillator circuit. A crystal, a ceramic resonator, a resistor/capacitor combination, or an external signal connects to these pins providing a system clock. A mask option selects either a crystal/ceramic resonator or a resistor/capacitor as the frequency determining element. The oscillator frequency is two times the internal bus rate.

1.4.4 RESET*

This active low pin is used to reset the MCU to a known start-up state by pulling RESET* low. The RESET* pin contains an internal Schmitt trigger as part of its input to improve noise immunity.

1.4.5 TCMP

This pin provides an output for the output compare feature of the on-chip timer system.

1.4.6 PA0-PA7

These eight I/O lines comprise port A. The state of any pin is software programmable and all port A lines are configured as inputs during power-on reset. In addition, these pins can be used as keyboard scanners if their interrupts are mask enabled. **See Section 5.1, PORT A for more detail.**

1.4.7 PB5-PB7

These three I/O lines comprise port B. The state of any pin is software programmable and all port B lines are configured as inputs during power-on reset. One of the I/O lines, PB7, has the capability to sink and source high current. **See Section 5.2, PORT B for more detail.**

1.4.8 PC0-PC7

These eight I/O lines comprise port C. The state of any pin is software programmable and all port C lines are configured as inputs during power-on reset. **See Section 5.3, PORT C for more detail.**

1.4.9 PD5, TCAP/PD7

These two bits comprise port D. PD5 is I/O and TCAP/PD7 is input-only shared with the timer input capture. Only the state of PD5 is software programmable and both port D lines are configured as inputs during power-on reset. **See Section 5.4, PORT D for more detail.**

SECTION 2 OPERATING MODES

The MCU has three modes of operation: Single-Chip Mode, Self-Check Mode, and CPU Test Mode. **Test Mode is reserved for factory use only.** Table 2-1: Operating Mode Conditions shows the conditions required to go into either Single-Chip Mode or Self-Check Mode.

Table 2-1: Operating Mode Conditions

RESET	IRQ	PD7/TCAP	MODE
⌐	V_{SS} to V_{DD}	V_{SS} to V_{DD}	Single-Chip
	V_{TST}	V_{DD}	Self-Check

$V_{TST} = 2 \times V_{DD}$

2.1 SINGLE-CHIP MODE

In Single-chip mode, the address and data buses are not available externally, but there are two 8-bit I/O ports, one 3-bit I/O port, and one 2-bit port. This mode allows the MCU to function as a self-contained microcontroller, with maximum use of the pins for on-chip peripheral functions. All address and data activity occurs within the MCU. Single-Chip Mode is entered on the rising edge of RESET* if the IRQ* pin is within normal operating range. RESET* must be held low for 4064 cycles after POR, or for a time t_{RL} for any other reset. See **Figure 9-1: Power-On Reset and RESET**.

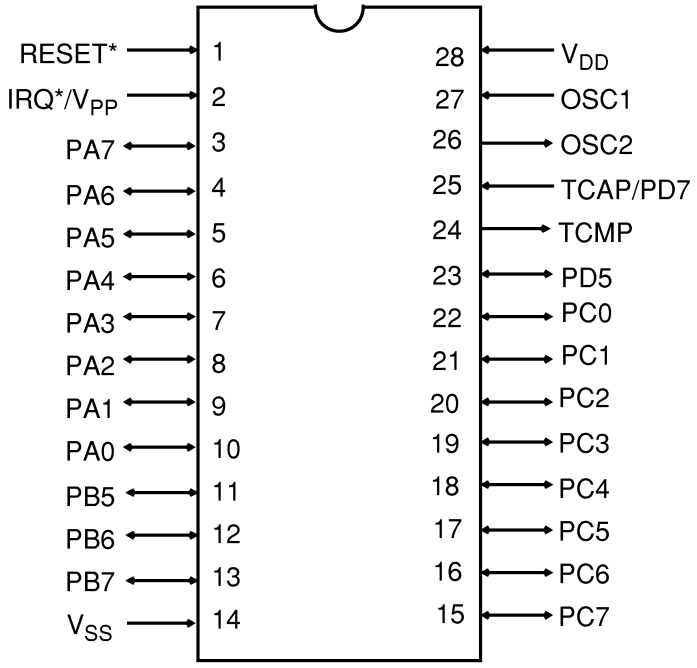


Figure 2-1: Single-Chip Mode Pinout of the MC68HC05PE0

2.2 SELF-CHECK MODE

The Self-Check program resides at mask ROM location $1F00 to $1FEF. This program is designed to check the part's functionality with a minimum of support hardware. **Figure 2-2: MC68HC05PE0 Self-Check Circuit.** The COP subsystem is disabled in the Self-Check Mode.

The Self-Check Mode is entered on the rising edge of RESET* if the IRQ* pin is at V_{TST} and the TCAP/PD7 pin is at logic one. RESET* must be held low for 4064 cycles after POR, or for a time t_{RL} for any other reset. After reset, the I/O, RAM, ROM, Timer, and Personality EPROM are tested. Self-check results (using LEDs as monitors) are shown in **Table 2-2: Self-Check Results.**

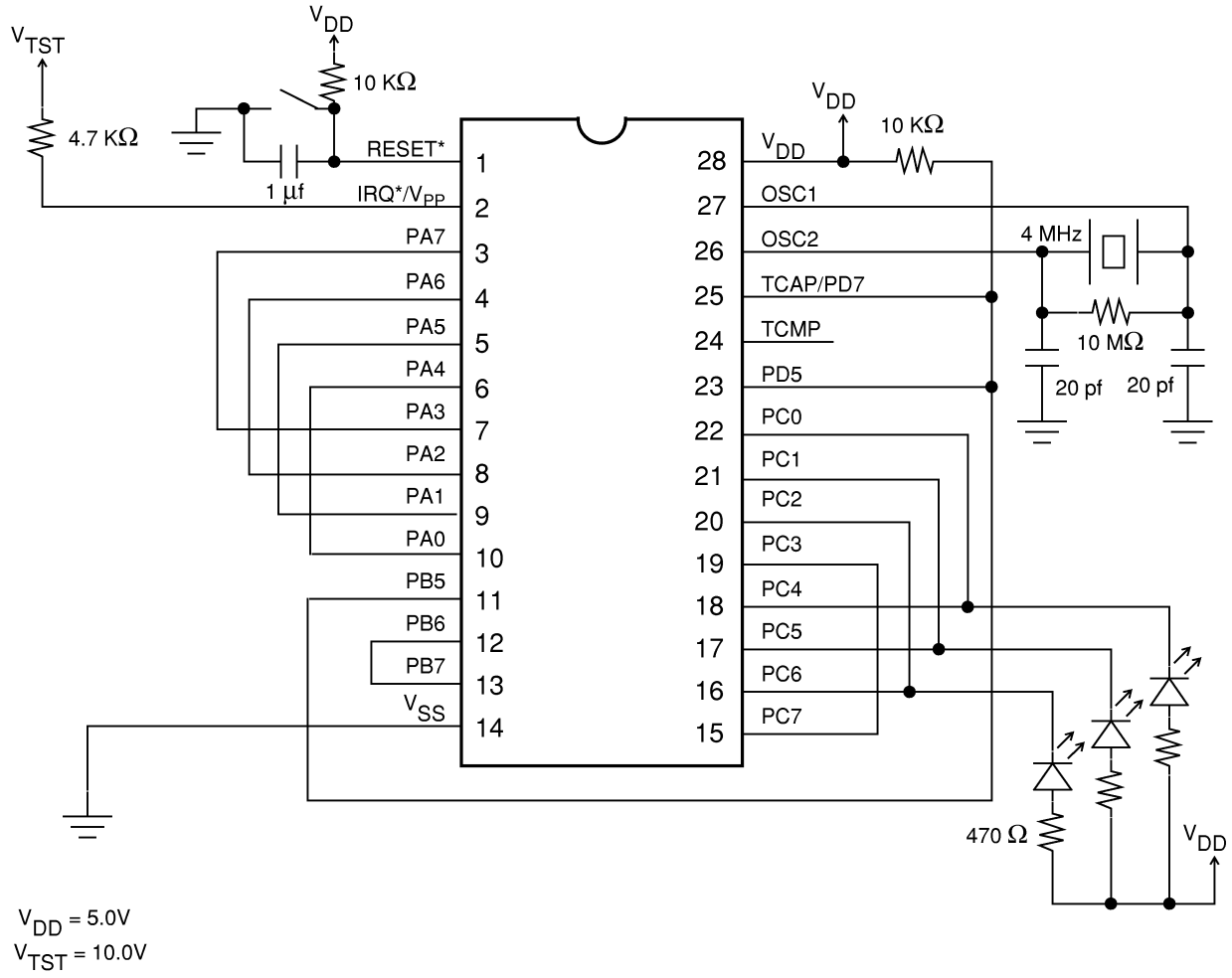


Figure 2-2: MC68HC05PE0 Self-Check Circuit

Table 2-2: Self-Check Results

PC2	PC1	PC0	REMARKS
0	0	1	Bad I/O
0	1	0	Bad RAM
0	1	1	Bad Timer
1	0	0	Bad ROM
1	0	1	Bad PEPROM
Flashing			Good Device
All Others			Bad Device

0 indicates LED is on; 1 indicates LED is off.

SECTION 3 MEMORY

The MC68HC05PE0 has an 8K byte memory map, consisting of user ROM, user RAM, Self-Check ROM, and I/O. See **Figure 3-1: Memory Map** and **Figure 3-2: I/0 Registers.**

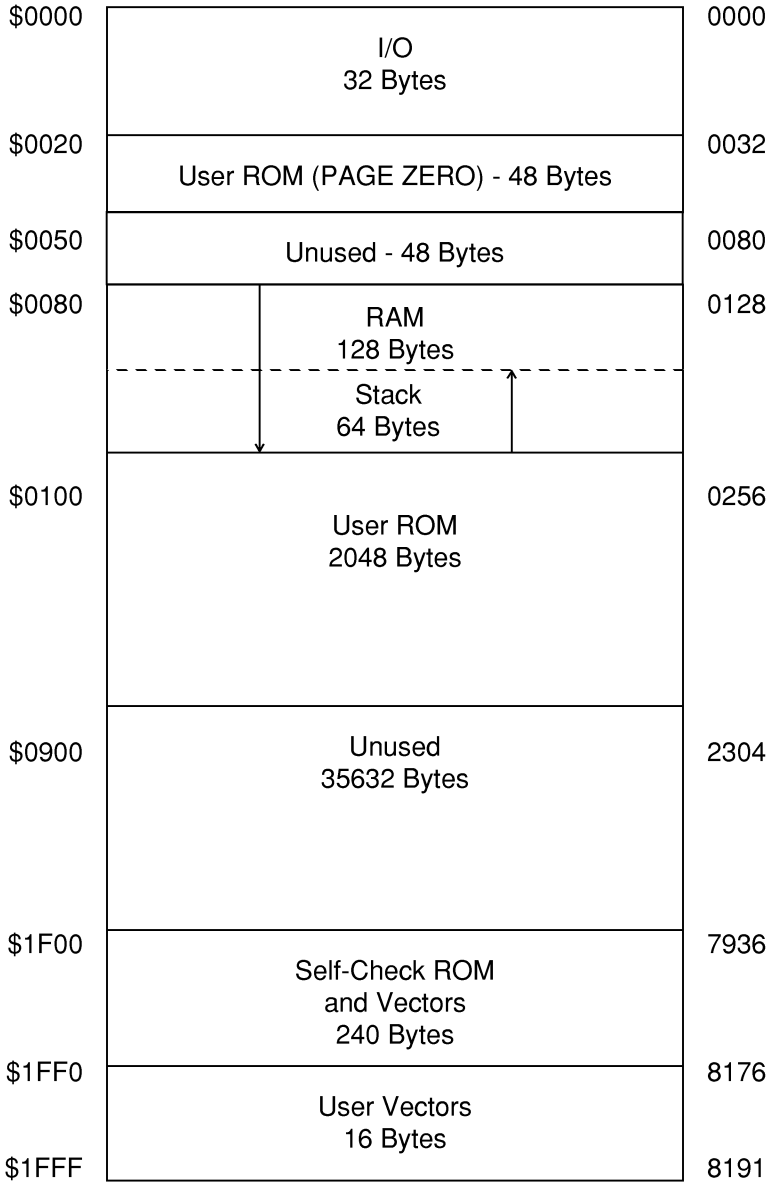


Figure 3-1: Memory Map

3.1 ROM

The user ROM consists of 48 bytes of page zero ROM from $0020 to $004F, 2048 bytes of ROM from $0100 to $08FF and 16 bytes of user vectors from $1FF0 to $1FFF. The Self-Check ROM and vectors are located from $1F00 to $1FEF.

3.2 RAM

The user RAM consists of 128 bytes of a shared stack area. The stack begins at address $00FF. The stack pointer can access 64 bytes of RAM in the range $00FF to $00C0.

NOTE: Using the stack area for data storage or temporary work locations requires care to prevent it from being overwritten due to stacking from an interrupt or subroutine call.

3.3 Personality EPROM

The 64 bits of personality EPROM is not part of the 8K memory map. They are accessible through PEBSR Select Register ($0E) and PECSR Control / Status Register ($0F).

ADDRESS $0000 TO $001F	DATA 7	6	5	4	3	2	1	0
$00 PORT A DATA								
$01 PORT B DATA								
$02 PORT C DATA								
$03 PORT D DATA								
$04 PORT A DDR								
$05 PORT B DDR								
$06 PORT C DDR								
$07 PORT D DDR								
$08 UNUSED								
$09 UNUSED								
$0A UNUSED								
$0B UNUSED								
$0C UNUSED								
$0D UNUSED								
$0E PEP BIT SELECT REGISTER	PEB7	PEB6	COL2	COL1	COL0	ROW2	ROW1	ROW0
$0F PEP CONTROL AND STATUS REGISTER	PEDATA	0	PEPGM	0	-	-	-	PEPRZF
$10 UNUSED								
$11 UNUSED								
$12 TIMER CONTROL REGISTER	ICIE	OCIE	TOIE	0	0	0	IEDG	OLVL
$13 TIMER STATUS REGISTER	ICF	OCF	TOF	0	0	0	0	0
$14TIMER INPUT CAPTURE REG (MSB)	Bit 15							Bit 8
$15 TIMER INPUT CAPTURE REG (LSB)	Bit 7							Bit 0
$16 TIMER OUTPUT COMPARE REG (MSB)	Bit 15							Bit 8
$17 TIMER OUTPUT COMPARE REG (LSB)	Bit 7							Bit 0
$18 TIMER COUNTER REG (MSB)	Bit 15							Bit 8
$19 TIMER COUNTER REG (LSB)	Bit 7							Bit 0
$1A TIMER ALT COUNTER REG (MSB)	Bit 15							Bit 8
$1B TIMER ALT COUNTER REG (LSB)	Bit 7							Bit 0
$1C UNUSED								
$1D UNUSED								
$1E UNUSED								
$1F RESERVED	-	-	-	-	-	-	-	-

Figure 3-2: I/0 Registers

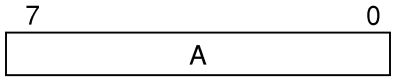
SECTION 4 CPU CORE

4.1 REGISTERS

The MCU contains the registers described in the following paragraphs.

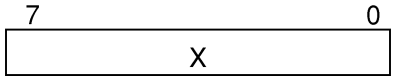
4.1.1 ACCUMULATOR (A)

The accumulator is a general purpose 8-bit register used to hold operands and results of arithmetic calculations or data manipulations.



4.1.2 INDEX REGISTER (X)

The index register is an 8-bit register used for the indexed addressing value to create an effective address. The index register may also be used as a temporary storage area.



4.1.3 CONDITION CODE REGISTER (CCR)

The CCR is a 5-bit register in which four bits are used to indicate the results of the instruction just executed, and the fifth bit indicates whether interrupts are masked. These bits can be individually tested by a program, and specific actions can be taken as a result of their state. Each bit is explained in the following paragraphs.

4.1.3.1 H - HALF CARRY

This bit is set during ADD and ADC operations to indicate that a carry occurred between bits 3 and 4.

4.1.3.2 I - INTERRUPT

When this bit is set, the timer and external interrupt is masked (disabled). If an interrupt occurs while this bit is set, the interrupt is latched and processed as soon as the interrupt bit is cleared.

4.1.3.3 N - NEGATIVE

When set, this bit indicates that the result of the last arithmetic, logical, or data manipulation was negative.

4.1.3.4 Z - ZERO

When set, this bit indicates that the result of the last arithmetic, logical, or data manipulation was zero.

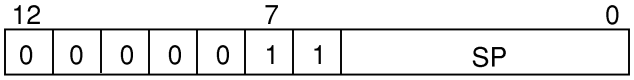
4.1.3.5 C - CARRY/BORROW

When set, this bit indicates that a carry or borrow out of the arithmetic logical unit (ALU) occurred during the last arithmetic operation. This bit is also affected during bit test and branch instructions and during shifts and rotates.

4.1.4 STACK POINTER (SP)

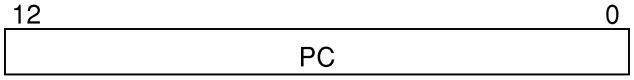
The stack pointer contains the address of the next free location on the stack. During an MCU reset or the reset stack pointer (RSP) instruction, the stack pointer is set to location $00FF. The stack pointer is then decremented as data is pushed onto the stack and incremented as data is pulled from the stack.

When accessing memory, the seven most significant bits are permanently set to 0000011. These seven bits are appended to the six least significant register bits to produce an address within the range of $00FF to $00C0. Subroutines and interrupts may use up to 64 (decimal) locations. If 64 locations are exceeded, the stack pointer wraps around and looses the previously stored information. A subroutine call occupies two locations on the stack; an interrupt uses five locations.



4.1.5 PROGRAM COUNTER (PC)

The program counter is a 13-bit register that contains the address of the next byte to be fetched.



NOTE: The HC05 CPU core is capable of addressing a 64 K byte memory map. For this implementation, however, the addressing registers are limited to an 8 K byte memory map.

4.2 INSTRUCTION SET

The MCU has a set of 62 basic instructions. They can be divided into five different types: register/memory, read-modify-write, branch, bit manipulation, and control. The following paragraphs briefly explain each type. For more information on the instruction set, refer to the M6805 Family User's Manual (M6805UM/AD3) or the MC68HC05C4 Data Sheet (MC68HC05C4/D).

This MCU uses all the instructions available in the M146805 CMOS Family plus one more: the unsigned multiply (MUL) instruction. This instruction allows unsigned multiplication of the contents of the accumulator (A) and the index register (X). The high-order product is then stored in the index register, and the low-order product is stored in the accumulator. A detailed definition of the MUL instruction is shown below.

Operation	X:A X*A			
Description	Multiplies the eight bits in the index register by the eight bits in the accumulator to obtain a 16-bit unsigned number in the concatenated accumulator and index register.			
Condition Codes	H: Cleared I: Not affected N: Not affected Z: Not affected C: Cleared			
Source	MUL			
Form(s)	Addressing Mode Inherent	Cycles 11	Bytes 1	Opcode $42

Figure 4-1: I/0 Registers

4.2.1 REGISTER/MEMORY INSTRUCTIONS

Most of these instructions use two operands. One operand is either the accumulator or the index register. The other operand is obtained from memory using one of the addressing modes. The jump unconditional (JMP) and jump to subroutine (JSR) instructions have no register operand. Refer to the following instruction list.

Function	Mnemonic
Load A from Memory	LDA
Load X from Memory	LDX
Store A in Memory	STA
Store X in Memory	STX
Add Memory to A	ADD
Add Memory and Carry to A	ADC
Subtract Memory	SUB
Subtract Memory from A with Borrow	SBC
AND Memory to A	AND
OR Memory with A	ORA
Exclusive OR Memory with A	EOR
Arithmetic Compare A with Memory	CMP
Arithmetic Compare X with Memory	CPX
Bit Test Memory with A (Logical Compare)	BIT
Jump Unconditional	JMP
Jump to Subroutine	JSR
Multiply	MUL

4.2.2 READ-MODIFY-WRITE INSTRUCTIONS

These instructions read a memory location or a register, modify or test its contents, and write the modified value back to memory or to the register. The test for negative or zero (TST) instruction is an exception to the read-modify-write sequence since it does not modify the value. Refer to the following list of instructions.

Function	Mnemonic
Increment	INC
Decrement	DEC
Clear	CLR
Complement	COM
Negate (Two's Complement)	NEG
Rotate Left Thru Carry	ROL
Rotate Right Thru Carry	ROR
Logical Shift Left	LSL
Logical Shift Right	LSR
Arithmetic Shift Right	ASR
Test for Negative or Zero	TST

4.2.3 BRANCH INSTRUCTIONS

This set of instruction branches if a particular condition is met; otherwise, no operation is performed. Branch instructions are two-byte instructions. Refer to the following list for branch instructions.

Function	Mnemonic
Branch Always	BRA
Branch Never	BRN
Branch if Higher	BHI
Branch if Lower or Same	BLS
Branch if Carry Clear	BCC
Branch if Higher or Same	BHS
Branch if Carry Set	BCS
Branch if Lower	BLO
Branch if Not Equal	BNE
Branch if Equal	BEQ
Branch if Half Carry Clear	BHCC
Branch if Half Carry Set	BHCS
Branch if Plus	BPL
Branch if Minus	BMI
Branch if Interrupt Mask Bit is Clear	BMC
Branch if Interrupt Mask Bit is Set	BMS
Branch if Interrupt Line is Low	BIL
Branch if Interrupt Line is High	BIH
Branch to Subroutine	BSR

4.2.4 BIT MANIPULATION INSTRUCTIONS

The MCU is capable of setting or clearing any writable bit which resides in the first 256 bytes of the memory space where all port registers, port DDRs, timer, timer control, EEPROM, and on-chip RAM reside. An additional feature allows the software to test and branch on the state of any bit within these 256 locations. The bit set, bit clear and bit test, and branch functions are all implemented with a single instruction. For test and branch instructions, the value of the bit tested is also placed in the carry bit of the condition code register. These instructions are also read-modify-write instructions. Do not bit manipulate write-only locations. Refer to the following list for bit manipulation instructions.

Function	Mnemonic
Branch if Bit n is Set	BRSET n (n = 0. . .7)
Branch if bit n is Clear	BRCLR n (n = 0. . .7)
Set Bit n	BSET n (n = 0. . .7)
Clear Bit n	BCLR n (n = 0. . .7)

4.2.5 CONTROL INSTRUCTIONS

These instructions are register reference instructions and are used to control processor operation during program execution. Refer to the following list for control instructions.

Function	Mnemonic
Transfer A to X	TAX
Transfer X to A	TXA
Set Carry Bit	SEC
Clear Carry Bit	CLC
Set Interrupt Mask Bit	SEI
Clear Interrupt Mask Bit	CLI
Software Interrupt	SWI
Return from Subroutine	RTS
Return from Interrupt	RTI
Reset Stack Pointer	RSP
No-Operation	NOP
Stop	STOP
Wait	WAIT

4.3 ADDRESSING MODES

The MCU uses ten different addressing modes to provide the programmer with an opportunity to optimize the code for all situations. The various indexed addressing modes make it possible to locate data tables, code conversion tables, and scaling tables anywhere in the memory space. Short indexed accesses are single byte instructions; the

longest instructions (three bytes) permit accessing tables throughout memory. Short and long absolute addressing is also included. One- or two-byte direct addressing instructions access all data bytes in most applications. Extended addressing permits jump instructions to reach all memory.

The term “effective address” (EA) is used in describing the various addressing modes. Effective address is defined as the address from which the argument for an instruction is fetched or stored.

4.3.1 IMMEDIATE

In the immediate addressing mode, the operand is contained in the byte immediately following the opcode. The immediate addressing mode is used to access constants that do not change during program execution (e.g., a constant used to initialize a loop counter).

4.3.2 DIRECT

In the direct addressing mode, the effective address of the argument is contained in a single byte following the opcode byte. Direct addressing allows the user to directly address the lowest 256 bytes in memory with a single two-byte instruction.

4.3.3 EXTENDED

In the extended addressing mode, the effective address of the argument is contained in the two bytes following the opcode byte. Instructions with extended addressing mode are capable of referencing arguments anywhere in memory with a single three-byte instruction. When using the Motorola assembler, the user need not specify whether an instruction uses direct or extended addressing. The assembler automatically selects the shortest form of the instruction.

4.3.4 RELATIVE

The relative addressing mode is only used in branch instructions. In relative addressing, the contents of the 8-bit signed byte (the offset) following the opcode is added to the PC if, and only if, the branch conditions are true. Otherwise, control proceeds to the next instruction. The span of relative addressing is from -126 to +129 from the opcode address. The programmer need not calculate the offset when using the Motorola assembler, since it calculates the proper offset and checks to see that it is within the span of the branch.

4.3.5 INDEXED, NO OFFSET

In the indexed, no offset addressing mode, the effective address of the argument is contained in the 8-bit index register. This addressing mode can access the first 256 memory locations. These instructions are only one byte long. This mode is often used to move a pointer through a table or to hold the address of a frequently referenced RAM or I/O location.

4.3.6 INDEXED, 8-BIT OFFSET

In the indexed, 8-bit offset addressing mode, the effective address is the sum of the contents of the unsigned 8-bit index register and the unsigned byte following the opcode.

The addressing mode is useful for selecting the Kth element in an n element table. With this two-byte instruction, K would typically be in X with the address of the beginning of the table in the instruction. As such, tables may begin anywhere within the first 256 addressable locations and could extend as far as location 510 ($1FE is the last location at which the instruction may begin).

4.3.7 INDEXED, 16-BIT OFFSET

In the indexed, 16-bit offset addressing mode, the effective address is the sum of the contents of the unsigned 8-bit index register and the two unsigned bytes following the opcode. This address mode can be used in a manner similar to indexed, 8-bit offset except that this three-byte instruction allows tables to be anywhere in memory. As with direct and extended addressing, the Motorola assembler determines the shortest form of indexed addressing.

4.3.8 BIT SET/CLEAR

In the bit set/clear addressing mode, the bit to be set or cleared is part of the opcode, and the byte following the opcode specifies the direct addressing of the byte in which the specified bit is to be set or cleared. Any read/write bit in the first 256 locations of memory, including I/O, can be selectively set or cleared with a single two-byte instruction.

4.3.9 BIT TEST AND BRANCH

The bit test and branch addressing mode is a combination of direct addressing and relative addressing. The bit that is to be tested and its condition (set or clear) is included in the opcode. The address of the byte to be tested is in the single byte immediately following the opcode byte. The signed relative 8-bit offset in the third byte is added to the PC if the specified bit is set or cleared in the specified memory location. This single three-byte instruction allows the program to branch based on the condition of any readable bit in the first 256 locations of memory. The span of branching is from -125 to +130 from the opcode address. The state of the tested bit is also transferred to the carry bit of the condition code register.

4.3.10 INHERENT

In the inherent addressing mode, all the information necessary to execute the instruction is contained in the opcode. Operations specifying only the index register or accumulator as well as the control instruction with no other arguments are included in this mode. These instructions are one byte long.

4.4 RESETS

The MCU can be reset three ways: by the initial power-on reset function, by an active low input to the RESET* pin, and by a computer operating properly (COP) watchdog-timer time-out.

4.4.1 POWER-ON RESET (POR)

An internal reset is generated on power-up to allow the internal clock generator to stabilize. The power-on reset is strictly for power turn-on conditions and should not be

used to detect a drop in the power supply voltage. There is a 4064 internal processor clock cycle (t_{cyc}) oscillator stabilization delay after the oscillator becomes active. If the RESET* pin is low at the end of this 4064 cycle delay, the MCU will remain in the reset condition until RESET* goes high.

4.4.2 RESET* PIN

The MCU is reset when a logic zero is applied to the RESET* input for a period of one and one-half machine cycles (t_{cyc}).

4.4.3 COMPUTER OPERATING PROPERLY (COP) RESET

The MCU contains a watchdog timer that automatically times out if not reset (cleared) within a specific time by a program reset sequence. If the COP watchdog timer is allowed to time-out, an internal reset is generated to reset the MCU. Because the internal RESET* signal is used, the MCU comes out of a COP reset in the same operating mode it was in when the COP time-out was generated.

The COP reset function is enabled or disabled by a mask option.

See SECTION 7, COP - COMPUTER OPERATING PROPERLY for more details.

4.5 INTERRUPTS

The MCU can be interrupted in four different ways: the ten maskable hardware interrupts (IRQ*, timer and each eight I/O lines of port A) and the nonmaskable software interrupt instruction (SWI).

Interrupts cause the processor to save register contents on the stack and to set the interrupt mask (I bit) to prevent additional interrupts. The RTI instruction causes the register contents to be recovered from the stack and normal processing to resume.

Unlike RESET*, hardware interrupts do not cause the current instruction execution to be halted, but are considered pending until the current instruction is complete.

NOTE: The current instruction is the one already fetched and being operated on.

When the current instruction is complete, the processor checks all pending hardware interrupts. If interrupts are not masked (CCR I bit clear) and if the corresponding interrupt enable bit is set, the processor proceeds with interrupt processing; otherwise, the next instruction is fetched and executed.

If both an external interrupt and a timer interrupt are pending at the end of an instruction execution, the external interrupt is serviced first. The SWI is executed the same as any other instruction, regardless of the I-bit state.

Table 4-1: Vector Address for Interrupts and Reset

Register	Flag Name	Interrupts	CPU Interrupt	Vector Address
N/A	N/A	Reset	RESET*	$1FFE-$1FFF
N/A	N/A	Software	SWI	$1FFC-$1FFD
N/A	N/A	External Interrupt	IRQ*	$1FFA-$1FFB
TSR	ICF	Timer Input Capture	TIMER	$1FF8-$1FF9
TSR	OCF	Timer Output Compare	TIMER	$1FF8-$1FF9
TSR	TOF	Timer Overflow	TIMER	$1FF8-$1FF9

4.5.1 HARDWARE CONTROLLED INTERRUPT SEQUENCE

The following three functions (RESET*, STOP, and WAIT) are not in the strictest sense an interrupt; however, they are acted upon in a similar manner. **Figure 4-2: Hardware Interrupt Flowchart** and **Figure 4-5: STOP/WAIT Flowcharts**. A discussion is provided below.

1. RESET* - A low input on the RESET* input pin causes the program to vector to its starting address which is specified by the contents of memory location $1FFE and $1FFF. The I bit in the condition code register is also set. Much of the MCU is configured to a known state during this type of reset as previously described in **SECTION 4.4, RESETS**.
2. STOP - The STOP instruction causes the oscillator to be turned off and the processor to “sleep” until an external interrupt (IRQ*) or reset occurs.
3. WAIT - The WAIT instruction causes all processor clocks to stop, but leaves the timer clock running. This “rest” state of the processor can be cleared by reset, an external interrupt (IRQ*), or Timer interrupt. There are no special wait vectors for these individual interrupts.

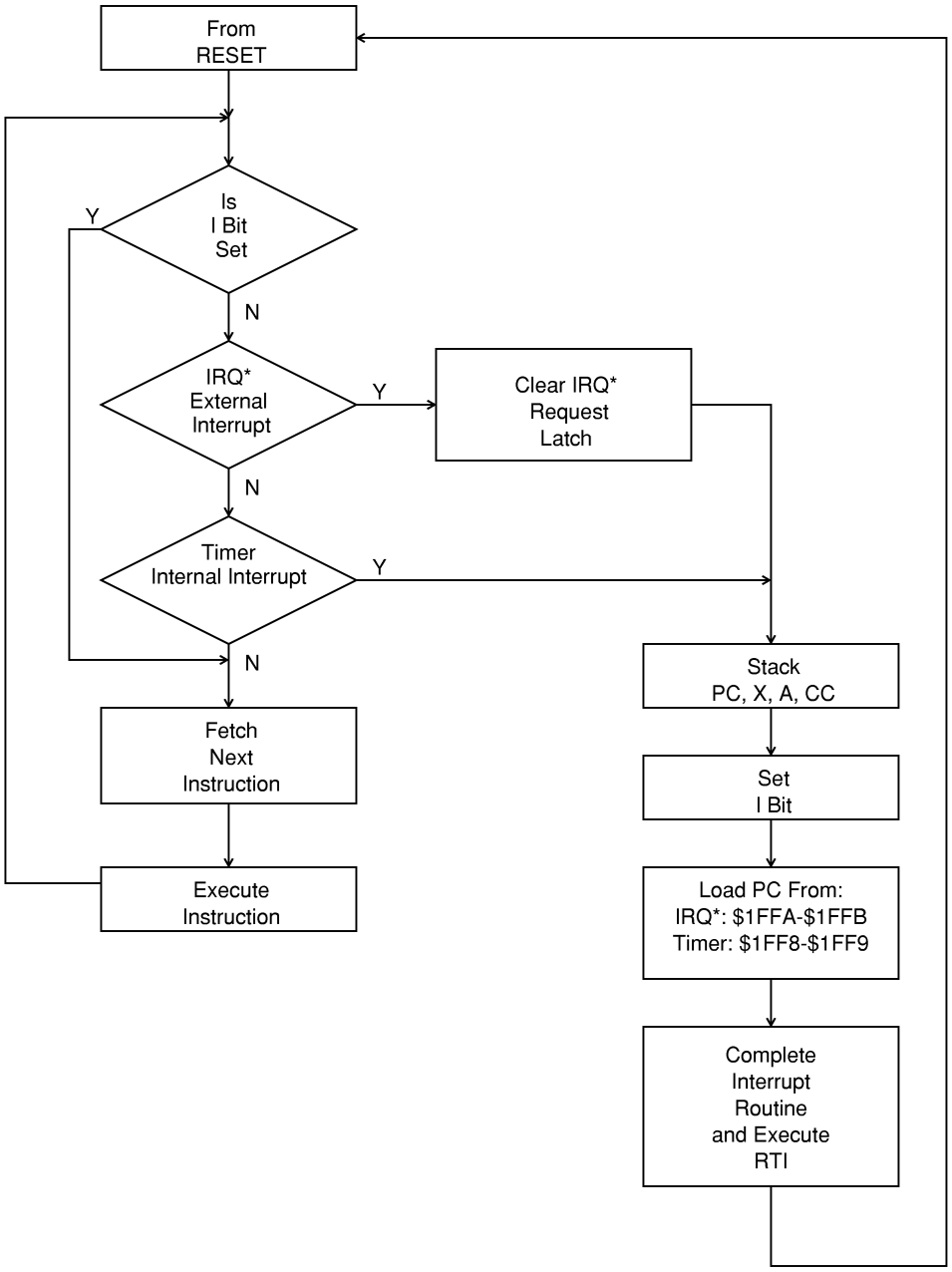


Figure 4-2: Hardware Interrupt Flowchart

4.5.2 TIMER INTERRUPT

There are three different timer interrupt flags that cause a timer interrupt whenever they are set and enabled. The interrupt flags are in the Timer Status Register (TSR), and the enable bits are in the Timer Control Register (TCR). Any of these interrupts will vector to the same interrupt service routine, located at the address specified by the contents of memory location $1FF8 and $1FF9.

4.5.3 EXTERNAL INTERRUPT

If the interrupt mask bit (I bit) of the CCR is set, all maskable interrupts (internal and external) are disabled. Clearing the I bit enables interrupts. The interrupt request is latched immediately following the falling edge of IRQ*. It is then synchronized internally and serviced as specified by the contents of $1FFA and $1FFB.

Either a level-sensitive and edge-sensitive trigger, or an edge-sensitive-only trigger is available as a mask option.

NOTE: The internal interrupt latch is cleared in the first part of the interrupt service routine; therefore, another external interrupt pulse could be latched and serviced as soon as the I bit is cleared.

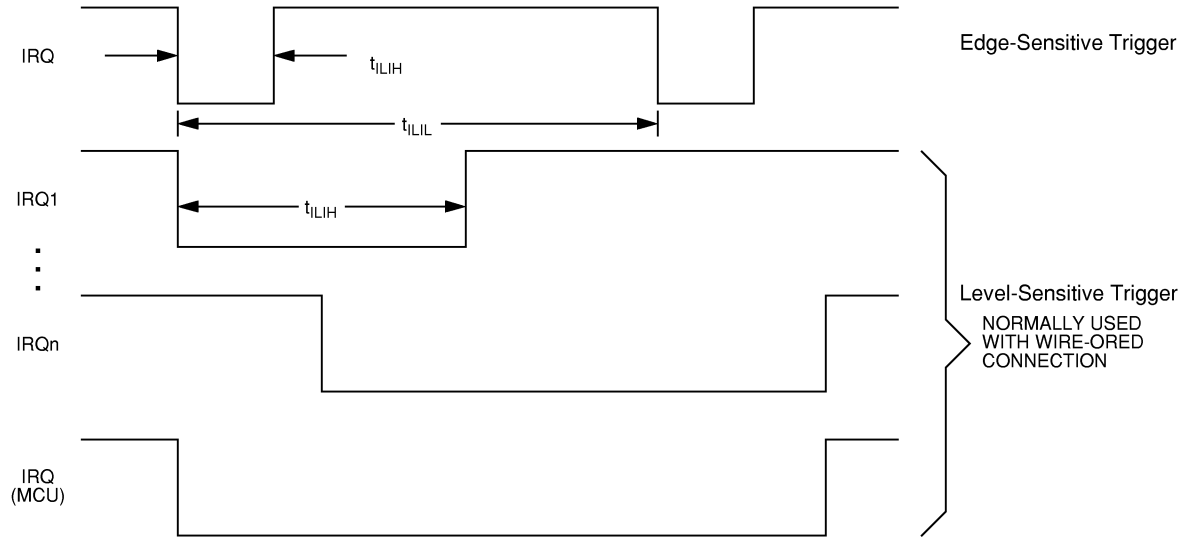


Figure 4-3: External Interrupt Timing

4.5.4 PORT A INTERRUPTS

Each I/O line of port A can cause an interrupt if it is selected as a mask option. The interrupts are shared with IRQ* internally. Therefore, they act like an external interrupt. All of **Section 4.5.3, EXTERNAL INTERRUPT** also applies for port A interrupts.

4.5.5 SOFTWARE INTERRUPT (SWI)

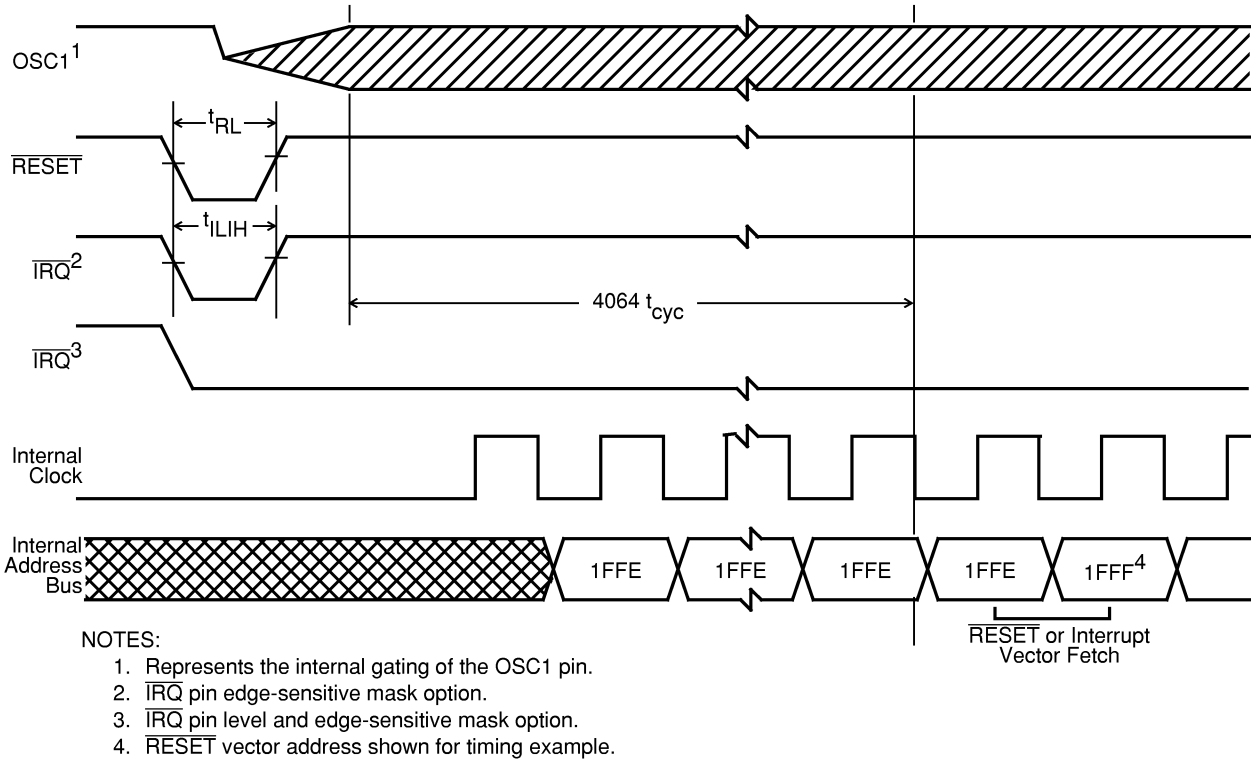
The SWI is an executable instruction and a non-maskable interrupt: it is executed regardless of the state of the I bit in the CCR. If the I bit is zero (interrupts enabled), SWI executes after interrupts which were pending when the SWI was fetched, but before interrupts generated after the SWI was fetched. The interrupt service routine address is specified by the contents of memory locations $1FFC and $1FFD.

4.6 LOW-POWER MODES

4.6.1 STOP

The STOP instruction places the MCU in its lowest power consumption mode. In STOP mode, the internal oscillator is turned off, halting all internal processing, including timer (and COP Watchdog timer) operation.

During STOP mode, the input capture, output compare and overflow interrupt enable bits in TCR ($12) are cleared to remove any pending timer interrupt request and to disable any further timer interrupts. The timer prescaler is cleared. The I bit in the CCR is cleared to enable external interrupts. All other registers and memory remain unaltered. All input/output lines remain unchanged. The processor can be brought out of the STOP mode only by an external interrupt or reset.



NOTES:
1. Represents the internal gating of the OSC1 pin.
2. $\overline{IRQ}$ pin edge-sensitive mask option.
3. $\overline{IRQ}$ pin level and edge-sensitive mask option.
4. $\overline{RESET}$ vector address shown for timing example.

Figure 4-4: STOP Recovery Timing

4.6.2 WAIT

The WAIT instruction places the MCU in a low-power consumption mode, but the WAIT mode consumes more power than the STOP mode. All CPU action is suspended, but the timer and the oscillator remain active. Any interrupt or reset (including a COP reset) will cause the MCU to exit the WAIT mode.

During the WAIT mode, the I bit in the CCR is cleared to enable interrupts. All other registers, memory, and input/output lines remain in their previous state. The timer may be enabled to allow a periodic exit from the WAIT mode. WAIT mode must be exited and the COP must be reset to prevent a COP timeout.

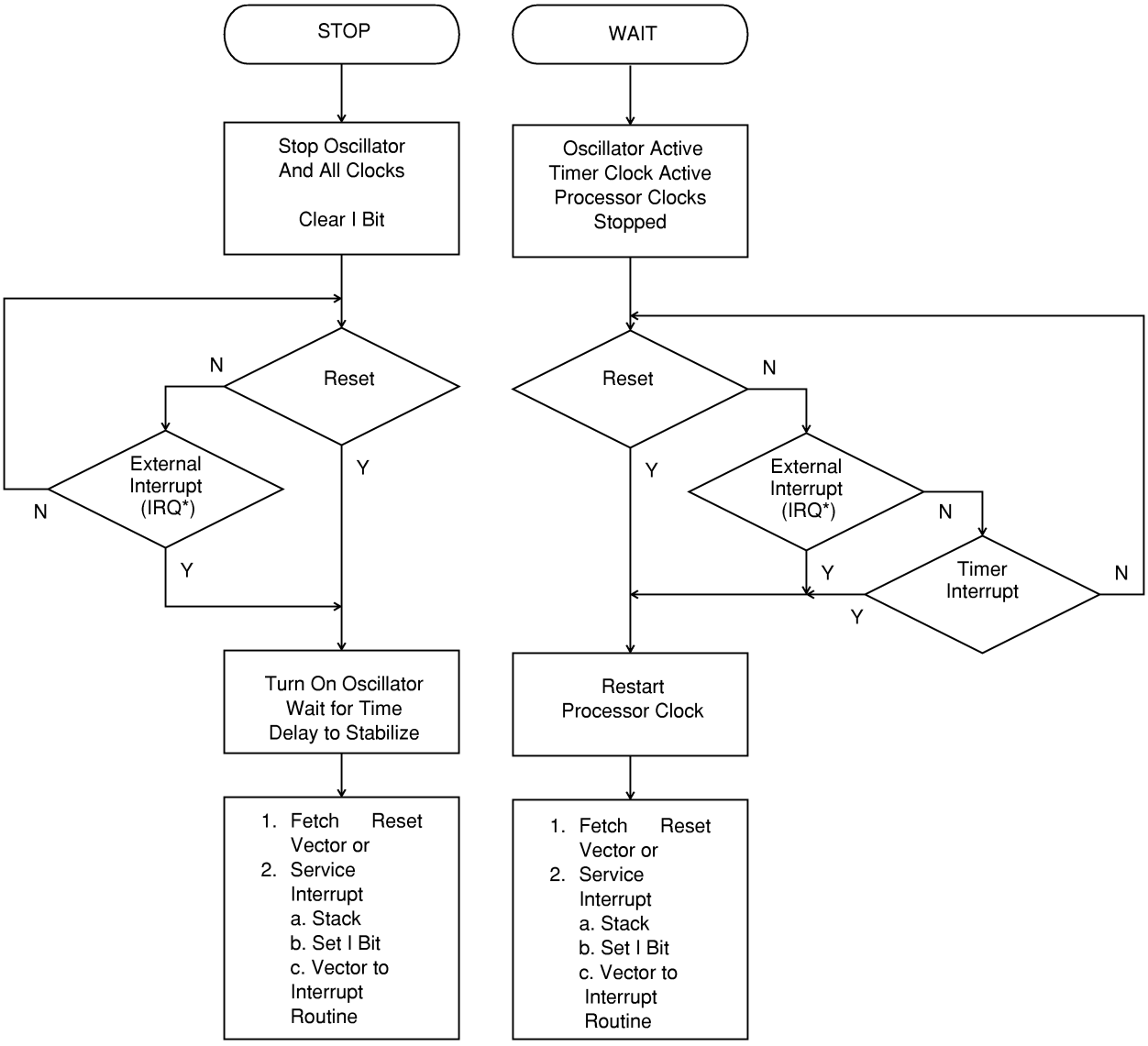


Figure 4-5: STOP/WAIT Flowcharts

SECTION 5 INPUT/OUTPUT PORTS

In Single-Chip mode, there are 21 lines arranged as two 8-bit I/O ports, one 3-bit I/O port, and one 1-bit I/O and 1-bit input port. These ports are programmable as either inputs or outputs under software control of the data direction registers.

NOTE: To avoid a glitch on the output pins, write data to the I/O Port Data Register before writing a one to the corresponding Data Direction Register.

5.1 PORT A

Port A is an 8-bit bidirectional port. The port A data register is at $0000 and the data direction register (DDR) is at $0004. Reset does not affect the data registers, but clears the data direction registers, thereby returning the ports to inputs. Writing a one to a DDR bit sets the corresponding port bit to output mode.

Each Port A pin has an optional pullup device that can be enabled with a mask option. When the pullup device is enabled, this pin will become an interrupt pin. The edge or edge and level sensitivity of the $\overline{IRQ}$ pin will pertain to the enabled Port A pins. See **Section 4.5.3, EXTERNAL INTERRUPT** and **Section 4.5.4, PORT A INTERRUPTS** for more details.

NOTE: To avoid any accidental interrupts when switching from output to input mode, precondition the data in the data register to 1.

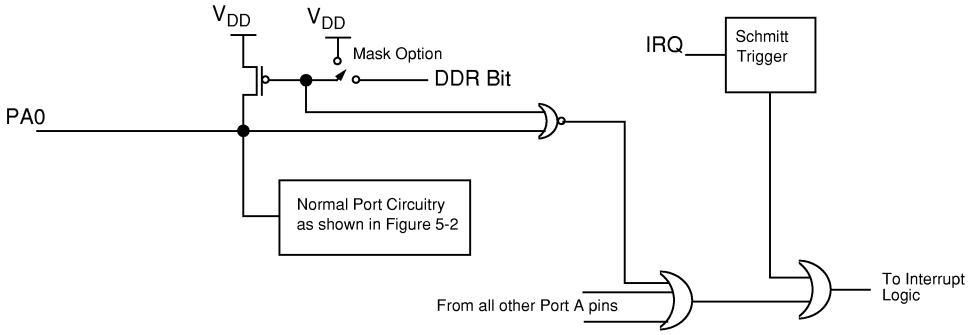


Figure 5-1: Port A Pullup Option

5.2 PORT B

Port B is a 3-bit bidirectional port. The address of the port B data register is $0001 and the data direction register (DDR) is at address $0005. Reset does not affect the data registers, but clears the data direction registers, thereby returning the ports to inputs. Writing a one to a DDR bit sets the corresponding port bit to output mode.

PB7 is capable of sinking and sourcing high current. See **Sections 9.3** and **9.4** concerning DC electrical characteristics.

5.3 PORT C

Port C is an 8-bit bidirectional port. The address of the port C data register is $0002 and the data direction register (DDR) is at address $0006. Reset does not affect the data registers, but clears the data direction registers, thereby returning the ports to inputs. Writing a one to a DDR bit sets the corresponding port bit to output mode.

5.4 PORT D

Port D is a 2-bit port. PD5 is an I/O pin and TCAP/PD7 is an input only pin. The address of the port D data register is $0003 and the data direction register (DDR) is at address $0007. Reset does not affect the data registers, but clears the data direction registers, thereby returning the ports to inputs. Writing a one to a DDR bit sets the corresponding port bit to output mode. TCAP/PD7 pin controls the input capture feature for the on-chip programmable time. This pin can be read at any time even if the TCAP function is enabled.

5.5 INPUT/OUTPUT PROGRAMMING

Each bit of ports A, B, and C can be programmed as an input or an output under software control. The direction of the pins is determined by the state of the corresponding bit in the port data direction register (DDR). Each port has an associated DDR. Any port pin is configured as an output if its corresponding DDR bit is set to a one. A pin is configured as an input if its corresponding DDR bit is cleared to a zero.

At power-on or reset, all DDRs are cleared, which configures all port A, B, and C pins as inputs. The data direction registers are capable of being written to or read by the processor. During the programmed output state, a read of the data register actually reads the value of the output data latch and not the I/O pin. See **Table 5-1: I/O Pin Functions** and **Figure 5-2: Port I/O Circuitry**.

Table 5-1: I/O Pin Functions

R/W*	DDR	I/O Pin Function
0	0	The I/O pin is in input mode. Data is written into the output data latch.
0	1	Data is written into the output data latch and output of the I/O pin.
1	0	The state of the I/O pin is read.
1	1	The I/O pin is in an output mode. The output data latch is read.

R/W is an internal signal.

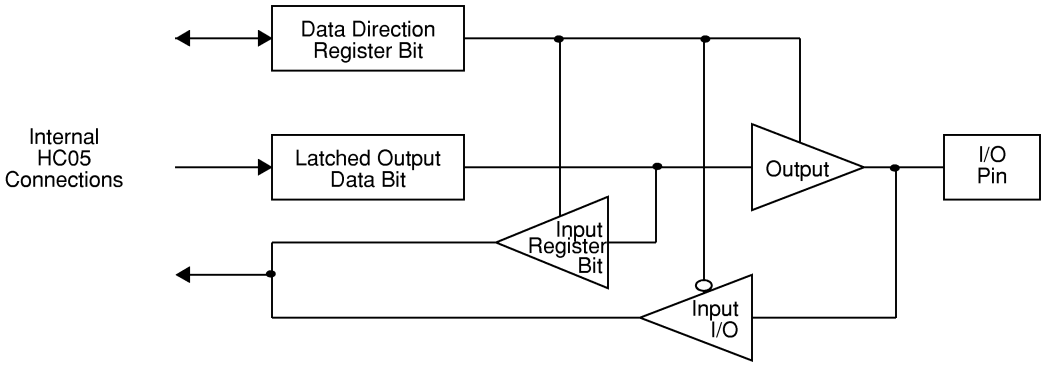


Figure 5-2: Port I/O Circuitry

SECTION 6 TIMER

The timer consists of a 16-bit, software-programmable counter driven by a fixed divide-by-four prescaler. This timer can be used for many purposes, including input waveform measurements while simultaneously generating an output waveform. Pulse widths can vary from several microseconds to many seconds. Refer to **Figure 6-1** for a timer block diagram.

Because the timer has a 16-bit architecture, each specific functional segment (capability) is represented by two registers. These registers contain the high and low byte of that functional segment. Generally, accessing the low byte of a specific timer function allows full control of that function; however, an access of the high byte inhibits that specific timer function until the low byte is also accessed.

NOTE: Note: The I bit in the CCR should be set while manipulating both the high and low byte register of a specific timer function to ensure that an interrupt does not occur.

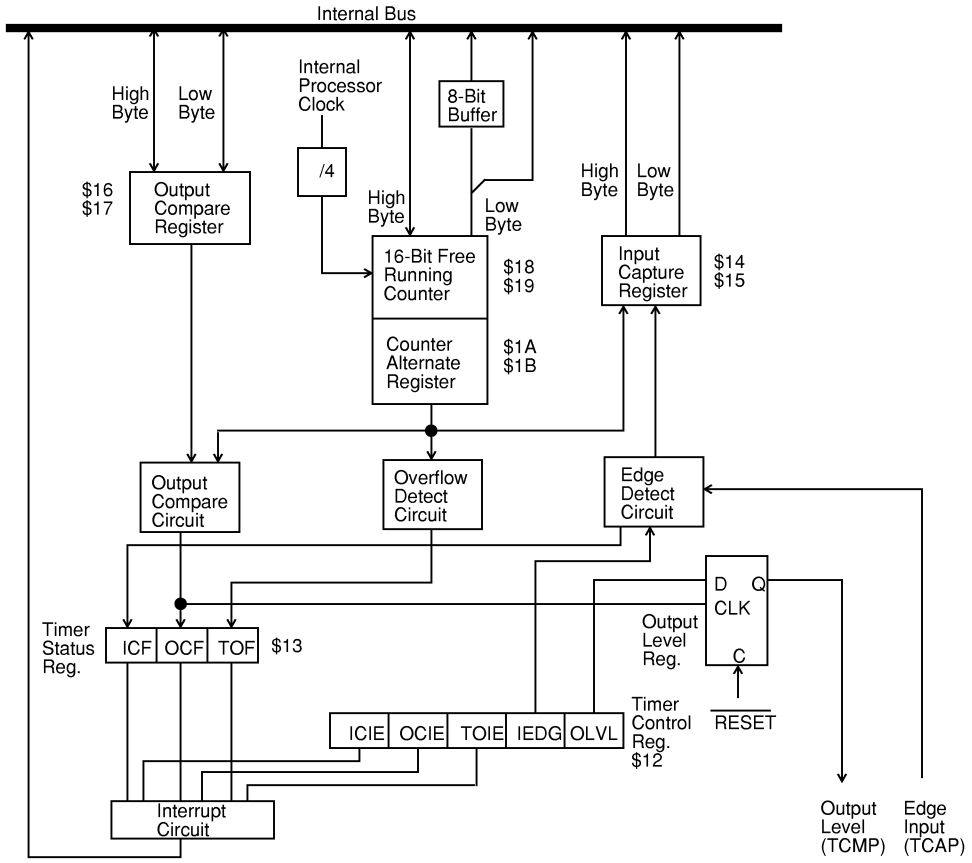


Figure 6-1: Timer Block Diagram

6.1 COUNTER - $18:$19, $1A:$1B

The key element in the programmable timer is a 16-bit, free-running counter or counter register, preceded by a prescaler that divides the internal processor clock by four. The prescaler gives the timer a resolution of 2.0 microseconds if the internal bus clock is 2.0 MHz. The counter is incremented during the low portion of the internal bus clock. Software can read the counter at any time without affecting its value.

The double-byte, free-running counter can be read from either of two locations, $18-$19 (counter register) or $1A-$1B (counter alternate register). A read from only the least significant byte (LSB) of the free-running counter ($19, $1B) receives the count value at the time of the read. If a read of the free-running counter or counter alternate register first addresses the most significant byte (MSB) ($18, $1A), the LSB ($19, $1B) is transferred to a buffer. This buffer value remains fixed after the first MSB read, even if the user reads the MSB several times. This buffer is accessed when reading the free-running counter or counter alternate register LSB ($19 or $1B) and, thus, completes a read sequence of the total counter value. In reading either the free-running counter or counter alternate register, if the MSB is read, the LSB must also be read to complete the sequence.

The counter alternate register differs from the counter register in one respect: a read of the counter register MSB can clear the timer overflow flag (TOF). Therefore, the counter alternate register can be read at any time without the possibility of missing timer overflow interrupts due to clearing of the TOF.

The free-running counter is configured to $FFFC during reset and is always a read-only register. During a power-on reset, the counter is also preset to $FFFC and begins running after the oscillator start-up delay. Because the free-running counter is 16 bits preceded by a fixed divided-by-four prescaler, the value in the free-running counter repeats every 262,144 internal bus clock cycles. When the counter rolls over from $FFFF to $0000, the TOF bit is set. An interrupt can also be enabled when counter rollover occurs by setting its interrupt enable bit (TOIE).

6.2 OUTPUT COMPARE REGISTER -$16:$17

The 16-bit output compare register is made up of two 8-bit registers at locations $16 (MSB) and $17 (LSB). The output compare register is used for several purposes, such as indicating when a period of time has elapsed. All bits are readable and writable and are not altered by the timer hardware or reset. If the compare function is not needed, the two bytes of the output compare register can be used as storage locations.

The output compare register contents are compared with the contents of the free-running counter continually, and if a match is found, the corresponding output compare flag (OCF) bit is set and the corresponding output level (OLVL) bit is clocked to an output level register. The output compare register values and the output level bit should be changed after each successful comparison to establish a new elapsed timeout. An interrupt can also accompany a successful output compare provided the corresponding interrupt enable bit (OCIE) is set.

After a processor write cycle to the output compare register containing the MSB ($16), the output compare function is inhibited until the LSB ($17) is also written. The user must write both bytes (locations) if the MSB is written first. A write made only to the LSB ($17) will not inhibit the compare function. The free-running counter is updated every four internal bus clock cycles. The minimum time required to update the output compare register is a function of the program rather than the internal hardware.

The processor can write to either byte of the output compare register without affecting the other byte. The output level (OLVL) bit is clocked to the output level register regardless of whether the output compare flag (OCF) is set or clear.

6.3 INPUT CAPTURE REGISTER - $14:$15

Two 8-bit registers, which make up the 16-bit input capture register, are read-only and are used to latch the value of the free-running counter after the corresponding input capture edge detector senses a defined transition. The level transition which triggers the counter transfer is defined by the corresponding input edge bit (IEDG). Reset does not affect the contents of the input capture register.

The result obtained by an input capture will be one more than the value of the free-running counter on the rising edge of the internal bus clock preceding the external transition. This delay is required for internal synchronization. Resolution is one count of the free-running counter, which is four internal bus clock cycles.

The free-running counter contents are transferred to the input capture register on each proper signal transition regardless of whether the input capture flag (ICF) is set or clear. The input capture register always contains the free-running counter value that corresponds to the most recent input capture.

After a read of the input capture register ($14) MSB, the counter transfer is inhibited until the LSB ($15) is also read. This characteristic causes the time used in the input capture software routine and its interaction with the main program to determine the minimum pulse period.

A read of the input capture register LSB ($15) does not inhibit the free-running counter transfer since they occur on opposite edges of the internal bus clock.

6.4 TIMER CONTROL REGISTER (TCR) $12

The TCR is a read/write register containing five control bits. Three bits control interrupts associated with the timer status register flags ICF, OCF and TOF.

$12	ICIE	OCIE	TOIE	0	0	0	IEDG	OLVL
RESET:	0	0	0	0	0	0	U	0

Figure 6-2: Timer Control Register

6.4.1 ICIE - Input Capture Interrupt Enable

1 = Interrupt enabled
0 = Interrupt disabled

6.4.2 OCIE - Output Compare Interrupt Enable

1 = Interrupt enabled
0 = Interrupt disabled

6.4.3 TOIE - Timer Overflow Interrupt Enable

1 = Interrupt enabled
0 = Interrupt disabled

6.4.4 IEDG - Input Edge

Value of input edge determines which level transition on TCAP pin will trigger free-running counter transfer to the input capture register.

1 = Positive edge
0 = Negative edge

Reset does not affect the IEDG bit (U=unaffected).

6.4.5 OLVL - Output Level

Value of output level is clocked into output level register by the next successful output compare and will appear on the TCMP pin.

1 = High output
0 = Low output

6.4.6 Bits 2, 3 and 4 - Not used

Always read zero

6.5 TIMER STATUS REGISTER (TSR) $13

The TSR is a read-only register containing three status flag bits.

$13	ICF	OCF	TOF	0	0	0	0	0
RESET:	U	U	U	0	0	0	0	0

Figure 6-3: Timer Status Register

6.5.1 ICF - Input Capture Flag

1 = Flag set when selected polarity edge is sensed by input capture edge detector
0 = Flag cleared when TSR and input capture low register ($15) are accessed

6.5.2 OCF - Output Compare Flag

1 = Flag set when output compare register contents match the free-running counter contents
0 = Flag cleared when TSR and output compare low register ($17) are accessed

6.5.3 TOF - Timer Overflow Flag

1 = Flag set when free-running counter transition from $FFFF to $0000 occurs
0 = Flag cleared when TSR and counter low register ($19) are accessed

6.5.4 Bits 0-4 - Not used

Always read zero

Accessing the timer status register satisfies the first condition required to clear status bits. The remaining step is to access the register corresponding to the status bit.

A problem can occur when using the timer overflow function and reading the free-running counter at random times to measure an elapsed time. Without incorporating the proper precautions into software, the timer overflow flag could unintentionally be cleared if:

1) The timer status register is read or written when TOF is set, and
2) The LSB of the free-running counter is read but not for the purpose of servicing the flag.

The counter alternate register at address $1A and $1B contains the same value as the free-running counter (at address $18 and $19); therefore, this alternate register can be read at any time without affecting the timer overflow flag in the timer status register.

6.6 TIMER DURING WAIT MODE

The CPU clock halts during the WAIT mode, but the timer remains active. If interrupts are enabled, a timer interrupt will cause the processor to exit the WAIT mode.

6.7 TIMER DURING STOP MODE

In STOP mode, all interrupt enable bits including input capture, output compare and timer overflow in TCR ($12) are cleared to remove any pending timer interrupt request and to disable any further timer interrupts.

The timer stops counting and holds the last count value when STOP mode is entered. If STOP is exited by IRQ*, the timer resumes counting from the previous count value saved before STOP was entered. If RESET is used, the timer starts counting from $FFFC.

During STOP, if at least one valid input capture edge occurs at the TCAP pin, the input capture detect circuit is armed. This does not set any timer flags nor wake up the MCU. If IRQ* wakes up the MCU, the input capture flag is set. If RESET is used to exit STOP mode, then input capture flag is cleared.

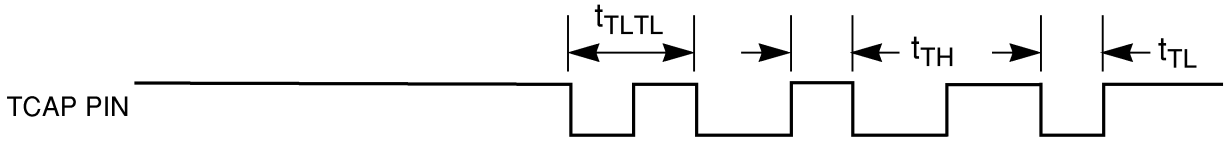


Figure 6-4: TCAP Timing

SECTION 7 COP - COMPUTER OPERATING PROPERLY

This device includes a “Watchdog” COP feature as a mask option. The COP is implemented with an 18-bit ripple counter. This provides a timeout period of 64 milliseconds at a bus rate of 2 MHz. If the COP should timeout, a system reset will occur and the device will be re-initialized in the same fashion as a POR or external Reset. See **Figure 1-1: Block Diagram**.

7.1 RESETTING THE COP

Preventing a COP reset is done by writing a “0” to the COPF bit. This action will reset the counter and begin the timeout period again. The COPF bit is bit 0 of address $1FF0. A read of address $1FF0 will result in the user defined ROM data at that location.

7.2 COP DURING WAIT MODE

The COP will continue to operate normally during WAIT mode. The software should pull the device out of WAIT mode periodically and reset the COP by writing to the COPF bit to prevent a COP reset.

7.3 COP DURING STOP MODE

STOP mode disables the oscillator circuit and thereby turns the clock off for the entire device. The COP counter will be reset when STOP mode is entered. If a reset is used to exit STOP mode, the COP counter will be reset after the 4064 cycles of delay after STOP mode. If an IRQ is used to exit STOP mode, the COP counter will not be reset after the 4064 cycle delay and will have that many cycles already counted when control is returned to the program.

7.4 COP DURING SELF-CHECK MODE

The COP if enabled by mask option is disabled by hardware in self-check mode.

SECTION 8 PERSONALITY EPROM

The 64 bits of on-chip Personality EPROM (PEPROM) are provided as a simple EPROM array and control logic which requires serial reading of the data. This PEPROM utilizes two registers which directly interface with the PEPROM array. The actual implementation of the PEPROM software will vary depending on customer requirements. The PEPROM array is arranged as 8 bytes which have a single column select. Each bit in each byte (column) has a separate row select. See **Figure 8-1: Simple PEPROM Block Diagram**.

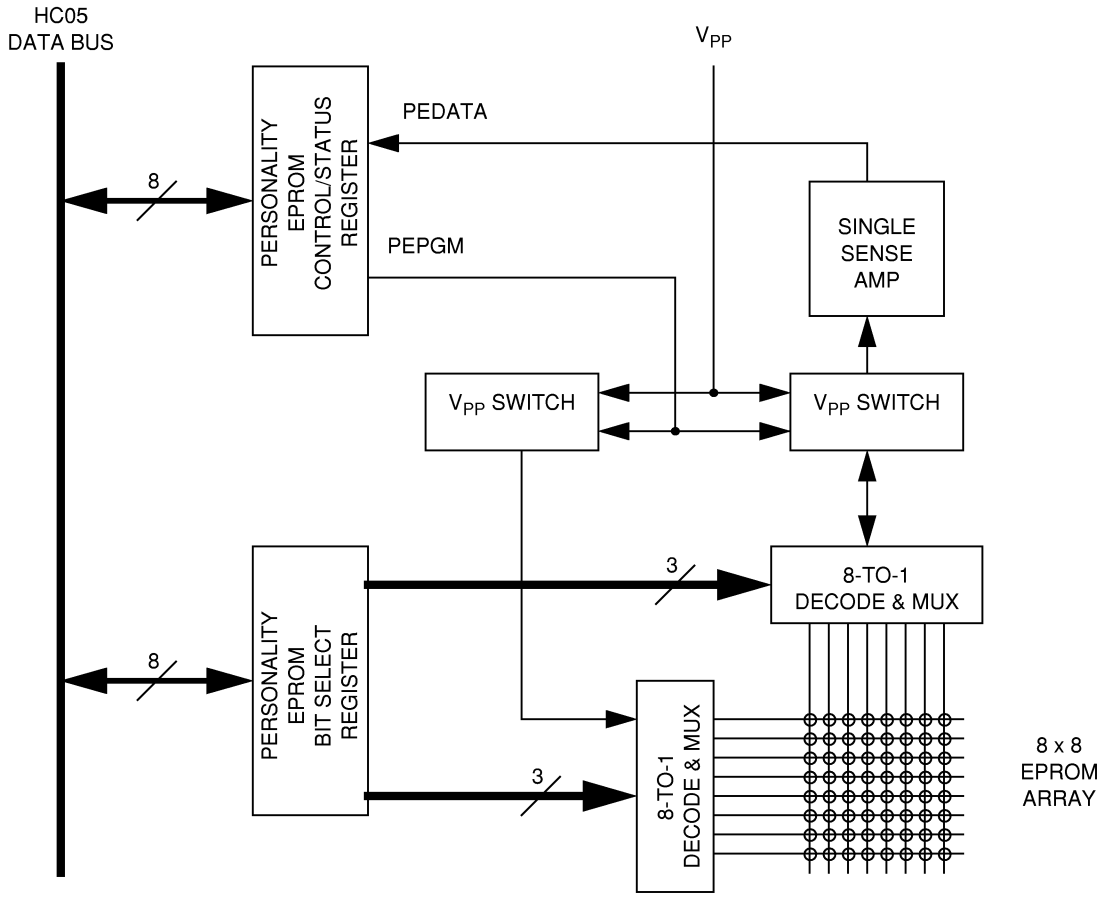


Figure 8-1: Simple PEPROM Block Diagram

8.1 PEPROM REGISTERS

Two register locations are used to support the PEPROM array. These are the Bit Select and Control/Status registers.

8.1.1 PEPROM BIT SELECT REGISTER - PEBSR

The PEPROM Bit Select Register is located at $000E and contains the enable signals for the rows and columns to access the bits in the PEPROM array. The placement of these

bits is shown in **Figure 8-2: PEBSR Select Register**. The output of this register is connected to two decoders, one for the array column and one for the array row.

The bit selected in the PEPROM is the binary weighted result of the lower six bits in PEBSR (ROW0 thru ROW2 and COL0 thru COL2), with ROW0 being the lowest order bit). The two upper bits in PEBSR (PEB6 and PEB7) are not connected to any logic in the Single-Chip Mode and may be used as storage locations. All of the bits in the PEBSR register are cleared by reset.

PEBSR $0E	PEB7	PEB6	COL2	COL1	COL0	ROW2	ROW1	ROW0
RESET	0	0	0	0	0	0	0	0

Figure 8-2: PEBSR Select Register

8.1.2 PEPROM CONTROL/STATUS REGISTER - PECSR

The PEPROM Control/Status Register is located at $000F and contains two user bits as shown in **Figure 8-3: PEPCSR Control/Status Register**. Bits 1 thru 3 are used for factory test features. All bits are cleared by reset except PEPRZF which is set.

PECSR $0F	PEDATA	0	PEPGM (DATA IN)	0	RESERVED	RESERVED	RESERVED	PEPRZF
RESET	0	0	0	0	0	0	0	1

Figure 8-3: PEPCSR Control/Status Register

8.1.2.1 PEPRZF - PEPROM Row Zero Flag

The PEPRZF is a flag bit that is set to a logical one when the first row (ROW0) of the PEPROM array is selected. If any other row is selected the PEPRZF flag bit is cleared. This flag bit can be used to reduce the software code required to access one 8-bit byte of PEPROM. The following code is suggested for reading one 8-bit byte from the PEPROM:

```
      lda   #$xy          ;XY is the base address. XY should start on a first row.
                          ;Keep the column constant and increment the rows.
                          ; i.e 00, 08, 10, 18, 20, 28, 30, 38
      sta   PEBSR         ;Store in the bit select register.
loop  rol   PECSR         ;Rotate the PEDATA into the carry bit.
      rorx                ;Rotate the carry bit into the index register.
      inc   PEBSR         ;Go to the next bit in the array.
      brclr 0,PECSR,LOOP;Go through 8 rows and when row0 is decoded again
                          ;then bit 4 will be set and the branch will not occur.
      stx   RAM           ;Save the byte of data gathered from the PEPROM
```

8.1.2.2 PEDATA - PEPROM Data

The PEDATA bit is the read-only state of the PEPROM sense amplifier.

8.1.2.3 PEPGM - PEPROM Program Control

The PEPGM bit is a read/write bit to control the switches that apply an externally provided V_{PP} to the device's drain and gate in the PEPROM array to be programmed. Since the state of the PEPGM bit determines the state of the programmed bit in the PEPROM array, it is similar to a DATA IN bit.

8.2 PEPROM PROGRAMMING

The PEPROM array is usually programmed in the expanded mode. The procedures are as follows:

1. Write the location of the desired bit to be programmed into the PEBSR register at location $000E.
2. Set the PEPGM bit in the PECSR Register located at $000F.
3. Wait for a 3 millisecond time delay.
4. Clear the PEPGM bit.

The PEPROM is then ready to be set up for another bit of data for programming.

NOTE: The programming of a PEPROM bit only requires access of that bit through the PEBSR followed by setting the PEPGM bit in the PECSR. Do not access any bits that are to be left unprogrammed (erased) while the PEPGM bit is set in the PECSR and the programming voltage is applied to the IRQ/VPP pin.

The PEPROM can be programmed in the Single-Chip Mode. In this case, the programming software must be provided in the user's ROM, $\overline{IRQ}/V_{PP}$ pin must be pulled to V_{PP} programming voltage level, and several I/O pins are made available for data transfer and handshake control.

8.3 PEPROM READ ACCESS

The contents of the PEPROM array are read by applying the proper bit select to the PEBSR register at location $000E. After each bit is selected, the PEDATA bit in the PECSR register located at $000F is tested and its state is moved to an appropriate bit location in RAM or register. The time between the setting of the bit select in the PEBSR and testing the state of the PEDATA bit in the PECSR must be greater than the minimum access time, t_{PEPACC}, for the PEPROM. The complete array can be easily accessed by starting with $3F for the PEBSR and decrementing the PEBSR after each test of the PEDATA bit. The decrement sequence can end when the contents of the PEBSR are zero.

NOTE: One byte of data from the PEPROM can be recreated in the PEBSR itself. This can be done if the read routine builds the 8-bit data byte in the index register or the accumulator and then transfers that result to the PEBSR when completed. Subsequent reads of the PEBSR will quickly yield that retrieved data byte.

8.4 PEPROM ERASING

The MC68HC05PE0 is normally supplied as an OTP device which cannot be erased. Any low-quantity custom windowed MC68HC05PE0 device can be erased by the exposure of a high-intensity ultraviolet (UV) light with a wavelength of 2537 angstroms. The recommended dose (UV intensity × exposure time) is 15 Ws/cm^2. UV lamps should be without shortwave filters, and the PEPROM device positioned about one inch from the UV lamp. A blank PEPROM bit will read as logical zero.

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SECTION 9 ELECTRICAL SPECIFICATIONS

9.1 MAXIMUM RATINGS

(Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	-0.3 to +7.0	V
Input Voltage	V_{in}	V_{SS} - 0.3 to V_{DD} + 0.3	V
Self-Check Mode (IRQ* Pin Only)	Vin	V_{SS} - 0.3 to $2 \times V_{DD}$ + 0.3	V
Current Drain Per Pin Excluding V_{DD} and V_{SS}	I	25	mA
Operating Temperature Range MC68HC05PE0P (Standard) MC68HC05PE0CP (Extended)	T_A	T_L to T_H 0 to +70 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum-rated voltages to this high-impedance circuit. For proper operation, it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$. Reliability of operation is enhanced if unused inputs are connected to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

9.2 THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance Plastic SOIC	θ_{JA}	 60 60	°C/W

9.3 DC ELECTRICAL CHARACTERISTICS (5.0 Vdc)

(V_{DD} = 5.0 Vdc±10%, V_{SS} = 0 Vdc, T_A = -40°C to +85°C, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Output voltage I_{Load} = 10.0 µA I_{Load} = -10.0 µA	 V_{OL} V_{OH}	 — V_{DD}-0.1	 — —	 0.1 —	 V
Output High Voltage (I_{Load} = -0.8 mA) PA0-7, PB5-6,PC0-7, PD5 (I_{Load} = -5.0 mA) PB7	 V_{OH} V_{OH}	 V_{DD}-0.8 V_{DD}-0.8	 — —	 — —	 V V
Output Low Voltage (I_{Load} = 1.6 mA) PA0-7, PB5-6, PC0-7, PD5 (I_{Load} = 20.0 mA) PB7	 V_{OL} V_{OL}	 — —	 — —	 0.4 0.4	 V V
Input High Voltage PA0-7, PB5-7,PC0-7, PD5, TCAP/PD7, IRQ*,RESET*,OSC1	V_{IH}	0.7×V_{DD}	—	V_{DD}	V
Input Low Voltage PA0-7, PB5-7,PC0-7, PD5, TCAP/ PD7, IRQ*,RESET*,OSC1	V_{IL}	V_{SS}	—	0.2×V_{DD}	V
Supply Current (see Notes) Run Wait Stop 25°C 0°C to +70°C (STANDARD)	 I_{DD} I_{DD} I_{DD} I_{DD}	 — — — —	 TBD TBD TBD —	 TBD TBD TBD TBD	 mA mA µA µA
I/O Ports Hi-Z Leakage Current PA0-7, PB5-6,PC0-7,PD5, TCAP/PD7	I_{OZ}	—	—	±10	µA
Port A Switch Resistance External Pull-down PA0-7	R_{PTA}	—	—	50	KΩ
Input Current RESET*, IRQ*, OSC1	I_{in}	TBD	TBD	TBD	mA
Input Current with Port A Pullups Enabled PA0-7	I_{in}	—	—	±TBD	µA
Capacitance Ports (as Input or Output) RESET*, IRQ	 C_{out} C_{in}	 — —	 — —	 12 8	 pF pF
PEPROM Programming Voltage (NOTE 8)	V_{PP}	—	16.5	—	V
PEPROM Programming Current	I_{PP}	—	5	10	mA

NOTES:

1. All values shown reflect average measurements.
2. Typical values at midpoint of voltage range, 25°C only.
3. Wait I_{DD}: Only timer system active.
4. Run (Operating) I_{DD}, Wait I_{DD}: Measured using external square wave clock source (f_{osc} = 4.2 MHz), all inputs 0.2 V from rail; no dc loads, less than 50 pF on all outputs, C_L = 20 pF on OSC2.
5. Wait, Stop I_{DD}: All ports configured as inputs, V_{IL} = 0.2 V, V_{IH} = V_{DD}-0.2 V.
6. Stop I_{DD} measured with OSC1 = V_{SS}.
7. Wait I_{DD} is affected linearly by the OSC2 capacitance.
8. Programming voltage measured at $\overline{IRQ}$/V_{PP} pin.

9.4 DC ELECTRICAL CHARACTERISTICS (3.3 V_{dc})

(V_{DD} = 3.3 Vdc ±10%, V_{SS} = 0 Vdc, T_A = -40°C to +85°C, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Output voltage I_{Load} = 10.0 µA I_{Load} = -10.0 µA	 V_{OL} V_{OH}	 — V_{DD}-0.1	 — —	 0.1 —	 V
Output High Voltage (I_{Load} = -0.2 mA) PA0-7, PB5-6,PC0-7, PD5 (I_{Load} = TBD mA) PB7	 V_{OH} V_{OH}	 V_{DD}-0.3 V_{DD}-0.3	 — —	 — —	 V V
Output Low Voltage (I_{Load} = 0.4 mA) PA0-7, PB5-6, PC0-7, PD5 (I_{Load} = TBD mA) PB7	 V_{OL} V_{OL}	 — —	 — —	 0.3 0.3	 V V
Input High Voltage PA0-7, PB5-7,PC0-7, PD5, TCAP/PD7, IRQ*,RESET*,OSC1	V_{IH}	0.7×V_{DD}	—	V_{DD}	V
Input Low Voltage PA0-7, PB5-7,PC0-7, PD5, TCAP/ PD7, IRQ*,RESET*,OSC1	V_{IL}	V_{SS}	—	0.2×V_{DD}	V
Supply Current (see Notes) Run Wait Stop 25°C 0°C to +70°C (STANDARD)	 I_{DD} I_{DD} I_{DD} I_{DD}	 — — — —	 TBD TBD TBD —	 TBD TBD TBD TBD	 mA mA µA µA
I/O Ports Hi-Z Leakage Current PA0-7, PB5-6,PC0-7,PD5, TCAP/PD7	I_{OZ}	—	—	±10	µA
Port A Switch Resistance External Pull-down PA0-7	R_{PTA}	—	—	90	KΩ
Input Current RESET*, IRQ*, OSC1	I_{in}	TBD	TBD	TBD	mA
Input Current with Port A Pullups Enabled PA0-7	I_{in}	—	—	±TBD	µA
Capacitance Ports (as Input or Output) RESET*, IRQ	 C_{out} C_{in}	 — —	 — —	 12 8	 pF pF

NOTES:

1. All values shown reflect average measurements.
2. Typical values at midpoint of voltage range, 25°C only.
3. Wait I_{DD}: Only timer system active.
4. Run (Operating) I_{DD}, Wait I_{DD}: Measured using external square wave clock source (f_{osc} = 2.1 MHz), all inputs 0.2 V from rail; no dc loads, less than 50 pF on all outputs, C_L = 20 pF on OSC2.
5. Wait, Stop I_{DD}: All ports configured as inputs, V_{IL} = 0.2 V, V_{IH} = V_{DD}-0.2 V.
6. Stop I_{DD} measured with OSC1 = V_{SS}.
7. Wait I_{DD} is affected linearly by the OSC2 capacitance.

9.5 CONTROL TIMING (5.0 Vdc)

(V_{DD} = 5.0 Vdc ±10%, V_{SS} = 0 Vdc, T_A = -40°C to +85°C, unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Frequency of Operation Crystal Option External Clock Option	 f_{osc} f_{osc}	 — dc	 4.2 4.2	 MHz MHz
Internal Operating Frequency Crystal (f_{osc} ÷ 2) External Clock (f_{osc} ÷ 2)	 f_{op} f_{op}	 — dc	 2.1 2.1	 MHz MHz
Cycle Time	t_{cyc}	480	—	ns
Crystal Oscillator Start-up Time	t_{OXOV}	—	100	ms
Stop Recovery Start-up Time (Crystal Oscillator)	t_{ILCH}	—	100	ms
RESET* Pulse Width	t_{RL}	1.5	—	t_{cyc}
Interrupt Pulse Width Low (Edge-Triggered)	t_{ILIH}	125	—	ns
Interrupt Pulse Period	t_{ILIL}	NOTE 1	—	t_{cyc}
OSC1 Pulse Width	t_{OH},t_{OL}	90	—	ns
Power-On Time	t_{VDDR}	TBD	—	ns
Capture/Compare Timer Resolution (refer to NOTE 2) Input Capture Pulse Width Input Capture Pulse Period	 f_{RESL} f_{TH}, f_{TL} t_{TLTL}	 4.0 125 NOTE 3	 — — —	 t_{cyc} ns t_{cyc}
Personality EPROM Programming Time	t_{EPGM}	—	15	ms
Personality EPROM Access Time	t_{PEPACC}	TBD	—	ns

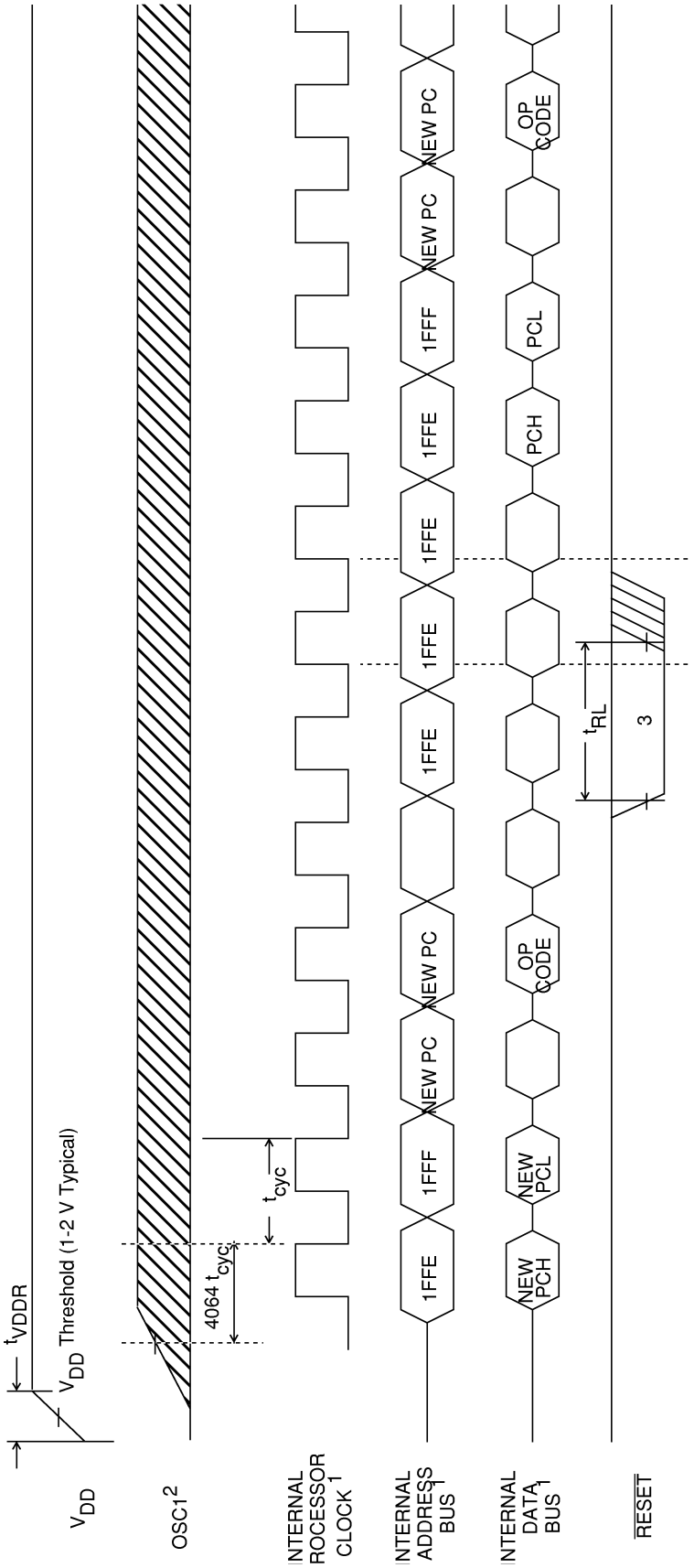
NOTES:
1. The minimum period T_{ILIL} should not be less than the number of cycles it takes to execute the interrupt service routine plus 19 t_{cyc}.
2. Because a 2-bit prescaler in the capture / compare timer must count four internal cycles (t_{cyc}), this is the limiting minimum factor in determining the timer resolution.
3. The period t_{TLTL} should not be less than the number of cycles it takes to execute the capture interrupt service routine plus 24 t_{cyc}.

9.6 CONTROL TIMING (3.3 Vdc)

(V_{DD} = 3.3 Vdc ±10%, V_{SS} = 0 Vdc, T_A = -40°C to +85°C, unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Frequency of Operation Crystal Option External Clock Option	 f_{osc} f_{osc}	 — dc	 2.0 2.0	 MHz MHz
Internal Operating Frequency Crystal (f_{osc} ÷ 2) External Clock (f_{osc} ÷ 2)	 f_{op} f_{op}	 — dc	 1.0 1.0	 MHz MHz
Cycle Time	t_{cyc}	1000	—	ns
Crystal Oscillator Start-up Time	t_{OXOV}	—	200	ms
Stop Recovery Start-up Time (Crystal Oscillator)	t_{ILCH}	—	100	ms
RESET* Pulse Width	t_{RL}	1.5	—	t_{cyc}
Interrupt Pulse Width Low (Edge-Triggered)	t_{ILIH}	250	—	ns
Interrupt Pulse Period	t_{ILIL}	NOTE 1	—	t_{cyc}
OSC1 Pulse Width	t_{OH},t_{OL}	200	—	ns
Power-On Time	t_{VDDR}	TBD	—	ns
Capture/Compare Timer Resolution (refer to NOTE 2) Input Capture Pulse Width Input Capture Pulse Period	 f_{RESL} f_{TH}, f_{TL} t_{TLTL}	 4.0 250 NOTE 3	 — — —	 t_{cyc} ns t_{cyc}
Personality EPROM Access Time	t_{PEPACC}	TBD	—	ns

NOTES:
1. The minimum period T_{ILIL} should not be less than the number of cycles it takes to execute the interrupt service routine plus 19 t_{cyc}.
2. Because a 2-bit prescaler in the capture / compare timer must count four internal cycles (t_{cyc}), this is the limiting minimum factor in determining the timer resolution.
3. The period t_{TLTL} should not be less than the number of cycles it takes to execute the capture interrupt service routine plus 24 t_{cyc}.

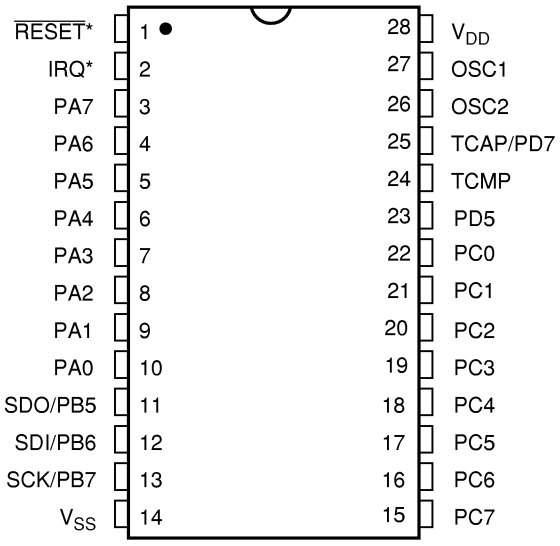


NOTES:
1. Internal timing signal and bus information not available externally.
2. OSC1 line is not meant to represent frequency. It is only used to represent time.
3. The next rising edge of the internal processor clock following the rising edge of RESET initiates the reset sequence.
4. The active low reset mask option is illustrated.

Figure 9-1: Power-On Reset and RESET

SECTION 10 MECHANICAL DATA

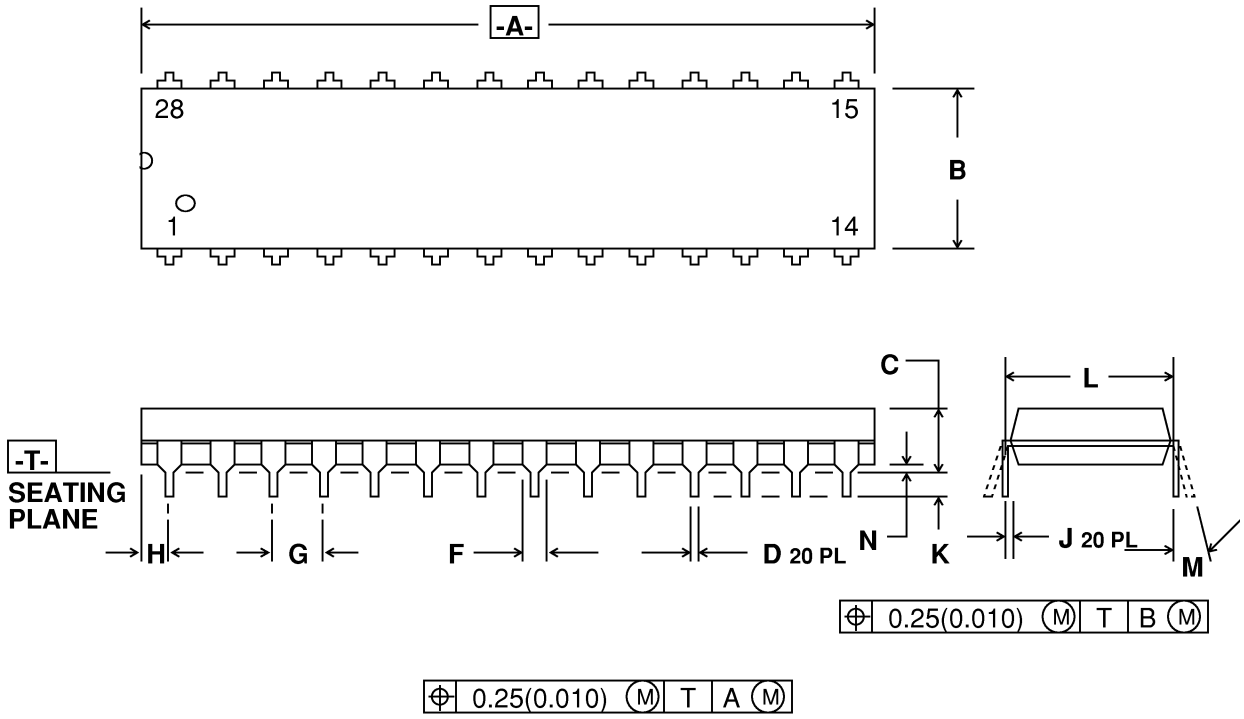
10.1 MECHANICAL DATA



10.2 PACKAGE DIMENSIONS

10.2.1 PLASTIC DIP

P SUFFIX
CASE # 710-02



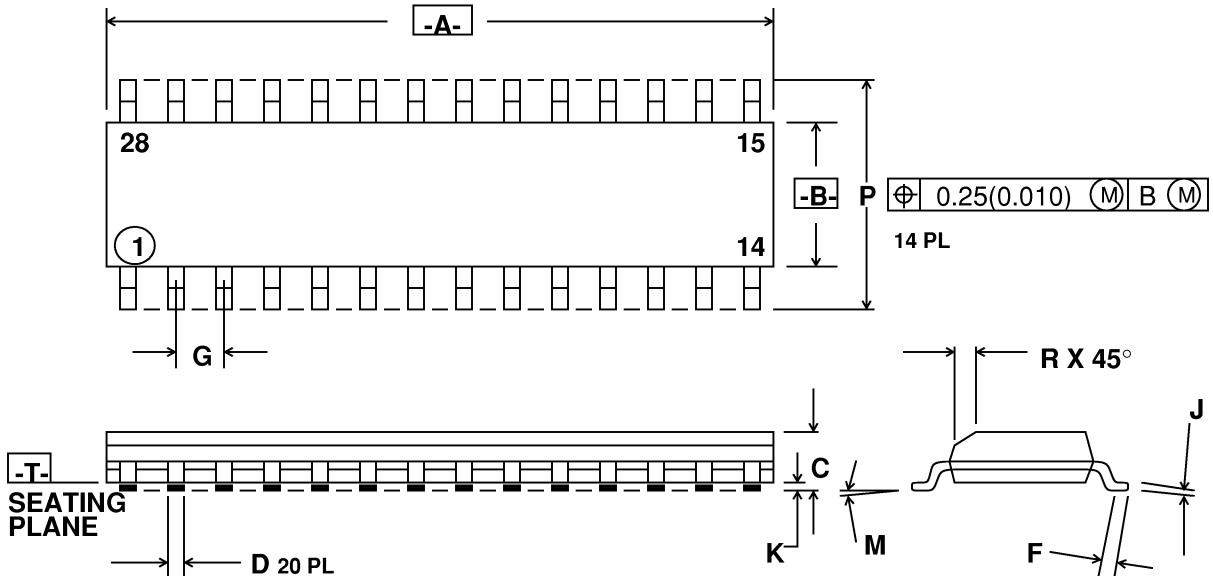
NOTES

1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	36.45	37.21	1.435	1.465
B	13.72	14.2	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

10.2.2 SOIC

DW SUFFIX
CASE # 751F-02



NOTES

1. DIMENSIONS "A" AND "B" ARE DATUMS AND "T" IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIM; MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
6. 751F-01 OBSOLETE, NEW STANDARD 751F-02.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	17.80	18.05	0.701	0.710
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050BSC	
J	0.25	0.32	0010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

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