Motorola Semiconductor Technical Data

Addendum to
MC68HC908BD48
Technical Data

This addendum provides corrections to:

MC68HC908BD48 Technical Data (Motorola document number MC68HC908BD48/D Rev. 1.0)

Page 274: Add VSYNC and HSYNC; and change LVI parameters in 21.6 DC Electrical Characteristics.

From:

Characteristic	Symbol	Min	Typ(2)	Max	Unit
Input High Voltage All ports, $\overline{IRQ}$, $\overline{RST}$, OSC1	V_{IH}	$0.7 \times V_{DD}$	—	V_{DD}	V
Input Low Voltage All ports, $\overline{IRQ}$, $\overline{RST}$, OSC1	V_{IL}	V_{SS}	—	$0.2 \times V_{DD}$	V
Low-Voltage Inhibit, trip falling voltage	V_{TRIPF}	3.5	3.8	4.5	V
Low-Voltage Inhibit, trip rising voltage	V_{TRIPR}	3.5	4.0	4.5	V

To:

Characteristic	Symbol	Min	Typ(2)	Max	Unit
Input High Voltage All ports, $\overline{IRQ}$, $\overline{RST}$, OSC1 VSYNC, HSYNC	V_{IH}	$0.7 \times V_{DD}$ 2.0	—	V_{DD} V_{DD}	V
Input Low Voltage All ports, $\overline{IRQ}$, $\overline{RST}$, OSC1 VSYNC, HSYNC	V_{IL}	V_{SS} V_{SS}	—	$0.2 \times V_{DD}$ 0.8	V
Low-Voltage Inhibit, trip falling voltage	V_{TRIPF}	3.4	3.6	3.8	V
Low-Voltage Inhibit, trip rising voltage	V_{TRIPR}	3.6	3.8	4.0	V

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