LTE3401L

SiGe:C low-noise amplifier MMIC with bypass switch for LTE

Rev. 3.2 — 18 December 2018 Product data sheet

1 General description

The LTE3401L is a high-gain Low-Noise Amplifier (LNA) with bypass switch for LTE receiver applications, available in a small plastic 6-pin thin leadless package.

The LTE3401L delivers system-optimized gain for both primary and diversity applications where sensitivity improvement is required. The high linearity of this low noise device ensures the required receive sensitivity independent of cellular transmit power level in frequency division duplex (FDD) systems. When receive signal strength is sufficient, the LTE3401L can be switched off to operate in bypass mode at increased $IP3_i$ level and a 1 µA supply current, to lower power consumption. The LTE3401L is internally AC coupled and requires only one external matching inductor.

The LTE3401L is optimized for 703 MHz to 960 MHz, but also can be tuned for 617 MHz to 652 MHz (B71).

2 Features and benefits

- Operating frequency from 617 MHz to 960 MHz
- Noise figure = 0.63 dB
- Gain 18.4 dB
- High input 1 dB compression point of -7.8 dBm
- High in band $IP3_i$ of +0.7 dBm
- Bypass switch insertion loss of 1.8 dB
- Supply voltage 1.5 V to 3.1 V
- Integrated RF supply decoupling capacitor
- Optimized performance at a supply current of 10.3 mA
- Bypass mode current consumption < 1 µA
- Integrated temperature stabilized bias for easy design
- Requires only one input matching inductor
- Input and Output AC coupled through DC blocking capacitors
- Integrated matching for the output
- ESD protection on all pins
- Low bill of materials (BOM)
- 6 pins leadless package: 1.1 mm x 0.7 mm x 0.37 mm: 0.40 mm pitch
- 180 GHz transit frequency - SiGe:C technology
- Moisture sensitivity Level 1

3 Applications

- LNA for LTE reception in smart phones
- feature phones
- tablet PCs
- RF front-end modules

4 Quick reference data

Table 1. Quick reference data

f = 882 MHz; V_{CC} = 2.8 V; $V_{I(CTRL)}$ > 0.8 V; T_{amb} = 25 °C. Input matched to 50 Ω using application diagram from Figure 3 and component values as in Table 10. Unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC}	supply current	in gain mode	-	10.3	12.7	mA
		in bypass mode	-	-	1	µA
G_p	power gain	in gain mode	-	18.4	-	dB
		in bypass mode	-	-1.8	-	dB
NF	noise figure	[1]	-	0.63	-	dB
$P_{i(1\ dB)}$	input power at 1 dB gain compression		-	-7.8	-	dBm
$IP3_i$	input third-order intercept point	Δf = 1 MHz	-	+0.7	-	dBm

[1] PCB losses are subtracted.

5 Ordering information

Table 2. Ordering information

Type number	Orderable part number	Package		
		Name	Description	Version
LTE3401L	LTE3401LX	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1.1 x 0.7 x 0.37 mm	SOT1232

6 Marking

Table 3. Marking code

Type number	Marking code
LTE3401L	V

7 Block diagram

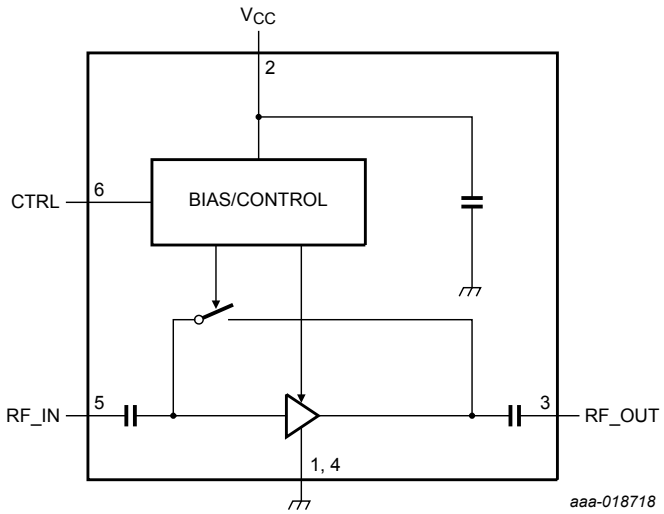


Figure 1. Block diagram

8 Pinning information

8.1 Pinning

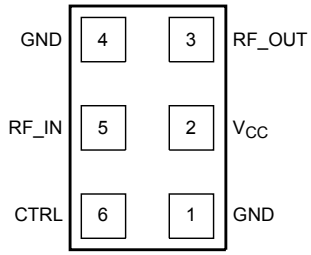


Figure 2. Pin configuration

8.2 Pin description

Table 4. Pinning

Symbol	Pin	Description
GND	1	RF ground
V_{CC}	2	supply voltage
RF_OUT	3	RF out
GND	4	RF ground
RF_IN	5	RF in
CTRL	6	gain control, switch between gain and bypass mode

9 Limiting values

Table 5. Limiting values

In accordance with the absolute maximum rating system (IEC 60134).

See section 18.3 "Disclaimers", paragraph "Limiting values".

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+4.3	V
$V_{I(CTRL)}$	input voltage on pin CTRL	$V_{I(CTRL)} < V_{CC} + 0.6$ V	-0.5	+5.0	V
$V_{I(RF\_IN)}$	input voltage on pin RF_IN	DC [1]	-0.5	+0.6	V
$V_{I(RF\_OUT)}$	input voltage on pin RF_OUT	DC, $V_{I(RF\_OUT)} < V_{CC} + 0.6$ V [1]	-0.5	+5.0	V
P_i	input power	RF	-	26	dBm
		RF [2]	-	23	dBm
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature		-	150	°C
V_{ESD}	electrostatic discharge voltage	human body model (HBM) according to ANSI/ESDA/JEDEC standard JS-001 [3]	-	±2	kV
		charged device model (CDM) according to ANSI/ESDA/JEDEC standard JS-002	-	±1	kV

[1] The RF input and output are AC coupled through internal DC Blocking capacitors.
[2] f = 880 MHz, 200 Hrs at T_{amb} = 100 °C.
[3] HBM ESD protection level is according to JS-001 classification 2 (2000 V to < 4000 V).

10 Operating conditions

Table 6. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.5	-	3.1	V
T_{amb}	ambient temperature		-40	+25	+85	°C
$V_{I(CTRL)}$	input voltage on pin CTRL	bypass mode	-	-	0.25	V
		gain mode	0.8	-	-	V

11 Thermal characteristics

Table 7. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point		225	K/W

12 Characteristics

Table 8. Characteristics

703 MHz ≤ f ≤ 960 MHz; V_{CC} =1.8 V; T_{amb} = 25 °C; input matched 50 Ω using application diagram from Figure 3 and component values as in Table 10. Unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Gain mode						
I_{CC}	supply current	$V_{I(CTRL)}$ > 0.8 V	-	9.8	12.5	mA
G_p	power gain	f = 740 MHz	-	18.6	-	dB
		f = 882 MHz	-	18.3	-	dB
		f = 943 MHz	-	18.0	-	dB
ΔG/ΔT	gain variation with temperature		-	-0.01	-	dB/°C
NF	noise figure	f = 740 MHz [1]	-	0.68	-	dB
		f = 882 MHz [1]	-	0.67	-	dB
		f = 943 MHz [1]	-	0.70	-	dB
$P_{i(1dB)}$	input power at 1 dB gain compression	f = 740 MHz	-	-12.0	-	dBm
		f = 882 MHz	-	-11.2	-	dBm
		f = 943 MHz	-	-11.0	-	dBm
$IP3_i$	input third-order intercept point	f = 740 MHz, Δf = 1 MHz	-	-0.8	-	dBm
		f = 882 MHz, Δf = 1 MHz	-	-0.3	-	dBm
		f = 943 MHz, Δf = 1 MHz	-	0.4	-	dBm
RL_{in}	input return loss	f = 740 MHz	-	7.0	-	dB
		f = 882 MHz	-	10.0	-	dB
		f = 943 MHz	-	11.0	-	dB
RL_{out}	output return loss	f = 740 MHz	-	16.0	-	dB
		f = 882 MHz	-	16.0	-	dB
		f = 943 MHz	-	15.0	-	dB
ISL	isolation	f = 740 MHz	-	32.0	-	dB
		f = 882 MHz	-	30.0	-	dB
		f = 943 MHz	-	29.0	-	dB
K	Rollett stability factor		1	-	-	
t_{on}	turn-on time	time from $V_{I(CTRL)}$ ON, to 90 % of the gain	-	-	1	µs
t_{off}	turn-off time	time from $V_{I(CTRL)}$ OFF, to 10 % of the gain	-	-	1	µs

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Bypass mode						
I_{CC}	supply current	$V_{I(CTRL)}$ < 0.25 V	-	-	1.0	µA
G_p	power gain	f = 740 MHz	-	-1.9	-	dB
		f = 882 MHz	-	-2.0	-	dB
		f = 943 MHz	-	-2.1	-	dB
RL_{in}	input return loss	f = 740 MHz	-	21.0	-	dB
		f = 882 MHz	-	15.0	-	dB
		f = 943 MHz	-	14.0	-	dB
RL_{out}	output return loss	f = 740 MHz	-	10.0	-	dB
		f = 882 MHz	-	10.0	-	dB
		f = 943 MHz	-	9.0	-	dB

[1] PCB losses are subtracted.

Table 9. Characteristics

703 MHz ≤ f ≤ 960 MHz; V_{CC} = 2.8 V; T_{amb} = 25 °C; input matched 50 Ω using application diagram from Figure 3 and component values as in Table 10. Unless otherwise specified.

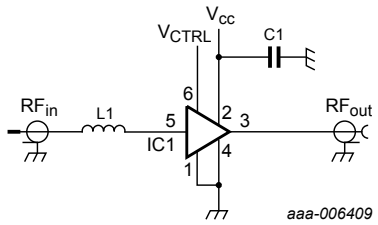
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Gain mode						
I_{CC}	supply current	$V_{I(CTRL)}$ > 0.8 V	-	10.3	12.7	mA
G_p	power gain	f = 740 MHz	-	18.8	-	dB
		f = 882 MHz	-	18.4	-	dB
		f = 943 MHz	-	18.2	-	dB
ΔG/ΔT	gain variation with temperature		-	-0.01	-	dB/°C
NF	noise figure	f = 740 MHz [1]	-	0.65	-	dB
		f = 882 MHz [1]	-	0.63	-	dB
		f = 943 MHz [1]	-	0.66	-	dB
$P_{i(1dB)}$	input power at 1 dB gain compression	f = 740 MHz	-	-8.7	-	dBm
		f = 882 MHz	-	-7.8	-	dBm
		f = 943 MHz	-	-7.4	-	dBm
$IP3_i$	input third-order intercept point	f = 740 MHz, Δf = 1 MHz	-	-0.3	-	dBm
		f = 882 MHz, Δf = 1 MHz	-	0.7	-	dBm
		f = 943 MHz, Δf = 1 MHz	-	1.4	-	dBm
RL_{in}	input return loss	f = 740 MHz	-	7.0	-	dB
		f = 882 MHz	-	10.5	-	dB
		f = 943 MHz	-	12.0	-	dB

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
RL_{out}	output return loss	f = 740 MHz	-	16.0	-	dB
		f = 882 MHz	-	17.0	-	dB
		f = 943 MHz	-	16.0	-	dB
ISL	isolation	f = 740 MHz	-	32.0	-	dB
		f = 882 MHz	-	30.0	-	dB
		f = 943 MHz	-	29.0	-	dB
K	Rollett stability factor		1	-	-	
t_{on}	turn-on time	Time from $V_{I(CTRL)}$ ON, to 90 % of the gain	-	-	1	µs
t_{off}	turn-off time	Time from $V_{I(CTRL)}$ OFF, to 10 % of the gain	-	-	1	µs
Bypass mode						
I_{CC}	supply current	$V_{I(CTRL)}$ < 0.25 V	-	-	1.0	µA
G_p	power gain	f = 740 MHz	-	-1.7	-	dB
		f = 882 MHz	-	-1.8	-	dB
		f = 943 MHz	-	-1.9	-	dB
RL_{in}	input return loss	f = 740 MHz	-	20.0	-	dB
		f = 882 MHz	-	15.0	-	dB
		f = 943 MHz	-	13.0	-	dB
RL_{out}	output return loss	f = 740 MHz	-	11.0	-	dB
		f = 882 MHz	-	10.0	-	dB
		f = 943 MHz	-	10.5	-	dB

[1] PCB losses are subtracted.

13 Application information

13.1 LTE LNA



For a list of components, see Table 10

Figure 3. Schematics LTE LNA evaluation board

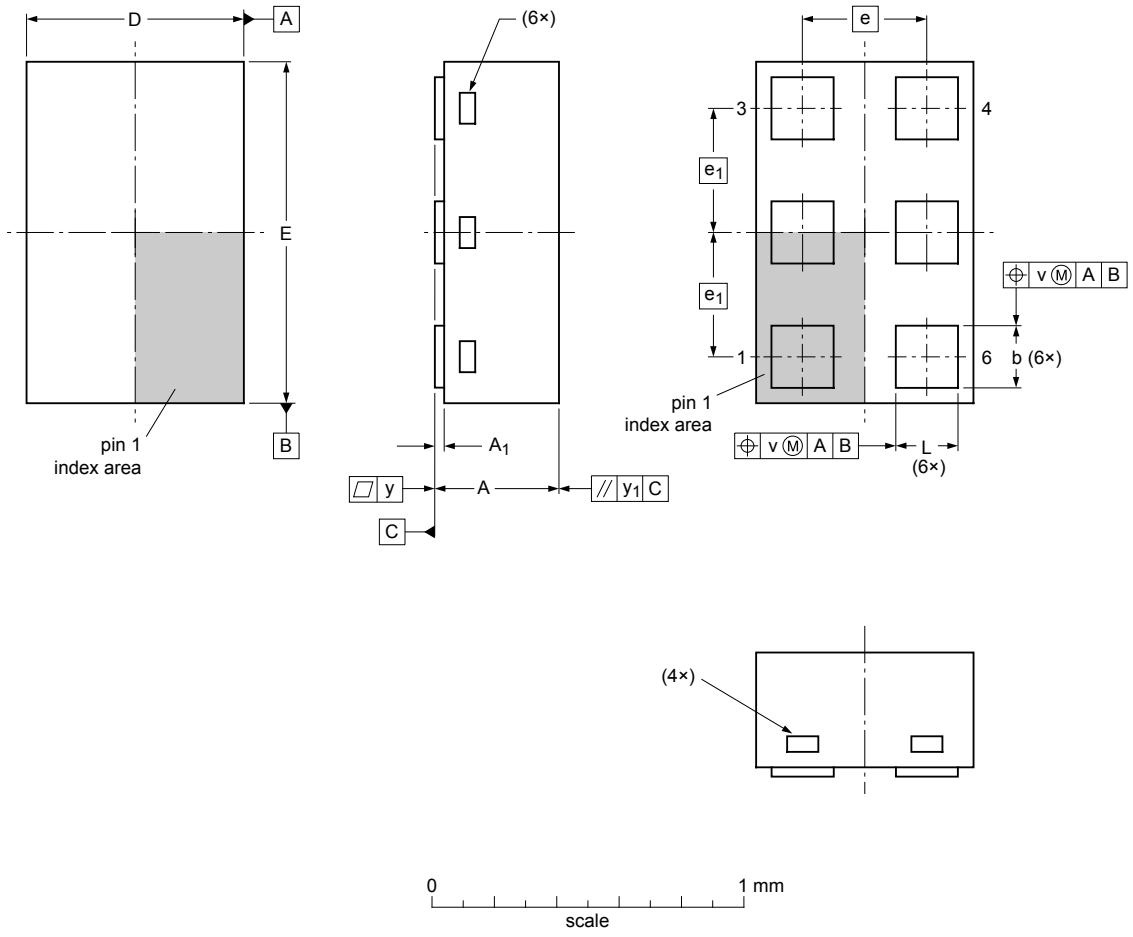
Table 10. List of components

For schematics, see Figure 3

Component	Description	Value	Remarks
C_1	decoupling capacitor	1 µF	The total capacitance on the V_{CC} node must be at least 1 µF. It must be positioned at a short distance from the V_{CC} pin (preferably within 15 mm). Typically, such capacitance is already present at the output of the V_{CC} voltage regulator.
IC1	LTE3401L		NXP
L1	high-quality matching inductor	18 nH	617 < f < 652 MHz Murata LQW15A
		8.7 nH	703 < f < 960 MHz Murata LQW15A

14 Package outline

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1.1 x 0.7 x 0.37 mm **SOT1232**



Dimensions (mm are the original dimensions)

Unit		A	A_1	D	E	e_1	e	b	L	V	Y	Y_1
	min	0.34		0.65	1.05			0.17	0.17			
mm	nom	0.37		0.70	1.10	0.4	0.4	0.20	0.20	0.1	0.05	0.1
	max	0.40	0.04	0.75	1.15			0.25	0.25			

Note
1. Dimension A is including plating thickness.

sot1232_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1232						~~13-04-12~~ 13-11-08

Figure 4. Package outline SOT1232 (XSON6)

15 Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.
Such precautions are described in the *ANSI/ESD S20.20, IEC/ST 61340-5, JESD625-A* or equivalent standards.

16 Abbreviations

Table 11. Abbreviations

Acronym	Description
ESD	electrostatic discharge
HBM	human body model
MMIC	monolithic microwave-integrated circuit
MSL	moisture sensitivity level
MUF	molded underfill
LTE	long-term evolution
PCB	printed-circuit board
SiGe:C	silicon germanium carbon

17 Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LTE3401L v.3.2	20181218	Product data sheet	-	LTE3401L v.3.1
modification	added extra column for Orderable part number to Ordering information table, to prevent confusion			
LTE3401L v.3.1	20181023	Product data sheet	-	LTE3401L v.3
modification	added orderable part number to Ordering information table			
LTE3401L v.3	20180810	Product data sheet	-	LTE3401L v.2
modification	data sheet changed from company confidential to public			
LTE3401L v.2	20180307	Product data sheet	-	LTE3401L v.1
modifications	corrected I_{CC} max (2.8 V) and mention B71 application			
LTE3401L v.1	20170807	Product data sheet	-	-

18 Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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