Freescale Semiconductor
Technical Data

Document Number: MC13883
Rev. 3, 02/2010

MC13883

Package Information
Plastic Package
Case 1624

Ordering Information

Device	Device Marking or Operating Temperature Range	Package
MC13883EP4	-30 to +85° C	QFN-40

MC13883

Integrated Charger USB Interface

1 Introduction

The MC13883 integrated charger, USB on-the-go transceiver, and carkit interface incorporates support for the CEA-936-A carkit specification. The MC13883 provides charging from a variety of sources, USB connectivity (including on-the-go, OTG), as well as support for phone-powered accessories. The MC13883 is an “all in one” IC that integrates nearly the entire interface, Li-Ion battery charging, and transceiver circuitry required to support these functions.

1.1 Key Features

- Allows charging of the phone through the USB connector
- Over-voltage protection for protecting the phone from faulty (high voltage) charging sources
- Reverse mode for charge path allows power to be sourced to the VBUS pin from the battery. This can be used to support phone powered device as described in the CEA-936-A standard.
- USB 2.0/OTG transceiver

Contents

freescale™ semiconductor

- UART and audio signaling follow the protocol defined by CEA-936-A carkit specification
- 6 x 6 mm QFN-40 package

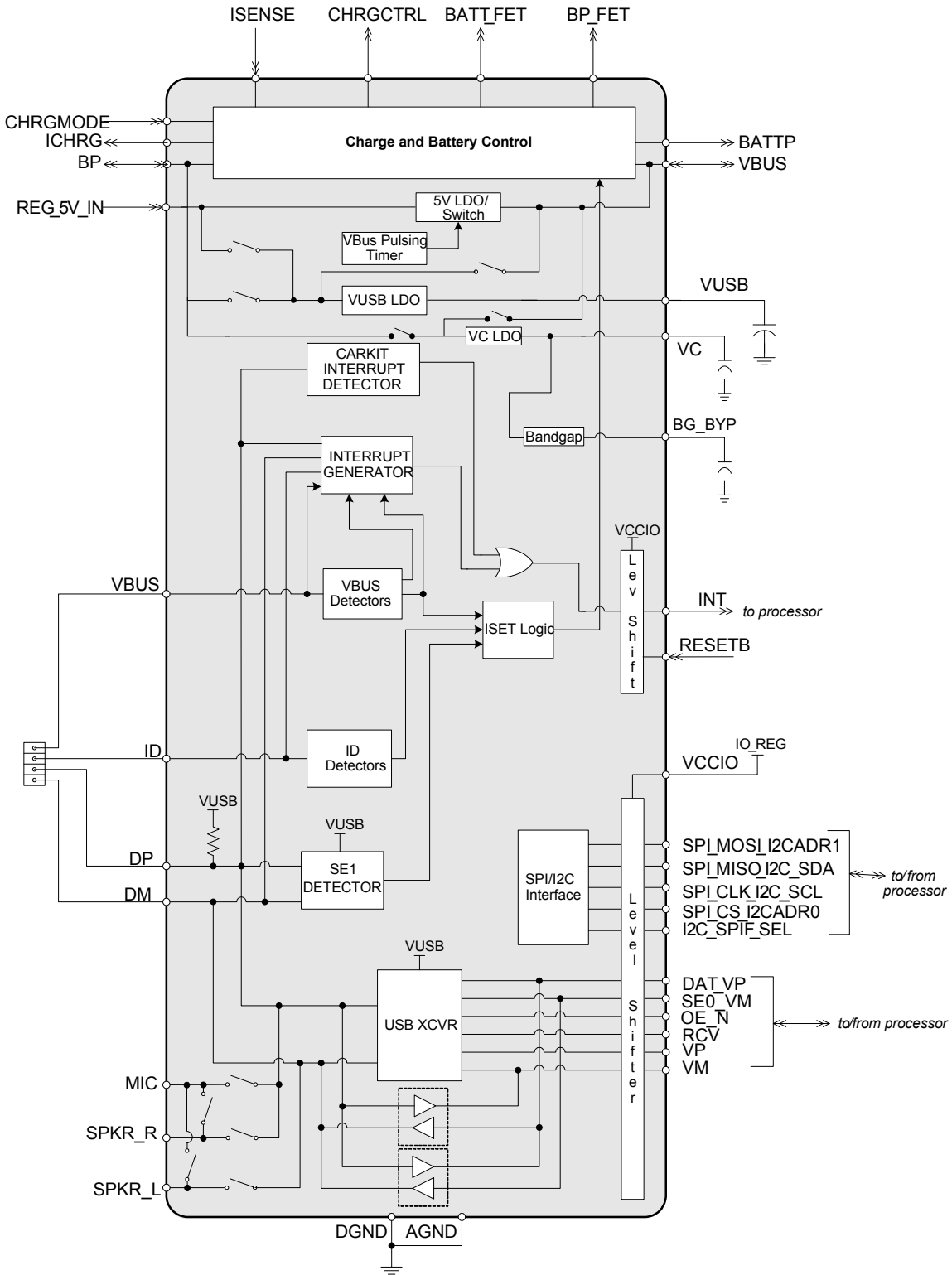

Figure 1. Block Diagram

1.2 Power Overview

1.2.1 Charging

The MC13883 allows charging of the phone via the mini-USB VBUS pin. This pin sources power from a variety of devices including wall chargers and carkits, as well as sources that traditionally are not used in charging. Specifically, the MC13883 allows the phone to be charged from a PC via a USB port. While this is a very useful feature from an end-user perspective, it is a feature that adds some additional requirements to the bus due to the unique limitations and requirements the USB specification places on devices that are attached to a USB port. The MC13883 simplifies the task of identifying whether a PC or a “traditional” charger is attached to the phone, allowing for a fairly simple methodology for handling these situations-a methodology that is not burdensome to the phone in terms of hardware or software cost and complexity.

The charge circuitry can be configured as “dual path” charging. This means the power from the charge supply is routed simultaneously to both the battery for charging and the phone B+ point to operate the phone. It can also be configured for “single path” charging, in which case charge power is only routed to the battery and from the battery to the phone's B+ point. Or it can be configured as "serial path", in which case the charger powers the phone and a special trickle-charge path charges a deeply discharged battery.

1.2.2 Over-Voltage/Over-Current Protection and Reverse Charge Overview

The MC13883 has built-in over-voltage protection for protecting the phone from faulty (high voltage) charging sources. In addition, the MC13883 IC has the ability to place the charge path in reverse mode-allowing power to be sourced to the VBUS pin from the battery. This can be used to support phone-powered devices as described in the CEA-936-A standard. In order to protect the phone from short circuit conditions on the external pins, this path also has built-in over-current protection.

1.2.3 USB Voltage Generation

In addition to providing power to the phone to charge the battery and generate the main phone supply, the MC13883 also generates the various voltage supplies needed to support USB OTG. This includes an internal regulator to supply the USB transceiver (VUSB) as well as a 5V linear regulator to provide power out through the VBUS pin to support SRP—Session Request Protocol—a basic requirement of USB OTG.

1.3 Connectivity Overview

Various self powered devices (SPD) and phone powered devices (PPD) may be connected to the MC13883 interface. The phone needs to properly detect and identify each of these devices.

There are four signaling modes that the MC13883 bus supports: two digital data modes and two analog audio modes. Two data modes are standard USB signaling and UART signaling. Two audio modes are mono signaling and stereo signaling. The USB signaling follows the protocol defined in the USB 2.0 specification. UART and audio signaling follow the protocol defined in the CEA-936-A Carkit specification.

Data and audio signaling modes share the same DP (Data Plus) and DM (Data Minus) pins of the mini-USB connector. The phone transitions between the four types of signaling modes using Signaling Negotiation Protocol (SNP) described in the CEA-936-A Carkit specification. The MC13883 bus supports both 4-wire and 5-wire protocols.

2 Signal Descriptions

Table 1. Pin Descriptions

Pin #	Pin Name	Description	Block	I/O Supply	Type	I/O
1	VC	Internal supply			Analog	Output
2	BG_BYP	Bandgap Bypass pin	Bandgap		Analog	Output
3	GNDREF	Ground	GND		GND	-
4	VCCIO	IO Supply	SPI/I2C	-	Analog	Input
5	ICHRG	Voltage proportional to the charge current.	Charger		Analog	Output
6	SPICS_I2CADR	SPI Chip Select / LSB of I2C Device Address Offset	SPI	VCCIO	Digital	Input
7	SPICLK_I2CSCL	SPI / I2C Clock	SPI/I2C	VCCIO	Digital	Input
8	SPIMOSI_I2CADR	SPI Master Out Slave In / MSB of I2C Device Address Offset	SPI/I2C	VCCIO	Digital	Input
9	SPIMISO_I2CSDA	SPI Master In Slave Out / I2C Data	SPI/I2C	VCCIO	Digital	Input/Output
10	INT	Interrupt signal	Control	VCCIO	Digital	Output
11	RESETB	Reset Input signal	SPI	VCCIO	Digital	Input
12	TXENB	USB Transmit Enable low	USB	VCCIO	Digital	Input
13	VP	Dplus Receive	USB	VCCIO	Digital	Output
14	VM	Dminus Receive	USB	VCCIO	Digital	Output
15	ID	ID pin of USB connector	USB		Analog	Input
16	DAT_VP	Data/DP input	USB	VCCIO	Digital	Input/Output
17	SEO_VM	Single Ended Zero / DM input	USB	VCCIO	Digital	Input/Output
18	SPKR_R	Audio Right output	AUDIO	VUSB	Analog	Input
19	MIC	Microphone input	AUDIO	VUSB	Analog	Output
20	SPKR_L	Audio Left output	AUDIO	VUSB	Analog	Input
21	DM	DM pin of USB connector	USB	VUSB	Analog	Input/Output
22	DGND	Digital Ground	GND		GND	-
23	DP	DP pin of USB connector	USB	VUSB	Analog	Input/Output

Table 1. Pin Descriptions (continued)

Pin #	Pin Name	Description	Block	I/O Supply	Type	I/O
24	VUSB	Cap for 3.3V Vusb regulator	USB		Analog	Output
25	REG_5V_IN	VUSB Regulator input	USB		Analog	Input
26	BOOTMODE	Trinary USB transceiver mode	USB	VC	Digital	Input
27	USB_EN	USB Xcvr enable	USB	VCCIO	Digital	Input
28	RCV	Differential Receive	USB	VCCIO	Digital	Output
29	VBUS	Charger Input Voltage	USB/Charger		Analog	Input/Output
30	CHRGCTRL	Gate driver output of Regulator	Charger		Analog	Output
31	AGND	Analog Ground	GND		GND	-
32	ISENSE	Current Sense pin	Charger		Analog	Input
33	PWR_ON	Turnon signal to phone	Control	VBUS	Digital	Output
34	BP_FET	Gate driver output for BP Switch	Charger		Analog	Output
35	BP	Bplus	Bandgap		Analog	Input
36	BATT_FET	Gate driver output for Battery Switch	Charger		Analog	Output
37	BATTP	Battery Voltage	Charger		Analog	Input
38	CHRG_LED	Output for Sign-of-life LED indicator				
39	CHRGMODE	Single /serial / dual path charging mode select	Control	VC	Digital	Input
40	I2C_SPIF_SEL	SPI/I2C Select	SPI/I2C	VC	Digital	Input

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 2 shows the absolute maximum voltage and temperature ratings of the MC13883 IC. Operation outside the limits shown may cause damage to the device and negatively affect performance.

Table 2. Absolute Maximum Ratings

Parameter	Condition	Min	Typ	Max	Units
VBUS, CHRGCTRL, BPFET, PATH_SEL Voltage Rating	to AGND	-0.3	-	20	V
All GNDs	to AGND	-0.3	0	-	V
DP, DM, ID	to AGND	-0.3	-	5.25	V
BP	to AGND	-0.3	-	5.5	V
All other pins Voltage Rating	to AGND	-0.3	-	4.5	V
*Operating Temperature Range (Ambient)		-30	-	85	°C
Storage Temperature Range		-65	-	150	°C
ESD Rating	All pins	2.5	-		kV
REG_5V_IN	to AGND	-	-	6.0	V

NOTE: Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Recommended Operating Conditions and Electrical Characteristics tables.

3.2 Operating Conditions

Table 3 gives the operating conditions under which the performance specifications provided in this document are guaranteed.

Table 3. Operating Conditions

Parameter	Condition	Min	Typ	Max	Units
Supply Input Voltage (-30°C < T_A < 85°C)					
VBUS		2.3		5.5	V
VUSB		1.65		3.6	V
REG_5V_IN		4.5		6.0	V
VCC_IO		1.65		2.9	V

Table 4. Quiescent Current
(2.7V < BP< 4.2 V), (-30°C < T_A< 85°C)

Parameter	Conditions	Min	Typ	Max	Units
Active Mode	(Phone On, RESETB=1, VBUS=5.25V)	-	300	-	µA
Idle Mode	(Phone On, RESETB=1, VBUS=0V) ID_MUX_ENB_1	-	100	-	µA
Off Mode	(Phone Off, RESETB=0, VBUS=0V)	-	22	-	µA

4 Power Architecture

4.1 Power Architecture Overview

The MC13883 IC contains the following power-related features:

- Single and dual-path charging from USB connector
- Fully compliant with USB, USB OTG, enhanced mini-USB, and CEA-936-A specifications
- Over-voltage protection
- Reverse charge mode (allowing battery power to be sourced out to the VBUS pin)
- VBUS generation (including VBUS pulsing in support of USB OTG)

The Power Architecture block diagram is shown in Figure 2.

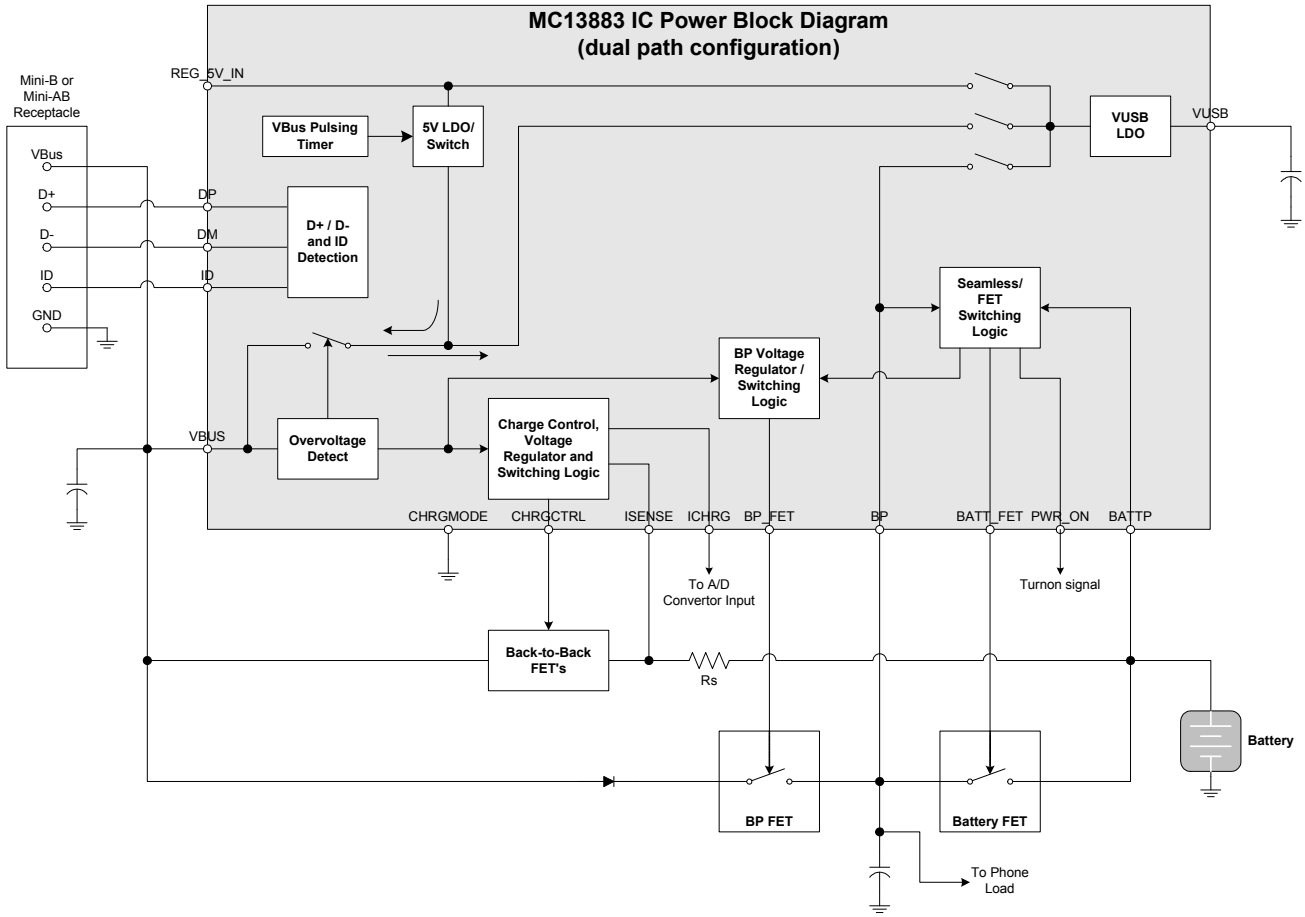

Figure 2. Power Architecture Block Diagram

4.2 Charging

This section details the charging functionality. Charge current comes into VBUS from a USB source or charger and is routed to the battery. Power is also routed to the phone circuitry. This can be accomplished in different manners as described below.

If it is desired that the phone circuitry be guaranteed to be powered during charge, the “dual path” technique is probably desirable, as power separately reaches the battery and the phone so that the phone functions even though the battery may be very deeply discharged.

Component count can be reduced with a single-path charge architecture, but at the cost of reduced or delayed functionality when charging a battery that is severely discharged.

Dual Path, Single Path and Serial Path charging is described below and shown in Figures 3, 4 and 5.

4.2.1 Dual-Path Charging Overview

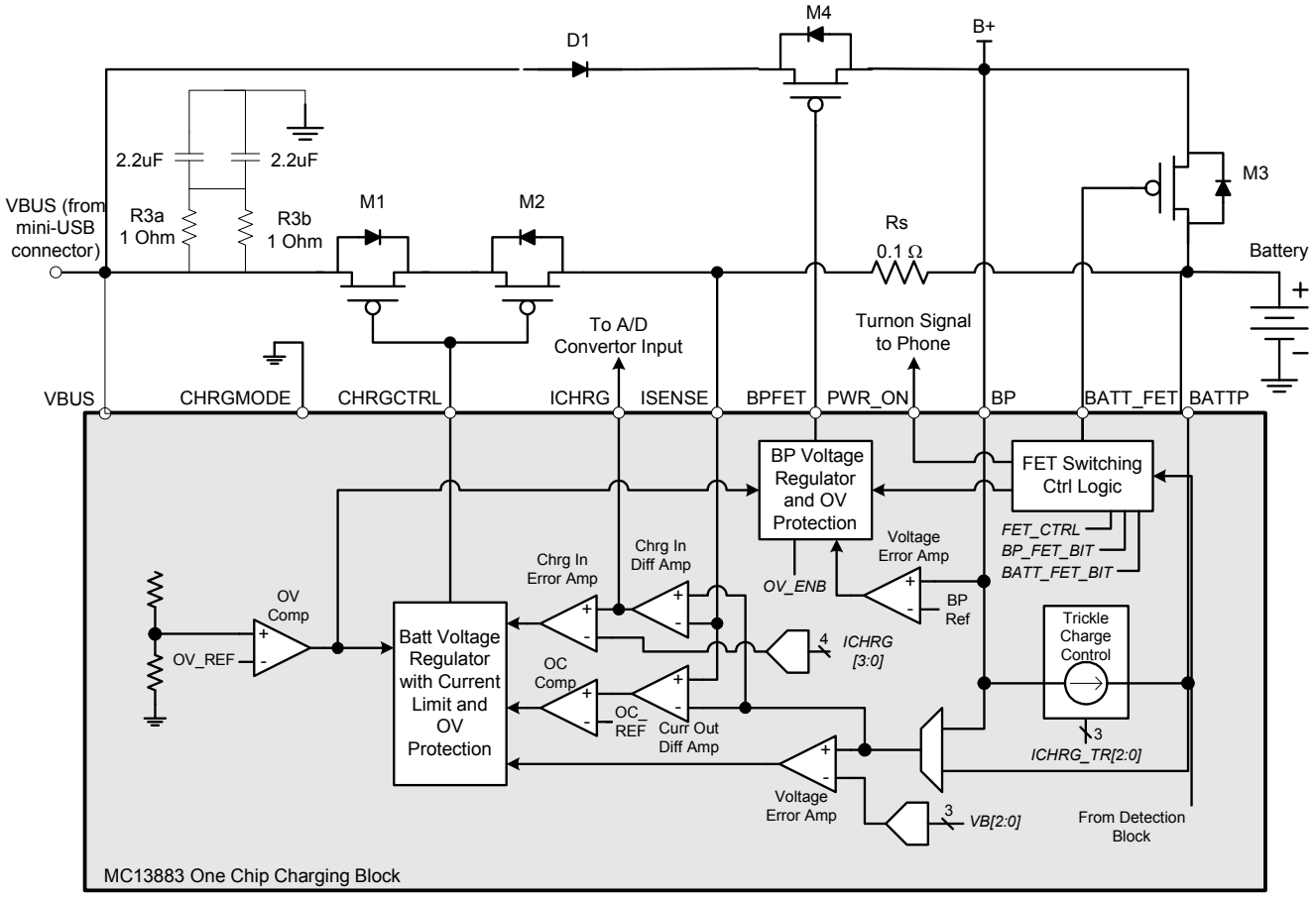

Figure 3. Dual-Path Charging Block Diagram

The basic feature of dual-path charging that sets it apart from single-path charging topologies is the fact that there are two separate current paths from the external charger input (VBUS) to the internal phone B+ supply rail (B+). One of these is a current-limited path through external FET's M1 and M2 to the battery positive terminal. This path is used to charge the battery and therefore is called the charge path. The second path is a non-charging path through D1 and M4 to the B+ node, (BP pin). (B+ is the main phone supply node from which most other internal phone power rails are derived, MC13883 pin BP is attached to it.) The basic supply path when a charger is not attached to the phone is from the battery through M3 to B+.

The charge current is sensed through an external sense resistor (nominally 100 mΩ) limited to a current set by register bits ICHRG[3:0] via control of M1 and M2 through the CHRGCTRL pin.

There are redundant 1 Ω and 2.2 uF capacitors on the VBUS pin which are required parts for stability reasons. Each of the 2.2 uF capacitors should be X5R or better with a minimum capacitance of 1.3 uF with 5 volts applied.

The value of a ceramic capacitor is a function of the voltage applied to it. It should be rated for a high voltage, such as 20 volts to withstand failed chargers.

The selection of devices appropriate for M1, M2 and M4 should be made carefully because of stability issues. The recommended device for these locations is shown in Table 5.

4.2.2 Serial Path Charging Overview

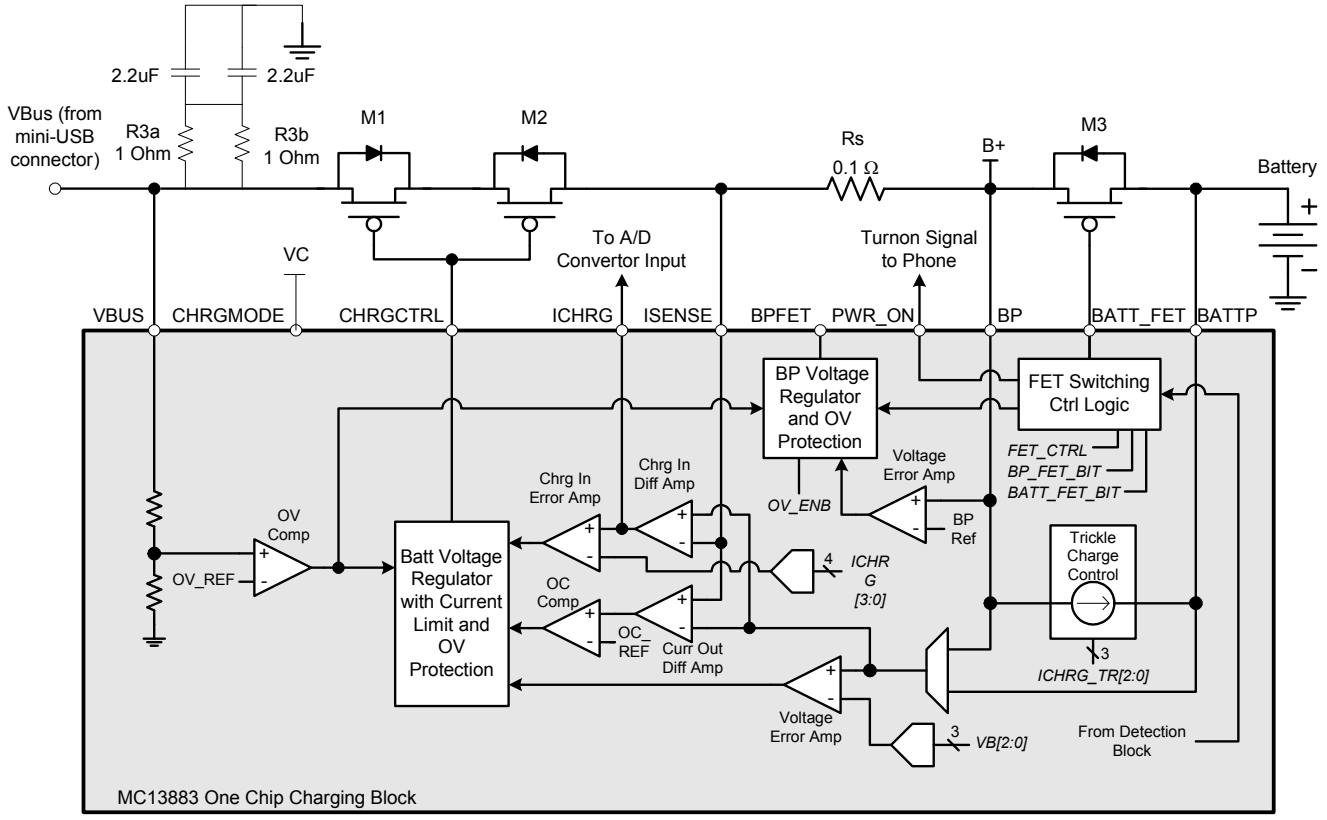

Figure 4. Serial-Path Charging Block Diagram

The serial path charging topology has the main charge path to the B+ node and a switch, M3, from the battery to the B+ node. When the battery is above 3.2 V, the charge current will pass to the battery via the B+ node. If the battery is below 3.2 V, FET M3 is opened and the charge path regulator powers the B+ node, so the phone can operate, the on-chip trickle current path simultaneously charges the battery. This way, the phone can turn on even with a deeply discharged battery.

There are redundant 1 ohm and 2.2 uF capacitors on the VBUS pin which are required parts for stability reasons. Each of the 2.2 uF capacitors should be X5R or better with a minimum capacitance of 1.3 uF with 5 volts applied.

The value of a ceramic capacitor is a function of the voltage applied to it. It should be rated for a high voltage, such as 20 volts to withstand failed chargers.

The selection of devices appropriate for M1 and M2 should be made carefully because of stability issues. The recommended device for these locations is shown in Table 5.

4.2.3 Single-Path Charging

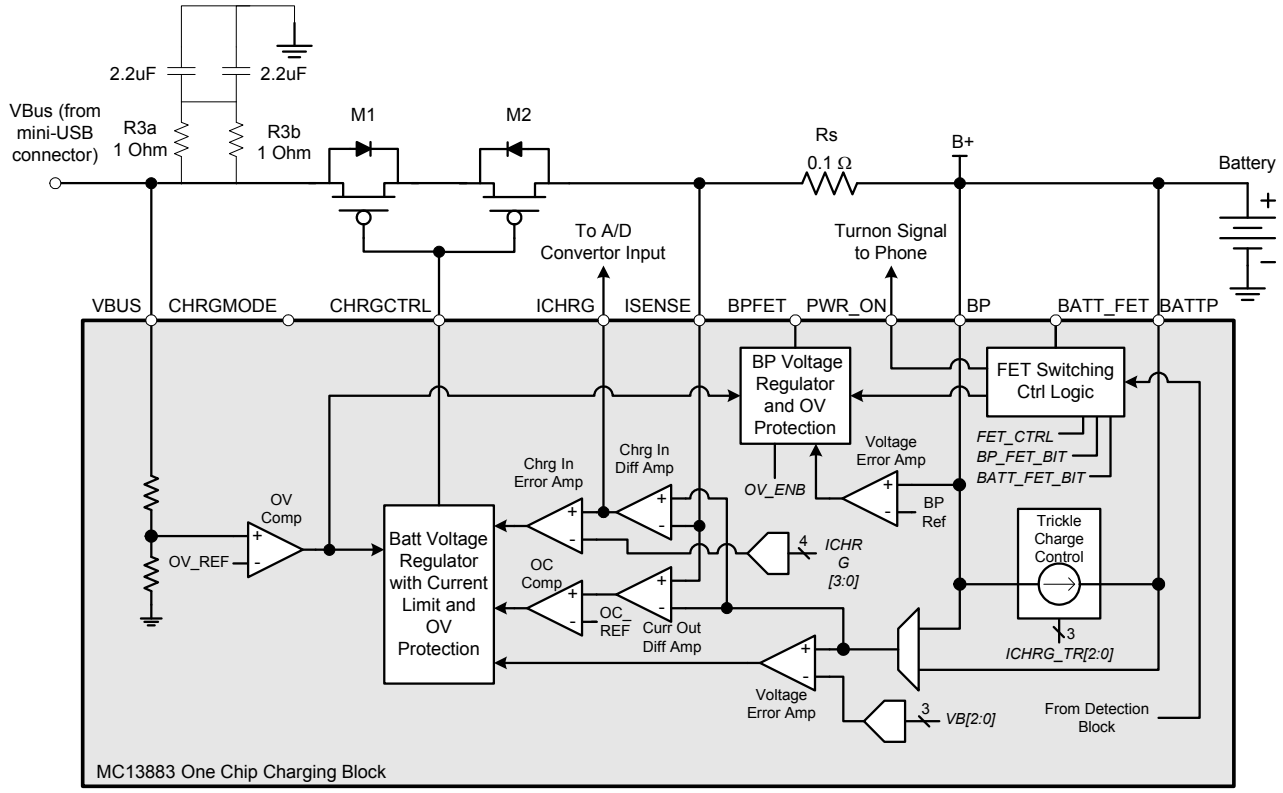

Figure 5. Single-Path Charging Block Diagram

As implied by its name, a single-path charging topology has only one path from the charger to B+. The phone operates from the voltage at the battery terminals during charge, if the battery is significantly discharged, the phone will not turn on until the battery has charged to 3.2 V.

There are redundant 1 Ω and 2.2 uF capacitors on the VBUS pin which are required parts for stability reasons. Each of the 2.2 uF capacitors should be X5R or better with a minimum capacitance of 1.3 uF with 5 volts applied.

The value of a ceramic capacitor is a function of the voltage applied to it. It should be rated for a high voltage, such as 20 volts to withstand failed chargers.

The selection of devices appropriate for M1 and M2 should be made carefully because of stability issues. The recommended device for these locations is shown in Table 5.

Table 5. FET Combinations

	M1	M2	M4
Combination 1	Si8401	Si8401	Si8401 or FDZ291P
Combination 2	Si8415	Si8401	Si8401 or FDZ291P
Combination 3	FDZ293P	FDZ293P	Si8401 or FDZ293P

4.2.4 Charger Block Signal Description

BATTP (BATT+)

Connection to the phone main battery positive terminal.

B+ (BP pin)

B+ is the main phone supply rail. Most internal voltage rails are derived from this supply. B+ is derived from the charger input (VBUS) and the main battery supply (BATT+).

CHRGCTRL

Charge control output voltage.

ICHRG

Muxed output voltage proportional to the charge current or the ID voltage.

ISENSE

Current sense input to the charge control circuitry.

PWR_ON

Turn-on signal to phone.

CHRGMODE

Selects whether the phone is configured for single-path, serial-path or dual-path charging. In order to select single path mode, the CHRGMODE pin should be left floating. For Serial Path, CHRGMODE pin is connected to the output of regulator V_C. For dual-path, CHRGMODE should be grounded.

VBUS

Charger input to phone.

BATT_FET

Gate drive to the battery FET (M3). This FET connects/disconnects the battery from the B+ (BP) node.

BP_FET

Gate drive to the BP FET (M4). This FET regulates the voltage at the BP or can be controlled as a switch. In single-path charging mode BP_FET is not used and can be left floating in single-path charging mode.

BATTPON (Internal Signal)

The BATTPON threshold is the threshold above which the phone will turn on while charging in either single-path mode or with a USB charger in serial- or dual-path mode.

CHRG_CURR (Internal Signal)

The CHRG_CURR threshold is 20 mA and is used as part of charger detection.

CHRGDET (Internal Signal)

The CHRGDET threshold is the voltage at the VBUS pin that indicates that a valid charger has been attached.

Table 6. CHRGDET, BATTPON and CHRG_CURR Thresholds

Parameter	Description	Min	Typ	Max	Unit
BATTPON Threshold	Low to High	3.33	3.43	3.53	Volts
BATTPON Hysteresis		50		200	mV
CHRGDET Threshold	Low to High	3.70		3.90	Volts
CHRGDET Threshold	High to Low	3.50		3.75	Volts
CHRGDET Hysteresis		50			mV
CHRG_CURR Threshold	High to Low	10	20	30	mA
CHRG_CURR Hysteresis			0.2		mA

4.2.5 Charger Control Logic

Tables 7, 8 and 9 show the BP_FET and BATT_FET states and charge and trickle currents as a function of Vbus, ID, BATTP voltage, RESETB, DP, DM inputs and FET_OVRD and FET_CTRL bits. This information is separated into 3 tables, Table 7 for dual path, Table 8 for serial path and Table 9 for single path.

Table 7. Charge Control Logic Table (Dual Path)

Vbus	ID	RESETB	DP	DM	FET_OVRD	FET_CTRL	BATTP Voltage	BP Regulator BP_FET (Dual Path Only)	BATT_FET	Charge Regulator	Trickle Charge	PWR_ON Signal	Description
H	<3V	L	L	L	X	X	<BATTPON	OFF	H	100 mA	OFF	L	USB Host Attach. Limited activation current, Open BP_FET, open BATT_FET
H	<3V	L	L	H	X	X	<BATTPON	OFF	H	100 mA	OFF	L	USB Host Attach. Limited activation current, Open BP_FET, open BATT_FET
H	<3V	L	H	L	X	X	<BATTPON	OFF	H	100 mA	OFF	L	USB Host Attach. Limited activation current, Open BP_FET, open BATT_FET
H	<3V	L	L	L	X	X	>BATTPON	OFF	L	100 mA	OFF	H	USB Host Attach. Limited activation current, Open BP_FET, open BATT_FET
H	<3V	L	L	H	X	X	>BATTPON	OFF	L	100 mA	OFF	H	USB Host Attach. Limited activation current, Open BP_FET, open BATT_FET
H	<3V	L	H	L	X	X	>BATTPON	OFF	L	100 mA	OFF	H	USB Host Attach. Limited activation current, Open BP_FET, open BATT_FET
H	<3V	L	H	H	X	X	<BATTPON	ON	H	OFF	OFF	H	Charger attached, Phone off, no activation current. FET controlled by SPI and Seamless comparator.
H	<3V	L	H	H	X	X	>BATTPON	ON	H	OFF	OFF	H	Charger attached, Phone off, no activation current. FET controlled by SPI and Seamless comparator.
H	<3V	H	L	L	0	X	X	OFF	L	*ICHRG bits	*ICHRG_TR bits	H	Charger or USB Host attached, Phone on, no activation current. FET controlled by Seamless comparator
H	<3V	H	L	H	0	X	X	OFF	L	*ICHRG bits	*ICHRG_TR bits	H	Charger or USB Host attached, Phone on, no activation current. FET controlled by Seamless comparator
H	<3V	H	H	L	0	X	X	OFF	L	*ICHRG bits	*ICHRG_TR bits	H	Charger or USB Host attached, Phone on, no activation current. FET controlled by Seamless comparator
H	<3V	H	H	H	0	X	X	ON	H	*ICHRG bits	*ICHRG_TR bits	H	Charger or USB Host attached, Phone on, no activation current. FET controlled by Seamless comparator
H	<3V	H	X	X	1	0	X	ON	H	*ICHRG bits	*ICHRG_TR bits	H	Charger or USB Host attached, Phone on, no activation current. FET controlled by SPI FET_CTRL bit
H	<3V	H	X	X	1	1	X	OFF	L	*ICHRG bits	*ICHRG_TR bits	H	Charger or USB Host attached, Phone on, no activation current. FET controlled by SPI FET_CTRL bit
H	>3V	X	X	X	X	X	<BATTPON	ON	H	*ICHRG bits	*ICHRG_TR bits	H	Factory Mode, no activation current. FET controlled by SPI and Seamless comparator
H	>3V	X	X	X	X	X	>BATTPON	ON	H	*ICHRG bits	*ICHRG_TR bits	H	Factory Mode, no activation current. FET controlled by SPI and Seamless comparator
L	X	X	X	X	X	X	X	OFF	L	OFF	OFF	L	No Charger or USB Host attaced, no activation current. FET controlled by SPI and Seamless comparator

Table 8. Charge Control Logic Table (Serial Path)

Vbus	ID	RESETB	DP	DM	FET_ OVRD	FET_ CTRL	BATTP Voltage	BATT_FET	Charge Regulator	Trickle Charge	PWR_ON Signal	Description
H	<3V	L	L	L	X	X	<BATTPON	L	100 mA	OFF	L	USB Host Attach. Limited activation current, Open BP_FET, open BATT_FET
H	<3V	L	L	H	X	X	<BATTPON	L	100 mA	OFF	L	USB Host Attach. Limited activation current, Open BP_FET, open BATT_FET
H	<3V	L	H	L	X	X	<BATTPON	L	100 mA	OFF	L	USB Host Attach. Limited activation current, Open BP_FET, open BATT_FET
H	<3V	L	L	L	X	X	>BATTPON	L	100 mA	OFF	H	USB Host Attach. Limited activation current, Open BP_FET, open BATT_FET
H	<3V	L	L	H	X	X	>BATTPON	L	100 mA	OFF	H	USB Host Attach. Limited activation current, Open BP_FET, open BATT_FET
H	<3V	L	H	L	X	X	>BATTPON	L	100 mA	OFF	H	USB Host Attach. Limited activation current, Open BP_FET, open BATT_FET
H	<3V	L	H	H	X	X	<BATTPON	H	Full Rate	OFF	H	Charger attached, Phone off, no activation current. FET controlled by SPI and Seamless comparator.
H	<3V	L	H	H	X	X	>BATTPON	H	Full Rate	OFF	H	Charger attached, Phone off, no activation current. FET controlled by SPI and Seamless comparator.
H	<3V	H	L	L	0	X	X	L	*ICHRG bits	*ICHRG_TR bits	H	Charger or USB Host attached, Phone on, no activation current. FET controlled by Seamless comparator
H	<3V	H	L	H	0	X	X	L	*ICHRG bits	*ICHRG_TR bits	H	Charger or USB Host attached, Phone on, no activation current. FET controlled by Seamless comparator
H	<3V	H	H	L	0	X	X	L	*ICHRG bits	*ICHRG_TR bits	H	Charger or USB Host attached, Phone on, no activation current. FET controlled by Seamless comparator
H	<3V	H	H	H	0	X	X	Upon entry into this state, H if already in Full Rate Otherwise L	*ICHRG bits	*ICHRG_TR bits	H	Charger or USB Host attached, Phone on, no activation current. FET controlled by Seamless comparator
H	<3V	H	X	X	1	0	X	H	*ICHRG bits	*ICHRG_TR bits	H	Charger or USB Host attached, Phone on, no activation current. FET controlled by SPI FET_CTRL bit
H	<3V	H	X	X	1	1	X	L	*ICHRG bits	*ICHRG_TR bits	H	Charger or USB Host attached, Phone on, no activation current. FET controlled by SPI FET_CTRL bit
H	>3V	X	X	X	X	X	<BATTPON	H	Full Rate	*ICHRG_TR bits	H	Factory Mode, no activation current. FET controlled by SPI and Seamless comparator
H	>3V	X	X	X	X	X	>BATTPON	H	Full Rate	*ICHRG_TR bits	H	Factory Mode, no activation current. FET controlled by SPI and Seamless comparator
L	X	X	X	X	X	X	X	L	OFF	OFF	L	No Charger or USB Host attaced, no activation current. FET controlled by SPI and Seamless comparator

Table 9. Charge Control Logic Table (Single Path)

Vbus	ID	RESETB	DP	DM	FET_OVRD	FET_CTRL	BATTP Voltage	BATT_FET	Charge Regulator	Trickle Charge	PWR_ON Signal	Description
H	<3V	L	L	L	X	X	<BATTPON	N/A	100 mA	N/A	L	USB Host Attach. Limited activation current, Open BP_FET, open BATT_FET
H	<3V	L	L	H	X	X	<BATTPON	N/A	100 mA	N/A	L	USB Host Attach. Limited activation current, Open BP_FET, open BATT_FET
H	<3V	L	H	L	X	X	<BATTPON	N/A	100 mA	N/A	L	USB Host Attach. Limited activation current, Open BP_FET, open BATT_FET
H	<3V	L	L	L	X	X	>BATTPON	N/A	100 mA	N/A	H	USB Host Attach. Limited activation current, Open BP_FET, open BATT_FET
H	<3V	L	L	H	X	X	>BATTPON	N/A	100 mA	N/A	H	USB Host Attach. Limited activation current, Open BP_FET, open BATT_FET
H	<3V	L	H	L	X	X	>BATTPON	N/A	100 mA	N/A	H	USB Host Attach. Limited activation current, Open BP_FET, open BATT_FET
H	<3V	L	H	H	X	X	<BATTPON	N/A	**100 / 300 mA	N/A	L	Charger attached, Phone off, no activation current. FET controlled by SPI and Seamless comparator.
H	<3V	L	H	H	X	X	>BATTPON	N/A	**100 / 300 mA	N/A	H	Charger attached, Phone off, no activation current. FET controlled by SPI and Seamless comparator.
H	<3V	H	L	L	X	X	X	N/A	*ICHRG bits	N/A	H	Charger or USB Host attached, Phone on, no activation current. FET controlled by Seamless comparator
H	<3V	H	L	H	X	X	X	N/A	*ICHRG bits	N/A	H	Charger or USB Host attached, Phone on, no activation current. FET controlled by Seamless comparator
H	<3V	H	H	L	X	X	X	N/A	*ICHRG bits	N/A	H	Charger or USB Host attached, Phone on, no activation current. FET controlled by Seamless comparator
H	<3V	H	H	H	X	X	X	N/A	*ICHRG bits	N/A	H	Charger or USB Host attached, Phone on, no activation current. FET controlled by Seamless comparator
H	<3V	H	X	X	X	X	X	N/A	*ICHRG bits	N/A	H	Charger or USB Host attached, Phone on, no activation current. FET controlled by SPI FET_CTRL bit
H	<3V	H	X	X	X	X	X	N/A	*ICHRG bits	N/A	H	Charger or USB Host attached, Phone on, no activation current. FET controlled by SPI FET_CTRL bit
H	>3V	X	X	X	X	X	<BATTPON	N/A	***100/300/ 600 mA	N/A	L	Factory Mode, no activation current. FET controlled by SPI and Seamless comparator
H	>3V	X	X	X	X	X	>BATTPON	N/A	***100/300/ 600 mA	N/A	H	Factory Mode, no activation current. FET controlled by SPI and Seamless comparator
L	X	X	X	X	X	X	X	N/A	OFF	N/A	L	No Charger or USB Host attaced, no activation current. FET controlled by SPI and Seamless comparator

* The control logic writes to the ICHRG[3:0] bits in the Power Control Register to set the current as indicated in the table above. When these bits are written to, the software overrides these settings.

** In single path mode, the maximum activation charge current varies according to the battery voltage. When BATTP <2.7 V, the maximum charge current is 100 mA, when BATTP >2.7 V, the maximum charge current is 300 mA.

*** In factory, single path mode, an additional current step allows the phone to automatically turn on when no battery is present. The maximum charge current in this case is 100mA when BATTP < 2.7 V, 300 mA when 2.7 V< BATTP <3.7 V, and 600 mA when BATTP >3.7 V.

**** For the purpose of this table, when the BP Regulator / BP_FET column indicates an “ON” condition, the BP regulator is ON if BP_SWITCH=0 (the BP Regulator is being used as a regulator). If BP_SWITCH=1 (indicating that the BP Regulator is acting as a switch) then an “ON” in this column indicates that the BP_FET should be driven low. An “OFF” condition in this column indicates that the BP regulator should be OFF (BP_SWITCH=0) or the BP_FET should be driven high (BP_SWITCH=1).

4.2.6 ICHRG Output

The ICHRG pin outputs either a voltage that is proportional to the current through Rs, the sense resistor, or outputs a voltage that is proportional to the ID pin voltage.

When the Charge regulator is enabled, the ICHRG pin outputs a voltage that is proportional to the current through Rs (from ISENSE to either BP or BATTP). When Reverse mode is enabled (RVRS_MODE = 1), the ICHRG pin outputs a voltage that is proportional to the current through Rs (from either BP or BATTP to ISENSE). This voltage is scaled from 0 to 2.3 V for currents from 0 to 1.8 A (full scale). The accuracy of the ICHRG voltage should be ±10% of the actual charge current (after scaling) for charge currents greater than 100 mA. For charge currents less than 100 mA, the accuracy requirement is ±10 mA compared to the actual charge current.

If both the Charge Regulator and Reverse mode are disabled, the ICHRG pin outputs a voltage that is proportional to the ID pin.

In idle mode, the MC13883 IC draws extra current when the MUX associated with the ICHRG pin is enabled. This extra current is significant enough that standby time will be affected. To disable drive to this pin, the ID_ICHRG_MUX_ENB can be asserted as listed in Table 50, Register 04 - Power Control 1 as Bit 4.

The ID pin voltage or the CHRG_I current will not be able to be read when this pin is disabled. When the MUX is disabled, the ICHRG pin is high impedance.

The ICHRG pin will have an output impedance of a maximum of 1.5 kΩ for load currents of 10 uA or less.[1]

Table 10. Charge Control Logic Table

Signal	Condition	Input Range	Equation	Tolerance
ICHRG	Charge Regulator Enabled	Icharge = 0 – 1.8A	Icharge*(2.3V/1.8A)	+/- 50 mV for Icharge ≤ 391mA, +/- 10% for Icharge > 391mA
ICHRG	RVRS_MODE = 1	Idischarge = 0 – 1.8A	Idischarge*(2.3V/1.8A)	+/- 50 mV for Icharge < 391 mA, +/- 10% for Icharge > 391 mA
ICHRG	ICHRG[3:0] = 0 and RVRS_MODE = 1	ID = 0 to 5V	ID Voltage*0.9	+ 75 mV/-3% for ID < 1.0 V, +/- 3% for 1.0 V < ID < 2.2 V, ICHRG = 2.2 V to 2.5 V for ID = 5.0 V

1. For version 3.1, the ICHRG output impendance in ID mode is ~50 kΩ.

4.2.7 Over-voltage Protection

There are three paths in the MC13883 IC that are protected from an over-voltage event: through the two external paths present in dual path charging as well as an internal path from VBUS to the USB section of the IC. When an over-voltage condition is sensed at the VBUS pin, all 3 paths are opened. This is accomplished by driving the CHRGCTRL and BP_FET pins high while opening the internal path. When an OV condition occurs, an interrupt will occur (VBUSOV_INT). Also, the ICHRG bits will clear and the BP regulator will be disabled.

The VBUSOV_SNS bit can be read to see if the OV condition has cleared.

Once the OV condition clears, the BP regulator will re-enable (in Dual Path mode) however the ICHRG bits will have to be reprogrammed by software.

Table 11. Over-voltage Protection Performance Specifications

Parameter	Condition	Min	Typ	Max	Units
Input/output voltage range	VBUS, CHRGCTRL, BP_FET	3.0		20	V
Input Voltage Slew Rate [dv/dt]Rise	0V< VBUS < 20V, at power up	0.00125		360	V/µs
Input Voltage Slew Rate [dv/dt]Rise	3V< VBUS < 20V, While in normal operation	0.00125		12	V/µs
OV Comparator Voltage Threshold (VTh), measured at VBUS	High to Low, Low to High	5.6	5.75	5.9	V
OV Comparator Voltage Hysteresis (VHyst), measured at VBUS		50		200	mV
Turn-off delay (TOFF)	CL=6nF, VBUS > VTh to CHRGCTRL=VBUS and BP_FET=VBUS			1	µs

4.2.8 Reverse Charge Mode

This mode allows the current to be sourced from the battery out the VBUS line to be used to power or charge external devices. The FET's M1 and M2 are turned on with CHRGCTRL and current is monitored through Rs from BP or BATTP to ISENSE. This mode is enabled with SPI Bit: RVRS_MODE. The current limit that disables the function and generates an interrupt (RVRS_MODE_INT) is shown in Table 4.

Because there may be a large capacitor in the phone powered device which needs to be charged and because rapid charging of it may cause a transient dip in the Battery voltage, the rate that M1 and M2 get turned on is controlled. The reverse path enable current is specified in Table 12. The rate at which M1 and M2 turn on is slowed as a result and the external large capacitor is charged up slowly.

In the event of a short in the phone powered device, the current flowing from the battery to the phone powered device may be excessive. A dual threshold system is employed so that the phone powered device path will shut off very quickly for high currents and will not trip for lower transient currents.

If the current through Rs goes above the first threshold Rth1 for a duration inside the RCR1 time window, without going over Rth2, then the Phone Powered Device path will be opened and an interrupt shall be generated.

If the current through Rs goes above the first threshold Rth2 for a duration above the RCR2 time threshold, then the Phone Powered Device path will be opened and an interrupt shall be generated.

Table 12. Reverse Over-current Protection Performance Specifications

Parameter	Condition	Min	Typ	Max	Units
Reverse Path Enable Current	CHRGCNTRL Pin Sink Current (RVRS_MODE bit = 1)	2	4	6	µA
Reverse Current Threshold 1 (Rth1)	Current Threshold 1	725	800	1010	mA
Reverse Current Threshold 2 (Rth2)	Current Threshold 2	1.7	-	2.3	A
Reverse Current Reaction Time 1 (RCR1)	Rth2 > Current > Rth1	1	-	5	mS
Reverse Current Reaction Time 2 (RCR2)	Current > Rth2	100	-	200	µS
RVRS_CHRG_INT current threshold (RCT)	RVRS_MODE=1, this current threshold applies to current flowing through the 100 mΩ sense resistor in the direction towards the battery	1	20	30	mA
RVRS_MODE Delay	Following RVRS_CHRG_INT being set by the hardware, the software needs to wait for at least this amount of time before enabling RVRS_MODE path.	1	-	5	mS

When RVRS_MODE = 1, then the phone will be sourcing power, not receiving power from the VBUS pin of the USB connector. Because the VCHRG regulator will be disabled in this mode, ensure the battery doesn't accidentally get charged in this mode. If the current going into the battery goes above 20 mA threshold (RCT) for a debounce period described in Table 41, then the RVRS_MODE path will be turned off and the RVRS_CHRG_INT bit will be set and the RVRS_MODE bit is cleared. Before re-enabling the RVRS_MODE path, the source of the over current condition should be understood and corrected. The RVRS_MODE bit cannot be set again until 1 ms has elapsed from the time of the interrupt. If the software tries to program the RVRS_MODE bit before 1ms has passed, the bit will remain cleared and the path will remain disabled.

If the software tries to program RVRS_MODE to 1 when the IC is not ready (within this 1 ms period), the RVRS_MODE bit will remain cleared and the RVRS path will remain disabled.

4.2.9 Charge Current Regulation

The ICHRG[3:0] bits set the maximum current for the main charger, as shown in Table 13. This current is the actual current that flows through the 100 MΩ sense resistor. It does not include any other currents that go into the CHRGRAW/VBUS pins including the charge LED.

Table 13. Battery Charge Current Control Settings

Parameter	Value	Charge Current (in mA)		
		min	nom	max
ICHRG[3:0]	0000	0	0	0
	0001	55	70	85
	0010	141	177	213
	0011	212	266	320
	0100	319	355	390
	0101	398	443	488
	0110	478	532	585
	0111	558	621	6835
	1000	638	710	781
	1001	717	798	878
	1010	797	886	976
	1011	877	975	1073
	1100	957	1064	1170
	1101	1037	1152	1268
	1110	1276	1596	1915
	1111[A]	Fully On - Disallow battery FET to be turned on in hardware		

[A] As an additional layer of protection, in mode 1111, “fully on”, BATT_FET will not attempt to turn on the path to B+.

Redundant 1 ohm and 2.2 uF capacitors on the VBUS pin are required parts for stability reasons. Each of the 2.2 uF capacitors should be X5R or better with a minimum capacitance of 1.3 uF with 5 volts applied.

The value of a ceramic capacitor is a function of the voltage applied to it. It should be rated for a high voltage, such as 20 volts to withstand failed chargers. See Figure 3, Figure 4, and Figure 5 for more information.

4.2.10 Trickle Charging

The ICHRG_TR[2:0] bits set the maximum current for the trickle charger, as shown in Table 14. The current tolerance is ± 30% (the table shows the nominal values in mA). This Trickle Charger is of use when the Battery is low while in the Serial Path Configuration. The values in Table 14 are valid for a difference between BP and BATTP of 1.0 Volt or more. When operated with a headroom of 0.8 Volts, the trickle current level will degrade from ± 30% to ± 40%.

Table 14. Trickle Charge Current Control Settings

Parameter	Value	Trickle Charge Current (in mA)		
		Min	Nom	Max
ICHRG_TR[2:0]	000	0	0	0
	001	6	9	12
	010	14	20	26
	011	25	36	47
	100	29	42	55
	101	35	50	65
	110	41	59	77
	111	50	68	86

4.2.11 Standalone Trickle Charging

MC13883 has a standalone trickle charge mode of operation in order to ensure that a completely discharged battery can be charged without the microprocessor's control. This is especially important in single path configurations and when charging from a USB host.

Upon plugging a valid USB Host to the phone in Dual Path or Serial Path mode, the trickle cycle is started at a current of TRICKLEL and remains at this level until charging is terminated. The standalone trickle charger will terminate upon charger removal, an over-voltage condition, when the charge current falls below the CHRG_CURR threshold or if SPI register 3 is written.

Similarly, in Single Path mode, the trickle charger will start upon the insertion of a valid USB host except that the charge current will vary based on the battery voltage. For an extremely low battery, below BATTL, the trickle charge current level is set to the TRICKLEL. When the battery voltage increases above the BATTL threshold and the charger is not a USB host, the trickle charge level is increased to the TRICKLEM level. When the battery voltage rises above the BATTON threshold, which is sufficient voltage for phone operation, a power up sequence is automatically initiated. Standalone trickle charging will terminate under the same conditions as those when in Dual Path and Serial Path mode; charger removal, an over-voltage condition, when the charge current falls below the CHRG_CURR threshold, or if SPI register 3 is written.

In all charge modes even after the phone has powered up, the standalone trickle charger will remain on until software does an initial write to Register 3. Also, if the standalone trickle charger is enabled and a read is performed on Register 3 prior to re-writing the bits, ICHRG(3:0) will read back "0000".

During hardware trickle charging at TRICKLEL and TRICKLEM levels, The PWR_ON pin remains low until the BATTON threshold is crossed. If the battery voltage was already greater than BATTON when a charger is attached, the phone will power up immediately without starting a trickle charge cycle. In any case, the charge path regulator will ensure the battery voltage during trickle charging will not exceed the value as set by VCHRG[2:0].

If factory mode (UID > 3V) is detected in the single path charging configuration and the battery voltage is above BATTH comparator threshold, the charge current is set to TRICKLEH.

When plugging a USB host without a battery placed in the phone, the trickle charge cycle will cause the battery voltage to rise, creating a power up event by setting the PWR_ON signal high. However, because of USB requirements, the charge current is set to TRICKLEL and the phone will immediately shut down because there will not be enough current to sustain a power-up cycle.

Built-in control prevents the phone from continuously power-up and power-down due to this condition. As a result, when applying a battery to the phone at a later stage, the USB trickle charge will not automatically start until the USB cable is removed and reinserted.

Since normal LED control via the SPI bus is not possible in the standalone trickle mode, a current sink at the CHRGLED pin will be active as long as the standalone trickle charge is active. This means that the trickle LED will remain on until the charger is programmed by SPI. The LED can be connected to either BP or VBUS. Once the phone has powered on, the trickle LED can be disabled by clearing the CHRGLEDEN SPI bit. The trickle LED is also disabled when an over-voltage condition occurs unless the CHRGLEDEN bit was set high by software.

Table 15. Trickle Charge Main Characteristics

Trickle current TRICKLEL	ICHRG[3:0]=0001 [A]
Trickle current TRICKLEM	ICHRG[3:0]=0011
Trickle current TRICKLEH	ICHRG[3:0]=0110

[A] For battery voltages under ~2.4V, the current may be slightly lower during trickle charging.

Table 16. Battery Detectors Main Characteristics

Parameter Description	Min	Typ	Max	Units
BATTL Threshold Low to High	-3%	2.7	+3%	V
BATTON Threshold Low to High	-3%	3.43	+3%	V
BATTH Threshold Low to High	-3%	3.7	+3%	V

4.2.12 Charge Voltage Regulator (VCHRG)

This is the Regulator-Charger (Voltage and Current Control) that controls current through M1 and M2 using CHRGCTRL. For charging, it has the capability of regulating to a fixed voltage.

- It requires an output capacitor of 10 µF on both BP and BATTP pins.
- Output voltage sensing is done at the ISENSE pin.

- Output current sensing is either the BATTP or BP pin.
- An interrupt is generated when the charge goes from constant current to constant voltage (CC to CV).
- It is designed for use with an external current sensing resistor of 100 mΩ.

Table 17. VCHRG Output Voltage Settings

Parameter	Value	Battery Regulator Output Voltage (V)
VCHRG[2:0]	000	4.05
	001	4.375
	010	4.15
	011	4.20
	100	4.25
	101	4.30
	110	3.80
	111	4.50

Table 18. VCHRG Performance Specifications

Parameter	Condition	Min	Typ	Max	Units
Load Cap, CL	Regulating the BP node	5	10	30	µF
Load Cap, CL	Regulating the BATT+ node	5	10	30	µF
Load Capacitor ESR	At capacitor resonance	4	-	30	mΩ
Output Voltage	BP/BATTP, 100 µA < IL < 100mA, (Vout +500 mV) < Vin	Nom –1.25%	nom	nom + 1%	
Output Voltage	BP/ BATTP, 100 mA < IL < 1.5 A, (Vout +500 mV) < Vin	Nom —5%	nom	Nom + 1%	
PSRR	Vin = Vout +1 V IL = 75% of Imax	20	-	-	dB
Start-Up Overshoot	IL = 0	-	1	-	%
Turn-on Time	ENABLE to 90% of Vout	-	-	100	ms
Transient Response	IL = 10 mA to 1.5A, Tr = 5 µs	-	1	-	%
VBUS to CHRGCTRL Voltage	Batt = 3.6V VBUS = 4.1V ICHRG ≠0000 Charge path is OPEN	1.9			V

4.2.13 PWR-ON

The PWR_ON signal has two functions. It is meant to turn on an external power management device when VBUS goes above the CHRGDET threshold. It is to be referenced to VBUS so that the charger voltage can be read by the phone's ADC.

Table 19. PWR_ON Performance Specifications

Parameter	Condition	Min	Typ	Max	Unit
PWR_ON Output High	VBUS > CHRGDET threshold Rload = 10 K	80% of VBUS			Volts
PWR_ON Output Low	VBUS < CHRGDET threshold			20% of VBUS	Volts

4.2.14 VC Regulator and Bandgap

The VC regulator is the MC13883's internal regulator. It gets powered by the BP or VBUS. It powers the bandgap. VC powers much of the ICs' internal functions. No external loading on VC or BG_BYP is allowed.

Table 20. VC and Bandgap Performance Specifications

Parameter		Target
VC	Output voltage in ON mode	2.775 V
	Accuracy in ON mode	3%
	Output voltage in OFF mode	2,65 V
	Bypass Capacitor	1 uF
Bandgap	Output voltage in ON mode	1.20 V
	Output voltage in OFF mode	0 V
	Absolute Accuracy	0.5%
	Temperature Drift	0.25%
	PSRR at BP = 3.0V	90 dB
	Bypass Capacitor	100 nF

4.2.15 Constant Current / Constant Voltage Sense Bit (CC_CV)

There are two phases used in the charging of lithium ion batteries, constant current and constant voltage. The sensing of the transition between these two phases is useful in charge metering.

During the constant current phase, the current regulator may be operating to regulate the current into the battery pack per the ICHRG bit settings or it may not be operating to regulate the current into the battery pack in the case of a collapsed charger. However, once the battery voltage reaches the VCHRG value, the voltage regulator will begin regulating. CC_CV is designed to trip at 97% of the programmed charge voltage, measured at the ISENSE Pin. A debounce and mask and interrupt bits are defined in Section 7, "SPI/I2C Register Tables", on page 53.

4.2.16 Shorted Charger Protection

If during the charge of a battery in the configurations of Section 4.2.1, “Dual-Path Charging Overview”, Section 4.2.2, “Serial Path Charging Overview”, and Section 4.2.3, “Single-Path Charging”, the charging input, CHRGRAW/VBUS is shorted to ground, a large current can flow from the battery pack out through M1/M2. This is undesirable.

Therefore, the ICHRG bits are automatically set to 0000 whenever the CHRGRAW voltage goes below the CHRG_DET threshold (see Table 6 in Section 4.2.4, “Charger Block Signal Description”) and the charge current going into the battery pack goes below the CHRG_CURR threshold (20 mA typical) as is the case when the current goes through M1/M2 in the direction towards CHRGRAW and debounced per the CHRG_CURR sense bit.

4.2.17 USB and Non-USB Dead Battery Recovery

The control logic in Section 4.2.5, “Charger Control Logic” supports this section. When a USB power source is connected, the IC recognizes it as a USB power source (no SE1). If the battery is low (less than the BATT_ON threshold of 3.43 volts), the M1/M2 charging path charges the battery at a charge rate below 100 mA (see ICHRG bit setting 0001). The phone is turn turned on, it enumerates, etc. and the battery finishes its charging.

When a non-USB power source is connected, the IC recognizes it as a non-USB power source by the presence of an SE1. The BP regulator will turn on, the main FET (M3) will turn off and the phone will power up. If the battery is low, it will need to be recovered in some way. If M1/M2 path is used, as the battery charges from below 2.5 volts to above 2.5 volts, a large current transient may occur. This does not occur if the internal trickle charger (controlled by the ICHRG_TR bits) is used. Therefore, it is strongly recommended that the internal trickle charger is used for dead battery recovery with non-USB chargers. This current transient when the battery is crossing 2.5 volts does not occur while USB charging (since BP regulator is off).

4.2.18 Charge LED (CHRGLED) Operation

In dual-path charging with a USB power source, the charging system is set up to be in current share mode (M4 - off, M3 - on, M1/M2 - on). With a depleted battery and a charger attached, the 'hardware' trickle is on at its 100 mA step until the battery charges to the BATTPON threshold. Then the phone will turn on and software can take control of the charging of the battery. Until this turn on event, the charged pins will be enabled and can be used as a sign-of-life signal for the system.

The CHRGLED is enabled whenever the 'hardware' trickle charge is enabled. In dual-path mode, 'hardware' trickle charging will be enabled when a USB power source is plugged into the phone that is off. Following this, the LED will remain on until the software writes to the ICHRG SPI bits. The CHRGLED is also enabled whenever the CHRGLEDEN SPI bit is set to 1, see Table 46—Table 51, Register 03 - Power Control 0 Bit 18.

Table 21. CHRGLED Performance Specifications

Parameter	Condition	Min	Typ	Max	Unit
CHRGLED Pin Voltage	Enabled	1.0			V
CHRGLED Current	Enabled	5.6	8	10.4	mA
CHRGLED Current	Disabled			1 uA	mA

4.2.19 Factory Mode Operation

Factory mode allows for the ability to power on the MC13883 through a USB cable without a battery being attached.

Factory mode is entered while when VBUS is greater than the CHRGDET threshold and ID is greater than 3.0 V. In this mode, the BP regulator is enabled without having an SE1 on D+ and D-. Therefore, power can be supplied to the system and the D+ and D- lines are kept free for normal USB transmission.

If the SPI bit ID_PU_CNTRL is set to a 1 while in factory mode, the IC will come out of factory mode which in turn disables the BP regulator.

4.2.20 BP Voltage Regulator (VB)

This regulator function controls FET M4 with the BPFET pin and regulates the voltage at pin BP (which is typically the phone's B+). This can be operated as a voltage regulator, or the regulator function can be disabled and the FET (M4) operated as a switch.

Table 22. VB Performance Specifications

Parameter	Condition	Min	Typ	Max	Units
Configuration Specifications					
Load Cap, CL		5	10	-	µF
Load Capacitor ESR	At capacitor resonance	4	-	30	mΩ
Performance Specifications					
Output Voltage	100 µA < IL < 1 A, (Vout +250 mV) < Vin; (Vin is the source of M4)	4.1	4.3	4.5	V
PSRR	Vin = Vout +1 V IL = 75% of Imax	20	-	-	dB
Start-Up Overshoot	IL = 0	-	1	-	%
Turn-on Time	ENABLE to 90% of Vout	-	-	1	ms
Transient Response	IL = 0 mA to Imax, Tr = 10 µs	-	1	-	%

4.2.21 USB Supply Voltage Generation

The two linear regulators that generate the USB supply rails are configured as shown in Figure 6. The 3 switches (sw1, sw2, and sw3) allow for a flexible means of powering the USB portion of the IC, depending

on the requirements of the system. VUSB can be powered by REG_5V_IN, VBUS, or B+ which is controlled by SPI register bits VUSB_IN[1:0] as shown in Table 23 below.

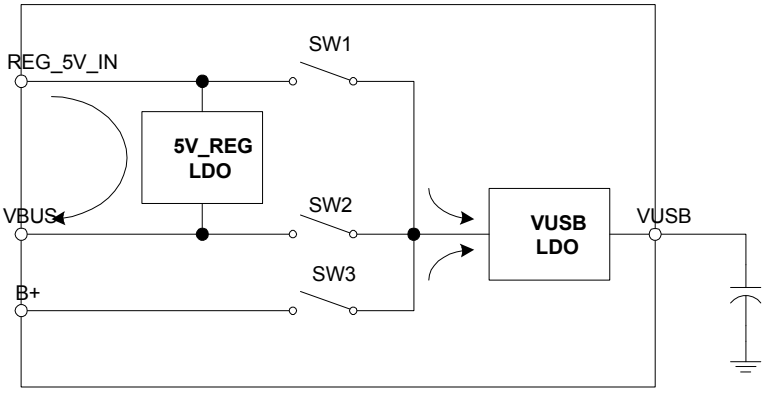

Figure 6. USB Supply Voltage Generation Block Diagram

Table 23. USB Switch Control

Parameter	Value	SW1	SW2	SW3
VUSB_IN[1:0]	00	Closed	Open	Open
	01	Open	Closed	Open
	10	Open	Open	Closed
	11	Open	Closed	Open

4.2.22 VUSB Voltage Regulator

Table 24. VUSB Control Register Bit Assignments

Parameter	Value	Function	Imax (mA)
VUSB0	0	output = 2.775 V	50
	1	output = 3.30 V	50

The performance of the VUSB regulator is shown in Table 25.

Table 25. VUSB Performance Specifications

Parameter	Condition	Min	Typ	Max	Units
Configuration Specifications					
Load Cap, CL		.65	1.0	6.5	µF
Load Capacitor ESR		0	-	0.5	Ω
Performance Specifications					
Output Voltage	100 µA < IL < Imax, (Vout+500mV) < Vin	nom. -3%	VUSB	3%	
Load Regulation	Vin = Vout +500 mV, 100 µA < IL < Imax	-	-	0.38	mV/mA

Table 25. VUSB Performance Specifications (continued)

Parameter	Condition	Min	Typ	Max	Units
Line Regulation	IL = 1 mA, (Vout +500 mV) < Vin <= BP max.	-	-	20	mV
Current Limit	Vin > (nom. Output + 500 mV), short circuit Vout	-	-	200	mA
PSRR	Vin = Vout +1 V IL = 75% of Imax	45	60	-	dB
Start-Up Overshoot	IL=0	-	1	-	%
Turn-on Time	ENABLE to 90% of Vout	-	-	1	ms
Transient Response	IL = 0 mA to Imax	-	-	3	%
V_dropout @ Imax		-	-	500	mV
V_dropout @ 1mA		-	-	250	mV
Active Quiescent current		-	-	25	µA
Discharge Resistor	Regulator disable	-	200	-	Ω
Output noise	100 Hz to 50 kHz	-	-	1	µV/√(Hz)
	50 kHz to 1 MHz	-	-	0.2	µV/√(Hz)

4.2.23 VBUS Voltage Generation

The VBUS regulator provides support for USB OTG master-mode operation, including SRP VBUS pulsing generation. Maximum output current (Imax) is 50mA in normal mode. The regulator has a controlled current limit of 200mA (nom). In addition to the normal mode of operation, the regulator has a secondary mode (selected by SPI control) in which the output current limit is 910 µA nominal.

Table 26. VBUS Regulator Performance Specifications

Parameter	Condition	Min	Typ	Max	Units
Configuration Specifications					
Load Cap, CL	On pin VBUS	1.3	2.2	6.5	µF
Load Capacitor ESR	@ the cap's resonant frequency	0	-	0.5	Ω
Performance Specifications					
Output Voltage	100 µA < IL < Imax, (Vout +250 mV) < Vin <= BP max	4.5	5V (nom)	5.15	V
Line Regulation	IL =1 mA, (Vout +250 mV) < Vin <= BP max	-	-	20	mV
Current Limit	Vin > (nom. output + 250 mV), short circuit Vout, 5V_REG_EN=1			300	mA
Current Limit	Vin > (nom. output + 250 mV), short circuit Vout, VBUS_PULSE_TMR[2:0]<>0005V_REG_EN=0	800	910	1500	µA
PSRR	Vin = Vout +1 V IL = 75% of Imax	30	-	-	dB
Start-Up Overshoot	IL = 0	-	1	-	%
Turn-on Time	ENABLE to 90% of Vout	-	-	1	ms
Transient Response	IL = 0 mA to Imax	-	-	3	%
V_dropout @ Imax		-	-	250	mV
Active Quiescent current		-	-	30	µA

4.2.24 VC Generator

The MC13883 has an internal voltage generator Vc. This voltage is used internally for a number of pull-up resistors and is also brought out to allow it to be used for CHRGMODE selection. A 1 µF capacitor must be connected to this pin.

5 Connectivity

To support the MC13883 bus data signaling modes the MC13883 IC contains a USB OTG transceiver and the UART controller. Audio switches are provided to support audio modes. Circuitry for accessory detection and identification is also incorporated.

5.1 Accessory Detection and Identification

Various Self Powered Devices (SPD) and Phone Powered Devices (PPD) may be connected to the MC13883 interface. In order to properly detect and identify each device that can be connected to the MC13883 bus, the VBUS Detector, ID Detector, and SE1 Detector, in conjunction with DP pull-up resistors and DP/DM pull-down resistors are implemented on the MC13883 IC.

5.1.1 VBUS Detector

The VBUS detector consists of three comparators that detect three levels on the VBUS pin. One comparator detects a 4.4 V level and is used to detect the VBUS valid threshold.

Two additional comparators detect a 0.8 V level and a 2.0 V level on the VBUS pin. These levels need to be detected to support two OTG session request protocol methods: “data line pulsing” and “VBUS pulsing”.

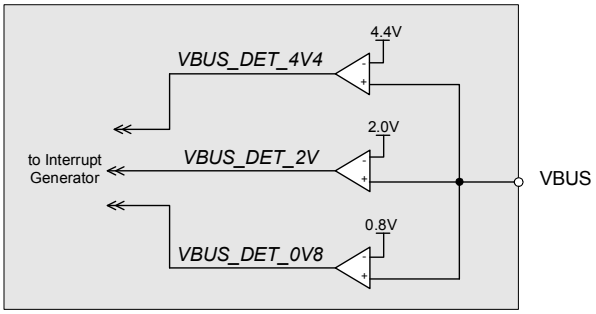

Figure 7. VBUS Detector Block Diagram

Each comparator can generate the *VBUS_DET_INT* interrupt at the high to low and low to high transition of its output. In addition, *VBUS_DET_4V4*, *VBUS_DET_2V*, and *VBUS_DET_0V8* bits are provided to indicate status of the corresponding comparator output.

The performance of the VBUS Detector is shown in Table 27.

Table 27. VBUS Detector Performance Specification

Parameter	Conditions	Min	Max	Unit
4.4 V VBUS Detector Comparator Turn On Threshold		4.4	4.65	V
4.4 V VBUS Detector Comparator Turn Off Threshold		4.4	4.65	V
4.4 V VBUS Detector Debounce Time	rising edge	15	20	ms
	falling edge	0.5	1	ms
4.4 V VBUS Detector Comparator Turn On Delay	VBUS>4.4V to VBUS_DET_4V4 = 1	-	100	µs
2 V VBUS Detector Comparator Turn On Threshold		1.6	2.0	V
2 V VBUS Detector Comparator Turn Off Threshold		1.6	2.0	V
2 V VBUS Detector Comparator Turn On Delay	VBUS>2V to VBUS_DET_2V = 1	-	100	µs
0.8 V VBUS Detector Comparator Turn Off Threshold		0.6	0.8	V

5.1.2 ID Detector

The ID Detector is used to determine if a mini-A or mini-B style plug has been inserted into a mini-AB style receptacle on the phone. It is also used for detection of a Phone Powered Device. In addition, the detector can be used to indicate a factory mode, this might be useful for phone designers. The detector senses the condition of the ID line and detects four levels on the ID pin:

- ID pin is floating (0.89 * VC < ID < 3V) – a B-type plug or no device is attached; indicates that a USB host, or default OTG master device, or no device is attached
- Resistor to ground is connected to the ID pin (0.18 * VC < ID < 0.77 * VC) – non-USB accessory is attached
- ID pin is grounded (ID < 0.12 * VC) – an A type plug is attached; indicates that the MC13883 IC is a default OTG master (A-Device)
- Voltage level on the ID pin is 3.3 V ±300 mV – factory mode

The block diagram in Figure 8 illustrates functionality of the ID detector.

Two different types of internal pull-ups can be connected to the ID line, depending on the state of the ID_PU_CNTRL bit. If ID_PU_CNTRL = 0, an internal 220 KΩ (+/-30%) resistor pulled to the VC supply is connected to the ID pin (SW1/SW3 closed, SW2/SW4 open). If ID_PU_CNTRL = 1, a 5 uA (+/-5%) current source is connected between VUSB and the ID pin (SW1/SW3 open, SW2/SW4 closed). The ID_PU_CNTRL bit defaults to "0".

In addition, the SW5 switch is provided to ground the ID pin. Refer to Section 5.2.4, “Mode Transitioning”, on page 43 for detail description of switch functionality.

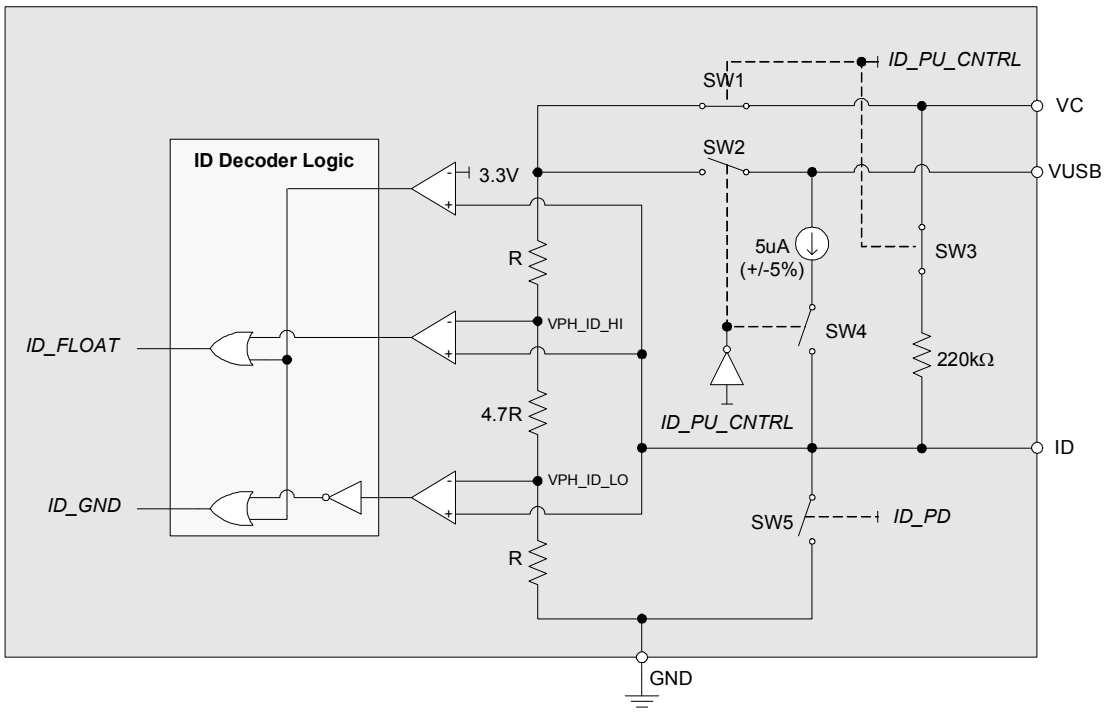

Figure 8. ID Detector Block Diagram

This block diagram describes functionality. It is not intended to describe the actual circuit implementation to be used.

Two bits are provided to indicate status of the ID line, as shown in Table 28.

Table 28. ID Pin Status Bits

ID_FLOAT	ID_GND	ID Pin Status
0	0	0.12 * VC < ID < 0.89 * VC
0	1	ID < 0.12 * VC
1	0	0.89 * VC < ID < VC
1	1	ID > 3.3 V

Each time the ID line changes its status the *ID_INT* interrupt is generated. When the VUSB regulator is disabled, the MC13883 needs to be able to detect at least ID interrupts generated by ID_FLOAT and ID_GND changing their status to 00, 01, or 10. In addition, the CHRGDETI interrupt needs to be detected while the VUSB regulator is disabled.

Detection of an interrupt includes setting the EMU_INT pin high.

Due to an interaction in the IC design, when the ID pin has no load (open) and the 5 uA current source pull-up is selected (IDPUCTRL=1), the IC can enter factory mode. Therefore, in order to avoid this scenario, factory mode is disabled when IDPUCTRL bit is set to 1 (5 uA pull-up selected).

When factory mode is desired (ID pin pulled > VUSB) and the IDPUCTRL bit is set to 1, the BP regulator may be turned off and M3 turned on. To keep this from happening, the following steps should be taken on phone power up:

1. Apply VBUS and ID pin voltages to enter factory mode. The phone turns on and the ID_PU_CNTRL defaults to 0.
2. Put the control of the BP regulator and M3 under software control by setting the FET_OVRD and FET_CTRL bits appropriately. Thus, the entry and exit from factory mode will not affect the switching of power paths to BP and BATTP.

5.1.3 SE1 Detector

The SE1 detector is used for identification of a self powered or phone powered device. The detector senses the condition of DP and DM lines and sets its output high if DP and DM are both high (SE1 condition). The detector output is de-bounced for approximately 1ms to generate the SE1_DET_INT interrupt on a high to low and low to high transition. The SE1_DET bit is provided to indicate status of the SE1 Detector output.

Table 29. SE1 Detector

Parameter	Conditions	Min	Typ	Max	Unit
SE1 Detector Input High Voltage	DP and DM	1.8	-	-	V
SE1 Detector Debounce Time	Rising Edge	-	1	-	ms

The IC separates the SE1 detector output, in that it goes separately to the charger circuitry and to the SPI sense/interrupt bit circuitry. When DM and DP are high (an SE1 condition), the SE1S bit will not always identify that an SE1 is present. The SE1S bit will always read as a zero when VBUS is less than the CHRG_DET threshold (Table 6).

When DM and DP are high and VBUS is less then the CHRG_DET threshold, the charging circuitry will operate properly even though the SE1 sense bit indicates otherwise. Therefore, when an SE1S bit reads zero, it is recommended that, using USB suspend mode, DM and DP are individually read to see if an SE1 is or isn't present.

5.1.4 DP Pull-Up and DP/DM Pull-Down Resistors

The MC13883 IC has integrated pull-up resistors on the DP line and pull-down resistors on the DP and DM lines (D+ and D-). These resistors can be switched in or out individually via control bits. The resistors' implementation is shown in Figure 9.

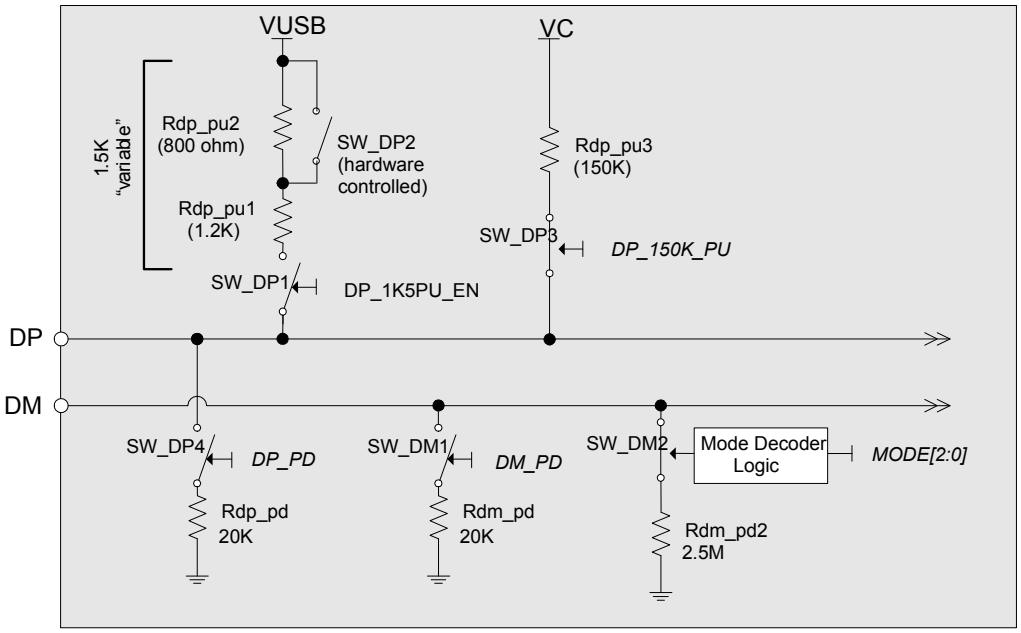

Figure 9. DP/DM Pull-Up and Pull-Down Resistors

SW_DP1 is used to switch in or out the variable DP pull-up resistor, while the combination of SW_DP2, Rdp_pu1 and Rdp_pu2 determine the resistor value in different bus states.

Switch SW_DP1 can be switched in and out via the *DP_1K5_PU* bit (switch closed if *DP_1K5_PU* = 1). Because during the data-line pulsing method of the OTG Session Request Protocol the DP line needs to be pulled up for a duration of 5 to 10 ms (full speed), the DP_SRP Timer of 7.5 ms (±2.5 ms) duration is implemented to time this task. The timer is enabled if *DP_SRP* = 1. When the timer duration expires, the SW_DP1 switch opens and *DP_SRP* bit is cleared. If *DP_SRP* is set high while *DP_1K5_PU* = 1, then the SW_DP1 switch remains closed as long as *DP_1K5_PU* = 1. The SW_DP1 switch defaults to an OPEN state when a power is applied to the device. When the USB_EN pin is asserted high while the USB_CNTRL bit is set high, the switch automatically closes, regardless of the state of the other SPI/I2C bits. Refer to Section 5.3, "Power-Up Control" for detailed description of the USB_EN pin functionality.

The SW_DP2 switch is controlled by hardware. When the bus is idle, the switch is closed and the DP pull-up resistor is set to 1.2 kΩ (900-1575 Ω), (SW_DP1 & SW_DP2 both closed). When the upstream device is transmitting data (J-K transition or J-SE0 transition detected), the switch is open and the DP pull-up resistor is set to about 2 kΩ (1425-3090 Ω), (SW_DP1 only closed).

In addition to the variable pull-up resistor, a 150 kΩ pull-up resistor to the VC supply is provided on the DP (D+) line. This resistor is used for the accessory identification when the phone is on and the variable pull-up is switched out. SW_DP3 connecting the 150 kΩ resistor is controlled by the *DP_150K_PU* bit; when *DP_150K_PU* = 1, the switch is closed and the 150 k pull-up resistor is connected to the DP line. The SW_DP3 switch defaults to a CLOSED state when power is applied to the device.

One DP and two DM pull-down resistors are also integrated. The Rdp_pd pull-down on the DP line is switched in and out via the *DP_PD* bit (switched in if *DP_PD* = 1). The Rdm_pd pull-down on the DM line is switched in and out via the *DM_PD* bit (switched in if *DM_PD* = 1). Rdp_pd and Rdm_pd are both about 20 kΩ (14.25 to 24.8 kΩ), in accordance with the USB ECN for Pull-Up/Pull-Down Resistor. At power up, both pull-downs are switched out. A 2.5 MΩ (±1.5 MΩ) pull-down resistor on the DM line is connected by default and is automatically disconnected in mono and stereo audio modes (MC13883 *MODE[2:0]* of 100 or 101).

The variable 1.5 kΩ DP pull-up and DP/DM 20 kΩ pull-downs are disconnected from the DP and DM lines during transmit. This is controlled via the TXENB line, such that when the transceiver is in transmit mode (TXENB=0), the internal control signals are overridden and the pull-up / pull-downs are disconnected. This is done to save battery power. If the bit *PULLOVR* = 0 this function is disabled.

In addition, the *SE0_CONN* bit is provided to automatically connect the variable 1.5 kΩ DP pull-up resistor when SE0 is detected.

The block diagram in Figure 10 illustrates the variable DP 1.5 kΩ pull-up control circuit.

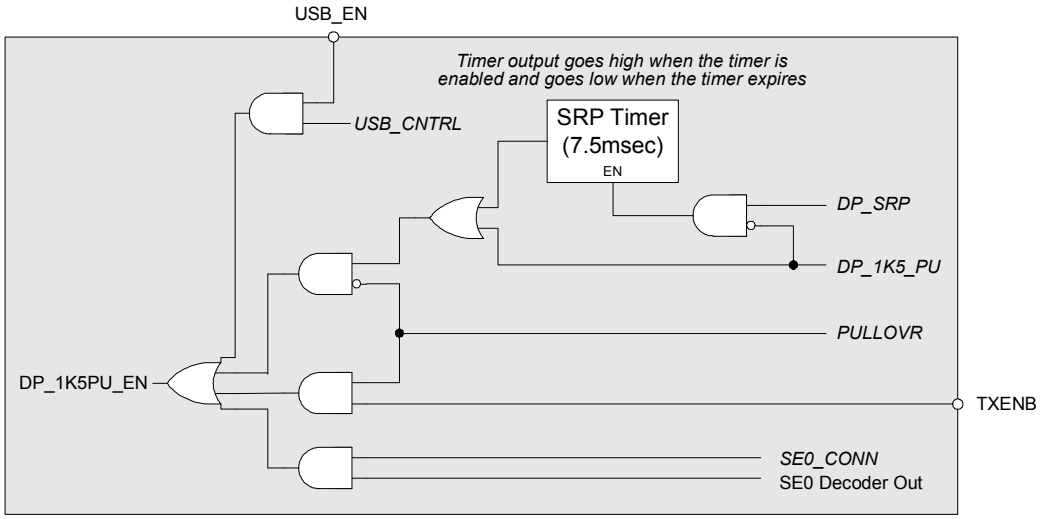

Figure 10. DP Pull-Up Control Circuit

This block diagram describes functionality. It is not intended to describe the actual circuit implementation to be used.

An effective resistance of 70 kΩ (+/-30 kΩ) pull-down resistor from the VBUS pin to ground is also integrated. Switching this pull-down out reduces current drain. An NMOS switch is provided to connect the pull-down when the VBUS_70KPD_ENB = 0, VBUS_3KPD_EN = 0 and REG_5V_EN = 0.

In the Dual path configuration there is a potential problem with a false charger detect caused by the reverse leakage of the Schottky diode in the BP regulator. Therefore, a pulldown resistor on VBUS is implemented and can be disconnected in order to reduce the current drain. Internal logic determines when the 3 kΩ pull-down is enabled. SPI bit VBUS_3KPD_EN allows for manual control of the 3 kΩ pull-down resister.

Table 30. Pull Up/Down Resistor Specifications

Parameter	Condition	Min	Typ	Max	Units
DP 1.5 kΩ Variable Pull-Up Resistor		900		3090	Ω
DP/DM 20 kΩ Pull-Down Resistors		14.3		24.8	kΩ
150 kΩ DP Pull-Up Resistor		105	150	195	kΩ
2.5 MΩ DM Pull-Down Resistor		1	2.5	4.0	MΩ
VBUS to GND Pull-Down Effective Resistance	VBUS_70KPD_ENB = 0 VBUS_3KPD_EN = 0 REG_5V_EN = 0	40	70	100	kΩ
4.1 Volt Comparator Threshold Voltage	1 is greater than this voltage 0 if less than this voltage	3.9	4.1	4.25	V
VBUS to GND Pull-Down Effective Resistance	VBUS_70KPD_ENB = 1 VBUS_3KPD_EN = 1 REG_5V_EN = 0	1.5	3	4.5	

5.1.5 VBUS Pulse Timer

In order to support the OTG session request protocol, a VBUS pulse timer and a programmable current limit on the 5V_REG regulator are implemented. When *5V_REG_EN* = 0, the current limit can be programmed to 910 µA by setting the *VBUS_PULSE_TMR[2:0]* to a value other than 000.

The low current limit on the 5V_REG regulator allows for easier detection of a legacy master device on the distance end of the USB cable (the timing requirements are less restrictive than if the higher current limit is utilized). The detection method utilizes the fact that a legacy master is required to have a minimum of 96 µF of capacitance on VBUS, where as the maximum capacitance that an OTG dual-role device can have on VBUS is 6.5 µF. Because of this magnitude of order difference, an OTG dual-role device can limit the amount of charge that is placed on the bus by limiting the time that the REG_5V regulator is turned on. This ensures that an OTG device will not source a significant amount of current into a legacy master device, which could have detrimental effects. Refer to the USB OTG specification for more details on legacy master detection.

The current limit of the VBUS regulator is set to 910 µA and is enabled for a time period specified by *VBUS_PULSE_TMR[2:0]* bits. When the timer duration expires, the *VBUS_PULSE_TMR[2:0]* bits are cleared and the regulator is disabled.

If the *VBUS_PULSE_TMR[2:0]* is programmed to 111 while *REG_5V_EN* = 0, the VBUS regulator is enabled with a current limit at 910 µA until software clears the *VBUS_PULSE_TMR[2:0]* bits. When

REG_5V_*EN* = 1, *VBUS_PULSE_TMR[2:0]* bits are ignored and the REG_5V regulator is enabled with the current limit of 100 mA.

Table 31 summarizes the VBUS pulse timer implementation.

Table 31. VBUS Pulse Timer Implementation

REG_5V_EN	VBUS_PULSE_ TMR[2:0]	REG_5V Status
1	X	Regulator enabled with current limit set to 100mA
0	000	Regulator disabled
0	001	Current limit set to 910 µA and regulator enabled for 10 ms
0	010	Current limit set to 910 µA and regulator enabled for 20 ms
0	011	Current limit set to 910 µA and regulator enabled for 30 ms
0	100	Current limit set to 910 µA and regulator enabled for 40 ms
0	101	Current limit set to 910 µA and regulator enabled for 50 ms
0	110	Current limit set to 910 µA and regulator enabled for 60 ms
0	111	Regulator enabled with current limit set to 910 µA

5.2 Signaling Modes

The MC13883 bus supports four signaling modes: USB, UART, mono audio and stereo audio. In addition, two loopback modes are provided for testing purposes. Table 32 summarizes the MC13883 signaling and test modes.

Table 32. Signaling and Test Modes

Mode	MODE 2:0	UART_SWAP	Description
USB	000	n/a	USB xcvr enabled UART disabled (Hi-Z) audio disabled (Hi-Z)
UART1	001	1	(UART_TXD = SE0_VM) => DP (UART_RXD = DAT_VP) <= DM USB xcver disabled (Hi-Z) audio disabled (Hi-Z)
		0	(UART_TXD = SE0_VM) => DM (UART_RXD = DAT_VP) <= DP USB xcver disabled (Hi-Z), audio disabled (Hi-Z)
UART2	010	1	(UART_TXD = DAT_VP) => DP (UART_RXD = VM) <= DM USB xcver disabled (Hi-Z) audio disabled (Hi-Z)
		0	(UART_TXD = DAT_VP) => DM (UART_RXD = VM) <= DP USB xcver disabled (Hi-Z) audio disabled (Hi-Z)

Table 32. Signaling and Test Modes (continued)

Mode	MODE 2:0	UART_SWAP	Description
N/A	011	n/a	Reserved
Mono Audio	100	n/a	SPKR_L => DM MIC <= DP USB xcver disabled (Hi-Z) UART disabled (Hi-Z)
Stereo Audio	101	n/a	SPKR_L => DM SPKR_R => DP USB xcver disabled (Hi-Z) UART disabled (Hi-Z)
Loopback Right	110	n/a	USB xcver enabled audio disconnected from DP/DM and MIC => SPKR_R UART disabled (Hi-Z)
Loopback Left	111	n/a	USB xcver enabled audio disconnected from DP/DM and MIC => SPKR_L UART disabled (Hi-Z)

In data mode, the audio lines shared on DP/DM are high impedance to prevent loading on the data signals. In audio mode, the UART and USB signals shared on DP/DM are high impedance to prevent loading and noise on the audio signals.

The Tx line at the cable side is normally active in UART mode. By setting the UART_TXENB bit to a 1 (default is 0), the Tx line will be tristated. Depending on the setting of UART_SWAP, this will occur on DM or DP.

5.2.1 USB Modes

The MC13883 IC contains a USB OTG transceiver that is compliant with the USB 2.0 specification and the USB On-the-Go supplement. The transceiver supports a low speed mode of 1.5 Mbits/second and a full speed mode of 12 Mbit/s. The speed of the transceiver is selected by the *FSENB* bit. The phone detects the speed requested by the peripheral by reading the DP and DM voltages. If the DP line is pulled high then the speed requested is full speed. If the DM line is pulled high then the speed requested is low speed.

The USB transceiver can be enabled only when the RESETB signal is de-asserted (set high). When RESETB is high, the transceiver is enabled if the USB_EN pin is asserted and *USB_CNTRL* = 1 or if *USBXCVR_EN = 1* and *MODE[2:0] = 000*.

A functional block diagram of the USB transceiver is shown in Figure 11.

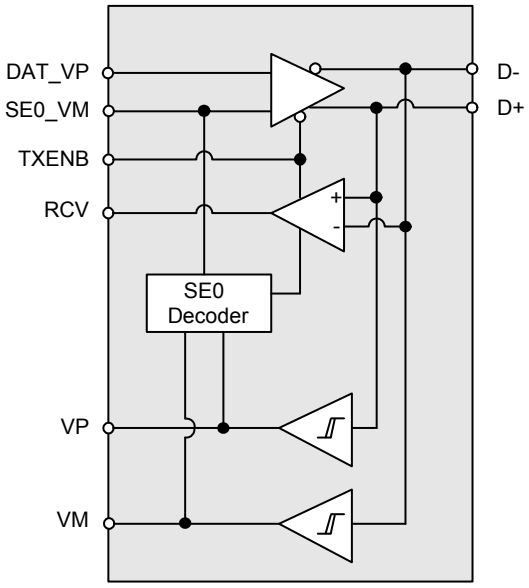

Figure 11. USB Transceiver Block Diagram

In order to support different USB interfaces, the MC13883 bus USB transceiver can be configured to operate in one of four different modes:

- VP_VM bidirectional, also known as 4-wire mode (*DET_SE0* = 0, *BI_DI* = 1)
- VP_VM unidirectional (*DET_SE0* = 0, *BI_DI* = 0)
- DAT_SE0 bidirectional, also known as 3-wire mode (*DET_SE0* = 1, *BI_DI* = 1)
- DAT_SE0 unidirectional, also known as 6-wire mode (*DET_SE0* = 1, *BI_DI* = 0)

In VP_VM bidirectional mode, if TXENB is low then the receiver is disabled and complementary transmit data present on DAT_VP and SE0_VM is output differentially on DP and DM. If TXENB is high then the transmit buffer is disabled and the data received differentially on DP and DM is output in CMOS format on RCV, while data on DP is buffered at DAT_VP, and data on DM is buffered on SE0_VM.

In VP_VM unidirectional mode, if TXENB is low then the receiver is disabled and the complementary transmit data present on DAT_VP and SE0_VM is output differentially on DP and DM. If TXENB is high then the transmit buffer is disabled and the data received differentially on DP and DM is output in CMOS format on RCV, while data on DP is buffered at VP, and data on DM is buffered on VM.

In DAT_SE0 bidirectional mode, if TXENB and SE0_VM are low then the receiver is disabled and the data present on DAT_VP is output differentially on DP and DM. If SE0_VM is high then both DP and DM are low regardless of the state of DAT_VP. If TXENB is high then the transmit buffer is disabled and the data received differentially on DP and DM is output in CMOS format on DAT_VP. If both DP and DM are low, then SE0_VM is pulled high by the SE0 Decoder.

In DAT_SE0 unidirectional mode, if TXENB and SE0_VM are low then the receiver is disabled and the data present on DAT_VP is output differentially on DP and DM. If SE0_VM is high then both DP and DM are low regardless of the state of DAT_VP. If TXENB is high then the data received differentially on DP and DM is output in CMOS format on RCV, while data on DP is buffered at VP, and data on DM is buffered on VM.

Table 33 summarizes different modes that the USB transceiver can operate in.

Table 33. USB Functional Modes[A]

USB Mode		Mode Selection		Mode Description	
		DAT_SE0	BI_DI	TXENB = 0	TXENB = 1
VP_VM	uni-directional (6-wire)	0	0	DAT_VP => DP SE0_VM => DM	DP => VP DM => VM DP/DM => RCV
	bi-directional (4-wire)		1	DAT_VP => DP SE0_VM => DM	DP => DAT_VP DM => SE0_VM DP/DM => RCV
DAT_SE0	uni-directional (6-wire)	1	0	DAT_VP => DP/DM SE0_VM => FSE0	DP => VP DM => VM DP/DM => RCV
	bi-directional (3-wire)		1	DAT_VP => DP/DM SE0_VM => FSE0	DP/DM => DAT_VP (active) DP => DAT_VP (suspend) RSE0 => SE0_VM

A internal condition FSE0 forces a single ended (SE0) condition on the DP, DM (D+, D-) lines. RSE0 indicates that a single ended (SE0) condition is received on DP, DM (D+, D-) lines

USB suspend mode is enabled through the *USB_SUSPEND* bit. When this bit is set, the USB differential receiver is powered down to reduce power consumption. The VUSB regulator is enabled and the variable 1.5 kΩ DP pull-up resistor is switched in.

Table 34. General USB Specifications[A]

Parameter	Condition	Min	Max	Units
Voltage Levels				
Input Low Voltage	DAT_VP, SE0_VM, TXENB	-	0.8	V
Input High Voltage	DAT_VP, SE0_VM, TXENB	VCCIO * 0.7	-	V
Input Voltage Range	DAT_VP, SE0_VM, TXENB	0	VCCIO	V
Output Low Voltage	DAT_VP, SE0_VM, VP, VM, RCV (400 µA)	-	0.4	V
Output High Voltage	DAT_VP, SE0_VM, VP, VM, RCV (400 µA)	VCCIO * 0.9	-	V
Output Low Voltage	DP, DM (1.5 kΩ to 3.6 V)	-	0.3	V
Output High Voltage	DP, DM (15 kΩ to GND)	VUSB * 0.9	VUSB	V
Output Cross Over Voltage	DP, DM	1.3	2.0	V
Differential Input Voltage	|(DP)-(DM)|	0.2	-	V
Common Mode Voltage	DP, DM	0.8	2.5	V
Single Ended Receive Threshold	DP, DM	0.8	2.0	V
Impedance				
Driver Output Impedance	DP, DM, II = 20 mA	8.4	19.6	Ω

Table 34. General USB Specifications[A] (continued)

Parameter	Condition	Min	Max	Units
Timing - USB Full Speed Mode				
Rise and Fall Time	DP, DM (CL = 50 pf)	4	20	ns
Rise/Fall Time Matching	DP, DM	0.8	1.2	
Propagation Delay	DAT_VP, SE0_VM to DP, DM	-	20	ns
Enable Delay	TXENB to DP, DM	-	20	ns
Disable Delay	TXENB to DP, DM	-	20	ns
Propagation Delay	DP, DM to DAT_VP, SE0_VM, RCV	-	20	ns
Rise and Fall Time	VM, VP, RCV (CL = 20 pF)		20	ns
Timing - USB Low Speed Mode				
Rise and Fall Time	DP, DM (CL = 250 pf)	75	300	ns
Rise/Fall Time Matching	DP, DM	0.8	1.2	
Propagation Delay	DAT_VP, SE0_VM to DP, DM	-	300	ns
Enable Delay	TXENB to DP, DM	-	200	ns
Disable Delay	TXENB to DP, DM	-	20	ns
Propagation Delay	DP, DM to DAT_VP, SE0_VM, RCV	-	30	ns
Propagation Delay	DP, DM to VP, VM	-	30	ns

[A] Timing assumes 50pf loading and series 22 Ω, 5% resistors on DP and DM unless otherwise noted.

In order to meet the requirement for the USB driver output impedance to be between 28 Ω and 44 Ω (full speed), two external 22 Ω resistors will be placed in series with the DP and DM lines.

The USB transceivers with output impedance different than the MC13883 one-chip transceiver will require different external resistors.

In the voltage level section of Table 34, the VIH and VIL for DM and DP during UART and USB SUSPEND modes are defined such that a CEA-936-A compliant DC audio level will be detected properly even though these audio mode DC levels are below the normal USB VIH level for DM and DP.

In USB suspended mode, the VP and VM receive pins are active and can be used for detection of logic levels on DP and DM, often used in accessory detection.

5.2.2 UART Mode

The MC13883 supports UART mode. To expand compatibility to with other devices, a SPI bit, USB_SWAP, is available in UART mode. Register 04 - Power Control 1, bit 6 swaps the RX and TX connections to DM and DP. Accordingly, the UART transmit and receive signals are multiplexed on DP/DM lines as in Table 35.

Table 35. UART Routing Selection

MC13883_MODE [2:0]	UART_SWAP = 0	UART_SWAP = 1
001	TX Signal SE0_VM => DM	TX Signal SE0_VM => DP
001	RX Signal DP => DAT_VP	RX Signal DM => DAT_VP
010	TX Signal DAT_VP => DM	TX Signal DAT_VP => DP
010	RX Signal DP => VM	RX Signal DM => VM

Since DP and DM pins are at the VUSB level (with 3.3 V setting), while UART transmit and received data are at the VCCIO level, logic level translators are provided.

In UART mode, the VP and VM receive pins are active and can be used for detection of logic levels on DP and DM, often used in accessory detection.

5.2.3 Audio Modes and Loopback Modes

The MC13883 bus supports mono and stereo audio modes in which audio signals are multiplexed on DP/DM lines as follows:

- in mono audio mode (*VUSB_EN* = 1, *VUSB0* = 0, *MODE[2:0]* = 100) the phone's speaker left output is routed to DM and the microphone input is connected to DP
- in stereo audio mode (*VUSB_EN* = 1, *VUSB0* = 0, *MODE[2:0]* = 101) the phone's speaker left output is routed to DM and the speaker right output is connected to DP

Three low impedance switches (50 to 220 Ω) are implemented for audio multiplexing.

In addition, two switches are provided to loop back microphone and speaker lines for testing purposes.

DM_SNS and DP_SNS will read the instantaneous values of DM and DP while in audio mode, but the value read may not be accurate due to the analog nature of the audio signal.

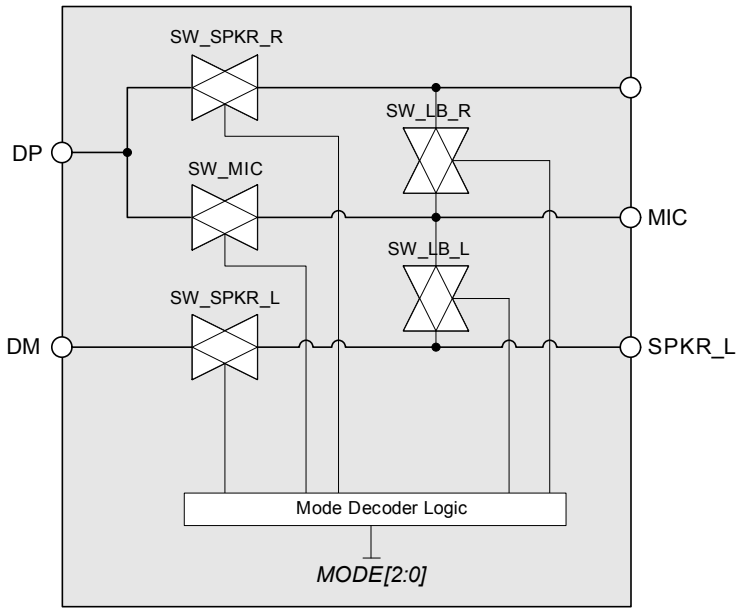

Figure 12. Audio Switches

Table 36 shows configuration of the audio switches in different modes.

Table 36. Audio Switches Configurations

MC13883 MODE[2:0]	SW_ SPKR_R	SW_ SPKR_L	SW_ MIC	SW_ LB_R	SW_ LB_L
0xx	open	open	open	open	open
100	open	closed	closed	open	open
101	closed	closed	open	open	open
110	open	open	open	closed	open
111	open	open	open	open	closed

All switches are powered from the VUSB regulator.

The impedance of audio switches, in conjunction with 22 ohm resistors placed externally in series with DP and DM lines, will not affect the audio signals. The RX audio path will not be loaded because the audio signal from a power management IC will be routed through the audio switch and 22 ohm resistor to a high impedance speaker amplifier in the MC13883 audio accessory (the MC13883 headset will also have a built-in amplifier). The TX audio path will not be loaded because the audio signal from the accessory microphone will be routed through the audio switch and 22 ohm resistor to a high impedance audio path input in a power management IC.

Table 37 shows specifications for audio switches.

Table 37. Audio Switches Specification

Parameter	Conditions	Min	Max	Unit
ON State impedance	Audio freq = 1 kHz	50	150	Ω
OFF State Impedance	VUSB = 2.775 V output setting, input to VUSB is BP	2		MΩ
Power Supply Rejection Ratio	0.5 Vpp 217 Hz noise on VUSB input (BP), 20 Hz – 20 kHz See Figure 10.	80	-	dB
Audio Crosstalk	1 kHz, 1 Vpp	-	-66	dB
Audio Distortion	1 kHz, 2.2 Vpp	-	1	%
	1 kHz, 2.0 Vpp	-	0.1	%
Data to audio isolation	USB 12 Mbit active on DP/DM, < 20 kHz signal components observed on SPKR_X/MIC pins	-	-80	dB
Audio input/output voltage range		0.1	2.3	V
SPKR_X/MIC pin capacitance	Measured from pin to ground	-	10	pF

5.2.4 Mode Transitioning

The ID pull-down resistor and the carkit interrupt detector are provided to allow transitioning between different MC13883 signaling modes.

While in audio mode, the phone can generate or receive an interrupt requesting a mode change. In addition, 5-wire and 4-wire signaling negotiation protocols are supported by the IC. In 5-wire interface protocol, the phone signals the accessory to exit audio mode by pulling the ID pin to ground for a time period Tph_id_int (6 ms ±2 ms). A switch, SW_ID2, in the ID detector is provided to ground the ID pin. The switch is controlled by bits *ID_PD* and *ID_PULSE*. When the *ID_PULSE* bit is set high while *ID_PD* = 0, the ID line is grounded for a time period Tph_id_int and the *ID_PULSE* bit is automatically cleared. When *ID_PD* = 1, SW_ID2 remains closed until *ID_PD* is cleared by software. Table 38 summarizes the ID pull-down control.

Table 38. ID Pull-Down Control

ID_PD	ID_PULSE	SW_ID2 State
0	0	OFF
0	1	ON for time of Tph_id_int, then OFF and bit *ID_PULSE* cleared
1	x	ON

In 4-wire interface protocol, the phone signals the accessory to exit audio mode by injecting a positive pulse on the DM line. When the *DM_PULSE* bit is set high while the phone is in audio signaling mode, the MC13883 IC generates a pulse of width between 200 to 500 ns and amplitude greater than 2.9 V. In addition, the *DM_PULSE* bit is automatically cleared.

The 4-wire interface protocol also specifies that when a carkit is in audio signaling mode, it can interrupt the phone by injecting a negative pulse of width between 200 to 500 ns on the DP line. This pulse is detected by the carkit interrupt detector implemented on the MC13883 IC. If the voltage on the DP line

dips below 0.58V while the phone is in audio mode, the output of the Carkit Interrupt Detector goes high and the *CK_DET_INT* interrupt is generated. The carkit interrupt detector is enabled only in audio signaling mode.

Table 39. Carkit Interrupt Specifications

Parameter	Condition	Min	Max	Units
4-Wire				
DP Interrupt Pulse Voltage	Audio signaling mode	0.4	0.58	V
DP Interrupt Pulse Width	Audio signaling mode	200	500	ns
DM Interrupt Pulse Voltage	Audio signaling mode	2.9	-	V
DM Interrupt Pulse Width	Audio signaling mode	200	500	ns
5-Wire				
ID Interrupt Pulse Voltage	Audio signaling mode	-	0.3	V
ID Interrupt Pulse Width	Audio signaling mode	4	8	ms

5.3 Power-Up Control

The MC13883 IC always powers up in USB mode (USB_EN must be pulled or wired high). The USB transceiver defaults to mode determined by the BOOTMODE pin. BOOTMODE is a “trinary” pin that can detect three different conditions: the pin is grounded, the pin is floating, or the pin is pulled high. Floating means it will be between 0.3*VC and 0.7*VC. Based on the state of the BOOTMODE pin, default states of *DAT_SE0* and *BI_DI* bits are set and therefore the default state of the USB transceiver is determined.

If the BOOTMODE pin is grounded, the transceiver powers up in DAT_SE0 unidirectional mode (default state of *DAT_SE0* = 1, default state of *BI_DI* = 0). If the BOOTMODE pin is pulled up to VC, the USB transceiver powers up in VP_VM bidirectional mode (default state of *DAT_SE0* = 0, default state of *BI_DI* = 1). If the BOOTMODE pin is floating, the USB transceiver powers up in DAT_SE0 bidirectional mode (default state of *DAT_SE0* = 1, default state of *BI_DI* = 1). See Table 40.

Table 40. Default USB Mode Selection

Pin	Default state of *DAT_SE0*	Default state of *BI_DI*	Default USB Mode
BOOTMODE grounded	1	0	DAT_SE0 unidirectional mode (6-wire)
BOOTMODE pulled to VC	0	1	VP_VM bidirectional mode (4-wire)
BOOTMODE floating	1	1	DAT_SE0 bidirectional mode (3-wire)
Parameter	Min	Max	Units
USBEN VIH	0.7 * VC	VC	V
USBEN VIL	0	VC * 0.3	V

During power up, the USB transceiver, 1.5 kΩ DP variable pull-up resistor, and VUSB regulator are controlled by the USB_EN and RESETB signals. The USB_EN pin is logically AND-ed with the USB_CNTRL bit, which defaults to a logic "1". At the beginning of the power up sequence, the USB_EN

pin is pulled high either by a processor's GPIO or because it is hard-wired to an external 2.775 V supply on the system PCB. When the USB_EN pin is pulled high, SPI/I2C settings are bypassed and the variable 1.5 kΩ DP pull-up resistor is automatically switched in and the input source for the VUSB regulator is set to BP. At a rising edge of RESETB, default states of DAT_SE0 and BI-DI bits (determined by the BOOTMODE pin state) are latched into SPI/I2C registers and 1 msec later the USB transceiver and the VUSB regulator are enabled. Upon completion of the power up sequence, the USB_EN pin is de-asserted (if it is controlled by GPIO) or the USB_CNTRL bit is set low (if the pin is hard-wired) to allow software control via SPI/I2C.

Figure 13 illustrates the power-up control circuit.

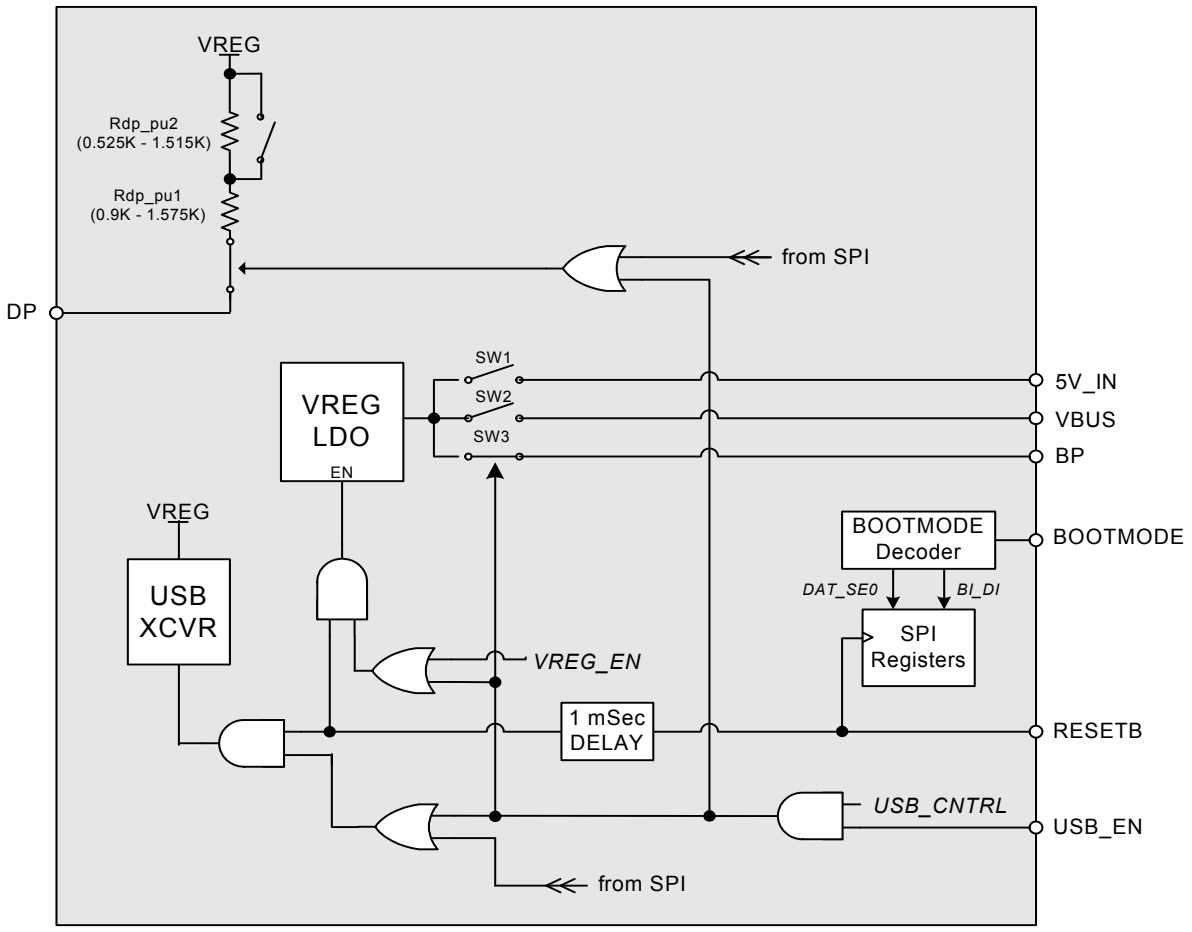

Figure 13. Power-Up Control Circuit

5.4 Interrupt

The MC13883 IC has interrupt generation capability. The following signals can generate an interrupt via the MC13883 INT line:

- VBUS detector:
  - VBUS_DET_4V4
  - VBUS_DET_2V
  - VBUS_DET_0V8
- Charge detector (CHRGDET_INT)
- ID detector
  - ID_FLOAT
  - ID_GND
- SE1 Detector (SE1_DET_INT)
- Battery Voltage Regulator (CC_CV_INT)
- Charge Current Monitor (CHRG_CURR_INT)
- Reverse Over-current Protection Circuit (RVRS_MODE_INT)
- Carkit Interrupt Detector output (CK_DET_INT)
- Reverse Mode Charge Detect (RVRS_CHRG_INT)
- Over-voltage Protection Circuit (VBUSOV_INT)

Each of these interrupts can be independently masked. Even when the interrupt is masked, the interrupt source can still be read from the Interrupt Status Register. Each interrupt is latched so that even if the interrupt source becomes inactive, the interrupt remains active. Each interrupt can be cleared by writing a 1 to the appropriate bit in the Interrupt Status Register.

The CHRGDET_INT, VBUS_3V4_INT, VBUSDET_INT, ID_INT, SE1_DET_INT, and CC_CV_INT interrupts are dual-edge triggered. The CHRG_CURR_INT, RVRS_MODE_INT, and CK_DET_INT interrupts are single-edge triggered.

All interrupts are summarized in Table 41.

Table 41. MC13883 Interrupts[A]

Name	Trigger	Debounce	Description
CHRGDET _INT			Logic high indicates that the interrupt is from a low to high or a high to low transition of CHRGDET comparator. Used to detect insertion or removal of a self powered device. Write a "1" to this location to clear the interrupt.
VBUS_3V4_INT	dual-edge	32 ms on rising and falling edge	Logic high indicates that the interrupt is from a low to high or a high to low transition of the 3.4V VBUS comparator output. Used to detect insertion or removal of a Self Powered Device. Write a “1” to this location to clear the interrupt.

Table 41. MC13883 Interrupts[A] (continued)

Name	Trigger	Debounce	Description
VBUSDET_INT	dual-edge	* 20 ms on a rising edge of VBUS_DET_4V4 * 1 ms on a falling edge of VBUS_DET_4V4 * no debounce on VBUS_DET_2V or VBUS_DET_0V8	Logic high indicates that the interrupt is from a low to high or a high to low transition of the VBUSDET_4V4, VBUSDET_2V, or VBUSDET_0V8 output of the VBUS Detector. Write a “1” to this location to clear the interrupt.
ID_INT	dual-edge	<100us on rising and falling edge	Logic high indicates that the interrupt is from a low to high or a high to low transition of the ID_FLOAT or ID_GND output of the ID Detector. Write a “1” to this location to clear the interrupt.
SE1_DET_INT	dual-edge	1ms on rising and falling edge	Logic high indicates that the interrupt is from a low to high or a high to low transition of the SE1 detector output. Write a “1” to this location to clear the interrupt.
RVRS_CHRG_INT	Rising edge	1 ms on rising edge	Logic high indicates that the interrupt is from a low to high transition of the RVRS_CHRG current (current going into the battery when it shouldn’t). Write a “1” to this location to clear the interrupt.
CC_CV_INT	dual-edge	2 Second debounce on rising and falling edge	Logic high indicates that the charger has switched its mode from CC to CV or from CV to CC. Charger removal does not trigger this interrupt. Write a “1” to this location to clear the interrupt.
CHRG_CURR_INT	single-edge	4 ms debounce	Logic high indicates that the charge current has dropped below 20 mA.
RVRS_MODE_INT	single-edge	Debounce based on values in Table 12.	Logic high indicates that the switched BP function has been disabled, because the Reverse Current Limit has been exceeded. Write a “1” to this location to clear the interrupt.
CK_DET_INT	single-edge	no debounce	Logic high indicates that a carkit has generated interrupt (a negative pulse on DP has been detected). Write a “1” to this location to clear the interrupt.
VBUSOV_INT	dual-edge	no debounce	Logic high indicates that the OV detector has detected an over voltage condition. Write a “1” to this location to clear the interrupt.

[A] The VBUS_3.4 comparator has a 3.8 V trip point on rising edge and a 3.5 V trip point on falling edge.

5.5 Interrupt Control Bits

The interrupt control bit register locations are listed in the I2C/SPI register section.

6 Serial Interface

The MC13883 IC contains one SPI interface port and one I2C port to allow processor access to the MC13883 resources. Four pins are shared for SPI and I2C signals. Also, their functions are listed in Table 42. The I2C_SPIF_SEL pin selects SPI or I2C mode as shown in Table 43.

Table 42. Serial Interface Pin Description

Pin	I2C_SPIF_SEL	Description
SPI_MOSI/ I2C_ADR2	open high	SPI serial data input line MSB of I2C device address offset
SPI_MISO/ I2C_SDA	open high	SPI serial data output line I2C serial bus data
SPI_CLK/ I2C_SCL	open high	Clock input line I2C serial bus clock
SPI_CS/ I2C_ADR1	open high	Clock enable line (active high) LSB of I2C device address offset

The supported I2C data rate is up to 400 kbps. The maximum SPI clock rate is 26 MHz. Both interfaces are powered though the VCCIO supply, so the host processor should power the interface from the same supply. When RESETB is asserted low all bits revert to their default state.

Table 43. I2C_SPIF_SEL Connection Functionality Description

I2C_SPIF_SEL	Description
Ground	Reserved
VC	I2C serial bus Mode Selected
Open Circuit	SPI BUS Mode Selected

6.1 SPI Interface

The SPI interface has the following characteristics:

1. The maximum clock rate is 26 MHz.
2. Data is transmitted most significant bit first. Each data field consists of a total of 32 bits.
3. Data and SPI_CLK signals are ignored as long as SPI_CS goes low (logic 0). SPI_MISO is tri-stated if SPI_CS is programmed low.
4. SPI_CS is active (logic 1) only during the serial data transmission.
5. All input data is sampled at the rising edge of the SPI_CLK signal. Any transition on SPI_MOSI should occur at least 5 ns before the rising edge of SPI_CLK and remain stable for at least 5 ns after the rising edge of SPI_CLK.
6. All output data is updated at the rising edge of the SPI_CLK signal. Any transition on SPI_MISO should occur at least 5 ns before the rising edge of SPI_CLK and remain stable for at least 19.23 ns after the rising edge of SPI_CLK.
7. SPI_CS has to be active (logic 1) at least 5 ns before the rising edge of the first SPI_CLK signal, and has to remain active (logic 1) at least 61.5 ns after the last falling edge of SPI_CLK.

8. Coincident rising or falling edges of SPI_CLK and SPI_CS are not allowed.
9. If SPI_CS goes low before enough bits are sent then the data bits sent are ignored.
10. When SPI_CS goes low to complete the SPI operation then the next rising edge of SPI_CS must be delayed by at least 30 ns.

Table 44. SPI Interface Electrical Characteristics

Parameter	Min	Max	Unit
Supply Voltage VCCIO	1.65	2.9	V
MISO low level output voltage	-	0.3	V
MISO high level output voltage	0.8*VCCIO	-	V
MOSI, SPI_CLK, SPI_CS low level input voltage	-	0.3*VCCIO	V
MOSI SPI_CLK, SPI_CS high level input voltage	0.7*VCCIO	-	V

The SPI port is configured to utilize 32-bit serial data words, using 1 bit for R/W, 5 for address, 1 null, and 25 for data.

For each SPI transfer, a one is written to the SPI_MOSI pin if this SPI transfer is to be a write. A zero is written to the SPI_MOSI pin if this is to be a read command only. If a zero is written, then any data sent after the address bits is ignored and the internal contents of the field addressed does not change when the 32nd SPI_CLK is sent. Next the 5-bit address is written to the SPI_MOSI pin MSB first. Finally, data bits are written to the SPI_MOSI pin MSB first. Once all the data bits are written then the data is transferred into the actual registers on the 32nd SPI_CLK. SPI_CS must go low and return high to start the next SPI data transfer.

To read a field of data, the SPI_MISO pin will output the data field pointed to by the five address bits loaded at the beginning of the SPI sequence.

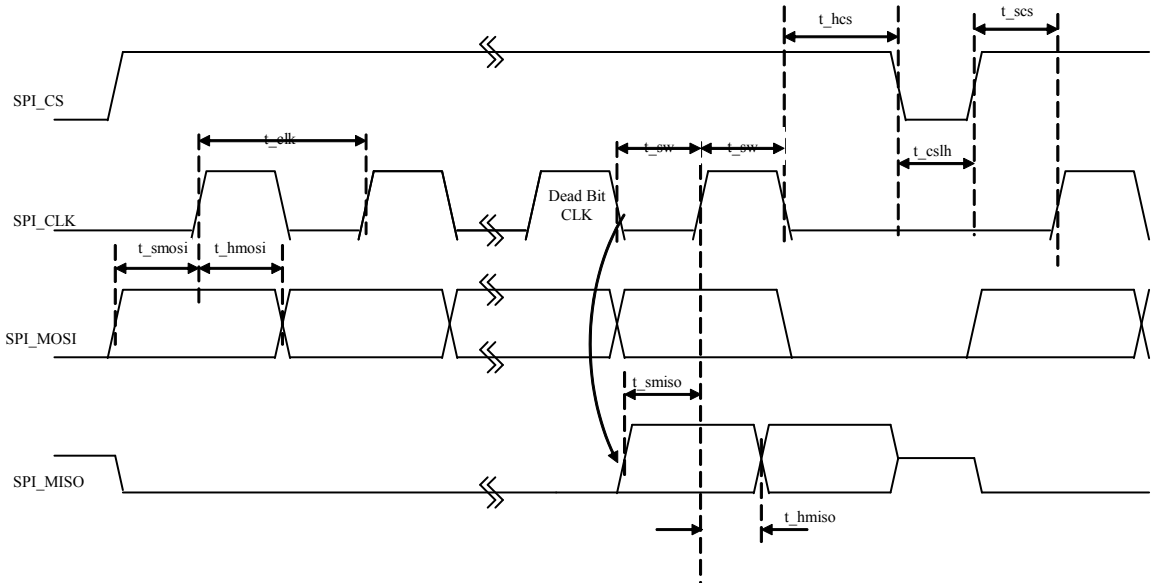

Figure 14. SPI Timing Diagram

Table 45. SPI Interface Switching Characteristics

Parameter	Symbol	Min	Max	Unit
SPI_CLK Cycle Time	t_clk	38.46	-	ns
SPI_CLK High or Low Time	t_sw	19.23	-	ns
SPI_CLK Rise or Fall Time	t_rise/fall	7.6	-	ns
Inter-Queue Transfer Delay	t_cslh	30	-	ns
Chip Select Lead Time (SPI_CS setup to SPI_CLK first rise edge)	t_scs	10	-	ns
Chip Select Lag Time (SPI_CS hold after SPI_CLK last fall edge)	t_hcs	61.5	-	ns
SPI_MOSI Setup Time (SPI_MOSI valid to SPI_CLK rise edge)	t_smosi	5	-	ns
SPI_MOSI Hold Time (SPI_CLK rise edge to SPI_MOSI valid)	t_hmosi	5	-	ns
SPI_MISO Setup Time (SPI_MISO valid to SPI_CLK rise edge)	t_smiso	5	-	ns
SPI_MISO Hold Time (SPI_CLK rise edge to SPI_MISO valid)	t_hmiso	19.23	-	ns

6.2 I2C Interface

The I2C serial control interface uses two signals: a serial transfer clock (I2C_SCL) and a serial data (I2C_SDA) signal. Always driven by a master, I2C_SCL synchronizes the serial transmission of data bits on I2C_SDA. The maximum clock frequency is 400 kHz. I2C_SDA is normally driven by the host. A slave device drives I2C_SDA only under two conditions. First, when responding with an acknowledge bit after reading data from the host, or second, when writing data to the host at the host's request.

The MC13883 operates as a slave. It has a 7 bit device address of ‘00101xx’ with the ‘xx’ being determined by the state of SPI_CS_I2C_ADR0 and SPI_MOSI_I2C_ADR1 pins. These pins are used to avoid any conflicts with other I2C devices, and thus, the MC13883’s device address can be offset by 00, 01, 10 or 11.

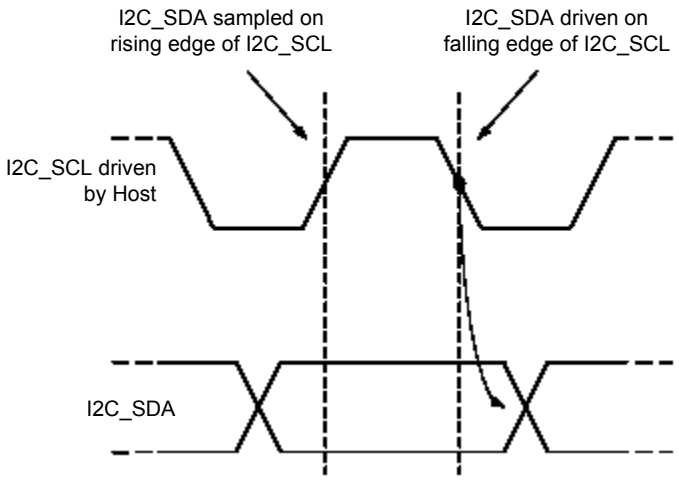

Figure 15. Synchronization of I2C Signals

The host initiates and terminates all data transfers. Data transfers are initiated by driving I2C_SDA from high to low while holding I2C_SCL high (START condition). Data transfers are terminated by driving I2C_SDA from low to high while SCLK is held high (STOP condition).

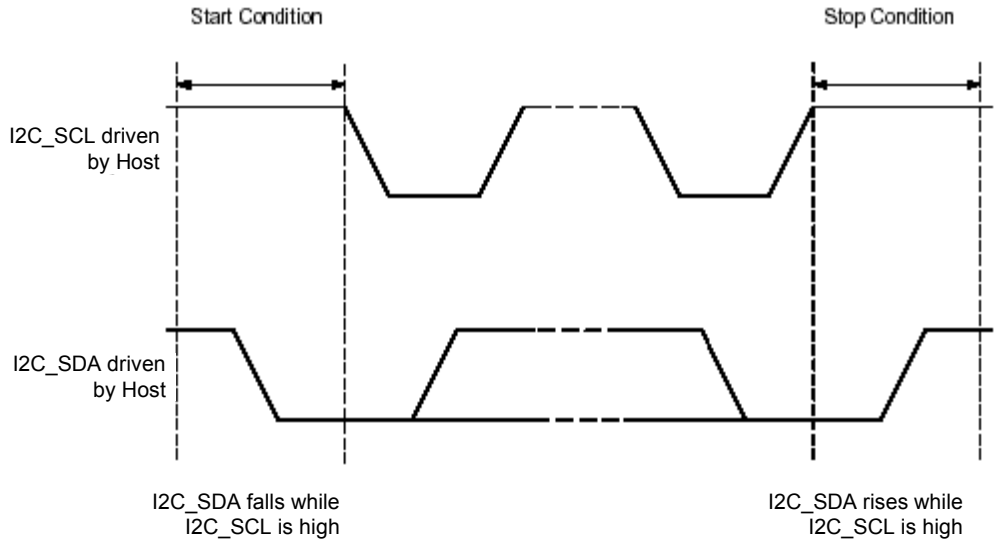

Figure 16. I2C Start and Stop Conditions

Read and write operations between the host and the MC13883 use three types of host driven packets (command, address, data) and one type of MC13883 driven packet (data). All packets are 8-bits long with the most significant sent bit first.

A command packet contains a 7-bit module device address and an active low Read/Write bit (R/W).

First bit of packet — Last bit of packet

Device Address							R/W
DA[6]	DA[5]	DA[4]	DA[3]	DA[2]	DA[1]	DA[0]	0= Write 1= Read

Figure 17. Command Packet

An address packet contains a 5-bit register address and 3 null bits.

First bit of packet — Last bit of packet

Register Address							
0	0	0	A[4]	A[3]	A[2]	A[1]	A[0]

Figure 18. Address Packet

A data packet contains 8 data bits. It may be sent by the host or the MC13883. Because the MC13883 registers contain 24-data bits, three data packets are needed for one data transfer.

First bit of packet — Last bit of packet

Data							
D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

Figure 19. Data Packet

Each 8-bit data packet is followed by a single Acknowledge/Not Acknowledge bit. The device receiving the data drives the Acknowledge/Not Acknowledge signal on I2C_SDA. Acknowledge (ACK) is defined as “0” and Not Acknowledge (NAK) is defined as “1”.

The host initiates all data transmissions with a Start condition. During data write, the MC13883 responds to each 8-bit data transmission with an Acknowledge signal (I2C_SDA = 0), unless there is an error. Data are transmitted with the most significant bit first. To terminate the transfer of host driven packets, the host follows the MC13883’s ACK with a Stop condition. The host can also issue a Start condition after the module's ACK if it wants to start a new data transfer.

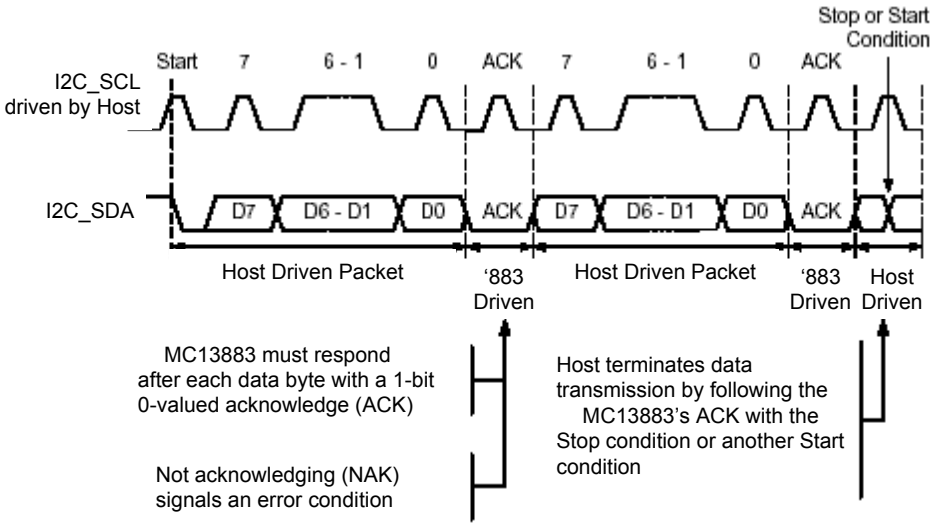

Figure 20. Host Driven Packets

When the host requests to read the data from the MC13883, the IC acknowledges the request and then writes a data byte transmitting the most significant bit (7) first. If the host wants to continue the data transfer, the host acknowledges the MC13883. If the host wants to terminate the transfer, it responds with Not Acknowledge (I2C_SDA = 1) and then drives I2C_SDA to generate a Stop condition. The host can also drive a Start condition if it wants to begin a new data transfer.

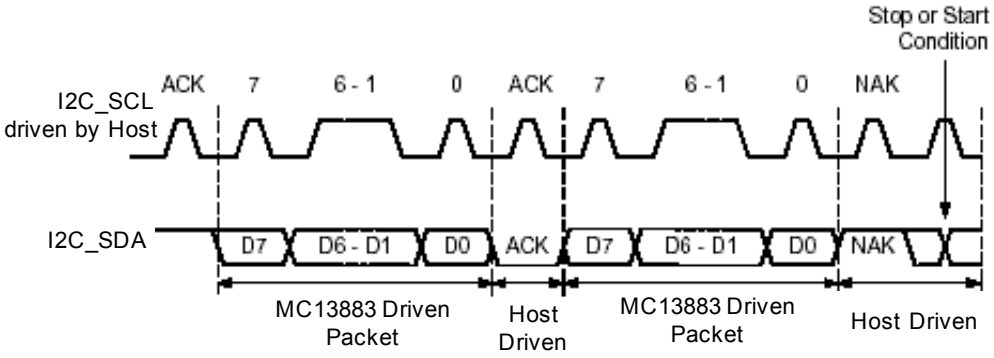

Figure 21. MC13883 Driven Packets

The following examples show how to write and read data to and from the MC13883. The host initiates and terminates all communication. The host sends a master command packet after driving the start condition. The MC13883 will respond to the host if the master command packet contains the MC13883 device address. In the following examples, the MC13883 is shown always responding with an ACK to transmissions from the host. If at any time a NAK is received, the host will terminate the current transaction and retry the transaction.

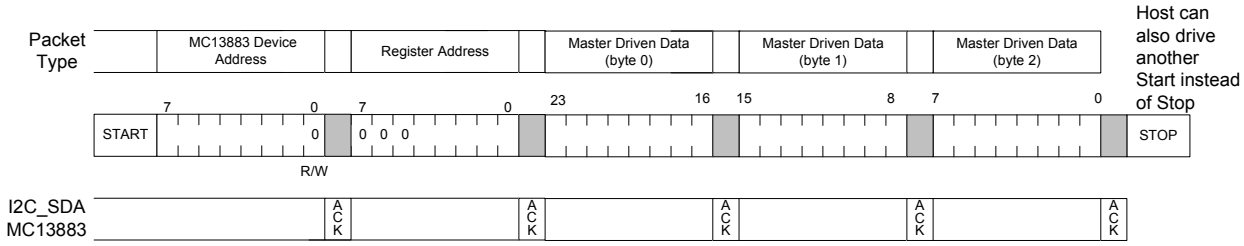

Figure 22. 3-byte Write

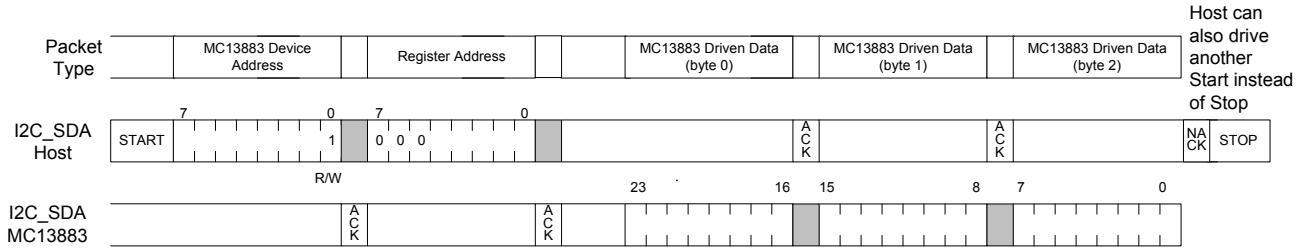

Figure 23. 3-byte Read

7 SPI/I2C Register Tables

7.1 SPI Register Table Summary

Table 46. Register 00 - Interrupt Status

Name	Bit #	R/W	Default	Description
CHRGDETI	0	R/W	0	Logic high indicates that the interrupt is from a low to high or a high to low transition of CHRGDET comparator. Used to detect insertion or removal of a self powered device. Write a "1" to this location to clear the interrupt.
VBUSDET_INT	1	R/W	0	Logic high indicates that the interrupt is from a low to high or a high to low transition of the VBUSDET_4V4, VBUSDET_2V, or VBUSDET_0V8 output of the VBUS Detector. Write a “1” to this location to clear the interrupt.
VBUSOV_INT	2	R/W	0	Logic high indicates that the interrupt is from a low to high transition of the Over-voltage detect circuit connected to the VBUS pin. Write a “1” to this location to clear the interrupt.

Table 46. Register 00 - Interrupt Status (continued)

Name	Bit #	R/W	Default	Description
RVRS_CHRG_INT	3	R/W	0	Logic high indicates that the interrupt is from a low to high transition of the RVRS_CHRG current (current going into the battery when it shouldn't). Write a "1" to this location to clear the interrupt.
ID_INT	4	R/W	0	Logic high indicates that the interrupt is from a low to high or a high to low transition of the ID_FLOAT or ID_GND output of the ID Detector. Write a "1" to this location to clear the interrupt.
Reserved	5	R/W	0	
SE1_DET_INT	6	R/W	0	Logic high indicates that the interrupt is from a low to high or a high to low transition of the SE1 detector output. Write a "1" to this location to clear the interrupt.
CC_CV_INT	7	R/W	0	Logic high indicates that the charger has switched its mode from Constant Current, CC, to Constant Voltage, CV, or from CV to CC. Charger removal does not trigger this interrupt. Write a "1" to this location to clear the interrupt.
CHRG_CURR_INT	8	R/W	0	Logic high indicates that the charge current has dropped below 20mA.
RVRS_MODE_INT	9	R/W	0	Logic high indicates that the switched BP function has been disabled, because the Reverse Current Limit has been exceeded. Write a "1" to this location to clear the interrupt.
CK_DET_INT	10	R/W	0	Logic high indicates that a carkit has generated interrupt (a negative pulse on DP has been detected). Write a "1" to this location to clear the interrupt.
BATTPON_INT	11	R/W	0	Logic 1 indicates a low to high or a high to low transition of BATTPON comparator. Write a "1" to this location to clear the interrupt.

Table 47. Register 01 - Interrupt Mask

Name	Bit #	R/W	Default	Description
CHRGDET_MASK	0	R/W	1	0 = VBUS_3V4_INT is not masked 1 = VBUS_3V4_INT is masked
VBUS_DET_MASK	1	R/W	1	0 = VBUSDET_INT is not masked 1 = VBUSDET_INT is masked
VBUSOV_MASK	2	R/W	1	0 = VBUSOV_INT is not masked 1 = VBUSOV_INT is masked.
RVRS_CHRG_MASK	3	R/W	0	0 = RVRS_CHRG_INT is not masked 1 = RVRS_CHRG _INT is masked
ID_MASK	4	R/W	1	0 = ID_INT is not masked 1 = ID_INT is masked
Reserved	5	R/W	0	
SE1_DET_MASK	6	R/W	1	0 = SE1_INT is not masked 1 = SE1_INT is masked
CC_CV_MASK	7	R/W	1	0 = CC_CV _INT is not masked 1 = CC_CV _INT is masked

Table 47. Register 01 - Interrupt Mask (continued)

Name	Bit #	R/W	Default	Description
CHRG_CURR_MASK	8	R/W	1	0 = CHRG_CURR _INT is not masked 1 = CHRG_CURR_INT is masked
RVRS_MODE_MASK	9	R/W	1	0 = RVRS_MODE _INT is not masked 1 = RVRS_MODE _INT is masked
CK_DET_MASK	10	R/W	1	0 = CK_DET_INT is not masked 1 = CK_DET_INT is masked
BATTPON_MASK	11	R/W	0	0 = BATTPON_INT is not masked 1 = BATTPON_INT is masked

Table 48. Register 02 – Interrupt Sense Register

Name	Bit #	R/W	Default	Description
CHRGDET	0	R	N/A	Status of the 3.4 V comparator:
VBUS_DET_4V4	1	R	N/A	Status of the 4.4 V VBUS Detector comparator:
VBUS_DET_2V	2	R	N/A	Status of the 2V VBUS Detector comparator:
VBUS_DET_0V8	3	R	N/A	Status of the 0.8 V VBUS Detector comparator:
ID_FLOAT	4	R	N/A	Status of the ID pin. See Table 28.
ID_GND	5	R	N/A	Status of the ID pin. See Table 28.
SE1_DET	6	R	N/A	Status of the SE1 Detector output: 0 = SE1 not detected 1 = SE1 detected
CC_CV	7	R	N/A	Charge mode indicator: 0 = constant current charging 1 = constant voltage charging
CHRG_CURR	8	R	N/A	Charge current monitor: 0 = charge current <20 mA 1 = charge current >20 mA
VBUSOV_SNS	9	R	N/A	0 = VBUS < OV threshold voltage 1 = VBUS > OV threshold voltage
REV0	10	R	N/A	IC Revision Bit 0
REV1	11	R	N/A	IC Revision Bit 1
REV2	12	R	N/A	IC Revision Bit 2
BATTPON	13	R	N/A	Status of the BATTPON comparator: 0 = BATTP < BATTPON Threshold 1 = BATTP > BATTPON Threshold
DP_SNS	14	R	N/A	0 = low DP logic state 1 = high DP logic state
DM_SNS	15	R	N/A	0 = low DM logic state 1 = high DM logic state

Table 49. Register 03 - Power Control 0

Name	Bit #	R/W	Default	Description
VCHRG0	0	R/W		Sets the output voltage of Charge Regulator. Default = 4.0V
VCHRG1	1	R/W		
VCHRG2	2	R/W		
ICHRG0	3	R/W		Sets the current of the main charger DAC. Default is determined by the charger control logic (OFF, 100mA, or fully ON)
ICHRG1	4	R/W		
ICHRG2	5	R/W		
ICHRG3	6	R/W		
ICHRG_TR0	7	R/W	0	Sets the current of the trickle charger. Default = OFF
ICHRG_TR1	8	R/W	0	
ICHRG_TR2	9	R/W	0	
FET_OVRD	10	R/W	0	0 = BATT_FET and BP_FET outputs are controlled by hardware 1 = BATT_FET and BP_FET are controlled by the state of the FET_CTRL bit
FET_CTRL	11	R/W	0	0 = BP_FET is driven low, BATT_FET is driven high if FET_OVRD is set 1 = BP_FET is driven high, BATT_FET is driven low if FET_OVRD is set
BP_SWITCH	12	R/W	0	0 = BP_FET is controlled as a voltage regulator (VB) 1 = BP_FET is controlled as a switch
RVRS_MODE	13	R/W	0	0 = Reverse charge mode disabled 1 = Reverse charge mode enabled (from battery out to VBUS)
Reserved	14	R/W	0	
Reserved	15	R/W	0	
Reserved	16	R/W	0	
Reserved	17	R/W	0	
CHRG_LED_EN	18	R/W	0	0 = LED off, 1 = LED on.
VBUS_3KPD_EN	19	R/W	0	0 = VBUS 3K pull-down NMOS switch is OFF 1 = VBUS 3K pull-down NMOS switch is ON if REG_5V_EN=0, OFF otherwise

Table 50. Register 04 - Power Control 1

Name	Bit #	R/W	Default	Description
VUSB_IN0	0	R/W	0	Controls the input source for the VUSB regulator. The default input is BP.
VUSB_IN1	1	R/W	1	
VUSB0	2	R/W	1	0 = VUSB output voltage set to 2.775V 1 = VUSB output voltage set to 3.3V
VUSB_EN	3	R/W	0	0 = VUSB output is disabled (unless USB_EN pin is asserted high) 1 = VUSB output is enabled (regardless of USB_EN pin)
ID_ICHRG_MUX_ENB	4	R/W	0	1 = ID ICHRG MUX disabled, the ICHRG pin is Hi-Z 0 = ID ICHRG MUX enabled
REG_5V_EN	5	R/W	0	0 = REG_5V output is disabled (unless VBUS_PULSE_TMR[2:0] <> 0) 1 = REG_5V output is enabled (regardless of VBUS_PULSE_TMR[2:0])

Table 50. Register 04 - Power Control 1 (continued)

Name	Bit #	R/W	Default	Description
UART_SWAP	6	R/W	0	0 = UART TX on UDM, RX on UDP 1 = UART TX on UDP, RX on UDM
UART_TXENB	7	R/W	0	0 = No Effect 1 = TX forced to Tristate in UART mode only
PWRON_ENB	8	R/W	0	1 = PWR ON forced Low 0 = PWR_ON logic level of control logic

Table 51. Register 05 - Connectivity Control

Name	Bit #	R/W	Default	Description
FSENB	0	R/W	0	0 = USB full speed mode selected 1 = USB low speed mode selected
USB_SUSPEND	1	R/W	0	0 = USB Suspend mode disabled 1 = USB Suspend mode enabled
DP_1K5_PU	2	R/W	0	1 = variable 1.5K DP pull-up switched in 0 = variable 1.5K DP pull-up switched out
DP_PD	3	R/W	0	0 = 15K DP pull-down switched out 1 = 15K DP pull-down switched in
DM_PD	4	R/W	0	0 = 15K DM pull-down switched out 1 = 15K DM pull-down switched in
DP_150K_PU	5	R/W	1	0 = 150K DP pull-up switched out 1 = 150K DP pull-up switched in
VBUS_70KPD_ENB	6	R/W	1	0 = VBUS 70K pull-down NMOS switch is ON if REG_5V_EN=0, OFF otherwise 1 = VBUS 70K pull-down NMOS switch is OFF
VBUS_PULSE_TMR_0	7	R/W	0	REG_5V regulator current limit control when *REG_5V_EN* = 0 000 = current limit set to 200mA 001 = current limit set to 910 µA for 10 ms 010 = current limit set to 910 µA for 20 ms 011 = current limit set to 910 µA for 30 ms 100 = current limit set to 910 µA for 40 ms 101 = current limit set to 910 µA for 50 ms 110 = current limit set to 910 µA for 60 ms 111 = current limit set to 910 µA
VBUS_PULSE_TMR_1	8	R/W	0	
VBUS_PULSE_TMR_2	9	R/W	0	
DLP_SRP	10	R/W	0	0 = DLP Timer disabled 1 = DLP Timer enabled
SE0_CONN	11	R/W	0	0 = variable DP pull-up is not automatically connected when SE0 is detected 1 = variable DP pull-up is automatically connected when SE0 is detected
USBXCVR_EN	12	R/W	0	0 = USB transceiver disabled if USB_EN is low or if *USB_CNTRL* = 0 1 = USB transceiver enabled if MC13883 MODE[2:0] = 000 and RESETB is high

Table 51. Register 05 - Connectivity Control (continued)

Name	Bit #	R/W	Default	Description
PULLOVR	13	R/W	0	1 = variable DP pull-up and DP/DM pull-downs are disconnected when TXENB is active 0 = variable DP pull-up and DP/DM pull-downs are connected when TXENB is active
MODE0	14	R/W	0	Mode select : 000 = USB mode 001 = UART1 mode 010 = UART2 mode 011 = reserved 100 = mono audio mode 101 = stereo audio mode 110 = Loopback Right mode 111 = Loopback Left mode
MODE1	15	R/W	0	
MODE2	16	R/W	0	
DAT_SE0	17	R/W	[A]	0 = VP_VM USB mode 1 = DAT_SE0 USB mode
BI_DI	18	R/W	[A]	0 = unidirectional USB transmission 1 = bidirectional USB transmission
USB_CNTRL	19	R/W	1	0 = 1.5K DP pull-up and USB xcvr is controlled by SPI bits 1 = USB_EN pin controls USB xcvr and 1.5K DP pull-up
ID_PD	20	R/W	0	0 = ID pull-down switched out 1 = ID pull-down switched in
ID_PULSE	21	R/W	0	0 = ID line not pulsed 1 = pulse to gnd on the ID line generated
ID_PU_CNTRL	22	R/W	0	0 = ID pin pulled up to BP through 220K resistor 1 = 5ua current source connected between the ID pin and VUSB
DM_PULSE	23	R/W	0	0 = DM line not pulsed 1 = a positive pulse on the DM line generated

[A] Default values of the DAT_SE0 and BI_DI bits are determined by the BOOTMODE pin as defined in Table 40.

8 Packaging Information

Figure 24 shows the pinout for the MC13883. Figure 25 through Figure 28 represent the package outline and provide package dimensions.

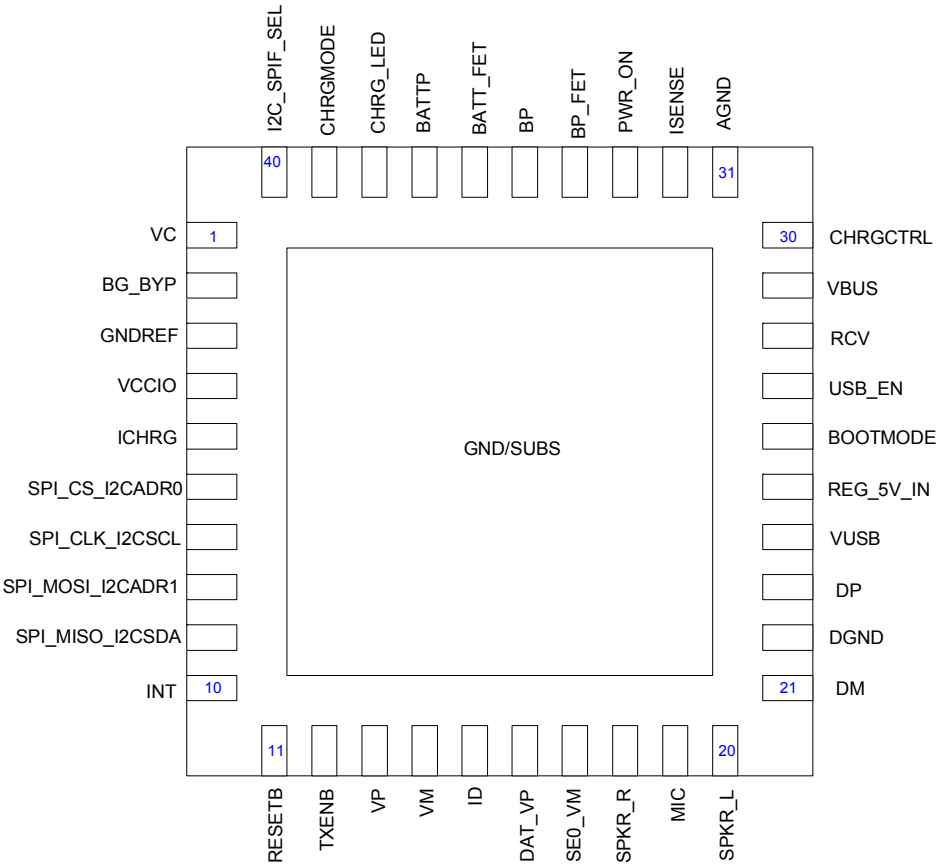

Figure 24. MC13883 Pinout

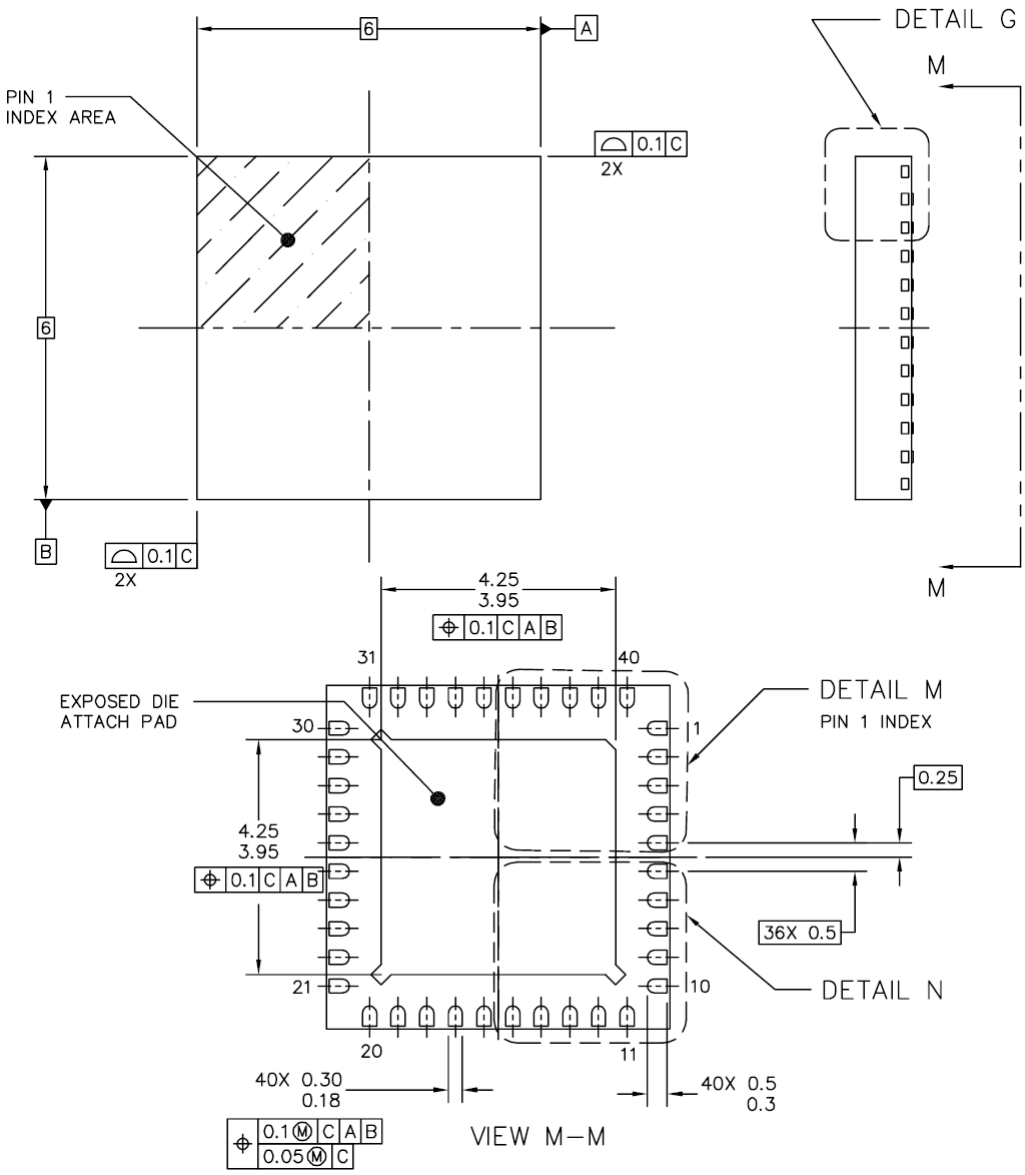

Figure 25. Outline Dimensions for QFN-40, 6x6 mm (Case Outline 1624-01, Issue O)

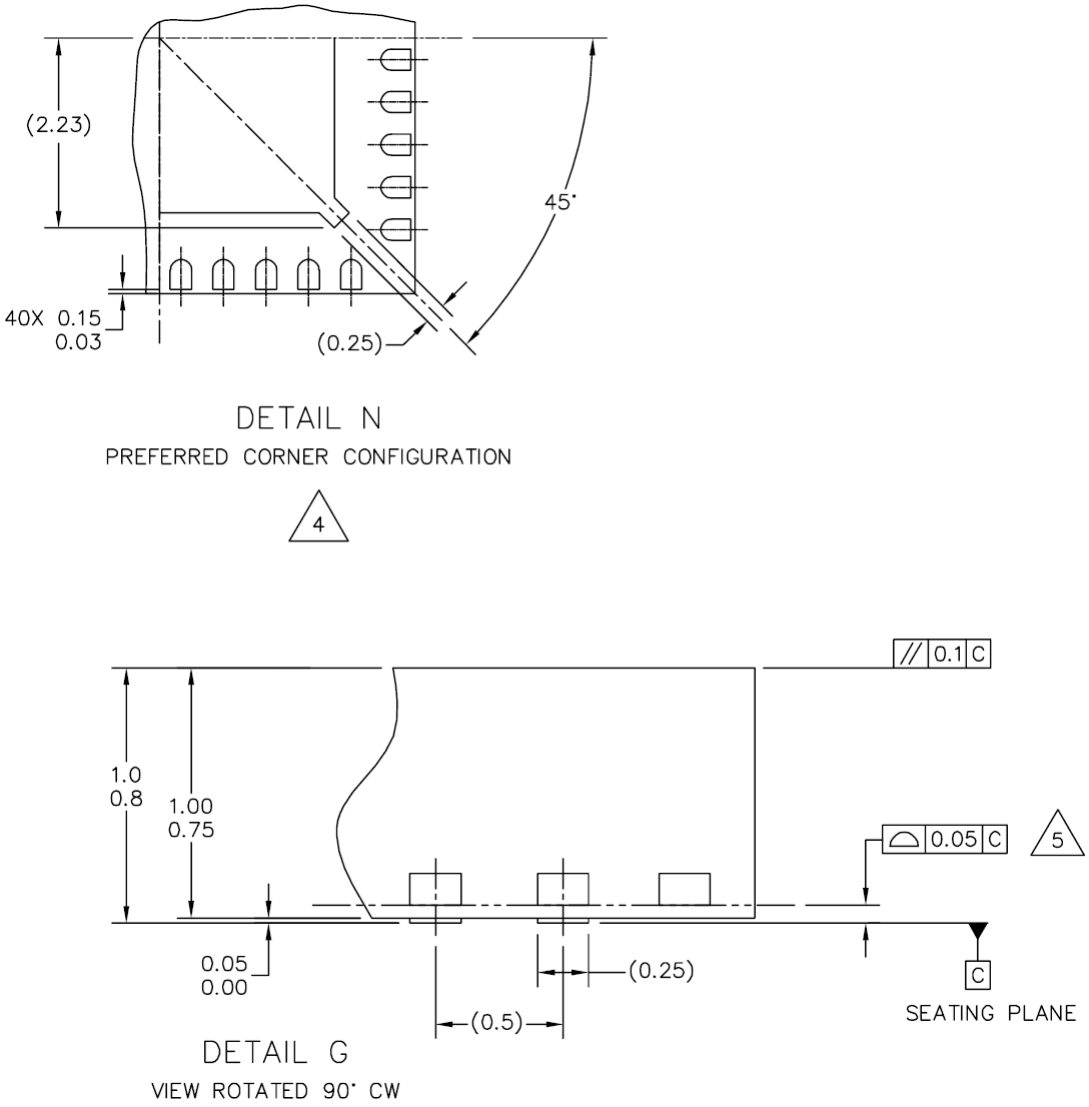

Figure 26. Outline Dimensions for QFN-40, 6x6 mm - Continued (Case Outline 1624-01, Issue O)

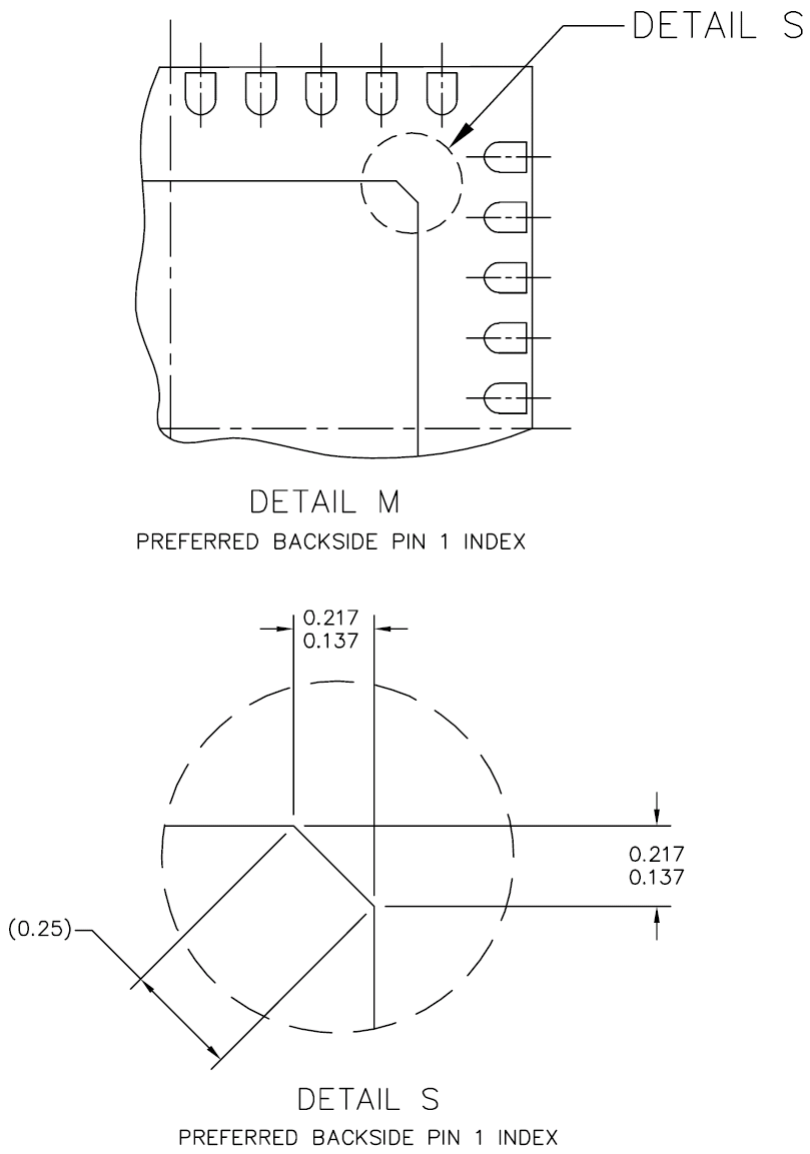

Figure 27. Outline Dimensions for QFN-40, 6x6 mm - Continued (Case Outline 1624-01, Issue O)

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. THE COMPLETE JEDEC DESIGNATOR FOR THIS PACKAGE IS: HF–PQFN.
4. CORNER CHAMFER MAY NOT BE PRESENT. DIMENSIONS OF OPTIONAL FEATURES ARE FOR REFERENCE ONLY.
5. COPLANARITY APPLIES TO LEADS, CORNER LEADS, AND DIE ATTACH PAD.
6. FOR ANVIL SINGULATED QFN PACKAGES, MAXIMUM DRAFT ANGLE IS 12°.
7. MINIMUM METAL GAP 0.2 MM.

Figure 28. Outline Dimensions for QFN-40, 6x6 mm - Continued (Case Outline 1624-01, Issue O)

9 Product Documentation

This data sheet is labeled as a particular type: Product Preview, Advance Information, or Technical Data. Definitions of these types are available at: http://www.freescale.com on the Documentation page.

Table 52 summarizes revisions to this document since the release (Rev. 2.2).

Table 52. Revision History

Location	Revision
Section 4.2.1, “Dual-Path Charging Overview”	Updated text
Section 4.2.2, “Serial Path Charging Overview”	Updated text
Section 4.2.3, “Single-Path Charging”	Updated text and added FET table
Table 7 Charge Control Logic Table (Dual Path)	Updated BATTP column
Table 8 Charge Control Logic Table (Serial Path)	Updated BATTP column
Table 9 Charge Control Logic Table (Single Path)	Updated FET_OVRD, FET_CTRL, BATT_FET, BATTP, and Trickle Charge columns
Section 4.2.11, “Standalone Trickle Charging”	New
Table 17 VCHRG Output Voltage Settings	Added VBUS to CHRGCTRL parameter
Section 4.2.15, “Constant Current / Constant Voltage Sense Bit (CC_CV)”	Updated text
Figure 13 Power-Up Control Circuit	Updated

Table 52 summarizes revisions to this document since the release (Rev. 2.3).

Table 53. Revision History

Location	Revision
Throughout Document	Changed from Product Preview to Technical Data.

How to Reach Us:

Home Page:
www.freescale.com

E-mail:
support@freescale.com

USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064, Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

***For Literature Requests Only*:**
Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-521-6274 or 303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

RoHS-compliant and/or Pb-free versions of Freescale products have the functionality and electrical characteristics of their non-RoHS-compliant and/or non-Pb-free counterparts. For further information, see http://www.freescale.com or contact your Freescale sales representative.

For information on Freescale’s Environmental Products program, go to http://www.freescale.com/epp.

Document Number: MC13883
Rev. 3
02/2010