MOTOROLA

*Advance Information*

# Dual PLL Frequency Synthesizers with DACs and Voltage Multiplier

**MC145225**
**MC145230**

**BiCMOS COMPONENT FOR 2 OR 3 VOLT SYSTEMS**

**SEMICONDUCTOR TECHNICAL DATA**

The MC145225 and MC145230 are dual frequency synthesizers containing very–low supply voltage circuitry. These devices support two independent loops with a single input reference and operate down to 1.8 V. Phase noise reduction circuitry is incorporated into each device.

The MC145225 is capable of direct usage up to 1.2 GHz on the main loop and up to 550 MHz on the secondary loop. The MC145230 is capable of direct usage up to 2.2 GHz on the main loop and up to 550 MHz on the secondary loop. Each device has a 32/33 prescaler for the main loop and an 8/9 prescaler for the secondary loop. Lock detection circuitry for each loop is multiplexed to a single output.

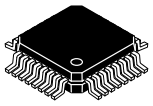
Two 8–bit DACs are powered through a dedicated pin. The DAC supply range is 1.8 to 3.6 V; this voltage may differ from the main supply.

An on–chip voltage multiplier supplies power to the phase/frequency detectors. Thus, in a 2 V application, the detectors are supplied with 4 V power. In 2.6 to 3.6 V applications, the multiplied voltage is regulated at approximately 5 V. The current source/sink phase/frequency detector for the main loop is designed to achieve faster lock times than a conventional detector. Both high and low current outputs are available along with a timer, double buffers, and a MOSFET switch to adjust the external low–pass filter response.

There are several levels of standby which are controllable with a 1–byte transfer through the serial port. Either of the PLLs and/or the reference oscillator may be independently placed in the low–power standby state. In addition, any of the phase/frequency detector outputs may be placed in the floating state to facilitate modulation of the external VCOs. Either DAC may be placed in standby via a 4–byte transfer.

- Operating Frequency
  MC145225 — Main Loop: 100 to 1200 MHz
  Secondary Loop: 50 to 550 MHz
  MC145230 — Main Loop: 500 to 2200 MHz
  Secondary Loop: 50 to 550 MHz
- Operating Supply Voltage: 1.8 to 3.6 V
- Nominal Supply Current, Both Loops Active — MC145225: 4 mA
  MC145230: 5 mA
- Maximum Standby Current, All Systems Shut Down: 10 μA
- Nominal Phase Detector Output Current:
  1.8 V Supply — $PD_{out}$–Hi: 2.8 mA, $PD_{out}$–Lo: 0.7 mA
  ≥ 2.5 V Supply — $PD_{out}$–Hi: 4.4 mA, $PD_{out}$–Lo: 1.1 mA
- Two Independent 8–Bit DACs with Separate Supply Pin (Up to 3.6 V)
- Lock Detect Output with Adjustable Lock Indication Window
- Independent R Counters Allow Independent Step Sizes for Each Loop
- Main Loop Divider Range: 992 to 262,143
- Secondary Loop Divider Range: 152 to 65,535
- Fractional Reference Counters Divider Range: 20 to 32,767.5
- Auxiliary Reference Divider with Small–Signal Differential Output — Ratios: 8, 10, 12.5
- Three General–Purpose Outputs
- Direct Interface to Motorola SPI Data Port Up to 10 Mbps

BitGrabber is a trademark of Motorola, Inc.



(Scale 2:1)

PLASTIC PACKAGE
CASE 873C
(LQFP–32, Tape & Reel Only)
VERY–SMALL 5 x 5 mm BODY

**DEVELOPMENT SYSTEM**

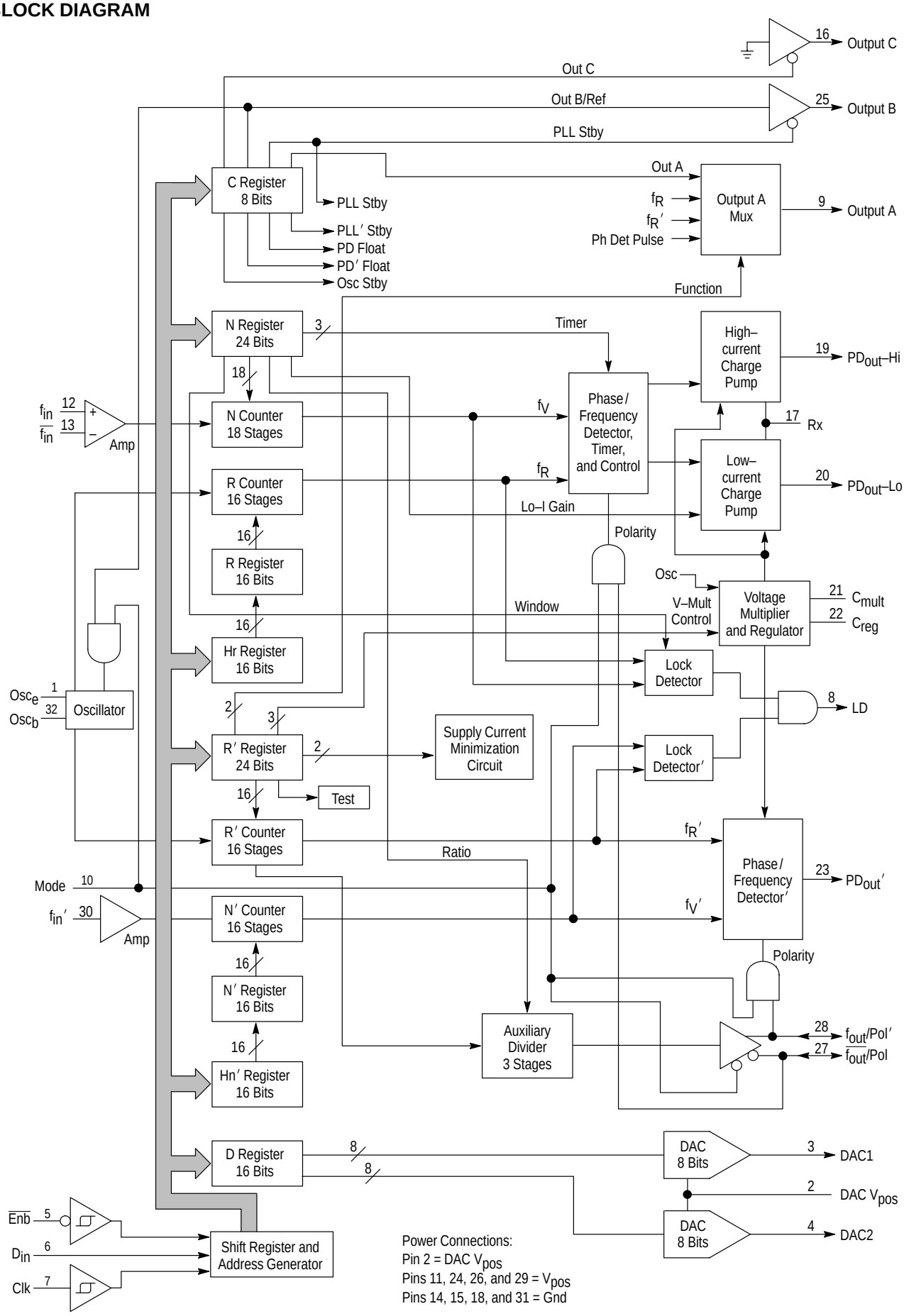
The MC145230EVK, which contains hardware and software, is strongly recommended for system development. (The user must provide the VCOs for evaluating the MC145181.) The software supports all features and modes of operation of the device. Up to four boards or devices can be controlled and the user is alerted to error conditions. The control program may be used with any board based on the MC145181, MC145225, or MC145230.

**ORDERING INFORMATION**

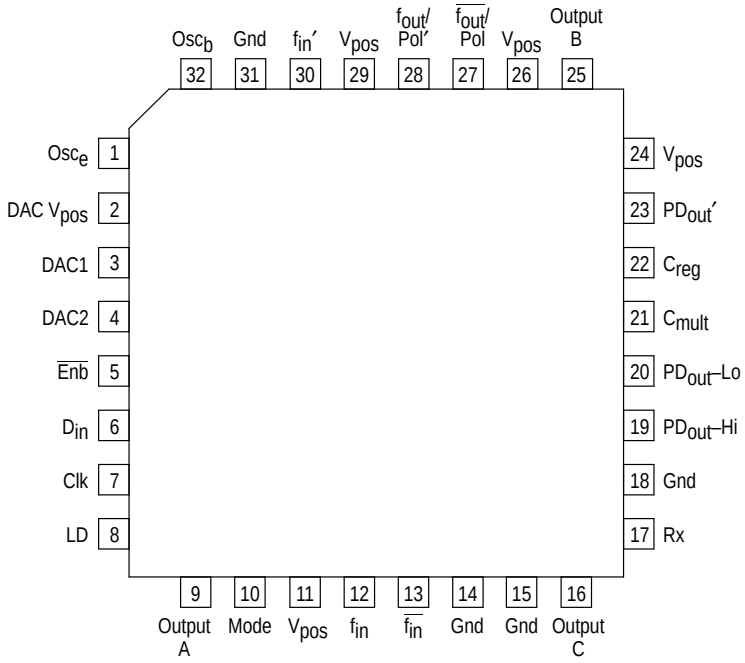
| Device | Main/Secondary Loop Maximum Frequency | Package |
|---|---|---|
| MC145225FTAR2 | 1200/550 MHz | LQFP–32 |
| MC145230FTAR2 | 2200/550 MHz | |

## CONTENTS

## 1. BLOCK DIAGRAM



## 2. PIN CONNECTIONS




This device contains 15,260 active transistors.

## 3. PARAMETER TABLES

### 3A. MAXIMUM RATINGS (Voltages Referenced to Gnd, unless otherwise stated)

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| DC Supply Voltages | $V_{pos}$, DAC $V_{pos}$ | –0.5 to 3.6 | V |
| DC Input Voltage — $Osc_e$, $f_{in}$, $f_{in}'$, Mode, $D_{in}$, Clk, $\overline{Enb}$, $f_{out}/Pol'$, $\overline{f_{out}}/Pol$ | $V_{in}$ | –0.5 to $V_{pos}$ + 0.5 | V |
| DC Output Voltage | $V_{out}$ | –0.5 to $V_{pos}$ + 0.5 | V |
| DC Input Current, per Pin | $I_{in}$ | ±10 | mA |
| DC Output Current, per Pin | $I_{out}$ | ±20 | mA |
| DC Supply Current, $V_{pos}$ and Gnd Pins | I | 25 | mA |
| Power Dissipation, per Package | $P_D$ | 100 | mW |
| Storage Temperature | $T_{stg}$ | –65 to 150 | °C |
| Lead Temperature, 1 mm from Case for 10 Seconds | $T_L$ | 260 | °C |

**NOTES:** 1. Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.
2. ESD (electrostatic discharge) immunity meets Human Body Model (HBM) up to 2000 V. Additional ESD data available upon request.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit.

### 3B. DC ELECTRICAL CHARACTERISTICS

$V_{pos}$ = 1.8 to 3.6 V, Voltages Referenced to Gnd, $T_A$ = –40 to 85°C, unless otherwise statedt

| Parameter | Condition | Symbol | Guaranteed Limit | Unit |
|---|---|---|---|---|
| Maximum Low–Level Input Voltage ($D_{in}$, Clk, $\overline{Enb}$, Mode, $f_{out}/Pol'$, $\overline{f_{out}}/Pol$) | $f_{out}/Pol'$ and $\overline{f_{out}}/Pol$ Configured as Inputs | $V_{IL}$ | 0.3 x $V_{pos}$ | V |
| Minimum High–Level Input Voltage ($D_{in}$, Clk, $\overline{Enb}$, Mode, $f_{out}/Pol'$, $\overline{f_{out}}/Pol$) | $f_{out}/Pol'$ and $\overline{f_{out}}/Pol$ Configured as Inputs | $V_{IH}$ | 0.7 x $V_{pos}$ | V |
| Minimum Hysteresis Voltage (Clk) | | $V_{Hys}$ | 100 | mV |
| Maximum Low–Level Output Voltage (LD, Output A, Output B) | $I_{out}$ = 20 µA | $V_{OL}$ | 0.1 | V |
| Minimum High–Level Output Voltage (LD, Output A, Output B) | $I_{out}$ = –20 µA | $V_{OH}$ | $V_{pos}$ – 0.1 | V |
| Minimum Low–Level Output Current (LD, Output A, Output B) | $V_{out}$ = 0.3 V | $I_{OL}$ | 0.7 | mA |
| Minimum High–Level Output Current (LD, Output A, Output B) | $V_{out}$ = $V_{pos}$ – 0.3 V | $I_{OH}$ | –0.7 | mA |
| Minimum Low–Level Output Current (Output C) | $V_{out}$ = 0.2 V | $I_{OL}$ | 2.8 | mA |
| Maximum Input Leakage Current ($D_{in}$, Clk, $\overline{Enb}$, Mode, $f_{out}/Pol'$, $\overline{f_{out}}/Pol$) | $V_{in}$ = $V_{pos}$ or Gnd; $f_{out}/Pol'$ and $\overline{f_{out}}/Pol$ Configured as Inputs | $I_{in}$ | ±1.0 | µA |
| Maximum Output Leakage Current (Output B, Output C) | $V_{out}$ = $V_{pos}$ or Gnd; Output in High–Impedance State | $I_{OZ}$ | ±1 | µA |
| Maximum ON Resistance (Output C) | 1.8 V ≤ $V_{pos}$ < 2.5 V Supply<br>2.5 V ≤ $V_{pos}$ ≤ 3.6 V Supply | $R_{on}$ | 75<br>50 | Ω |
| Maximum Standby Supply Current ($V_{pos}$ and DAC $V_{pos}$ Tied Together) | $V_{in}$ = $V_{pos}$ or Gnd; Outputs Open; Both PLLs in Standby Mode; Oscillator in Standby Mode; DAC1 and DAC2 Output = Zero; Keep–alive Oscillator Off (Notes 1, 2, and 3) | $I_{STBY}$ | 10 | µA |

**NOTES:** 1. The total supply current drain for the keep–alive oscillator, voltage multiplier, and regulator is approximately 250 µA.
2. When the Mode pin is tied high, bit C6 must be programmed to a 0 for minimum supply current drain. Otherwise, if C6 = 1, the current drain is approximately 8 µA for a 1.8 V supply and approximately 40 µA for a 3.6 V supply. This restriction on bit C6 does not apply when the Mode pin is tied low.
3. To ensure minimum standby supply current drain, the voltage potential at the $C_{mult}$ pin must not be allowed to fall below the potential at the $V_{pos}$ pins. See discussion in Section 5E under **$C_{mult}$**.

### 3C. $PD_{out}$–Hi AND $PD_{out}$–Lo PHASE/FREQUENCY DETECTOR CHARACTERISTICS

Nominal Output Current, $V_{pos}$ = 1.8 V: $PD_{out}$–Hi = 2.8 mA, $PD_{out}$–Lo = 0.7 or 0.35 mA
Nominal Output Current, $V_{pos}$ ≥ 2.5 V: $PD_{out}$–Hi = 4.4 mA, $PD_{out}$–Lo = 1.1 or 0.55 mA
Rx = 2.0 kΩ, Voltages Referenced to Gnd, Voltage Multiplier ON, $T_A$ = –40 to 85°C

| Parameter | Condition | Guaranteed Limit | Unit |
|---|---|---|---|
| Maximum Source Current Variation Part–to–Part (See Note) | $V_{out}$ = 0.5 x $V_{Cmult}$ | ±14 | % |
| Maximum Sink–versus–Source Mismatch (See Note) | $V_{out}$ = 0.5 x $V_{Cmult}$ | 20 | % |
| Output Voltage Range (See Note) | $I_{out}$ Variation ≤ 27% | 0.6 to $V_{Cmult}$ – 0.6 V | V |
| Maximum Three–State Leakage Current | $V_{out}$ = 0 or $V_{Cmult}$ | ±50 | nA |

**NOTE:** Percentages calculated using the following formula: (Maximum Value – Minimum Value) / Maximum Value.

### 3D. $PD_{out}'$ PHASE/FREQUENCY DETECTOR CHARACTERISTICS

$V_{pos}$ = 1.8 to 3.6 V, Voltages Referenced to Gnd, Voltage Multiplier ON, $T_A$ = –40 to 85°C

| Parameter | Condition | Guaranteed Limit | Unit |
|---|---|---|---|
| Minimum Low–Level Output Current | $V_{out}$ = 0.3 V | 0.3 | mA |
| Minimum High–Level Output Current | $V_{out}$ = $V_{Cmult}$ – 0.3 V | –0.3 | mA |
| Maximum Three–State Leakage Current | $V_{out}$ = 0 or $V_{Cmult}$ | ±50 | nA |

### 3E. DAC CHARACTERISTICS

$V_{pos}$ = 1.8 to 3.6 V, DAC $V_{pos}$ = 1.8 to 3.6 V; $T_A$ = –40 to 85°C

| Parameter | Condition | Guaranteed Limit | Unit |
|---|---|---|---|
| Resolution | | 8 | Bits |
| Maximum Integral Nonlinearity | | ±1 | LSB |
| Maximum Offset Voltage from Gnd | No External Load | 1 | LSB |
| Maximum Offset Voltage from DAC $V_{pos}$ | No External Load | 2 | LSB |
| Maximum Output Impedance | Over Entire Output Range, Including Zero Output (which is Low–power Standby) | 130 | kΩ |
| Maximum Standby Current | Zero Output, No External Load | (See $I_{STBY}$ in Section 3B) | |
| Maximum Supply Current per DAC @ DAC $V_{pos}$ pin | Except with Zero Output, No External Load | (DAC $V_{pos}$) / 36 | mA |

### 3F. VOLTAGE MULTIPLIER AND KEEP–ALIVE OSCILLATOR CHARACTERISTICS

Voltages Referenced to Gnd, $T_A$ = –40 to 85°C

| Parameter | Condition | Guaranteed Limit | Unit |
|---|---|---|---|
| Voltage Multiplier Output Voltage | 5 MHz Refresh Rate, 100 µA Continuous Sourcing, Measured at $C_{mult}$ pin<br>$V_{pos}$ = 1.8 V<br>$V_{pos}$ = 3.6 V | <br><br>3.32 to 3.78<br>4.75 to 5.35 | V |
| Keep–alive Refresh Frequency | $V_{pos}$ = 1.8 to 3.6 V | 300 to 700 | kHz |

### 3G. DYNAMIC CHARACTERISTICS OF DIGITAL PINS

$V_{pos}$ = 1.8 to 3.6 V, $T_A$ = –40 to 85°C, Input $t_r = t_f$ = 10 ns, $C_L$ = 25 pF

| Parameter | Figure No. | Symbol | Guaranteed Limit | Unit |
|---|---|---|---|---|
| Serial Data Clk Frequency<br>NOTE: Refer to Clk $t_w$ Below | 1 | $f_{clk}$ | dc to 10 | MHz |
| Maximum Propagation Delay, $\overline{Enb}$ to Output A (Selected as General–Purpose Output) | 2, 7 | $t_{PLH}$, $t_{PHL}$ | 200 | ns |
| Maximum Propagation Delay, $\overline{Enb}$ to Output B | 2, 3, 7, 8 | $t_{PLH}$, $t_{PHL}$, $t_{PZL}$, $t_{PLZ}$, $t_{PZH}$, $t_{PHZ}$ | 200 | ns |
| Maximum Propagation Delay, $\overline{Enb}$ to Output C | 4, 8 | $t_{PZL}$, $t_{PLZ}$ | 200 | ns |
| Maximum Output Transition Time, Output A; Output B with Active Pullup and Pulldown | 2, 7 | $t_{TLH}$, $t_{THL}$ | 75 | ns |
| Minimum Setup and Hold Times, $D_{in}$ versus Clk | 5 | $t_{su}$, $t_h$ | 30 | ns |
| Minimum Setup, Hold, and Recovery Times, $\overline{Enb}$ versus Clk | 6 | $t_{su}$, $t_h$, $t_{rec}$ | 100 | ns |
| Minimum Pulse Width, Inactive (High) Time, $\overline{Enb}$ | 6 | $t_w$ | * | cycles |
| Minimum Pulse Width, Clk | 1 | $t_w$ | 50 | ns |
| Maximum Input Capacitance — $D_{in}$, CLK, $\overline{Enb}$ | | $C_{in}$ | 10 | pF |

*For Hr register access, the minimum limit is 20 $Osc_e$ cycles.
For Hn′ register access, the minimum limit is 27 $f_{in}$′ cycles.
For N register access, the minimum limit is 20 $Osc_e$ cycles + 99 $f_{in}$ cycles.
When the timer is used for adapt, the minimum limit after the second N register access and before the next register access is the time–out interval + 99 $f_{in}$ cycles.

**Figure 1.**

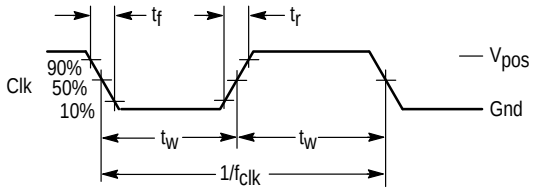



**Figure 2.**

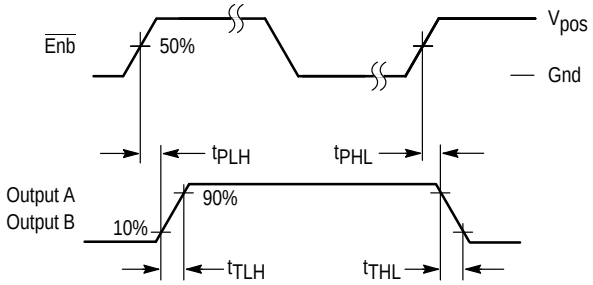



**Figure 3.**

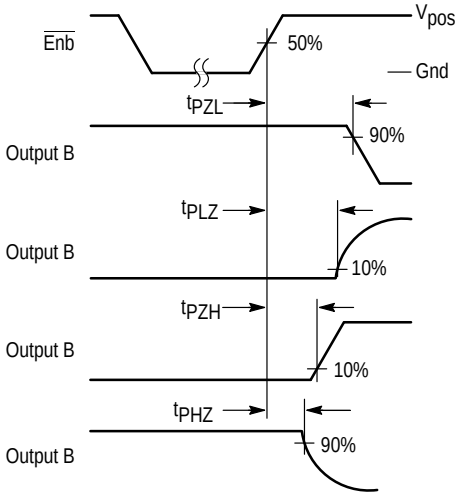



**Figure 4.**

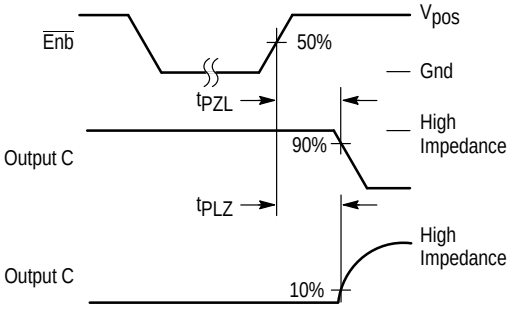



**Figure 5.**

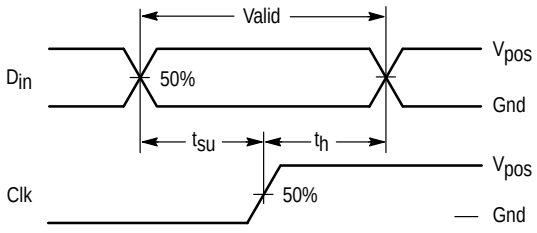



**Figure 6.**

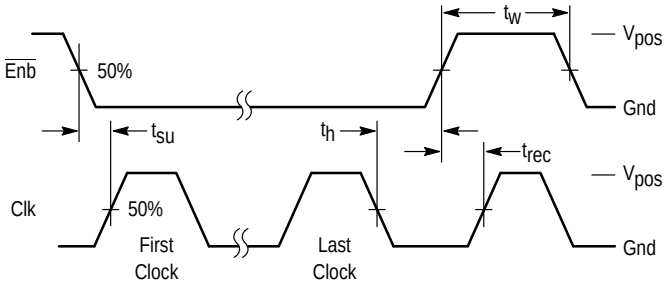
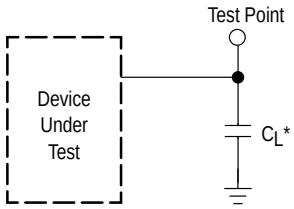
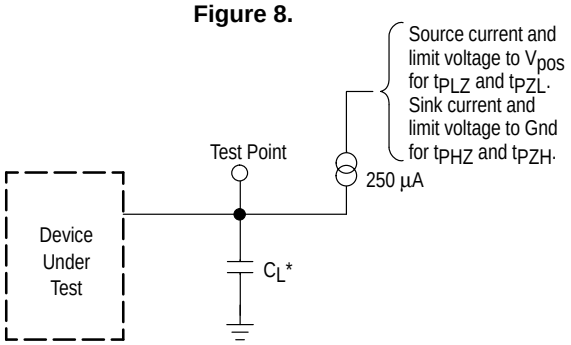



**Figure 7.**




* Includes all probe and fixture capacitance.

**Figure 8.**




* Includes all probe and fixture capacitance.

### 3H. DYNAMIC CHARACTERISTICS OF LOOP AND $f_{out}$ PINS

$V_{pos}$ = 1.8 to 3.6 V, $T_A$ = –40 to 85°C

| Symbol | Parameter | Condition | Figure No. | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $v_{in}$ | Input Voltage Range, $f_{in}$ | MC145225:<br>100 MHz ≤ $f_{in}$ < 400 MHz<br>400 MHz ≤ $f_{in}$ ≤ 1.2 GHz<br>MC145230:<br>500 MHz ≤ $f_{in}$ < 800 MHz<br>800 MHz ≤ $f_{in}$ ≤ 2.2 GHz | 9 | <br>300<br>100<br><br>200<br>100 | <br>600<br>500<br><br>600<br>500 | mVpp |
| $v_{in}'$ | Input Voltage Range, $f_{in}'$ | 50 MHz ≤ $f_{in}$ < 150 MHz<br>150 MHz ≤ $f_{in}$ ≤ 550 MHz | 10 | 400<br>175 | 600<br>600 | mVpp |
| $f_{Osce}$ | Input Frequency Range, $Osc_e$ | $v_{in}$ = 350 to 600 mVpp,<br>Device in External Reference Mode | 11 | 9 | 80 | MHz |
| $f_{Xtal}$ | Crystal Frequency, $Osc_b$ and $Osc_e$ | Device in Crystal Mode | * | 9 | 80 | MHz |
| $C_{in}$ | Input Capacitance of Pins $Osc_b$ and $Osc_e$ | | | — | — | pF |
| $f_{out}$ | Output Frequency Range, $f_{out}$ and $\overline{f_{out}}$ | Output Signal Swing > 300 mVpp per pin (600 mVpp differential) | 12 | 1 | 6.2 | MHz |
| $f_\phi$ | Operating Frequency Range of the Phase/Frequency Detectors, $PD_{out}$–Hi, $PD_{out}$–Lo, $PD_{out}'$ | | | dc | 600 | kHz |

* Refer to the **Crystal Oscillator Considerations** section.

**Figure 9.**

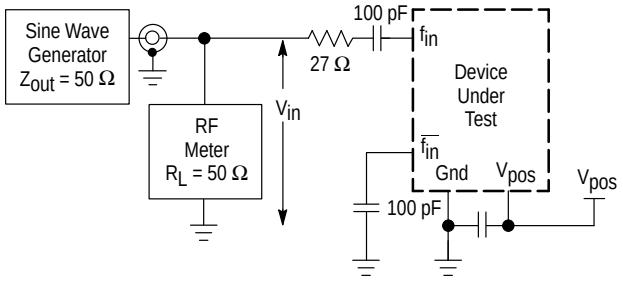



**Figure 10.**

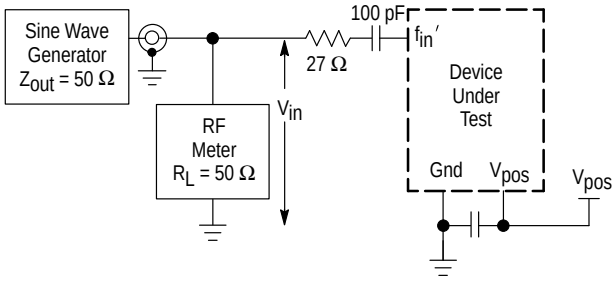



**Figure 11.**

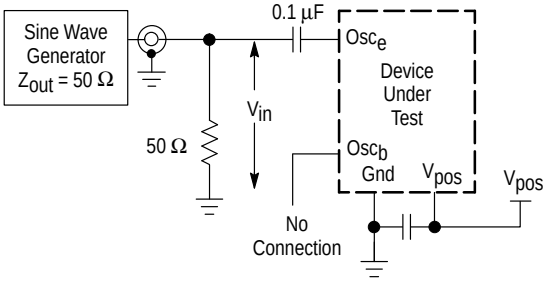
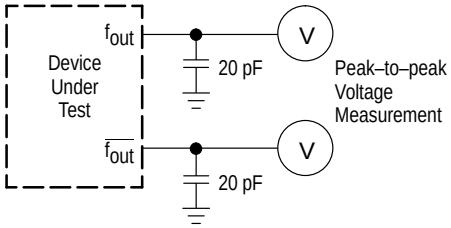



**Figure 12.**



## 4. DEVICE OVERVIEW

Refer to the Block Diagram in Section 1.

### 4A. SERIAL INTERFACE AND REGISTERS

The serial interface is comprised of a Clock pin (Clk), a Data In pin ($D_{in}$), and an Enable pin ($\overline{Enb}$). Information on the data input pin is shifted into a shift register on the low–to–high transition of the serial clock. The data format is most significant bit (MSB) first. Both Clk and $\overline{Enb}$ are Schmitt–triggered inputs.

The R and N registers contain counter divide ratios for the main loop, PLL. The R′ and N′ registers contain counter divide ratios for the secondary loop, PLL′. Additional contol bits are located in the R′, N, and C registers. The D register controls the digital–to–analog converters (DACs). Random access is allowed to the N, R′, Hr, Hn′, D, and C registers.

Two 16–bit holding registers, Hr and Hn′, feed registers R and N′, respectively. The R and N′ registers determine the divide ratios of the R and N′ counters, respectively. Thus, the information presented to the R and N′ counters is double–buffered. Using the proper programming sequence, new divide ratios may be presented to the N, R, and N′ counters; simultaneously.

$\overline{Enb}$ is used to activate the data port and allow transfer of data. To ensure that data is accepted by the device, the $\overline{Enb}$ signal line must initially be a high voltage (not asserted), then make a transition to a low voltage (asserted) prior to the occurrence of a serial clock, and must remain asserted until after the last serial clock of the burst. Serial data may be transferred in an SPI format (while $\overline{Enb}$ remains asserted). Data is transferred to the appropriate register on the rising edge of $\overline{Enb}$ (see Table 1). “Short shifting”, depicted as BitGrabber™ in the table, allows access to certain registers without requiring address bits. When $\overline{Enb}$ is inactive (high), Clk is inhibited from shifting the shift register.

The serial input pins may NOT be driven above the supply voltage applied to the $V_{pos}$ pins.

### 4B. REFERENCE INPUT AND COUNTERS CIRCUITS

#### Reference (Oscillator) Circuit

For the Colpitts reference oscillator, one pin ties to the base ($Osc_b$, pin 32) and the other ties to the emitter ($Osc_e$, pin 1), of an on–chip NPN transistor. In addition, the reference circuit may be operated in the external reference (XRef) mode as selectable via bit C6 when the Mode pin is high.

The $Osc_b$ and $Osc_e$ pins support an external fundamental or overtone crystal. The output of the oscillator is routed to both the reference counter for the main loop (R counter) and the reference counter for the secondary loop (R′ counter).

In a second mode, determined by bit C6 being 1 and the Mode pin being high, $Osc_e$ is an input which accepts an ac–coupled signal from a TCXO or other source. $Osc_b$ must be floated. If the Mode pin is low, this “XRef mode” is not allowed.

#### Reference Counter for Main Loop

Main reference counter R divides down the frequency at $Osc_e$ and feeds the phase/frequency detector for the main loop. The detector feeds the two charge pumps with outputs $PD_{out}$–Hi and $PD_{out}$–Lo. The division ratio of the R counter is determined by bits in the R register.

#### Reference Counter for Secondary Loop

Secondary reference counter R′ divides down the frequency at $Osc_e$ and feeds the phase/frequency detector for the secondary loop. The detector output is $PD_{out}$′. The division ratio of the R′ counter is determined by the 16 LSBs of the R′ register.

The R′ counter has a special mode to provide a frequency output at pins $f_{out}$ and $\overline{f_{out}}$ (differential outputs). These are low–jitter ECL–type outputs. With the Mode pin low, software control allows the $Osc_e$ frequency to be divided–by–8, –10, or –12.5 and routed to the $f_{out}$ pins. This output is derived by tapping off of a front–end stage of the R′ counter and feeding the auxiliary counter which provides the divided–down frequency. The chip must have the Mode pin low, which activates the $f_{out}$ pins. The actual R′ divide ratio must be divisible by 2 or 2.5 when the $f_{out}$ pins are activated. There is no such restriction when the Mode pin is high. See Section 6D, **R′ Register.**

### 4C. LOOP DIVIDER INPUTS AND COUNTER CIRCUITS

#### $f_{in}$ Inputs and Counter Circuit

$f_{in}$ and $\overline{f_{in}}$ are high–frequency inputs to the amplifier which feeds the N counter. A small signal can feed these inputs either differentially or single–ended.

The N counter divides down the external VCO frequency for the main loop. (The divide ratio of the N counter is also known as the loop multiplying factor.) The divide ratio of this counter is determined by the 18 LSBs of the N register. The output of the N counter feeds the phase/frequency detector for the main loop.

#### $f_{in}$′ Input and Counter Circuit

$f_{in}$′ is the high–frequency input to the amplifier which feeds the N′ counter. A small signal can feed this input single–ended.

The N′ counter divides down the external VCO frequency for the secondary loop. (The divide ratio of the N′ counter is also known as the loop multiplying factor.) The divide ratio of this counter is determined by bits in the N′ register. The output of the N′ counter feeds the phase/frequency detector for the secondary loop.

### 4D. VOLTAGE MULTIPLIER AND KEEP–ALIVE CIRCUITS

The voltage multiplier produces approximately two times the voltage present at the $V_{pos}$ pins over a supply range of 1.8 V to about 2.5 V. With a supply range of approximately 2.5 V to 3.6 V, the elevated voltage is regulated/limited to approximately 5 V. The elevated voltage, present at the $C_{mult}$ pin, is applied to both phase detectors. An external capacitor to Gnd is required on the $C_{mult}$ pin. The other capacitors required for the multiplier are on–chip.

A capacitor to Gnd is also required on the $C_{reg}$ pin. The voltage on this pin is equal to the voltage on the $V_{pos}$ pins over a supply range of 1.8 V to about 2.5 V. The voltage on

$C_{reg}$ is limited to approximately 2.5 V maximum when the $V_{pos}$ pins exceed 2.5 V.

The refresh rate determines the repetition rate that the capacitors for the voltage multiplier are charged. Refresh is normally derived off of the signal present at the $Osc_e$ pin, through a divider which is part of the voltage multiplier and regulator circuitry. The refresh rate is controlled via bits in the R′ register.

When the reference oscillator circuit is placed in standby, an on–chip keep–alive oscillator assists in maintaining the elevated voltage on the phase detectors. The keep–alive refresh rate is per the spec table in Section 3F.

If desired, the keep–alive oscillator can be inhibited from turning on, by placing the multiplier in the inactive state via R′ register bits. This causes the phase/frequency detector voltage to bleed off while in standby, but has the advantage of achieving the lowest supply current if all other sections of the chip are shut down.

### 4E. PHASE/FREQUENCY DETECTORS

#### Detector for Main Loop

The detector for the main loop senses the phase and frequency difference between the outputs of the R and N counters. The detector feeds both a high–current charge pump with output $PD_{out}$–Hi and a low–current charge pump with output $PD_{out}$–Lo.

The charge pumps can be operated in three conventional manners as controlled by bits in the N register. $PD_{out}$–Lo can be enabled with $PD_{out}$–Hi inhibited. Conversely, $PD_{out}$–Hi can be enabled with $PD_{out}$–Lo inhibited. Both outputs can be enabled and tied together externally for maximum charge pump current. Finally, both outputs can be inhibited. In this last case, they float. The outputs can also be forced to the floating state by a bit in the C register. This facilitates introduction of modulation into the VCO input.

The charge pumps can be operated in an adapt mode as controlled by bits in the N register. The bits essentially program a timer which determines how long $PD_{out}$–Hi is active. After the time–out, $PD_{out}$–Hi floats and $PD_{out}$–Lo becomes active. In addition, a second set of R and N counter values can be engaged after the time–out. For more information, see Table 16 and Section 8, **Programmer's Guide**.

#### Detector for Secondary Loop

The detector for the secondary loop senses the phase and frequency difference between the outputs of the R′ and N′ counters. Detector output $PD_{out}'$ is a voltage–type output with a three–state push–pull driver.

The output can be forced to the floating state by a bit in the C register. This facilitates introduction of modulation into the VCO input.

### 4F. LOCK DETECTORS

Window counters in each of the lock detector circuits determine the lock detector phase threshold for PLL and PLL′. The window counter divide ratio for the main loop's lock detector is controlled via a bit in the N register. The window counter divide ratio for the secondary loop is not controllable by the user.

The lock detector window determines a minimum phase difference which must occur before the Lock Detect pin goes high. Note that the lock detect signals for each loop drive an AND gate, which then feeds the LD pin. The LD pin indicates the condition of both loops, or the one active loop if the other is in standby. If both loops are in standby, LD is low indicating unlocked.

### 4G. DACs

The two independent 8–bit DACs facilitate crystal oscillator trimming and PA output power control. They are also suitable for any general–purpose use.

Each DAC utilizes an R–2R ladder architecture. The output pins, DAC1 and DAC2, are directly connected to the ladder; that is, there is no on–chip buffer.

The DAC outputs are determined by the contents of the D register. When a DAC output is zero scale, it is also in a low–power mode. The power–on reset (POR) circuit initializes the DACs in the low–power mode upon power up.

### 4H. GENERAL–PURPOSE OUTPUTS

There are three outputs which may be used as port expanders for a microcontroller unit (MCU).

Output A is actually a multi–purpose output with a push–pull output driver. See Table 2 for details.

Output B is a three–state output. The state of Output B depends on two bits; one of these bits also controls whether the main PLL is in standby or not. See Table 5 for details.

Output C is an open–drain output. The state of this output is controlled by one bit per Table 4. Output C is specified with a guaranteed ON resistance, and thus, may be used in an analog fashion.

## 5. PIN DESCRIPTIONS

### 5A. DIGITAL PINS

**$\overline{Enb}$, $D_{in}$, and Clk**
**Pins 5, 6, and 7 — Serial Data Port Inputs**

The $\overline{Enb}$ input is used to activate the serial interface to allow the transfer of data to the device. To transfer data to the device, the $\overline{Enb}$ pin must be low during the interval that the data is being clocked in. When $\overline{Enb}$ is taken back high (inactive), data is transferred to the appropriate register depending either on the data stream length or address bits. The C, Hr, and N registers can be accessed using either a unique data stream length (BitGrabber) or by using address bits (Conventional). The D, Hn′, and R′ registers can only be accessed using address bits. See Table 1.

The bit stream begins with the MSB and is shifted in on the low–to–high transition of Clk. The bit pattern is 1 byte (8 bits) long to access the C register, 2 bytes (16 bits) to access the Hr register, or 3 bytes (24 bits) to access the N register. A bit pattern of 4 bytes (32 bits) is used to access the registers when using address bits. The device has double buffers for storage of the N′ and R counter divide ratios. One double buffer is composed of the Hr register which feeds the R register. An Hr to R register transfer occurs whenever the N register is written. The other double buffer is the Hn′ register which feeds the N′ register. An Hn′ to N′ register transfer occurs whenever the N register is written. Thus, new divide ratios may be presented to the R, N′, and N counters simultaneously.

Transitions on $\overline{Enb}$ must not be attempted while Clk is high. This puts the device out of synchronization with the microcontroller. Resynchronization occurs whenever $\overline{Enb}$ is high (inactive) and Clk is low.

Data is retained in the registers over a supply range of 1.8 to 3.6 V. The bit–stream formats are shown in Figures 13 through 18.

**LD**
**Pin 8 — Lock Detectors Output**

This signal is the logical AND of the lock detect signals from both PLL and PLL′. For the main PLL, the phase window that defines “lock” is programmable via bit N22. The phase window for the secondary PLL′ is not programmable.

If either PLL or PLL′ is in standby, LD indicates the lock condition of the active loop only. If both loops are in standby, the LD output is a static low level.

Each PLL’s lock detector is in the high state when the respective loop is locked (the inputs to the phase detector being the same phase and frequency). The lock detect signal is in the low state when a loop is out of lock. See Figure 19.

Upon power up, the LD pin indicates a *not locked* condition. The LD pin is a push–pull CMOS output. If unused, LD should be left open.

**Output A**
**Pin 9 — Multiple–Purpose Digital Output**

Depending on control bits R′21 and R′20, Output A is selectable by the user as a general–purpose output (either high or low level), $f_R$ (output of main reference counter), $f_{R'}$ (output of secondary reference counter), or a phase detector pulse indicator for both loops. When selected as general–purpose output, bit C7 determines whether the output is a high or low level per Table 2. When configured as $f_R$, $f_{R'}$, or phase detector pulse, Output A appears as a normally low signal and pulses high.

Output A is a slew–rate limited CMOS totem–pole output. If unused, Output A should be left open.

**Table 1. Register Access**
(LSBs are C0, R0, N0, D0, R′0, and N′0)

| Access Type | Accessed Register | Address Nibble | Number of Clocks | Register Bit Nomenclature | Figure No. |
|---|---|---|---|---|---|
| BitGrabber | C | — | 8 | C7, C6, C5, ..., C0 | 13 |
| BitGrabber | Hr | — | 16 | R15, R14, R13, ..., R0 | 14 |
| BitGrabber | N | — | 24 | N23, N22, N21, ..., N0 | 15 |
| Conventional | C | $0 | 32 | C7, C6, C5, ..., C0 | 13 |
| Conventional | Hr | $1 | 32 | R15, R14, R13, ..., R0 | 14 |
| Conventional | N | $2 | 32 | N23, N22, N21, ..., N0 | 15 |
| Conventional | D | $3 | 32 | D15, D14, D13, ..., D0 | 18 |
| Conventional | R′ | $5 | 32 | R′23, R′22, R′21, ..., R′0 | 16 |
| Conventional | Hn′ | $4 | 32 | N′15, N′14, N′13, ..., N′0 | 17 |

**NOTE:** $0 denotes hexadecimal zero, $1 denotes hexadecimal one, etc.

**Table 2. Output A Configuration**

| Bit R′21 | Bit R′20 | Bit C7 | Function of Output A |
|---|---|---|---|
| 0 | 0 | 0 | General–Purpose Output, Low Level |
| 0 | 0 | 1 | General–Purpose Output, High Level |
| 0 | 1 | x | $f_R$ |
| 1 | 0 | x | $f_{R'}$ |
| 1 | 1 | x | Phase Detector Pulse Indicator |

### Mode
### Pin 10 — Mode Input

When the Mode pin is tied low (approximately Gnd), the pair of pins named $f_{out}$/Pol′ and $\overline{f_{out}}$/Pol become outputs $f_{out}$ and $\overline{f_{out}}$. As such, these pins are the divided down reference frequency. The division ratio is controlled by bits per Table 6. In addition, when Mode is low, the R′ counter is preceded by a fixed–divide prescaler. Also, only a crystal may be used at pins $Osc_b$ and $Osc_e$; an external reference, such as a TCXO, should not be used to drive either pin. The default on the phase detector polarity is positive. See the summary in Table 3.

When the Mode pin is tied high (approximately $V_{pos}$), the pair of pins named $f_{out}$/Pol′ and $\overline{f_{out}}$/Pol become inputs Pol′ and Pol. As such, these pins control the polarity of the phase/frequency detectors for PLL′ and PLL, respectively. In addition, when Mode is high, the R′ counter is preceded by a dual–modulus prescaler. Therefore, the R′ counter is completely programmable per Figure 16. Also, either a crystal or TCXO may be used with the device. See the summary in Table 3.

**Table 3. Mode Pin Summary**

| Attribute | Mode Pin = Low Level | Mode Pin = High Level |
|---|---|---|
| $f_{out}$/Pol′ pin | Pin is $f_{out}$ output; polarity of phase detector′ is positive | Pin is Pol′ input and controls polarity of phase detector′ |
| $\overline{f_{out}}$/Pol pin | Pin is $\overline{f_{out}}$ output; polarity of phase detector is positive | Pin is Pol input and controls polarity of phase detector |
| Oscillator circuit | Supports a crystal only | Supports crystal or accommodates TCXO |
| R′ counter | Programmable in increments of 2 or 2.5 | Programmable in increments of 0.5 |
| Output B pin | State of pin controlled by Bit C6 | Pin not used, Bit C6 controls whether crystal or TCXO is accommodated |

### Output C
### Pin 16 — General–Purpose Digital Output

This pin is controllable by bit C5 as either low level or high impedance per Table 4.

The output driver is an open–drain N–channel MOSFET connected to Gnd. The ESD (electrostatic discharge) protection circuit for this pin is tied to Gnd and $V_{pos}$. Thus, voltages above $V_{pos}$ are clipped at approximately 0.7 V above $V_{pos}$. If unused, Output C should be left open.

**Table 4. Output C Programming**

| Bit C5 | State of Output C Pin |
|---|---|
| 0 | Low level (ON resistance per Electrical Table) |
| 1 | High impedance (leakage per Electrical Table) |

### Output B
### Pin 25 — General–Purpose Digital Output

This pin is controllable by bits C6 and C1 as either low level, high level, or high impedance per Table 5. Note that whenever the main PLL is placed in standby by bit C1, Output B is forced to high impedance. The three–state MOSFET output is slew–rate limited. If unused, Output B should be left open.

**Table 5. Output B Programming**

| Bit C6 | Bit C1 | State of Output B Pin | Condition of Main PLL |
|---|---|---|---|
| 0 | 0 | Low level | Active |
| 0 | 1 | High impedance* | Standby* |
| 1 | 0 | High level | Active |
| 1 | 1 | High impedance | Standby |

*Power–up default.

### $f_{out}$/Pol′ and $\overline{f_{out}}$/Pol
### Pins 28 and 27 — Dual–purpose Outputs/Inputs

These pins are outputs when the Mode pin is low and inputs when the Mode pin is high.

When the Mode pin is low, these pins are small–signal differential outputs $f_{out}$ and $\overline{f_{out}}$ with a frequency derived from the signal present at the $Osc_e$ pin. The frequency of the output signal is per Table 6. If this function is not needed, the Mode pin should be tied high, which minimizes supply current. In this case, these inputs must be tied high or low per Tables 7 and 8.

**Table 6. $f_{out}$ and $\overline{f_{out}}$ Frequency**
(Mode Pin = Low)

| Bit N23 | Bit R′1 | Bit R′0 | Output Frequency |
|---|---|---|---|
| 0 | 0 | 0 | $Osc_e$ divided by 10 |
| 0 | 0 | 1 | $Osc_e$ divided by 12.5 |
| 0 | 1 | 0 | $Osc_e$ divided by 12.5 |
| 0 | 1 | 1 | $Osc_e$ divided by 12.5 |
| 1 | 0 | 0 | $Osc_e$ divided by 8 |
| 1 | 0 | 1 | $Osc_e$ divided by 10 |
| 1 | 1 | 0 | $Osc_e$ divided by 10 |
| 1 | 1 | 1 | $Osc_e$ divided by 10 |

When the Mode pin is high, these pins are digital inputs Pol′ and Pol which control the polarity of the phase/frequency detectors. See Tables 7 and 8. Positive polarity is used when an increase in an external VCO control voltage input causes an increase in VCO output frequency. Negative polarity is used when a decrease in an external VCO control voltage input causes an increase in VCO output frequency.

**Table 7. Main Phase/Frequency Detector Polarity**
(Mode Pin = High)

| Mode Pin | Pol Pin | Main Detector Polarity ($PD_{out}$–Lo and $PD_{out}$–Hi) |
|---|---|---|
| High | Low | Positive |
| High | High | Negative |
| Low | * | Positive |

*Pin configured as an output; should not be driven.

**Table 8. Secondary Phase/Frequency Detector Polarity**
(Mode Pin = High)

| Mode Pin | Pol′ Pin | Secondary Detector Polarity ($PD_{out}'$) |
|---|---|---|
| High | Low | Positive |
| High | High | Negative |
| Low | * | Positive |

*Pin configured as an output; should not be driven.

## 5B. REFERENCE PINS

### $Osc_e$ and $Osc_b$
**Pins 1 and 32 — Reference Oscillator Transistor Emitter and Base**

These pins can be configured to support an external crystal in a Colpitts oscillator configuration. The required connections for the crystal circuit are shown in the **Crystal Oscillator Considerations** section.

Additionally, the pins can be configured to accept an external reference frequency source, such as a TCXO. In this case, the reference signal is ac coupled into $Osc_e$ and the $Osc_b$ pin is left floating. See Figure 11.

Bit C6 and the Mode input pin control the configuration of these pins per Table 9.

**Table 9. Reference Configuration**

| Mode Input Pin | Bit C6 | Reference Configuration | Comment |
|---|---|---|---|
| Low | X | Supports Crystal (default) | C6 used to control Output B* |
| High | 0 | Supports Crystal | Output B not useful |
| High | 1 | Requires External Reference | Output B not useful |

*See Table 5.

## 5C. LOOP PINS

### $f_{in}$ and $\overline{f_{in}}$
**Pins 12 and 13 — Frequency Input for Main Loop (PLL)**

These pins feed the on–chip RF amplifier which drives the high–speed N counter. This input may be fed differentially. However, it is usually used in a single–ended configuration with $f_{in}$ driven while $\overline{f_{in}}$ is tied to a good RF ground (via a capacitor). The signal source driving this input must be ac coupled and originates from an external VCO.

The sensitivity of the RF amplifier is dependent on frequency as shown in the Loop Specifications table. Sensitivity of the $f_{in}$ input is specified as a level across a 50 Ω load driven by a 50 Ω source. A VCO that can drive a load within the data sheet limits can also drive $f_{in}$. Usually, to avoid load pull and resultant frequency modulation of the VCO, $f_{in}$ is lightly coupled by a small value capacitor and/or a resistor. See the applications circuit of Figure 65.

### $f_{in}'$
**Pin 30 — Frequency Input for Secondary Loop (PLL′)**

This pin feeds the on–chip RF amplifier which drives the high–speed N′ counter. This input is used in a single–ended configuration. The signal source driving this input must be ac coupled and originates from an external VCO.

The sensitivity of the RF amplifier is dependent on frequency as shown in the Loop Specifications table. Sensitivity of the $f_{in}'$ input is specified as a level across a 50 Ω load driven by a 50 Ω source. A VCO that can drive a load within the data sheet limits can also drive $f_{in}'$. Usually, to avoid load pull and resultant frequency modulation of the VCO, $f_{in}'$ is lightly coupled by a small value capacitor and/or a resistor. See the applications circuit of Figure 65.

If the secondary loop is not used, PLL′ should be placed in standby and $f_{in}'$ should be left open.

### $PD_{out}$–Hi and $PD_{out}$–Lo
**Pins 19 and 20 — Phase/Frequency Detector Outputs for Main Loop (PLL)**

Each pin is a three–state current source/sink/float output for use as a loop error signal when combined with an external low–pass loop filter. Under bit control, $PD_{out}$–Lo has either one–quarter or one–eighth the output current of $PD_{out}$–Hi per Table 10. The detector is characterized by a linear transfer function (no dead zone). The polarity of the detector is controllable. The operation of the detector is described below and shown in Figure 20.

**Table 10. Current Ratio of $PD_{out}$–Hi and $PD_{out}$–Lo**

| Bit N18 | Output Current Ratio $PD_{out}$–Hi:$PD_{out}$–Lo (Gain Ratio) |
|---|---|
| 0 | 4 : 1 |
| 1 | 8 : 1 |

When the Mode pin is high, positive polarity occurs when the Pol pin is low. Also, when the Mode pin is low, polarity

defaults to positive. Positive polarity is described below. $f_V$ is the output of the main loop's VCO divider (N counter). $f_R$ is the output of the main loop's reference divider (R counter).

(a) Frequency of $f_V > f_R$ or phase of $f_V$ leading $f_R$: current–sinking pulses from a floating state.
(b) Frequency of $f_V < f_R$ or phase of $f_V$ lagging $f_R$: current–sourcing pulses from a floating state.
(c) Frequency and phase of $f_V = f_R$: essentially a floating state, voltage at pin determined by loop filter.

When the Mode pin is high, negative polarity occurs when the Pol pin is high. Negative polarity is described below. $f_V$ is the output of the main loop's VCO divider (N counter). $f_R$ is the output of the main loop's reference divider (R counter).

(a) Frequency of $f_V > f_R$ or phase of $f_V$ leading $f_R$: current–sourcing pulses from a floating state.
(b) Frequency of $f_V < f_R$ or phase of $f_V$ lagging $f_R$: current–sinking pulses from a floating state.
(c) Frequency and phase of $f_V = f_R$: essentially a floating state, voltage at pin determined by loop filter.

These outputs can be enabled and disabled by bits in the C and N registers. Placing the main PLL in standby (bit C1 = 1) forces the detector outputs to a floating state. In addition, setting the PD Float bit (bit C4 = 1) forces the detector outputs to a floating state while allowing the counters to run for the main PLL. For selection of the outputs, see Table 11.

The phase detector gain (in amps per radian) = $PD_{out}$ current (in amps) divided by $2\pi$.

If a detector output is not used, that pin should be left open.

**Table 11. Selection of Main Detector Outputs**

| Bit N21 | Bit N20 | Bit N19 | Result |
|---|---|---|---|
| 0 | 0 | 0 | Both outputs not enabled |
| 0 | 0 | 1 | $PD_{out}$–Lo enabled |
| 0 | 1 | 0 | $PD_{out}$–Hi enabled |
| 0 | 1 | 1 | Both $PD_{out}$–Lo and $PD_{out}$–Hi enabled |
| 1 | 0 | 0 | $PD_{out}$–Hi enabled for 16 $f_R$ cycles only, then $PD_{out}$–Lo enabled |
| 1 | 0 | 1 | $PD_{out}$–Hi enabled for 32 $f_R$ cycles only, then $PD_{out}$–Lo enabled |
| 1 | 1 | 0 | $PD_{out}$–Hi enabled for 64 $f_R$ cycles only, then $PD_{out}$–Lo enabled |
| 1 | 1 | 1 | $PD_{out}$–Hi enabled for 128 $f_R$ cycles only, then $PD_{out}$–Lo enabled |

**NOTES:** 1. When a detector output is not enabled, it is floating.
2. Setting bit N21 = 1 places the IC in an adapt mode and engages a timer.

**$PD_{out}'$**
**Pin 23 — Phase/Frequency Detector Output for Secondary Loop (PLL′)**

This pin is a three–state voltage output for use as a loop error signal when combined with an external low–pass loop filter. The detector is characterized by a linear transfer function (no dead zone). The polarity of the detector is controllable. The operation of the detector is described below and shown in Figure 21.

When the Mode pin is high, positive polarity occurs when the Pol′ pin is low. Also, when the Mode pin is low, polarity defaults to positive. Positive polarity is described below. $f_V'$ is the output of the secondary loop's VCO divider (N′ counter). $f_R'$ is the output of the secondary loop's reference divider (R′ counter.)

(a) Frequency of $f_V' > f_R'$ or phase of $f_V'$ leading $f_R'$: negative pulses from high impedance.
(b) Frequency of $f_V' < f_R'$ or phase of $f_V'$ lagging $f_R'$: positive pulses from high impedance.
(c) Frequency and phase of $f_V' = f_R'$: essentially a high–impedance state, voltage at pin determined by loop filter.

When the Mode pin is high, negative polarity occurs when the Pol′ pin is high. Negative polarity is described below. $f_V'$ is the output of the secondary loop's VCO divider (N′ counter). $f_R'$ is the output of the secondary loop's reference counter (R′ counter.)

(a) Frequency of $f_V' > f_R'$ or phase of $f_V'$ leading $f_R'$: positive pulses from high impedance.
(b) Frequency of $f_V' < f_R'$ or phase of $f_V'$ lagging $f_R'$: negative pulses from high impedance.
(c) Frequency and phase of $f_V' = f_R'$: essentially a high–impedance state, voltage at pin determined by loop filter.

This output can be enabled and disabled by bits in the C register. Placing the secondary PLL′ in standby (bit C0 = 1) forces the detector output to a high–impedance state. In addition, setting the PD′ Float bit (bit C3 = 1) forces the detector output to a high–impedance state while allowing the counters to run for PLL′.

The phase detector gain (in volts per radian) = $C_{mult}$ voltage (in volts) divided by $4\pi$.

If the secondary loop is not used, PLL′ should be placed in standby and $PD_{out}'$ should be left open.

## 5D. ANALOG OUTPUTS

**DAC1 and DAC2**
**Pins 3 and 4 — Digital–to–Analog Converter Outputs**

These are independent outputs of the two 8–bit D/A converters. The output voltage is determined by bits in the D register. Each output is a static level with an output impedance of approximately 100 kΩ.

The DACs may be used for crystal oscillator trimming, PA (power amplifier) output power control, or other general–purpose use.

If a DAC output is not used, the pin should be left open.

## 5E. EXTERNAL COMPONENTS

### Rx
**Pin 17 — Current–Setting Resistor**

An external resistor to Gnd at this pin sets a reference current that is used to determine the current at the phase/frequency detector outputs $PD_{out}$–Hi and $PD_{out}$–Lo. A value of 2 kΩ is required.

### $C_{mult}$
**Pin 21 — Voltage–Multiplier Capacitor**

An external capacitor to Gnd at this pin is used for the on–chip voltage multiplier circuit. The value of this capacitor must be greater than 20 times the value of the largest loop filter capacitor. For example, if the largest loop filter capacitor on either the main loop or the secondary loop is 0.01 μF, then a 0.22 μF capacitor could be used on the $C_{mult}$ pin.

To ensure minimum standby supply current drain, the voltage potential at the $C_{mult}$ pin must not be allowed to fall below the potential at the $V_{pos}$ pins. Therefore, if the keep–alive oscillator is shut off, the user should tie a large value resistor (> 10 MΩ) between the $C_{mult}$ pin and $V_{pos}$. This resistor should be sized to overcome leakage from $C_{mult}$ to Gnd due to the printed circuit board and the external capacitor. The consequence of not using the resistor is higher supply current drain in standby. If standby is not used, the resistor is not necessary. Also, if the keep–alive oscillator is used, the resistor can be omitted.

### $C_{reg}$
**Pin 22 — Regulator Capacitor**

An external capacitor to Gnd at this pin is required for the on–chip voltage regulator. A value of 1 μF is recommended.

## 5F. SUPPLY PINS

### DAC $V_{pos}$
**Pin 2 — Positive Supply Potential for DACs**

This pin supplies power to both DACs and determines the full–scale output of the DACs. The full–scale output is approximately equal to the voltage at DAC $V_{pos}$. The voltage applied to this pin may be more, less, or equal to the potential applied to the $V_{pos}$ pins. The voltage range for DAC $V_{pos}$ is 1.8 to 3.6 V with respect to the Gnd pins.

If both DACs are not used, DAC $V_{pos}$ should be tied to the same potential as $V_{pos}$.

### $V_{pos}$
**Pins 11, 24, 26, and 29 — Principal Positive Supply Potential**

These pins supply power to the main portion of the chip. All $V_{pos}$ pins must be at the same voltage potential. The voltage range for $V_{pos}$ is 1.8 to 3.6 V with respect to the Gnd pins.

For optimum performance, all $V_{pos}$ pins should be tied together and bypassed to a ground plane using a low–inductance capacitor mounted very close to the device. Lead lengths and printed circuit board traces between the capacitor and the IC package should be minimized. (The very–fast switching speed of the device can cause excessive current spikes on the power leads if they are improperly bypassed.)

### Gnd
**Pins 14, 15, 18, and 31 — Ground**

Common ground for the device. All Gnd pins must be at the same potential and should be tied to a ground plane.

## 6. DETAILED REGISTER DESCRIPTIONS

### 6A. C REGISTER

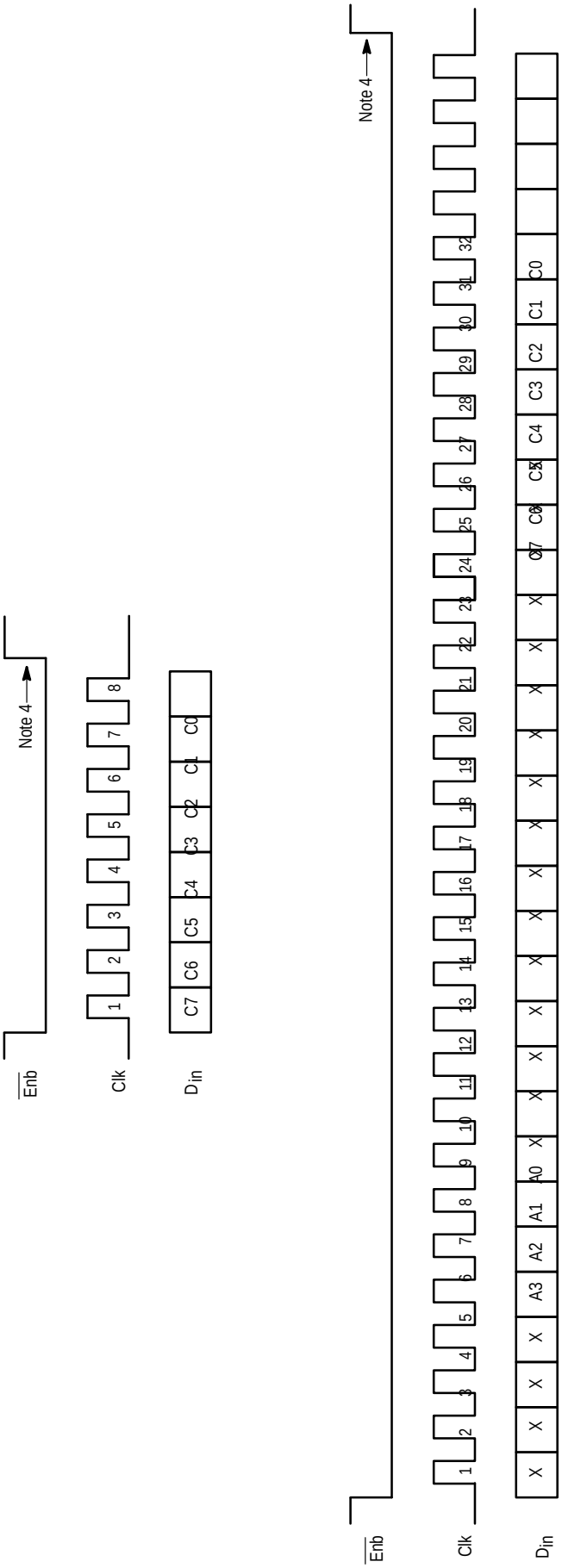



**Figure 13. C Register Access and Formats**

**NOTES:**
1. To access the C register, either 8 or 32 clock cycles can be used.
2. For the 8–bit stream, no address bits are needed.
3. For the 32–bit stream, address bits A3 through A0 are required.
4. At this point, the new byte is transferred to the C register. No other register is affected.
5. X signifies a don't care bit.

### C REGISTER BITS

See Figure 13 for C register access and serial data formats.

### Out A (C7)

When the Output A pin is selected as a General–Purpose Output (via bits R′21 = R′20 = 0), bit C7 determines the state of the pin. When C7 is 1, Output A is forced to a high level. When C0 is 0 Output A is forced low.

When Output A is not selected as a General–Purpose Output, bit C7 has no function; i.e., C7 is a “don’t care” bit.

### Out B/XRef (C6)

Bit C6 is a dual–purpose bit.

When the Mode pin is tied low, C6 and C1 (PLL Stby), can be used to control Output B. See Table 12. (The reference circuit defaults to crystal configuration.)

When the Mode pin is tied high, additional control of the reference circuit is allowed. See Table 13.

**Table 12. Out B/XRef Bit with Mode Pin = Low**

| Bit C6 | Bit C1 | State of Output B Pin | Condition of Main PLL |
|---|---|---|---|
| 0 | 0 | Low level | Active |
| 0* | 1* | High impedance* | Standby* |
| 1 | 0 | High level | Active |
| 1 | 1 | High impedance | Standby |

*Power up default.

**Table 13. Out B/XRef Bit with Mode Pin = High**

| Bit C6 | Reference Configuration |
|---|---|
| 0* | Supports Crystal* |
| 1 | Accommodates External Reference |

*Power up default.

### Out C (C5)

This bit determines the state of the Output C pin. When C5 is 1, Output C is forced to a high–impedance state. When C5 is 0, Output C is forced low.

### PD Float (C4)

This bit controls the phase detector for the main loop, outputs $PD_{out}$–Hi and $PD_{out}$–Lo. When this bit is 0, the main phase detector operates normally. When the bit is 1, the outputs are forced to the floating state which opens the loop and allows modulation to be introduced into the external VCO input. During this time, the counters are still active. This bit is inhibited from affecting the phase detector during a $PD_{out}$–Hi or $PD_{out}$–Lo pulse.

If the loop is locked prior to C4 being set to 1, the lock detect signal from the main loop continues to indicate “lock” immediately after PD Float is set to 1. If the phase of the loop drifts outside the lock detect window, then the lock detect signal indicates “not locked”. If the loop is not locked, and PD Float is set to 1, then the lock detect signal from the main loop continues to indicate “not locked”.

### PD′ Float (C3)

This bit controls the phase/frequency detector for the secondary loop, output $PD_{out}'$. When this bit is 0, the secondary phase detector operates normally. When the bit is 1, the output is forced to the floating state which opens the loop and allows modulation to be introduced into the external VCO input. During this time, the counters are still active. This bit is inhibited from affecting the phase detector during a $PD_{out}'$ pulse.

If the loop is locked prior to C3 being set to 1, the lock detect signal from the secondary loop continues to indicate “lock” immediately after PD′ Float is set to 1. If the phase of the loop drifts outside the lock detect window, then the lock detect signal indicates “not locked”. If the loop is not locked, and PD′ Float is set to 1, then the lock detect signal from the secondary loop continues to indicate “not locked”.

### Osc Stby (C2)

This bit controls the crystal oscillator and external reference input circuit. When this bit is 0, the circuit is active. When the bit is 1, the circuit is shut down and is in the low–power standby mode. When this circuit is shut down, a keep–alive oscillator for the voltage doubler is activated, unless the doubler is shut off via bits in the R′ register. In the crystal oscillator mode, when C2 transitions from a 1 to a 0 state, a kick–start circuit is engaged for a few milliseconds. The kick–start circuit ensures self–starting for a properly–designed crystal oscillator

**NOTE**

Whenever C2 is 1, both bits C1 and C0 must be 1, also.

To minimize standby supply current, the voltage multiplier may be shut down (by bits R′19, R′18, and R′17 being all zeroes). If this is the case and the voltage multiplier feature is being used, the user must allow sufficient time for the phase/frequency detector supply voltage to pump up when the multiplier is brought out of standby. This “pump up” time is dependent on the $C_{mult}$ capacitor size. Pump current is approximately 100 μA. During the pump up time, either the PLL standby bits C1 and C2 must be 1 or the phase/frequency detector float bits C3 and C4 must be 1.

### PLL Stby (C1)

When set to 1, this bit places the main PLL in the standby mode for reduced power consumption. $PD_{out}$–Hi and $PD_{out}$–Lo are forced to the floating state, the N and R counters are inhibited from counting, the main loop’s input amp is shut off, the Rx current is inhibited, and the main phase/frequency detector is shut off. The reference oscillator circuit is still active and independently controlled by bit C2.

When this bit is programmed to 0, the main PLL is taken out of standby in two steps. First, the input amplifier is activated, all counters are enabled, and the Rx current is no longer inhibited. Any $f_R$ and $f_V$ signals are inhibited from toggling the phase/frequency detectors and lock detector at this time. Second, when the $f_R$ pulse occurs, the N counter is loaded, and the phase/frequency and lock detectors are initialized via both flip–flops being reset. Immediately after the load, the N and R counters begin counting down together. At this point, the $f_R$ and $f_V$ pulses are enabled to the phase

and lock detectors, and the phase/frequency detector output is enabled to issue an error correction pulse on the next $f_R$ and $f_V$ pulses. (Patent issued on this method.)

During standby, data is retained in all registers and any register may be accessed. When setting or clearing the PLL Stby bit, other bits in the C register may be changed simultaneously.

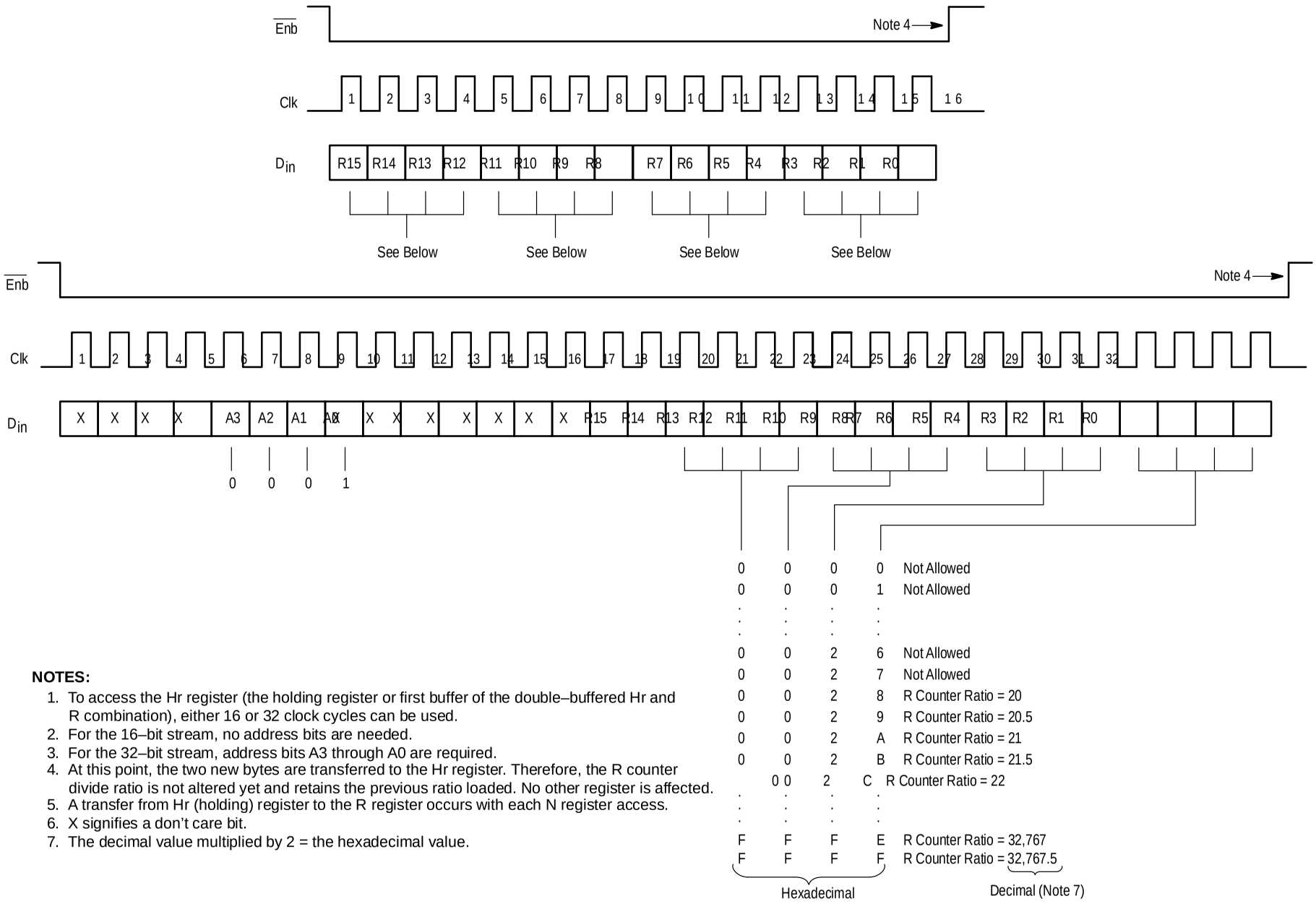
**PLL′ Stby (C0)**

When set to 1, this bit places the PLL′ section of the chip, which includes the on–chip $f_{in}$′ input amp, in the standby mode for reduced power consumption. $PD_{out}$′ is forced to the floating state. The R′ and N′ counters are inhibited from counting and placed in the low–current mode. The exception is the R′ counter's prescaler when the Mode pin is low. The R′ counter's prescaler remains active along with the $f_{out}$ and $\overline{f_{out}}$ pins when PLL′ is placed in standby (Mode pin = low). When the Mode pin is low, the $f_{out}$ pin, $\overline{f_{out}}$ pin, and R′ counter's prescaler are shut down only when Osc Stby bit C2 is set to 1.

When C0 is reset to 0, PLL′ is taken out of standby in two steps. All PLL′ counters and the input amp are enabled. Any $f_R$′ and $f_V$′ signals are inhibited from toggling the associated phase/frequency detector at this time. Second, when the $f_R$′ pulse occurs, the N′ counter is loaded and the phase/frequency detector is initialized via both flip–flops being reset. Immediately after the load, the N′ and R′ counters begin counting down together. At this point, the $f_R$′ and $f_V$′ pulses are enabled to the phase and lock detectors, and the phase/frequency detector output is enabled to issue an error correction pulse on the next $f_R$′ and $f_V$′ pulses. (Patent issued on this method.)

During standby, data is retained in all registers, and any register may be accessed. When setting or clearing the PLL′ Stby bit, other bits in the C register may be changed simultaneously.

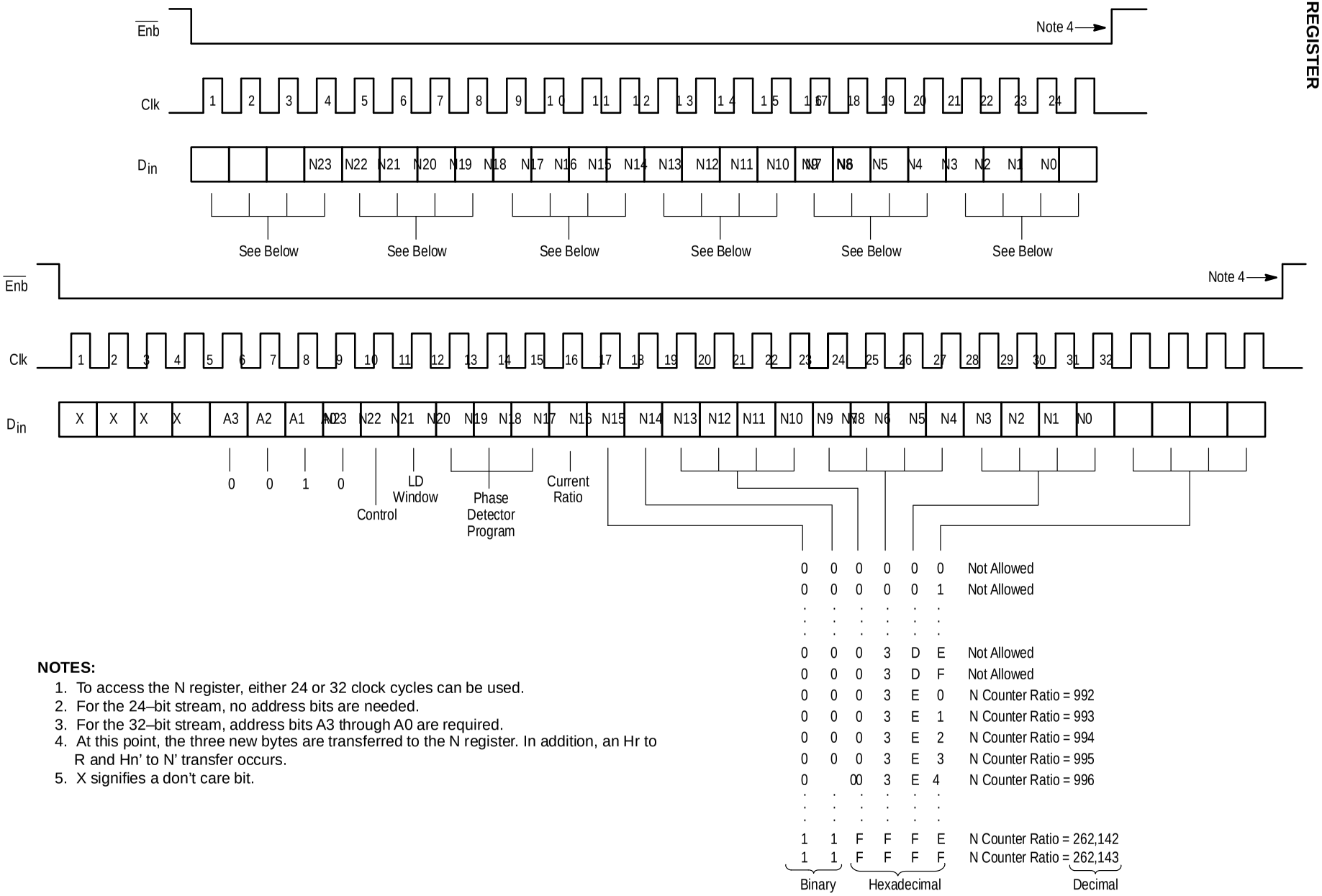
**Figure 14. Hr Register Access and Formats**




**NOTES:**

1. To access the Hr register (the holding register or first buffer of the double–buffered Hr and R combination), either 16 or 32 clock cycles can be used.
2. For the 16–bit stream, no address bits are needed.
3. For the 32–bit stream, address bits A3 through A0 are required.
4. At this point, the two new bytes are transferred to the Hr register. Therefore, the R counter divide ratio is not altered yet and retains the previous ratio loaded. No other register is affected.
5. A transfer from Hr (holding) register to the R register occurs with each N register access.
6. X signifies a don't care bit.
7. The decimal value multiplied by 2 = the hexadecimal value.

**Figure 15. N Register Access and Formats**




**NOTES:**

1. To access the N register, either 24 or 32 clock cycles can be used.
2. For the 24–bit stream, no address bits are needed.
3. For the 32–bit stream, address bits A3 through A0 are required.
4. At this point, the three new bytes are transferred to the N register. In addition, an Hr to R and Hn' to N' transfer occurs.
5. X signifies a don't care bit.

### N REGISTER BITS

See Figure 15 for N register access and serial data formats.

### Control (N23)

When the Mode pin is low, Control bit N23 determines the divide ratio of the auxiliary divider which feeds the buffers for the $f_{out}$ and $\overline{f_{out}}$ pins. See Table 14 for the overall ratio between $Osc_e$ and $f_{out}/\overline{f_{out}}$.

When the Mode pin is high, N23 must be programmed to 1.

**Table 14. $Osc_e$ to $f_{out}$ Frequency Ratio, Mode = Low**

| N23 | R′1 | R′0 | $Osc_e$ to $f_{out}$ Frequency Ratio |
|---|---|---|---|
| 0 | 0 | 0 | 10:1 |
| 0 | 0 | 1 | 12.5:1 |
| 0 | 1 | 0 | 12.5:1 |
| 0 | 1 | 1 | 12.5:1 |
| 1 | 0 | 0 | 8:1 |
| 1 | 0 | 1 | 10:1 |
| 1 | 1 | 0 | 10:1 |
| 1 | 1 | 1 | 10:1 |

### LD Window (N22)

Bit N22 determines the lock detect window for the main loop. Refer to Table 15 and Figure 19.

**Table 15. Lock Detect Window**

| N22 | LD Window (Approximated) |
|---|---|
| 0 | 32 $Osc_e$ periods |
| 1 | 128 $Osc_e$ periods |

### Phase Detector Program (N21, N20, N19)

These bits control which phase detector outputs are active for the main loop. These bits also control the timer interval when adapt is utilized for the main loop. See Table 16.

**Table 16. Main Phase Detector Control**

| N21 | N20 | N19 | Result |
|---|---|---|---|
| 0 | 0 | 0 | Both $PD_{out}$–Hi and $PD_{out}$–Lo floating |
| 0 | 0 | 1 | $PD_{out}$–Hi floating, $PD_{out}$–Lo enabled |
| 0 | 1 | 0 | $PD_{out}$–Hi enabled, $PD_{out}$–Lo floating |
| 0 | 1 | 1 | Both $PD_{out}$–Hi and $PD_{out}$–Lo enabled |
| 1 | 0 | 0 | $PD_{out}$–Hi enabled and $PD_{out}$–Lo floating for 16 $f_R$ cycles, then $PD_{out}$–Hi floating and $PD_{out}$–Lo enabled |
| 1 | 0 | 1 | $PD_{out}$–Hi enabled and $PD_{out}$–Lo floating for 32 $f_R$ cycles, then $PD_{out}$–Hi floating and $PD_{out}$–Lo enabled |
| 1 | 1 | 0 | $PD_{out}$–Hi enabled and $PD_{out}$–Lo floating for 64 $f_R$ cycles, then $PD_{out}$–Hi floating and $PD_{out}$–Lo enabled |
| 1 | 1 | 1 | $PD_{out}$–Hi enabled and $PD_{out}$–Lo floating for 128 $f_R$ cycles, then $PD_{out}$–Hi floating and $PD_{out}$–Lo enabled |

### Current Ratio (N18)

This bit allows for MCU control of the $PD_{out}$–Hi to $PD_{out}$–Lo current (or gain) ratio on the main loop phase/frequency detector outputs. See Table 17.

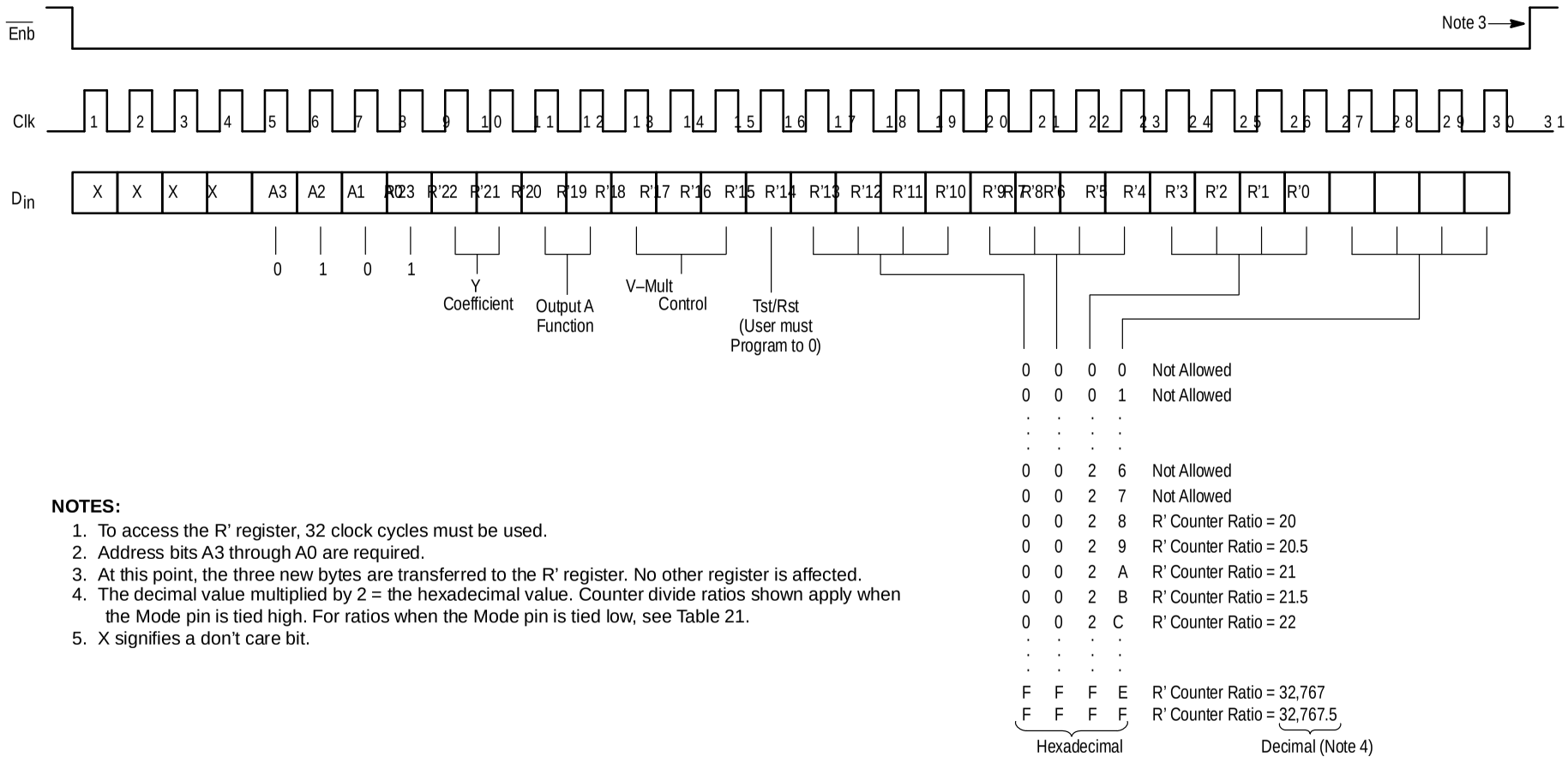
**Table 17. $PD_{out}$–Hi to $PD_{out}$–Lo Current Ratio**

| N18 | $PD_{out}$–Hi to $PD_{out}$–Lo Current Ratio | $PD_{out}$–Hi Current $C_{mult}$ Pin = 5 V (Nominal) | $PD_{out}$–Lo Current $C_{mult}$ Pin = 5 V (Nominal) |
|---|---|---|---|
| 0 | 4:1 | 4.4 mA | 1.1 mA |
| 1 | 8:1 | 4.4 mA | 0.55 mA |

### N Counter Divide Ratio (N17 to N0)

These bits control the N Counter divide ratio or loop multiplying factor. The minimum allowed value is 992. The maximum value is 262,143. For ease of programming, binary representation is used. For example, if a divide ratio of 1000 is needed, the 1000 in decimal is converted to binary 00 0000 0011 1110 1000 and is loaded into the device for N17 to N0. See Figure 15.

**Figure 16. R' Register Access and Format**




**NOTES:**

1. To access the R' register, 32 clock cycles must be used.
2. Address bits A3 through A0 are required.
3. At this point, the three new bytes are transferred to the R' register. No other register is affected.
4. The decimal value multiplied by 2 = the hexadecimal value. Counter divide ratios shown apply when the Mode pin is tied high. For ratios when the Mode pin is tied low, see Table 21.
5. X signifies a don't care bit.

### R′ REGISTER BITS

See Figure 16 for R′ register access and serial data format.

### Y Coefficient (R′23 and R′22)

These bits are programmed per Table 18. Note that for the MC145181, the bits are always programmed as 00. For compatibility, the other combinations are reserved for use with the MC145225 and MC145230.

**Table 18. Y Coefficient**

| R′23 | R′22 | Maximum Allowed Frequency at $f_{in}$ Pin |
|---|---|---|
| 0 | 0 | 550 MHz |
| 0 | 1 | 1.2 GHz |
| 1 | 0 | 2.2 GHz |
| 1 | 1 | (not used) |

### Output A Function (R′21 and R′20)

These bits control the function of the Output A pin per Table 19. When selected as a general–purpose output, bit C7 controls the state of the pin. The signals $f_R$ and $f_{R'}$ are the outputs of the R and R′ counters, respectively. The selection as a detector pulse is a test feature.

**Table 19. Output A Function Selection**

| R′21 | R′20 | Function Selected for Output A |
|---|---|---|
| 0 | 0 | General–Purpose Output |
| 0 | 1 | $f_R$ |
| 1 | 0 | $f_{R'}$ |
| 1 | 1 | Phase/Frequency Detector Pulse from both loops |

### V–Mult Control (R′19, R′18, R′17)

These bits control the voltage multiplier per Table 20. When the multiplier is in the active state, the bits determine the voltage multiplier's refresh rate of the capacitor tied to the $C_{mult}$ pin.

When active, the bits should be programmed for the lowest possible maximum frequency shown in the table. This ensures that the voltage multiplier is operating at optimum efficiency. For example, for a system utilizing a 16.8 MHz reference, bits R′19, R′18, and R′17 should be programmed as 001 if the user desires to use the voltage multiplier. If the user does not want to use the multiplier, the bits should be programmed as 000. In the latter case, only a 0.1 μF bypass capacitor is needed at the $C_{mult}$ pin and an external phase/frequency detector supply voltage of 3.6 to 5.25 V must be provided to the $C_{mult}$ pin.

**Table 20. Voltage Multiplier Control**

| R′19 | R′18 | R′17 | Multiplier State | Maximum Allowed Frequency at $Osc_e$ Pin |
|---|---|---|---|---|
| 0 | 0 | 0 | Inactive | 80 MHz |
| 0 | 0 | 1 | Active | 20 MHz |
| 0 | 1 | 0 | Active | 40 MHz |
| 0 | 1 | 1 | Active | 80 MHz |
| 1 | X | X | — | (for factory evaluation) |

### Test/Rst (R′16)

This bit must be programmed to 0 by the user.

### R′ Counter Divide Ratio (R′15 to R′0)

These bits control the R′ counter divide ratio. Thus, these bits determine the secondary loop's minimum step size. This step size is the same as the phase/frequency detector's operating frequency which must not exceed 600 kHz.

With the Mode pin tied high, the minimum allowed value is 20. The maximum value is 32,767.5. For ease of programming, binary representation is used. However, the binary value must be multiplied by 2. For example, if a divide ratio of 1000 is needed, the 1000 in decimal is converted to binary 0000 0011 1110 1000. This value is multiplied by 2 and becomes 0000 0111 1101 0000 and is loaded into the device for R′15 to R′0. See Figure 16.

With the Mode pin tied low, Table 21 shows the divide ratios available. There are two formulas for the divide ratio when Mode is low.

If R′1 R′0 are 00: R′ Ratio = (Value of R′15 to R′2) x 2.

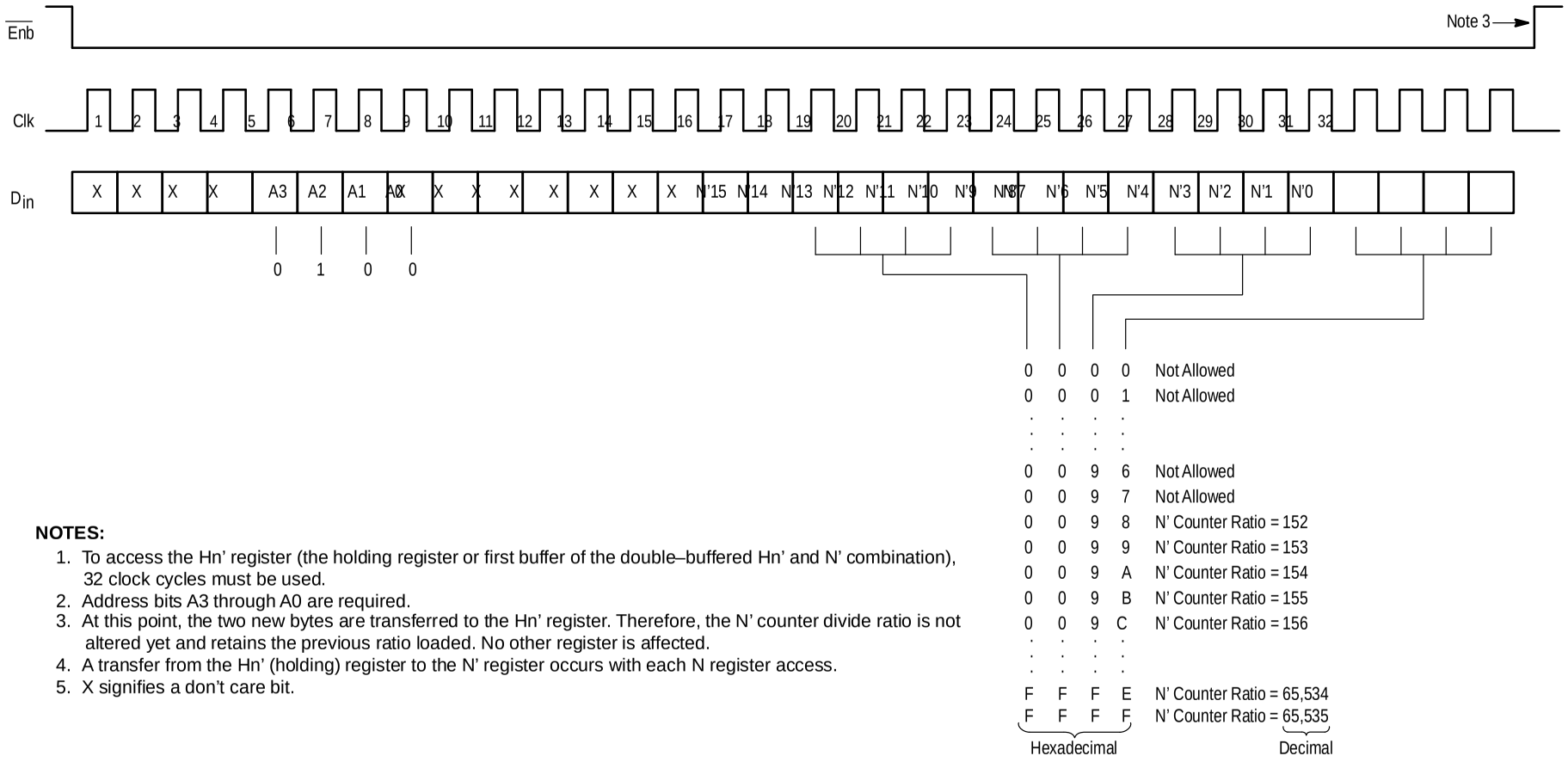
If R′1 R′0 are 01, 10, 11: R′ Ratio = (Value of R′15 to R′2) x 2.5.

Table 21. R′ Counter Divide Ratios with Mode Pin Tied Low*

| R′15 | R′14 | R′13 | R′12 | R′11 | R′10 | R′9 | R′8 | R′7 | R′6 | R′5 | R′4 | R′3 | R′2 | R′1 | R′0 | R′ Counter Divide Ratio |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Not Allowed |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Not Allowed |
| ⋮ | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | Not Allowed |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 20 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 25 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | X | 25 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 22 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 27.5 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | X | 27.5 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 24 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 30 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | X | 30 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 26 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 32.5 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | X | 32.5 |
| ⋮ | | | | | | | | | | | | | | | | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 32,766 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 40,957.5 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | X | 40,957.5 |

* Divide ratios with the Mode pin tied high are shown in Figure 16.

**Figure 17. Hn' Register Access and Format**




**NOTES:**

1. To access the Hn' register (the holding register or first buffer of the double–buffered Hn' and N' combination), 32 clock cycles must be used.
2. Address bits A3 through A0 are required.
3. At this point, the two new bytes are transferred to the Hn' register. Therefore, the N' counter divide ratio is not altered yet and retains the previous ratio loaded. No other register is affected.
4. A transfer from the Hn' (holding) register to the N' register occurs with each N register access.
5. X signifies a don't care bit.

## 6F. D REGISTER

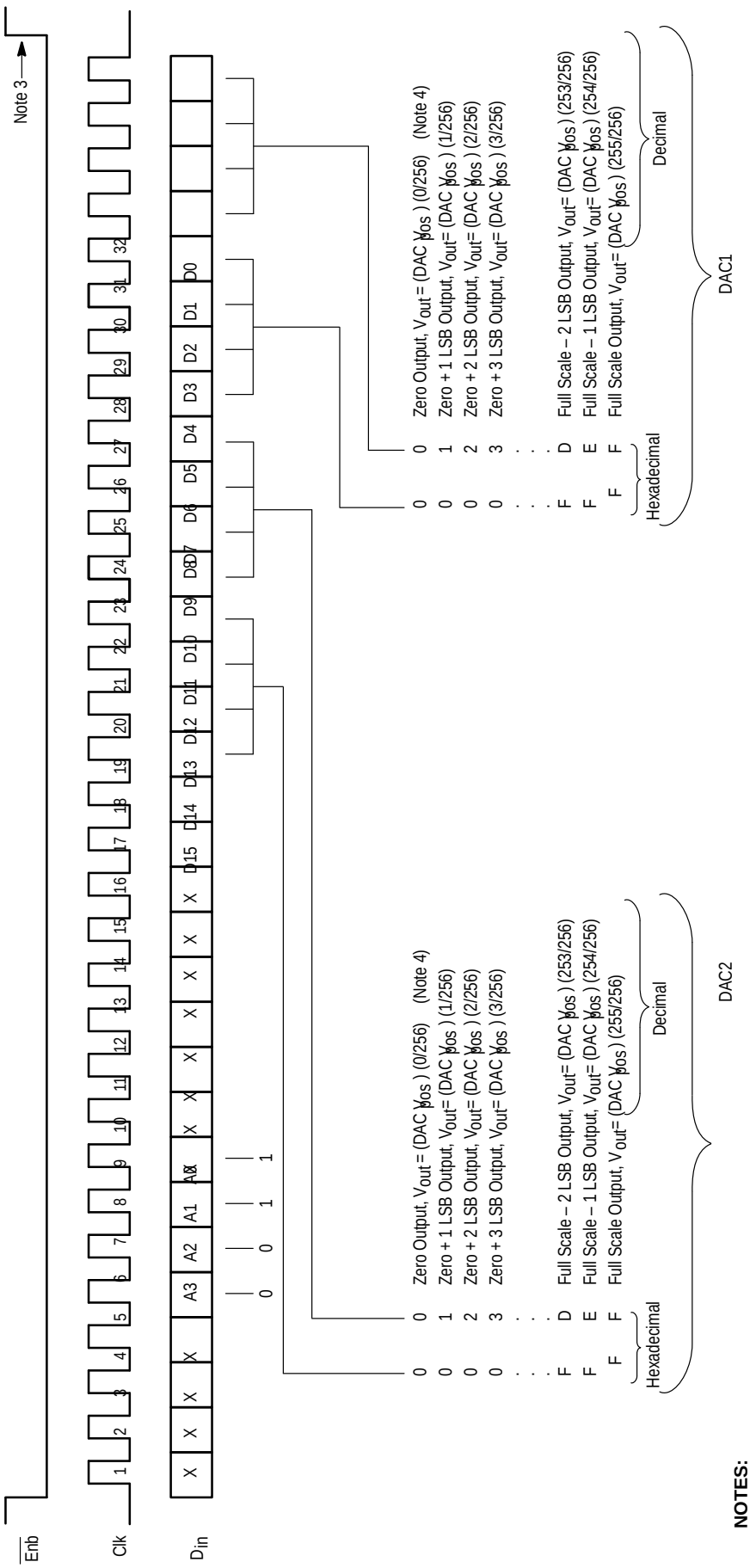
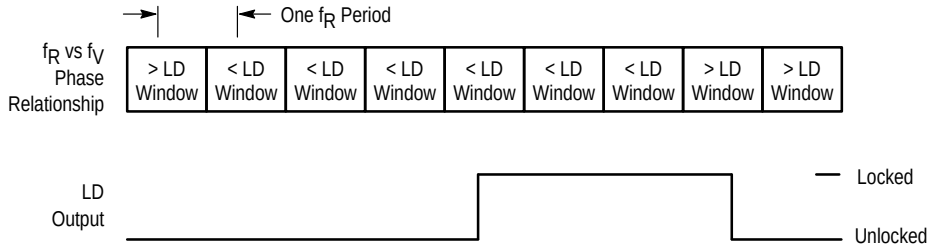



**Figure 18. D Register Access and Format**

**NOTES:**
1. To access the D Register, 32 clock cycles are used.
2. Address bits A3 through A0 are required.
3. At this point, the two new bytes are transferred to the D register. No other register is affected.
4. Low–power standby state.
5. X signifies a don't care bit.

**Figure 19. Lock Detector Operation**




**NOTES:**

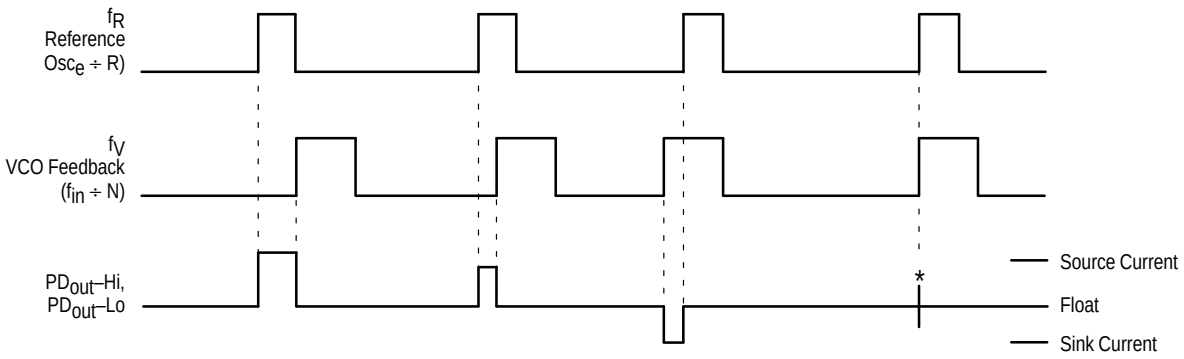
1. Illustration shown is for the main loop and applies when the secondary loop is either phase locked or in standby. The actual detector outputs for each loop are ANDed together at the LD pin.
2. The secondary loop is similar to the above illustration.
3. The approximate lock detect window for the main loop is either 64 or 256 $Osc_e$ cycles and is programmable via bit N22. The approximate window for the secondary loop is 64 $Osc_e$ cycles and is not programmable.
4. The LD output is low whenever the phase difference is more than the lock detect window.
5. The LD output is high whenever the phase difference is less than the lock detect window and continues to be less than the window for 3 $f_R$ periods or more.

## LOCK DETECTOR OUTPUT CONDITIONS

| $f_R$ versus $f_V$ Relation | Lock Detector Output | Microcontroller Action |
|---|---|---|
| Frequency is the same with phase inside the LD window | Static high level output | Senses high level and no edges, therefore loop is locked |
| Frequency is the same with phase outside the LD window | Static low level output | Senses low level, therefore loop is unlocked |
| Frequency is slightly different, thus phase is changing | Dynamic “chattering” output, output has transitions | Senses edges, therefore loop is unlocked |
| Frequency is grossly different | Static low level output | Senses low level, therefore loop is unlocked |

**NOTE:** For simplicity, this table applies to the main loop. The secondary loop is similar. The detector outputs feed an AND gate whose output is the LD pin.

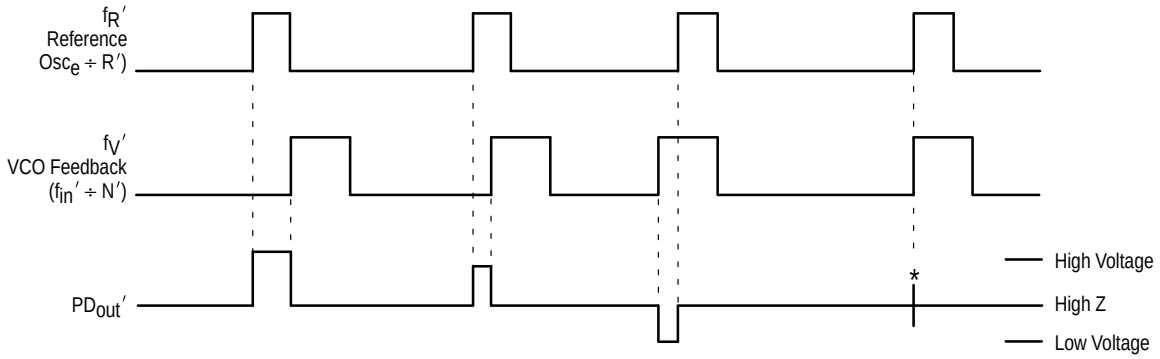
**Figure 20. $PD_{out}$–Hi and $PD_{out}$–Lo Detector Output Characteristics**




*At this point, when both $f_R$ and $f_V$ are in phase, the output source and sink circuits are turned on for a short interval.

**NOTES:**
1. The detector generates error pulses during out–of–lock conditions. When locked in phase and frequency, the output is high impedance and the voltage at that pin is determined by the low–pass filter capacitor.
2. Waveform shown applies when the $\overline{f_{out}}$/Pol pin is low and the Mode pin is high.
3. When the $\overline{f_{out}}$/Pol pin is high and Mode is high, the $PD_{out}$–Hi and $PD_{out}$–Lo waveform is inverted.
4. The waveform shown is also the default when the Mode pin is low.

**Figure 21. $PD_{out}'$ Detector Output Characteristics**




*At this point, when both $f_R'$ and $f_V'$ are in phase, the output source and sink circuits are turned on for a short interval.

**NOTES:**
1. The detector generates error pulses during out–of–lock conditions. When locked in phase and frequency, the output is high impedance and the voltage at that pin is determined by the low–pass filter capacitor.
2. Waveform shown applies when the $f_{out}$/Pol′ pin is low and the Mode pin is high.
3. When the $f_{out}$/Pol′ pin is high and Mode is high, the $PD_{out}'$ waveform is inverted.
4. The waveform shown is also the default when the Mode pin is low.

## 7. APPLICATIONS INFORMATION

### 7A. CRYSTAL OSCILLATOR CONSIDERATIONS

The oscillator/reference circuit may be connected to operate in either of two configurations. With the Mode pin placed “high” and bit C6 programmed to 1, the oscillator/reference circuit of the MC145181 will accept an external reference input. The external reference signal should be capacitive, connected to $Osc_e$ with $Osc_b$ left floating. Commercially available temperature compensated crystal oscillators (TCXOs) or crystal–controlled data clock oscillators provide a very stable reference frequency. For additional information about TCXOs and data clock oscillators, please consult the Electronic Engineers Master Catalog, internet web page, or similar publication/service.

The on–chip Colpitts reference oscillator can be selected by either tying the Mode pin low or by programming the C6 bit to zero when Mode is high. The oscillator may be operated in either the fundamental mode, as show by Figure 22, or as an overtone oscillator. The “kick start” feature ensures reduced “stalling” of hard–starting crystals.

#### Crystal Resonators

The equivalent circuit of a crystal resonator most commonly used is shown in Figure 23. The crystal itself is a specially cut (usually AT for overtone operation) block of quartz. The dimensions, (shape, thickness, length, and width) determine the operating characteristics of the crystal. When deformed and allowed to return naturally to its resting shape, it is observed to oscillate. This oscillation has the typical characteristics of a damped oscillation and an equivalent electrical signal can be found on the surface of the crystal. In addition, if an equivalent electrical signal is applied to the crystal, it will be observed to oscillate. The equivalent values for $R_S$, $L_S$, $C_S$, and $C_O$ can be used to predict the operation of the crystal when used as an electronic oscillator.

Due to the series/parallel arrangement of the equivalent components, the crystal exhibits two resonances. The first, sometimes just called resonance, is the series resonance of the $R_S$, $C_S$, $L_S$ branch. The other, sometimes called the anti–resonance, is the parallel resonance including $C_O$. For the series resonance the formula is

$$f_S = \frac{1}{2\pi\sqrt{L_S C_S}} .$$

For parallel resonance, the formula is

$$f_p = \frac{1}{2\pi\sqrt{\frac{L_S C_S C_O}{C_O + C_S}}} .$$

As can be seen from this equation, the anti–resonant frequency is higher than the series resonant frequency. The ratio between the resonant and anti–resonant frequency can be found using the formula

$$\frac{\Delta f}{f} = \frac{C_S}{2\,(C_O + C_S)}$$

where

$$\Delta f = |f_S - f_p|$$

and

$$f = \frac{f_S + f_p}{2} .$$

By exploiting this characteristic, the crystal oscillator frequency can be tuned slightly. If a capacitor is connected in series with the crystal operating in the resonance mode, the frequency will shift upward. If a capacitance is added in parallel with a crystal operating in an anti–resonant mode, the frequency will be shifted down.

**Figure 22. Fundamental Mode Oscillator Circuit**

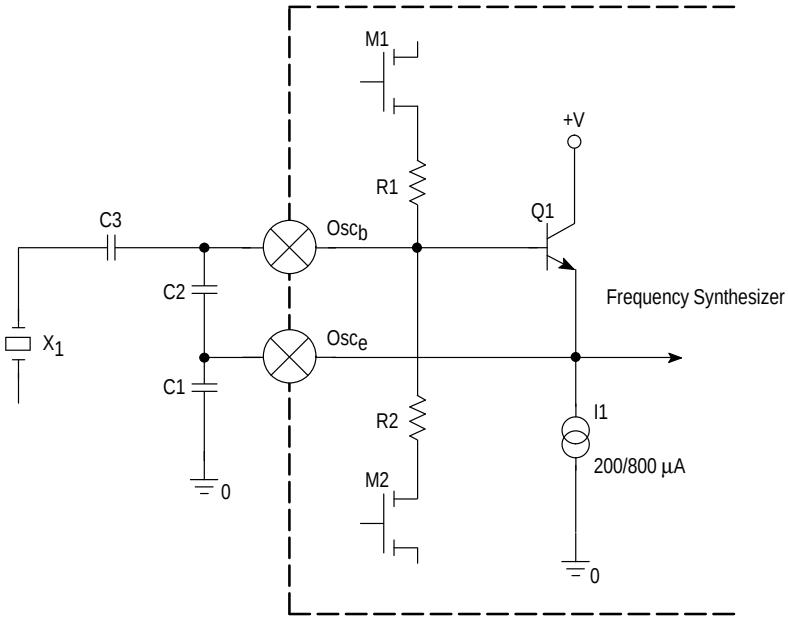
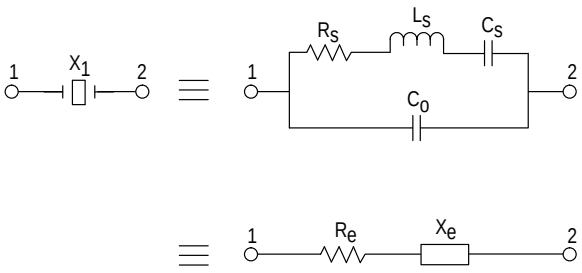
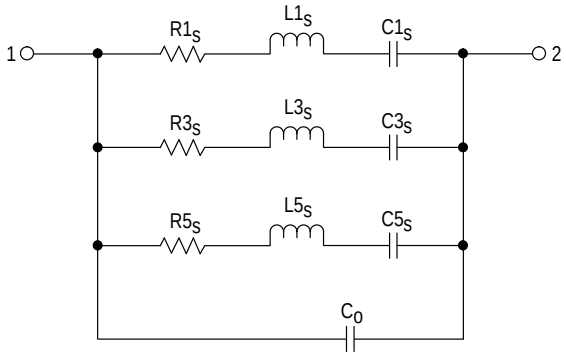


**Figure 23. Crystal Resonator Equivalent Circuit**




NOTE: Values are supplied by crystal manufacturer (parallel resonant crystal).

**Figure 24. Overtone Crystal Equivalent Circuit**




Because of the acoustic properties of the crystal resonator, the crystal "tank" responds to energy not only at its fundamental frequency, but also at specific multiples of the fundamental frequency. In the same manner that a shorted or open transmission line responds to multiples of the fundamental frequency, the crystal "tank" responds similarly. A shorted half–wave transmission line (or closed acoustic chamber) will not only resonate at its fundamental frequency, but also at odd multiples of the fundamental. These are called the overtones of the crystal and represent frequencies at which the crystal can be made to oscillate. The equivalent circuit of an overtone crystal is shown is Figure 24.

The components for the appropriate overtone are represented by 1, 3, and 5. The fundamental components are represented by 1, and those of importance for the third and fifth overtones, by 3 and 5.

### Fundamental Mode

The equivalent circuit for the Colpitts oscillator operating in the fundamental mode is shown in Figure 25.

C3 is selected to provide a small reduction in the inductive property of the crystal. In this manner, the frequency of the oscillator can be "pulled" slightly. The biasing combination of M1R1 and M2R2 provide the ability to start operation with a higher than normal operating current to stimulate crystal activity. This "kick start" current is nominally four times the normal current. An internal counter times the application of the "kick start" and returns the current to normal after the time out period.

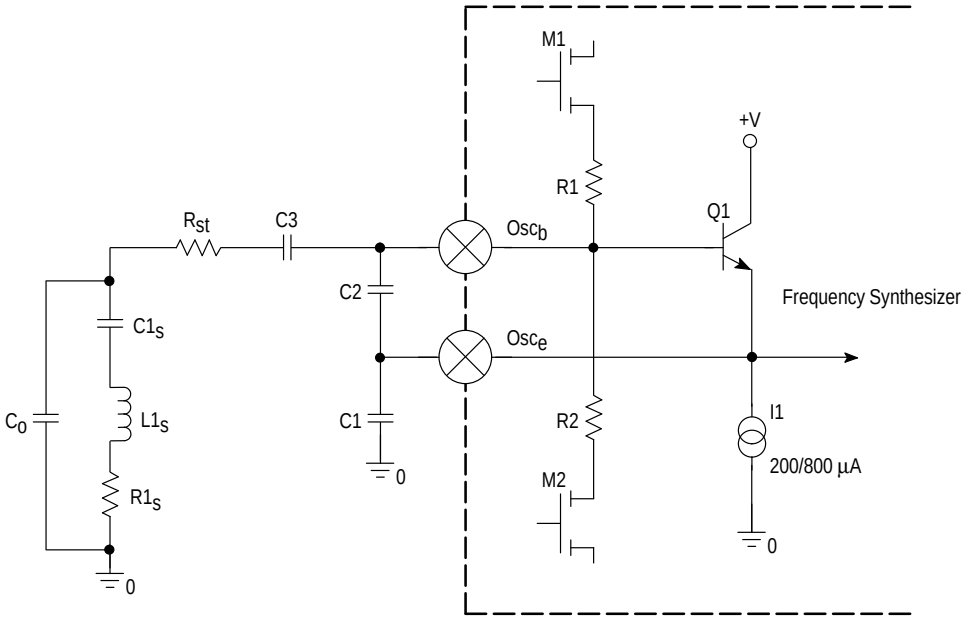
The mutual conductance (transconductance) of the transistor Q1 is useful in determining the conditions necessary for oscillation. The nominal value for the transconductance is found from the formula

$$gm = \frac{I_e}{26}$$

where Ie is the emitter current in mA.

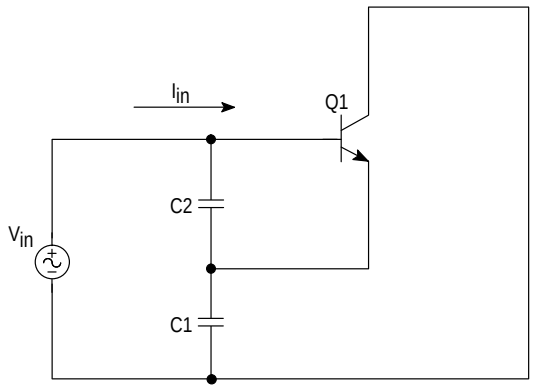
The operation of the oscillator can be described using the concept of "negative resistance". In a normal tuned circuit, any excitation tends to be dissipated by the resistance of the circuit and oscillation dies out. The resistive part of the crystal along with the resistance of the wiring and the internal resistance of C1, C2, and C3, make up this "damping" resistance. Some form of energy must be fed back into the circuit to sustain oscillation. This is the purpose of the amplifier.

**Figure 25. Fundamental Mode Colpitts Oscillator Equivalent Circuit**



If we define the damping as resistive, we can define the opposite or regenerative property as negative resistance. Figure 26 shows the basic circuit of the Colpitts oscillator. C3 has been combined with the crystal elements for simplicity. For the circuit to oscillate, there must be at least as much “negative resistance” (regeneration) as there is resistance (damping). We can define this by deriving the input impedance for the amplifier.

**Figure 26. Colpitts Oscillator Basic Circuit**




If a driving signal is defined as $V_{in}$, the resultant current that flows can be identified as $I_{in}$. The relationship of $V_{in}$ to $I_{in}$ is

$$V_{in} = I_{in}\,(Z_{c1} + Z_{c2}) - I_b\,(Z_{c2} - \beta Z_{c1})$$

and

$$0 = I_{in}\,(Z_{c2}) + I_b\,(Z_{c2} + r_b)$$

where $I_b$ is the base current of transistor Q1. Solving the two equations and assuming $Z_{c2} << r_b$, the input impedance can be expressed as

$$Z_{in} \sim \frac{-gm}{\omega^2\,C1\,C2} + \frac{1}{j\omega\left(\frac{C1\,C2}{C1 + C2}\right)}$$

where $\omega = 2\pi f$. This is equivalent to the series combination of a real part whose value is

$$REAL = \frac{-gm}{\omega^2\,C1\,C2}$$

and the imaginary part whose value is

$$IMAG = \frac{1}{j\omega\left(\frac{C1\,C2}{C1 + C2}\right)}$$

To sustain oscillation, the amplifier must generate a “negative resistance” equal or greater than the REAL part of the above equation and opposite in polarity.

$$R_{neg} = \frac{-gm}{\omega^2\,C1\,C2}$$

As long as the relation

$$-R_{neg} = -SUM\,(R_S + R_{st} + R_{c1} + R_{c2} + R_{c3}) \ ,$$

the circuit will oscillate and the frequency of oscillation will be defined as

$$f_o = \frac{1}{2\pi\sqrt{L_S\,(C1||C2||C3)}}$$

where C3 is the series frequency adjusting capacitor.

In determining values for C1, C2, and C3, two limits are considered. At one end is the relationship of C3 to C2 and C1. If C3 is made 0 or the reactance of C3 is small compared to the reactance of C1 and C2, no adjustment of the crystal frequency is possible. The other limit is the relationship

$$gm\,Z_{c1}\,Z_{c2} > R_{sum}$$

where $R_{sum}$ is the sum of resistances in the resonant loop. Since this equation must be true for the circuit to oscillate, it is obvious that as the values of C1 and C2 are increased, the series resistances must be reduced and/or gm increased. Since gm is a function of device current and there is a physical limit on how small $R_{sum}$ can be made, at some point oscillation can no longer be sustained.

Normally, it is desirable to choose the “negative resistance” to be several times greater than the “damping” resistance to ensure stable operation. A factor of four or five is a good “rule of thumb” choice.

To determine crystal power, the equivalent circuit shown in Figure 27 can be used. In this case, we are addressing a condition where the transistor amplifier is operating at the limit of class A; that is, the device is just at cutoff during the peak negative excursions. At this point,

$$R_e = gm\,X_{c1}\,X_{c2}$$

if the amplitude is constant and the oscillator is stable. For this to occur, the sum of all resistances in the resonant loop will be equal to $R_e$, where $R_e$ represents the effective resistance of I1. This can be written as

$$R_{sum} = R_S + R_{st} = R_e$$

where $R_S$ is the crystal resistance and $R_{st}$ is the additional distributed resistances within the resonant loop. At the point where the transistor enters cutoff we have the equation

$$-I_{in} = \frac{v1 + v2}{X_{ls} + R_e} = \frac{(I_{in} - I_b)\,Z_{c2} + (I_{in} + \beta i_b)\,Z_{c1}}{X_{ls} + R_e} \ .$$

$\beta$ = current gain of the transistor. Rewriting:

$$I_{in} = \frac{I_b\,(Z_{c2} - \beta Z_{c1})}{Z_{c1} + Z_{c2} + X_{ls} + R_e} \ .$$

For oscillation to occur, we must have

$$Z_{c1} + Z_{c2} + X_{ls} \sim 0 \ .$$

If we assume $\beta Z_{c1}$ is normally much greater than $Z_{c2}$ then

$$I_{in} \sim \frac{-I_e\,Z_{c1}}{R_e} \ .$$

For the condition we have specified,

$$I_e(bias) + I_e(instantaneous\ ac) = 0$$

the transistor is just cutting off and the peak current, $I_{in}$ is equal to the bias current. The peak input current is represented as

$$I_{in}(peak) = \frac{I_e|Z_{c1}|}{R_e} \ .$$

The power dissipation of the series resistances in the resonant loop can be written as

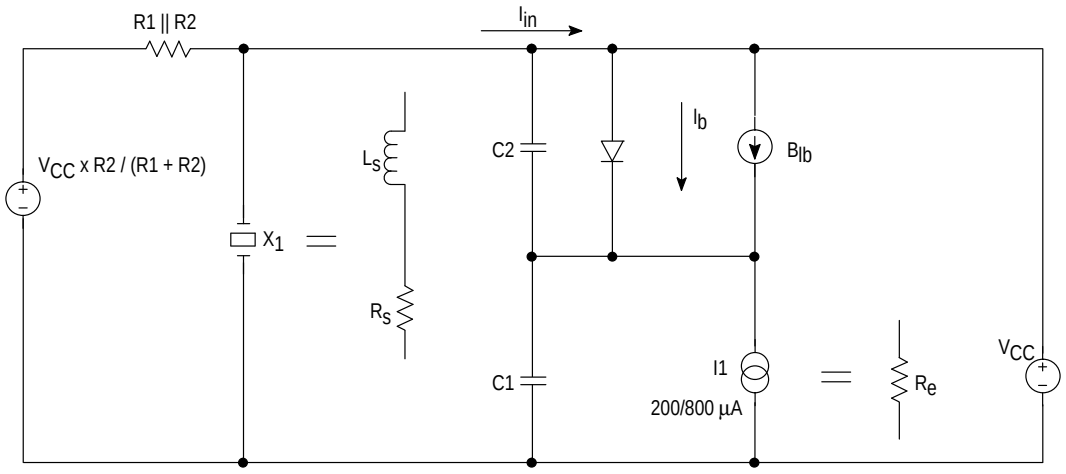
$$P = \frac{I_{in}(peak)^2\,R}{2} = \frac{(I_e|Z_{c1}|)^2}{2\,R_{sum}}$$

where $R_{sum} = R_e$.

The power dissipation for the crystal itself becomes

$$P_{crystal} = \frac{(I_e|Z_{c1}|)^2}{2\,R_S} \ .$$

Figure 27. Equivalent Circuit for Crystal Power Estimation




**Overtone Operation**

For overtone operation, the circuit is modified by the addition of an inductor, L1; and a series capacitor, C4. C4 is inserted as a dc blocking capacitor whose capacitance is chosen sufficiently large so that its reactance can be ignored. This circuit is shown in Figure 28.

For oscillation to occur at the overtone frequency, the condition

$$gm\ Z_{c1}\ Z_{c2} > R_S$$

must exist.

$Z_{c1}$ represents the impedance across C1 and can be defined as

$$Z_{c1} = jX_{c1} \,||\, (R_{l1} + jX_{l1})$$

where $R_{l1}$ is the dc resistance of the inductor L1.

For overtone operation, this must occur at the desired harmonic. For example, if the crystal is chosen to oscillate at the third overtone, C1 and C2 must be chosen so that the above condition exists for $Z_{c1}$ and $Z_{c2}$ at the third harmonic of the fundamental frequency for the crystal. In addition, care must be taken that the “negative resistance” of the amplifier is not sufficient at the fundamental frequency to induce oscillation at the fundamental frequency. It may be necessary to add additional filtering to reduce the gain of the amplifier at the fundamental frequency. The key to achieving stable overtone oscillator operation is ensuring the existence of the above condition at the desired overtone while ensuring its failure at all other frequencies.

L1 and C1 are chosen so that

$$\frac{1}{2\pi\sqrt{L_1\,C_1}} > F_f$$

where $F_f$ is the fundamental frequency of the crystal resonator. If L1 and C1 are chosen to be net capacitive at the desired overtone frequency and if the condition

$$gm\ Z_{c1}\ Z_{c2} > R_S$$

is true only at the desired overtone frequency, the oscillator will oscillate at the frequency of the overtone. Normally, L1 and C1 are not chosen to be resonant at the overtone frequency but at a lower frequency to ensure that the parallel combination of L1 and C1 is capacitive at the overtone frequency and inductive at the fundamental frequency.

$$F_f < \frac{1}{2\pi\sqrt{L_1\,C_1}} < F_o$$

The net inductance of the rest of the resonant loop then balances this capacitance at the overtone frequency.

$$\frac{1}{\frac{1}{X_{ls} - X_{cs}} - \frac{1}{X_{c0}}} + X_{l2} + X_{l(stray)} - X_{c3}$$

$$+ \frac{1}{\frac{1}{X_{l1}} - \frac{1}{X_{c1}}} = 0$$

L2 and C3 are chosen to provide the desired adjustment to the resonant overtone frequency. This is normally computed by calculating the expected ppm change at the resonant frequency and using this to define the value of the reactance necessary to produce this change.

$$\Delta F_f\ (ppm) = \frac{X\ (of\ L2\ and\ C3)}{Z\ (crystal\ at\ resonance)}$$

$$\Delta F_f\ (ppm) = X(of\ L2\ and\ C3)/Z(crystal\ at\ resonance)$$

The values needed for this calculation can be derived from the value of the fundamental frequency and $C_o$. If $C_o$ is known or can be measured, $C_s$ is defined as

$$C_s = \frac{C_o}{200}$$

for an AT cut crystal.

The fundamental frequency can be used to calculate the value for $L_s$ using either the series resonant or parallel resonant formulas given earlier. Since the Q of the crystal,

$$Q = \frac{X}{R}$$

is usually sufficiently large at the resonant frequency so that

$$R_S << Z(crystal)$$

$R_S$ can be ignored. The value for C3 and L2 are chosen so that

$$X_{C3} = X_{I2}$$

when C3 is adjusted to approximately half its maximum capacitance. At this setting, the combination produces a zero change in the overtone frequency. If C3 is then chosen so that $X_{C3}$ at minimum capacitance is

$$[X_{C3}(max)] - X_{I2} >= \Delta F_f \text{ (ppm) } Z(crystal)$$

and L2 is approximately

$$X_{I2} = \frac{X_{C3}(max)}{2}$$

then

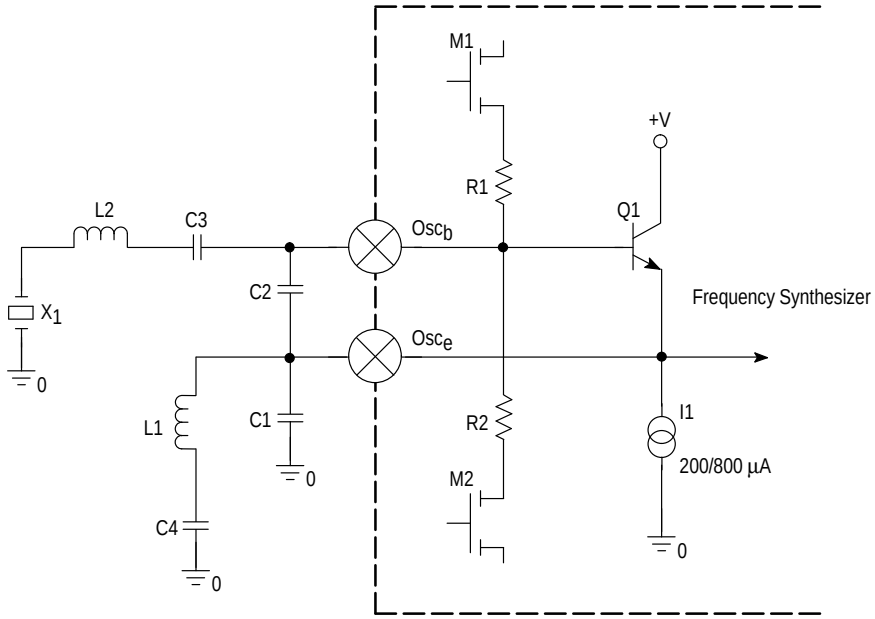
$$X_{C3}(max) >= 2[\Delta F_f \text{ (ppm)}] Z(crystal)$$

and

$$X_C(min) = \frac{X_C(max)}{4}$$

This results in an adjustable change in the operating frequency of $+[\Delta F_f \text{ (ppm)}]$ and $-[\Delta F_f \text{ (ppm)}]/2$. If ratios nearer to 1:1 are used for $X_{C3}(max)$ and $X_{I2}$, the tuning range will be skewed with a wider $-[\Delta F_f \text{ (ppm)}]$ but at the expense of less adjustability over the $+[\Delta F_f \text{ (ppm)}]$ range.

**Figure 28. Colpitts Oscillator Configured for Overtone Operation**



### 7B. MAIN LOOP FILTER DESIGN — CONVENTIONAL

The current output of the charge pump allows the loop filter to be realized without the need of any active components. The preferred topology for the filter is illustrated in Figure 29.

The $R_o/C_o$ components realize the primary loop filter. $C_a$ is added to the loop filter to provide for reference sideband suppression. If additional suppression is needed, the $R_x/C_x$ realizes an additional filter. In most applications, this will not be necessary. If all components are used, this results in a fourth order PLL, which makes analysis difficult. To simplify this, the loop design will be treated as a second order loop ($R_o/C_o$), and additional guidelines are provided to minimize the influence of the other components. If more rigorous analysis is needed, mathematical/system simulation tools should be used.

| Component | Guideline |
|---|---|
| $C_a$ | <0.1 x $C_o$ |
| $R_x$ | >10 x $R_o$ |
| $C_x$ | <0.1 x $C_o$ |

The focus of the design effort is to determine what the loop's natural frequency, $\omega_o$, should be. This is determined by $R_o$, $C_o$, $K_p$, $K_v$, and $N_t$. Because $K_p$, $K_v$, and $N_t$ are given, it is only necessary to calculate values for $R_o$ and $C_o$. There are three considerations in selecting the loop bandwidth:

1. Maximum loop bandwidth for minimum tuning speed.
2. Optimum loop bandwidth for best phase noise performance.
3. Minimum loop bandwidth for greatest reference sideband suppression.

Usually a compromise is struck between these three cases, however, for a fixed frequency application, minimizing the tuning speed is not a critical parameter.

To specify the loop bandwidth for optimal phase noise performance, an understanding of the sources of phase noise in the system and the effect of the loop filter on them is required. There are three major sources of phase noise in the phase–locked loop — the crystal reference, the VCO, and the loop contribution. The loop filter acts as a low–pass filter to the crystal reference and the loop contribution. The loop filter acts as a high–pass filter to the VCO with an in–band gain equal to unity. The loop contribution includes the PLL IC, as well as noise in the system; supply noise, switching noise, etc. For this example, a loop contribution of 15 dB has been selected.

The crystal reference and the VCO are characterized as high–order 1/f noise sources. Graphical analysis is used to determine the optimum loop bandwidth. It is necessary to have noise plots from the manufacturers of both devices. This method provides a straightforward approximation suitable for quickly estimating the optimal bandwidth. The loop contribution is characterized as white–noise or low–order 1/f noise, given in the form of a noise factor which combines all the noise effects into a single value. The phase noise of the crystal reference is increased by the noise factor of the PLL IC and related circuitry. It is further increased by the total divide–by–N ratio of the loop. This is illustrated in Figure 30. The point at which the VCO phase noise crosses the amplified phase noise of the crystal reference is the point of the optimum loop bandwidth. In the example of Figure 30, the optimum bandwidth is approximately 15 kHz.

To simplify analysis further, a damping factor of 1 will be selected. The normalized closed loop response is illustrated in Figure 31 where the loop bandwidth is 2.5 times the loop natural frequency (the loop natural frequency is the frequency at which the loop would oscillate if it were unstable). Therefore, the optimum loop bandwidth is 15 kHz/2.5 or 6.0 kHz (37.7 krads) with a damping coefficient, $\zeta \sim 1$. T(s) is the transfer function of the loop filter.

where

$N_t$ = Total PLL Divide Ratio — 8 x N
where (N = 25 ... 40),
$K_v$ = VCO Gain – 2π Hz/V,
$K_p$ = Phase Detector/Charge Pump Gain – A
= ( $|I_{OH}|$ + $|I_{OL}|$ ) / 4π.

Technically, $K_v$ and $K_p$ should be expressed in radian units [$K_v$ (rad/V), $K_p$ (A/rad)]. Since the component design equation contains the $K_v$ x $K_p$ term, the 2π cancels and the value can be expressed as AHz/V (amp hertz per volt).

**Figure 29. Loop Filter**

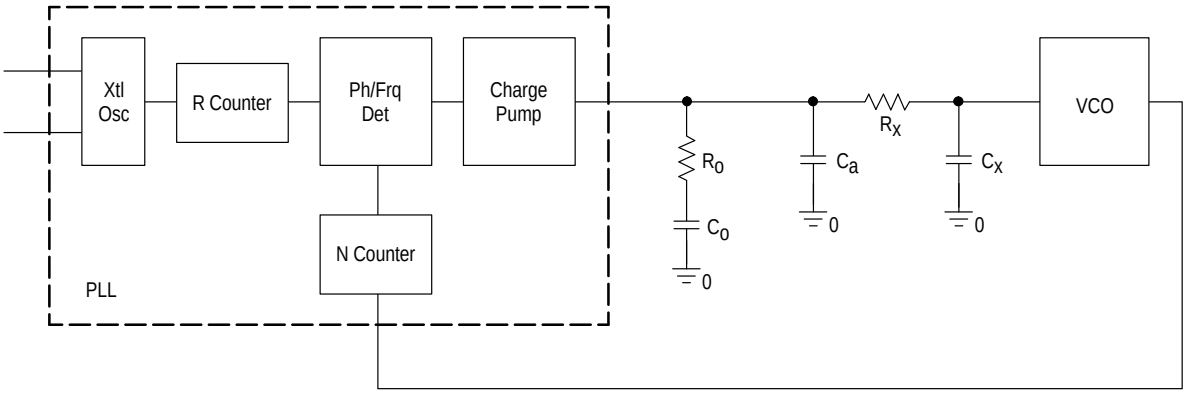


**Figure 30. Graphical Analysis of Optimum Bandwidth**

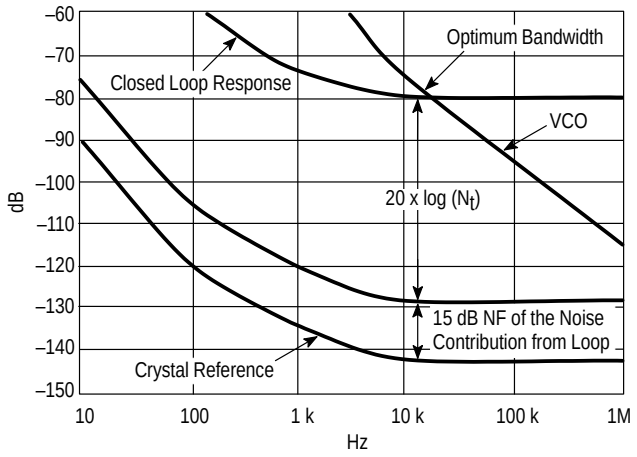
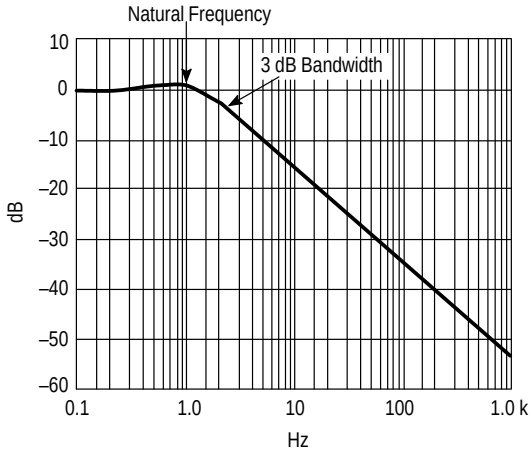



**Figure 31. Closed Loop Frequency Response for ζ = 1**




In summary, follow the steps given below:

Step 1: Plot the phase noise of crystal reference and the VCO on the same graph.

Step 2: Increase the phase noise of the crystal reference by the noise contribution of the loop.

Step 3: Convert the divide–by–N to dB (20log 8 x N) and increase the phase noise of the crystal reference by that amount.

Step 4: The point at which the VCO phase noise crosses the amplified phase noise of the crystal reference is the point of the optimum loop bandwidth. This is approximately 15 kHz in Figure 30.

Step 5: Correlate this loop bandwidth to the loop natural frequency per Figure 31. In this case the 3.0 dB bandwidth for a damping coefficient of 1 is 2.5 times the loop's natural frequency. The relationship between the 3.0 dB loop bandwidth and the loop's "natural" frequency will vary for different values of ζ. Making use of the equations defined in Figure 32, a math tool or spread sheet is useful to select the values for $R_O$ and $C_O$.

### Appendix: Derivation of Loop Filter Transfer Function

The purpose of the loop filter is to convert the current from the phase detector to a tuning voltage for the VCO. The total transfer function is derived in two steps.

Step 1 is to find the voltage generated by the impedance of the loop filter.

Step 2 is to find the transfer function from the input of the loop filter to its output. The "voltage" times the "transfer function" is the overall transfer function of the loop filter. To use these equations in determining the overall transfer function of a PLL, multiply the filter's impedance by the gain constant of the phase detector, then multiply that by the filter's transfer function. Figure 33 contains the transfer function equations for the second, third, and fourth order PLL filters.

### PSpice Simulation

The use of PSpice or similar circuit simulation programs can significantly reduce laboratory time when refining a PLL design. The following describes the use of behavioral modeling to develop useful models for studying loop filter performance. In many applications the levels of sideband spurs can also be studied.

Behavioral modeling is chosen, as opposed to discrete device modeling, to improve performance and reduce simulation time. PLL devices can contain several thousand individual transistors. To simulate at this level can result in generation of an enormous amount of data when compared to a simpler behavioral model. For example, a logic NAND gate can contain several transistors. Each of these requires a data set for each of the transistor terminals. If a half dozen transistors are used in the gate design, both current and voltage measurements for each terminal of each device for every node in the circuit is calculated. The gate can be expressed as a behavioral model, which is treated and simulated as a single device. Since PSpice sees this as a single rather than multiple devices, the amount of accumulated data is much less, resulting in a faster simulation.

For applications using integrated circuits such as PLLs, it is desirable to investigate the performance of the circuitry added externally to the integrated circuit. By using behavioral modeling rather than discrete device modeling to represent the integrated circuit, the engineer is able to study the performance of the design without the overhead contributed by simulating the integrated circuit.

### Phase Frequency Detector Model

The model for the phase frequency detector is derived using the waveforms shown in Figure 20. Two signals are present at the input of the phase frequency detector. These are the reference input and the feedback from the VCO and/or prescaler. The two signals are compared to determine the lag/lead relationship between the two signals and pulses generated to represent the leading edge of each signal. A pulse whose width equals the lead of one input signal over the other is generated by an RS flip–flop (RSFF). One RSFF generates a pulse whose width equals the lead of the reference signal over the feedback signal, and a second RSFF generates a signal whose width is the lead of the feedback signal over the reference signal. The logical model for the phase frequency detector is shown in Figure 34.

**Figure 32. Design Equations for the Second Order System**

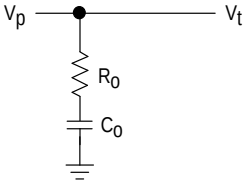
$$T(s) = \frac{R_0C_0s + 1}{\left(\frac{NC_0}{K_pK_v}\right)s^2 + R_0C_0s + 1} = \frac{\left(\frac{2\zeta}{\omega_0}\right)s + 1}{\left(\frac{1}{\omega_0^2}\right)s^2 + \left(\frac{2\zeta}{\omega_0}\right)s + 1}$$

$$\left(\frac{NC_0}{K_pK_v}\right) = \left(\frac{1}{\omega_0^2}\right) \rightarrow \omega_0 = \sqrt{\frac{K_pK_v}{NC_0}} \rightarrow \boxed{C_0 = \left(\frac{K_pK_v}{N\omega_0^2}\right)}$$

$$R_0C_0 = \left(\frac{2\zeta}{\omega_0}\right) \rightarrow \zeta = \left(\frac{\omega_0R_0C_0}{2}\right) \rightarrow \boxed{R_0 = \left(\frac{2\zeta}{\omega_0C_0}\right)}$$

**Figure 33. Overall Transfer Function of the PLL**

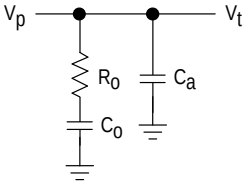
For the Second Order PLL:




$$Z_{LF}(s) = \frac{R_0C_0s + 1}{C_0s}$$

$$T_{LF}(s) = \frac{V_t(s)}{V_p(s)} = 1 \quad , \quad V_p(s) = K_p(s)Z_{LF}(s)$$

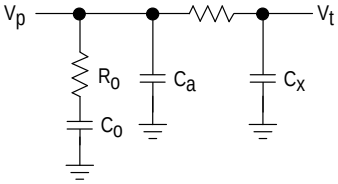
For the Third Order PLL:




$$Z_{LF}(s) = \frac{R_0C_0s + 1}{C_0R_0C_as^2 + (C_0 + C_a)s}$$

$$T_{LF}(s) = \frac{V_t(s)}{V_p(s)} = 1 \quad , \quad V_p(s) = K_p(s)Z_{LF}(s)$$

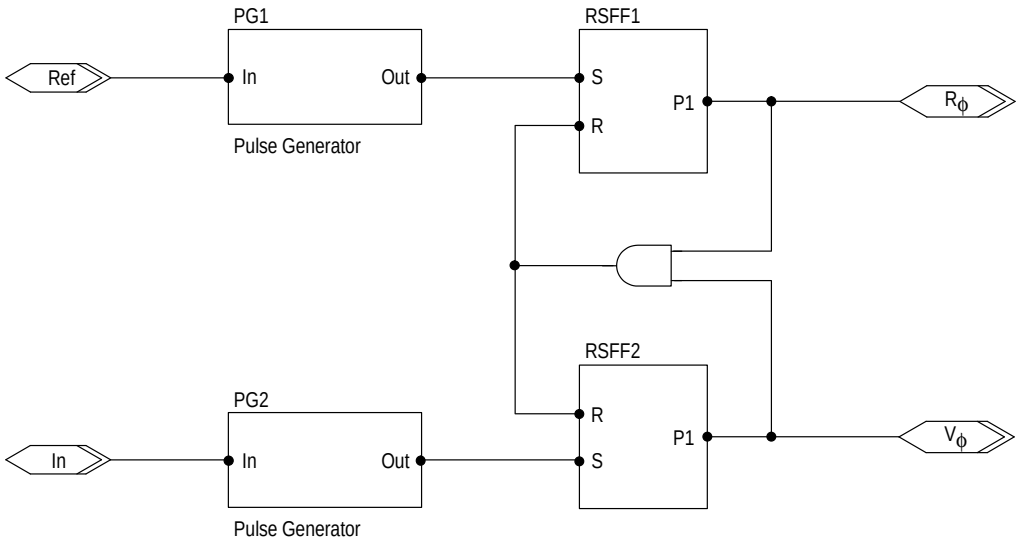
For the Fourth Order PLL:




$$Z_{LF}(s) = \frac{(R_0C_0s + 1)(R_xC_xs + 1)}{C_0R_0C_aR_xC_xs^3 + [(C_0 + C_a)R_xC_x + C_0R_0(C_x + C_a)]s^2 + (C_0 + C_a + C_x)s}$$

$$T_{LF}(s) = \frac{V_t(s)}{V_p(s)} = \frac{1}{(R_xC_xs + 1)} \quad , \quad V_p(s) = K_p(s)Z_{LF}(s)$$

**Figure 34. Phase Frequency Detector Logic Diagram**




The behavioral model of the phase frequency detector shown in Figure 35 is derived using the phase frequency detector logic diagram. Behavioral models for the pulse generator, AND gate (Figure 36), and RS flip–flops (Figure 37) are created using analog behavioral blocks. The pulse generator is created using a delay block and a “gate” defined by the behavioral expression:

If [V(v1) ≥ 1 & V(v2) , 1, 5, 0]

v1 and v2 represent the two inputs to the block.

This is the behavioral expression for an AND gate with one input inverted. The addition of the delay element produces a pulse whose width equals the delay element.

The pulses appearing at the output of HB1 and HB2 (Figure 35) are used to set the flip–flops, RSFF1, and RSFF2. The leading pulse will set the appropriate flip–flop resulting in a high at the output of that flip–flop. The output of this flip–flop will remain high until the arrival of the second (or lagging) pulse sets the second RS flip–flop. The presence of a high on both RS flip–flop outputs results in the generation of the reset pulse. The reset pulse is generated by the analog behavioral block (configured as an AND gate) and the delay element. The delay element is necessary to eliminate the zero delay paradox of input to output to input.

The output of the phase frequency detector is two pulse trains appearing at $R_\phi$ and $V_\phi$. When the PLL is locked, the pulses in both pulse trains will be of minimum width. When the phase frequency detector is out of lock, one pulse train will consist of pulses of minimum width while the width of the pulses in the second train will be equal to the lead/lag relationship of the input signals. If the Ref input leads ‘In’, the pulse train at $R_\phi$ will consist of pulses whose width equals the lead of Ref. If Ref lags ‘In’, the width of the pulses appearing at $V_\phi$ will equal this lag.

The terms lead and lag used in this explanation represent an occurrence in time rather than a phase relationship. At any condition other than locked, one input (either In or Ref), will be of a higher frequency. This results in the arrival of the pulse at that input ahead of the pulse at the other input, or leading. The second then is lagging.

To simulate the operation of the phase frequency detector in an actual circuit, a charge pump needs to be added. The behavioral model for this is shown in Figure 38. Two voltage–to–current behavioral models are used to produce the charge pump output. Two voltage–controlled switches with additional behavioral models, monitor the voltage of the output of the charge pump and clamp to 0 or $V_{CC}$ to simulate a real circuit.

To ensure the model conforms to the PLL, the delay blocks in the phase frequency detector should be set to the expected value as specified by the MC145181 data sheet. In addition, the charge pump sink and source current behavioral model should also be set to deliver the desired current and $V_{CC}$ specified to ensure correct clamping.

### Modeling the VCO

The VCO (Figure 39) is also modeled using Analog Behavioral Modeling (ABM). The model used in the following examples assumes a linear response; however, the control voltage equation can be modified as desired. The circuit is modeled as a sine generator controlled by the control voltage. The sine generator can be modeled using the EVALUE function or the ABM function. In Figure 39, the EVALUE function is used to generate the divided output and the ABM function is used for the undivided output. Either the GVALUE or the ABM/I function can be used for the control voltage.

Figure 35. Behavioral Model of the Phase Frequency Detector

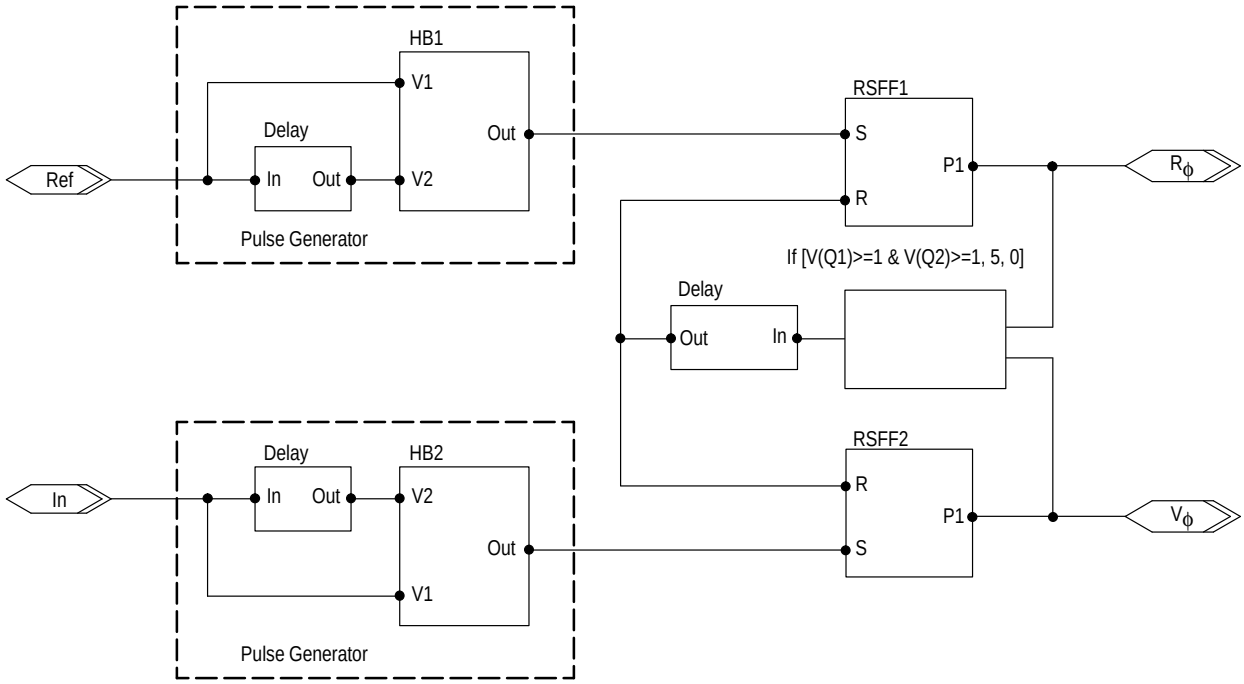



Figure 36. Behavioral Block Used for the Pulse Generator

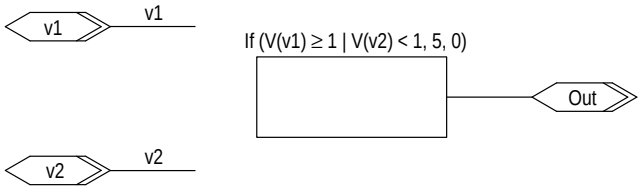



Figure 37. Behavioral Block Used as an RS Flip–flop

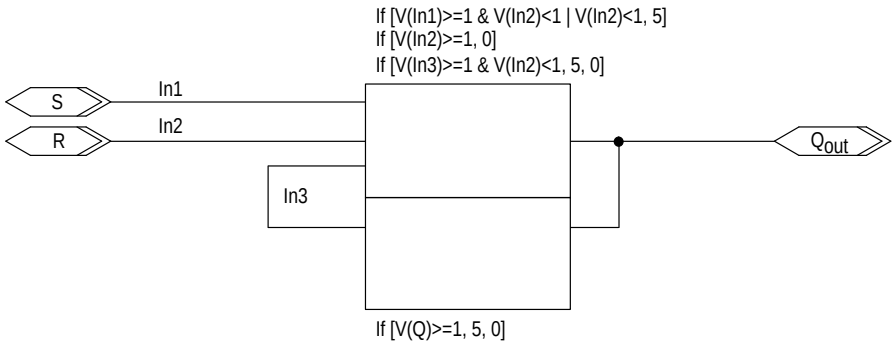


**Figure 38. Charge Pump Model**

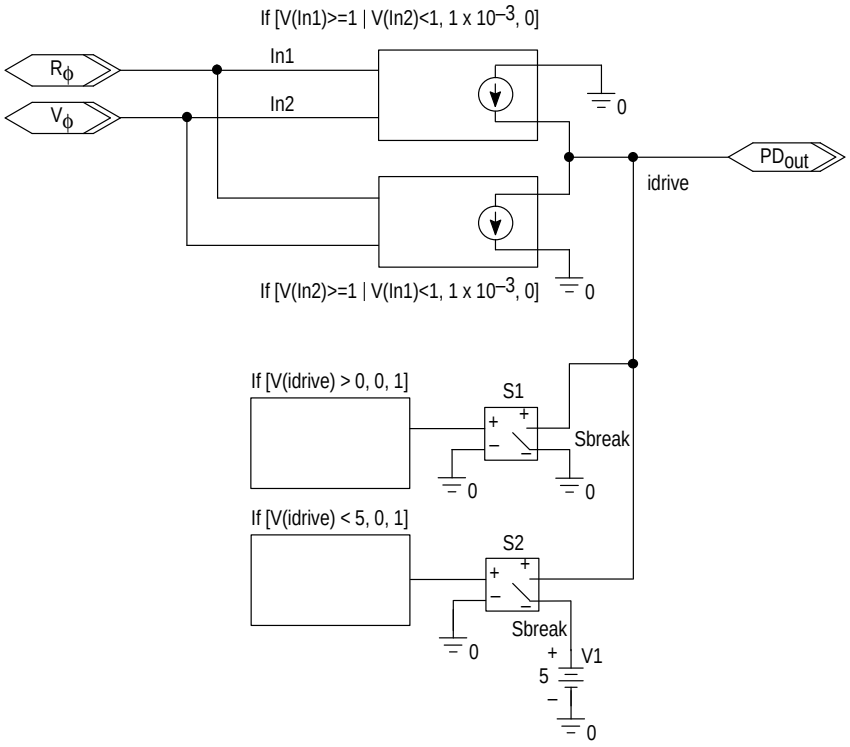
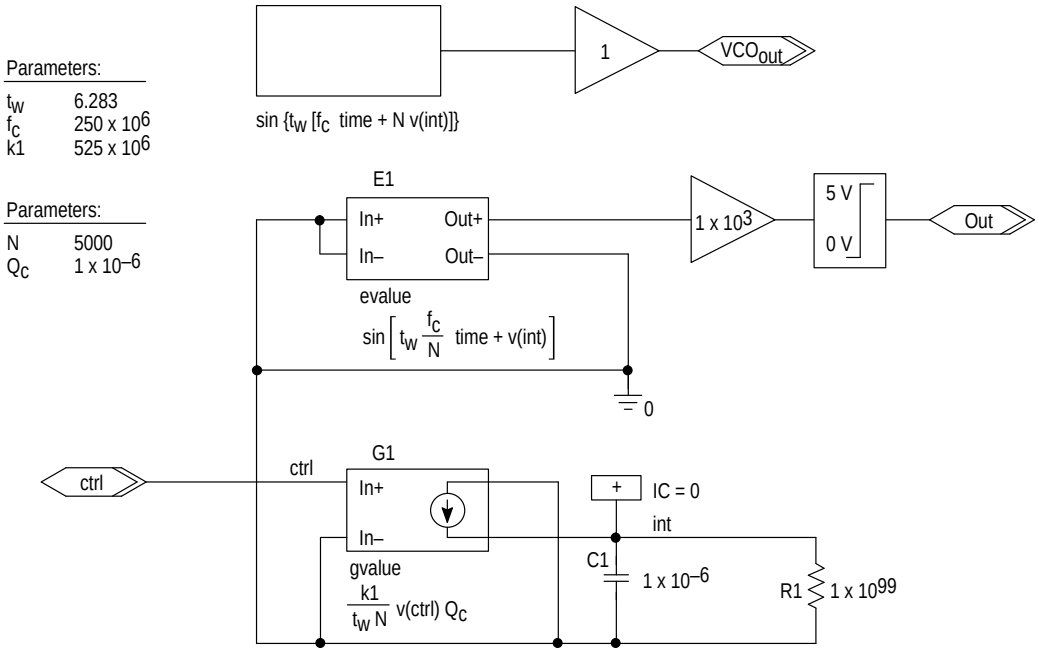



**Figure 39. VCO Behavioral Model**



The equation for the sine generator is:

$$e = \sin\left[t_W \frac{f_C}{N} \text{ time} + v(\text{int})\right] \quad .$$

$f_C$ is defined as the output frequency when the control voltage is 0. This is the expected VCO frequency before frequency division. For the purpose of simulation, the counter value, N, has been written into the equation to ensure the correlation between the modeled circuit and the mathematical loop filter calculations. $t_W$ is $2\pi$; additional decimal places can be added as needed. v(int) is the control voltage effect and is defined in these examples as:

$$v(\text{int}) = \frac{k1}{t_W N} v(\text{cntl}) \; 1 \times 10^{-6} \quad .$$

where k1 is the VCO gain in rad/V.

The value C1 in the schematic of the VCO can be arbitrarily changed; however, the value must match that of $Q_C$. $Q_C$ determines the value of the current to be integrated by the capacitor C1. R1 is arbitrarily set to $1 \times 10^{99}$ and is not an active part of the circuit; however, it must be included to prevent open pin errors from the PSpice software. The GVALUE function is used to perform the generation of v(int). There is some interaction between the integrator, (GVALUE output and C1) and R1. V(int) is a continuous ramp that is loaded by the resistance of R1. Unless the GVALUE output current is sufficiently large for the value chosen for R1, the VCO control voltage required to maintain lock will increase throughout the simulation producing nonlinear operation. Modifications to the circuit can be performed either by changing the values in the parameter list or for major changes to the VCO characteristics, the equations for the sine generator, or control voltage can be altered.

The output of the sine generator is amplified by 1000 to produce a sharp rise/fall time and the output limited to swing between the values of 0 V and 5 V to convert it to a digital output. The resultant circuit/symbol accepts a voltage input from the loop filter and produces a square wave output at the desired frequency. This frequency should be chosen to represent the frequency present at the output of the N counter of the PLL frequency synthesizer.

The second output represented by the ABM function is a sine wave output of the frequency expected from the actual VCO. The primary purpose of this output is to allow full frequency simulation for spectrum analysis. By running a transient analysis of sufficient time, it is possible to determine spur content and level. If sufficient resolution is used in the simulation, the PSpice probe FFT transform can be used to provide the typical spectrum analyzer display.

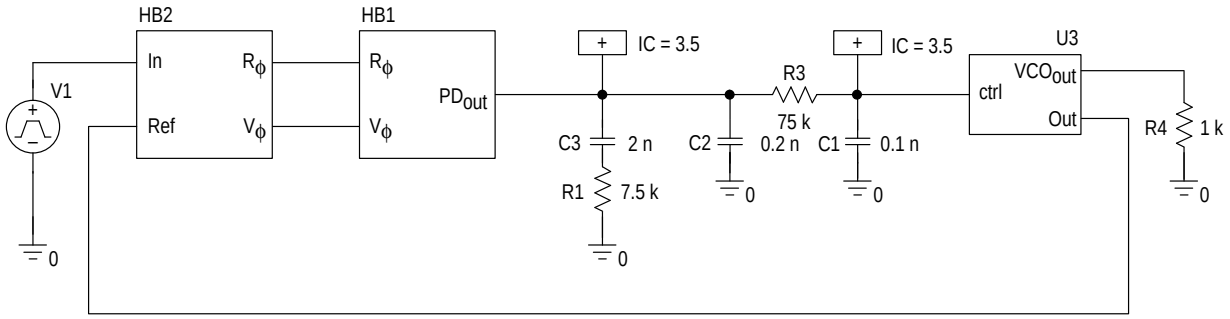
### Loop Filter Simulation

The circuit shown in Figure 40 is used to simulate the closed loop operation for a single charge pump output. Component values for the loop filter should be computed using information from the previous section. Initial conditions can be set using the “IC1” symbol with starting values specifying the initial condition.

By adjusting component values for the loop filter, performance of the closed loop operation can be monitored. The control voltage to the input of the VCO can be monitored for a variety of conditions including settling time, lock time, and ripple present at the VCO input. In addition, the output of the VCO can be monitored for spur sidebands caused by ripple on the loop filter output; however, expected operation at high frequencies may be difficult due to the excessive data that can be generated.

As the divider ratio, N, increases for a fixed step frequency, the number of data points required to obtain sufficient information to overcome aliasing problems may become excessively large. In addition, the number of samples required should be three or more per cycle. For VCO frequencies in the range of 500 MHz, this means the step ceiling needs to be in the range of 100 to 500 ps. If a simulation time of 1 ms is needed, the actual computer time can be several hours with data accumulation in the 1– to 2–Gbyte range.

**Figure 40. PLL Closed Loop Model**



## 7C. MAIN LOOP FILTER DESIGN — ADAPT

### Introduction

For PSpice simulation, the schematic model shown in Figure 41 was chosen. The classical PLL model employing a phase–frequency detector, a VCO, and an adaptive loop filter is used to simplify visualization of circuit operation. The parameter tables allow for modification of circuit performance by providing an easy method for altering critical values without necessitating changes to sub–level schematics. The definition for the terms are:

$t_W$ = 2π,
$f_r$ = reference frequency,
$t_d$ = time delay; allows delay of the start of the high current mode (used to perform reference spur measurements),
CPL = charge pump low current,
CPH = charge pump high current,
N = N counter value,
$S_Z$ = amount the N counter is being increased (or decreased) by,
$S_t$ = number of $f_r$ cycles that CPH is active; this value is either 16, 32, 64, or 128,
VCPHH = charge pump voltage – high,
VCPHL = charge pump voltage – low,
K1 = VCO gain (Hz/volt),
$f_C$ = VCO frequency at 0 V control voltage,
H = reference spur scaling factor.

### Modeling the Phase–frequency Detector

Figure 42 is a schematic of the phase–frequency detector. It includes the reference oscillator model, phase–frequency detector model, and charge pump models. V1 is the control element used to generate the step time for switching between CPL and CPH. The signal source VPULSE, is used to simulate the timer that controls when CPL and CPH are turned on. PW calculates the pulse width that simulates the counter from the values for $S_t$ and $f_r$ that are entered in the parameter tables on the top level schematic.

**Figure 41. Top Level PLL Model**

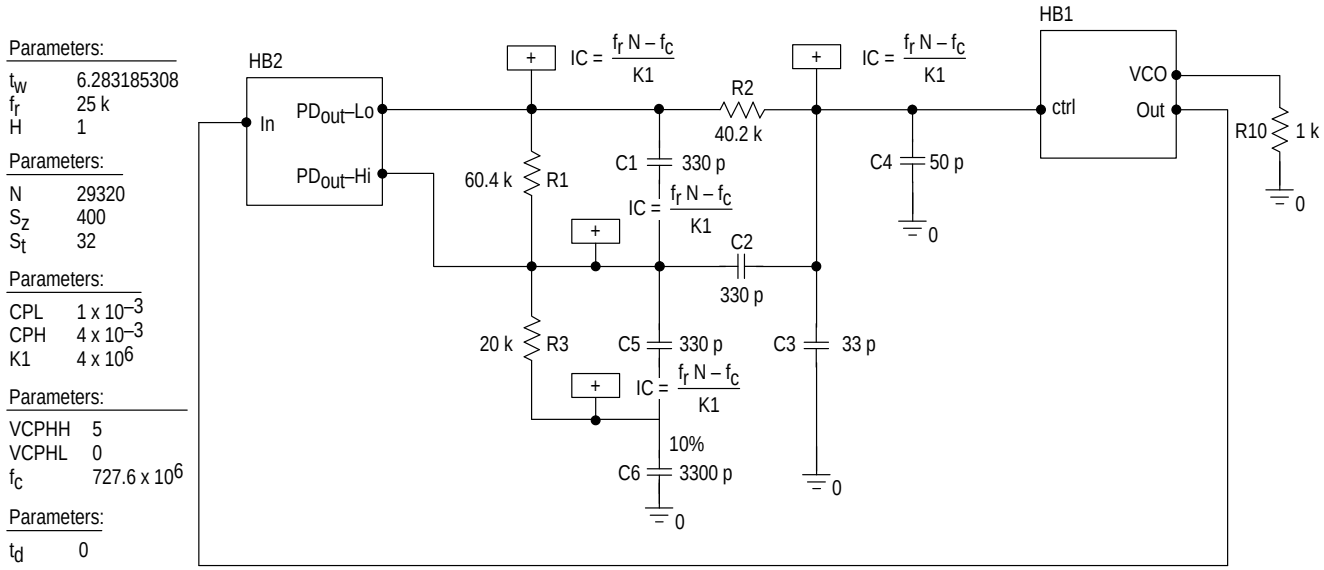
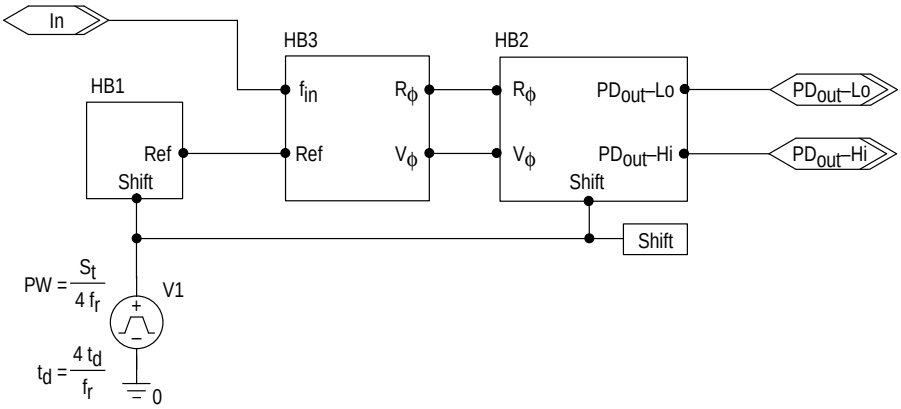


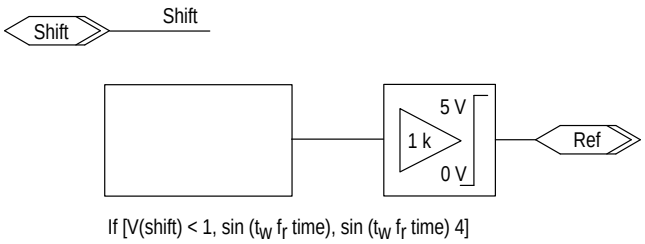

**Figure 42. Phase–frequency Detector with Dual Charge Pumps**



### Reference Oscillator

The reference oscillator is shown in Figure 43. The oscillator is modeled using an analog behavioral block. The function for the block is written as an “If” condition. If the signal shift is low, the reference frequency $f_r$ will be generated if shift is high, a signal of four times $f_r$ will be generated. The limiter/gain block converts the low level sine wave output of the analog behavioral block into a square wave. The values of 0 for the low value and 5 for the high value are used throughout. These values are chosen out of habit and are not critical in an analog behavioral environment, providing the conformity is universal throughout the design.

**Figure 43. Reference Oscillator**




### Phase–frequency Detector

The actual phase–frequency detector model minus reference oscillator and charge pumps is shown in Figure 44. The detector is composed of three delay modules: a behavioral AND gate, and two RS flip–flops. The STP function resets the phase/frequency detector logic on initiation of the simulator. The circuit for the behavioral RS flip–flop is shown in Figure 45.

The RS flip–flop equation illustrates the benefit of using the behavioral block instead of using a primitive logic element. A delay block and the behavioral gate equation generate a pulse whose width is equal to the value of the delay block. To generate the output using a primitive logic element such as a NAND gate, an inverter would be necessary to invert one of the NAND inputs. This approach requires three elements to be used instead of the two of the behavioral approach just for the pulse generator. In the behavioral approach, the equation for the behavioral AND gate is folded into the RS flip–flop, eliminating a separate gate altogether. Constructing the model with classic logic elements would require two NOR gates for the flip–flop, a delay element, an inverter, and an AND gate; five elements as compared with three for the behavioral approach. Since the RS flip–flop is used in two places in the model, four less components are needed for simulation. Since the speed of the simulation is directly impacted by the number of components being simulated, any reduction in the total number of components is a savings in simulation time and computer memory.

The RS flip–flops generate the lead or lag outputs that are used to “steer” the VCO. The pulse generator equation produces narrow pulses coincident with the leading edge of each of the input signals. These pulses set the appropriate RS flip–flop. Once set, the leading flip–flop must wait until the lagging flip–flop is also set. The behavioral AND gate provides the necessary output pulse to reset the flip–flops. The delay element placed at the output of the behavioral AND gate prevents an undefined state for the detector. The value 5 ns is chosen to correspond with the data sheet. The logic functions as a three state phase/frequency detector with an operating range of $\pm 2\pi$. $R_\phi$ and $V_\phi$ deliver positive pulses, whose width represents the amount of the lead of each input over the other input.

**Figure 44. Phase–frequency Detector Logic**

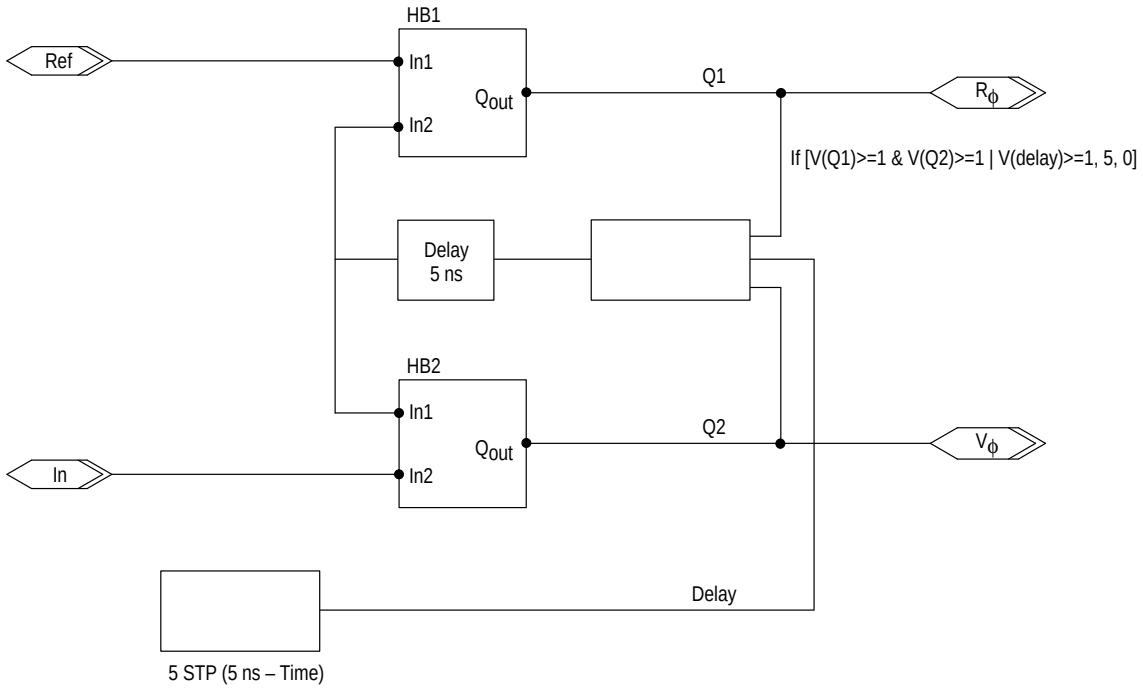
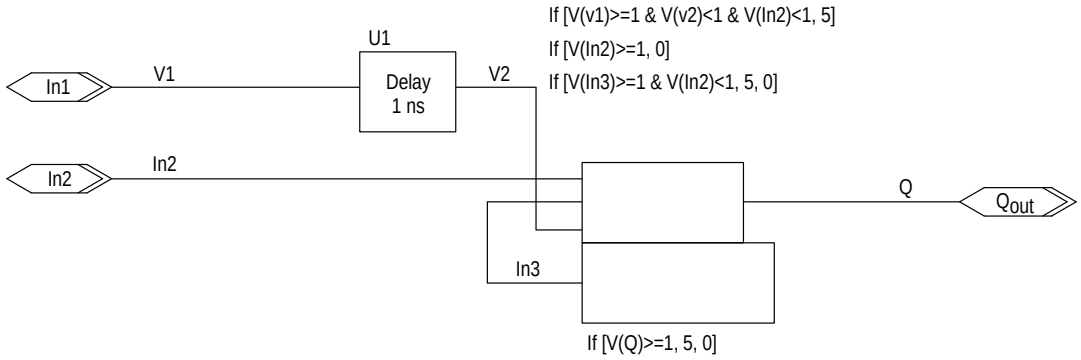


Figure 45. Behavioral RS Flip–flop






### Charge Pump Model

The schematic used for the charge pump in the phase–frequency detector model is shown in Figure 46. Each charge pump is made from two analog behavioral blocks. The blocks chosen are three input behavioral blocks with current outputs. The two blocks are connected in push–pull to generate the appropriate source and sink output. The output of each block is defined using an “If” statement to monitor the input signals and generate the correct output at the appropriate time.

One note about this type of design. SPICE does not limit the output voltage swing necessary to generate the programmed current. It is possible to implement values for the loop filter, which will cause the charge pump to exceed the rail voltage. To limit the output voltage to prevent exceeding the value of the rails, the two behavioral blocks, voltage–controlled switches S1 and S2, and constants VCPHH and VCPHL are added. S1 and S2 on/off resistance is set to 1 Ω and 1 x $10^{12}$ Ω, and the off/on voltage is set to 0 V and 1 V to correspond to the behavioral blocks. The values defined by the constants are accessible from the parameter tables on the top level schematic.

### VCO Model

The model used for simulating the VCO is shown in Figure 47. The VCO is composed of a sine wave generator and a control element. An analog behavioral block is used as a sine wave generator and a GVALUE element is used as a control element. The GVALUE is operated as an integrator. The output of the integrator is defined as

$$v(int) = k1\ v(ctrl)\ Q_C \quad .$$

The block designated to provide the feedback to the phase–frequency detector uses a single input analog behavioral block. The signal shift generated by V1 in the phase–frequency detector block is used to define the output frequency of the behavioral block. In this manner, the switching of the N and R values for the programmable counters can be simulated. In the implementation shown, the two frequencies will be either 25 kHz or 100 kHz when locked to the reference oscillator.

The other behavioral block is used to generate a VCO output dependent on the loop, but not contributing to the operation of the loop. This is used to emulate the actual VCO output with one modification. “H” has been added to the equation generating the sine wave. If H is defined as 1, the sine wave generated will be the same as the expected VCO output. If H is chosen as some value greater than 1, the frequency of the output will be reduced accordingly. This is useful when running simulations designed to show reference spur levels.

In cases where it is desirable to view reference spur levels, simulation can become difficult or impossible. For example, consider the circuit that is being discussed. This circuit represents the evaluation kit (MC145230EVK) using a VCO tunable between 733 MHz to 742 MHz, with a step frequency of 25 kHz.

**NOTE**

This example is for reference only. The maximum operating frequency of the MC145181 is 550 MHz. Operation of the VCO at frequencies greater than 550 MHz requires the inclusion of additional external division such as a prescaler.

To obtain useful information from the simulation, a sampling rate greater than the Nyquist limit must be used (three to five samples per cycle). This dictates a step size less than 1/2 nanosecond. Additionally, the reference frequency is only 25 kHz. To accurately represent the conditions for spur generation, the simulation time must be long enough to include a sufficient number of $f_r$ periods. Otherwise, no spurs are generated. In addition, the data file system is limited to 2 Gbyte, either in the NT 4.0 operating system or in PSpice itself. If the file exceeds 2 Gbyte, the data is discarded. To simulate reference spur generation at 730 MHz, a 1 ms simulation time was chosen. The simulation ran for several hours and generated a data file just under 2 Gbyte. The result is shown in Figure 48. The plot obtained from the EVK is shown in Figure 49 for comparison.

Figure 46. CPL and CPH Charge Pumps

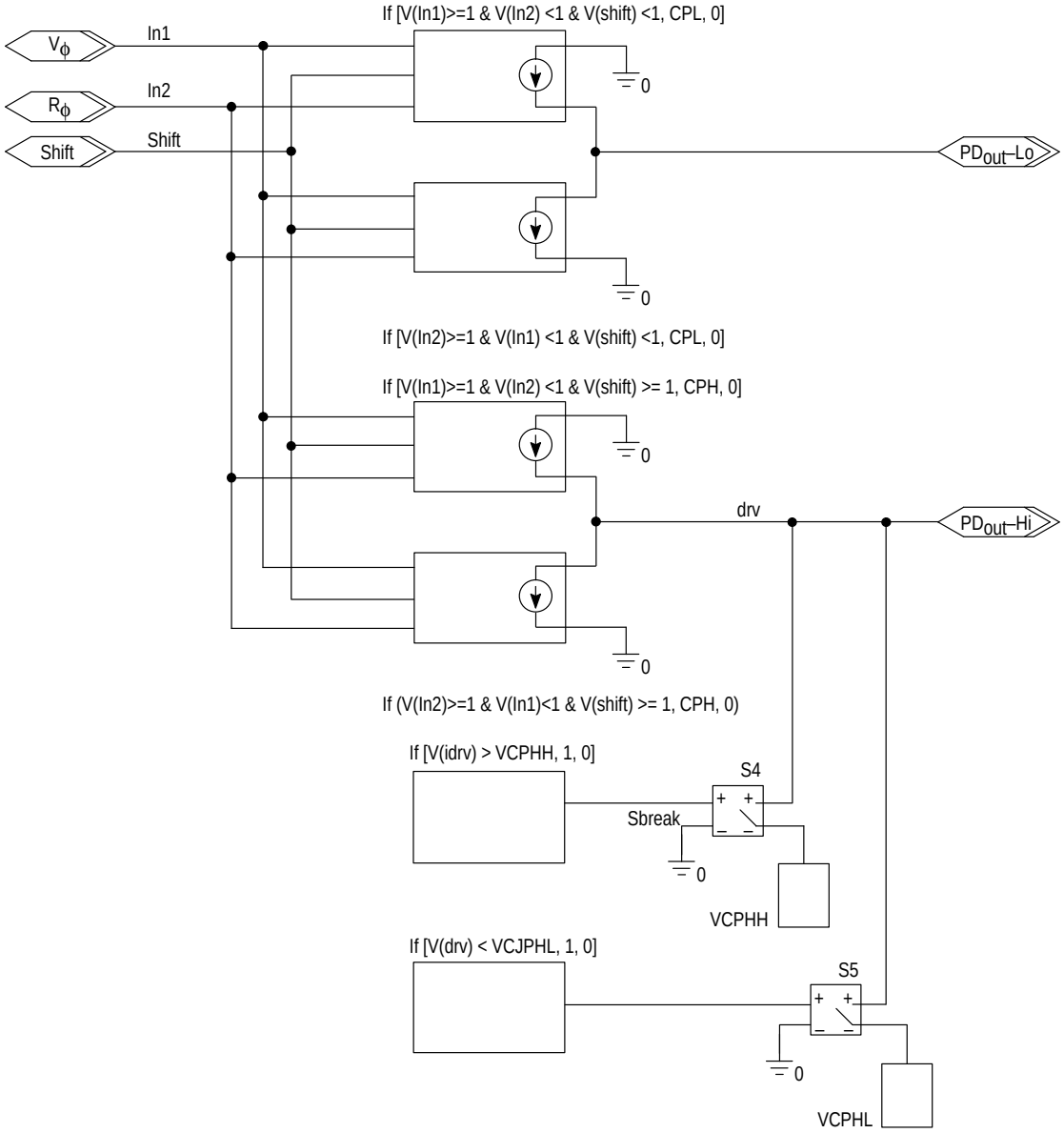


**Figure 47. VCO Model**

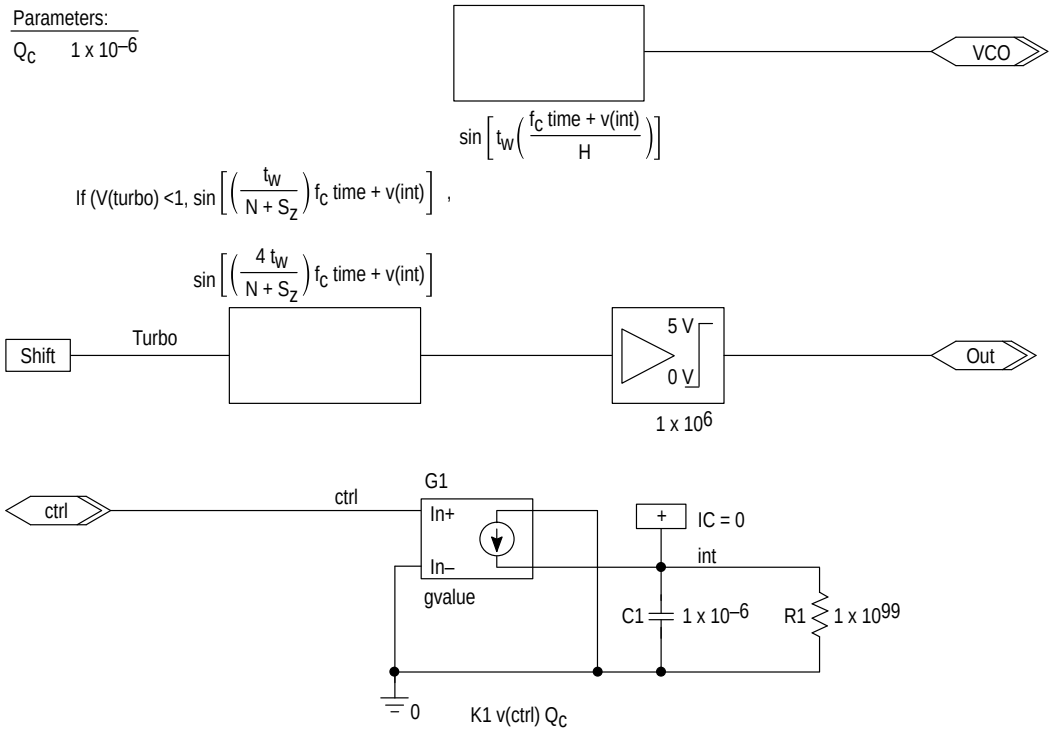



**Figure 48. Reference Spur Simulation at 730 MHz**

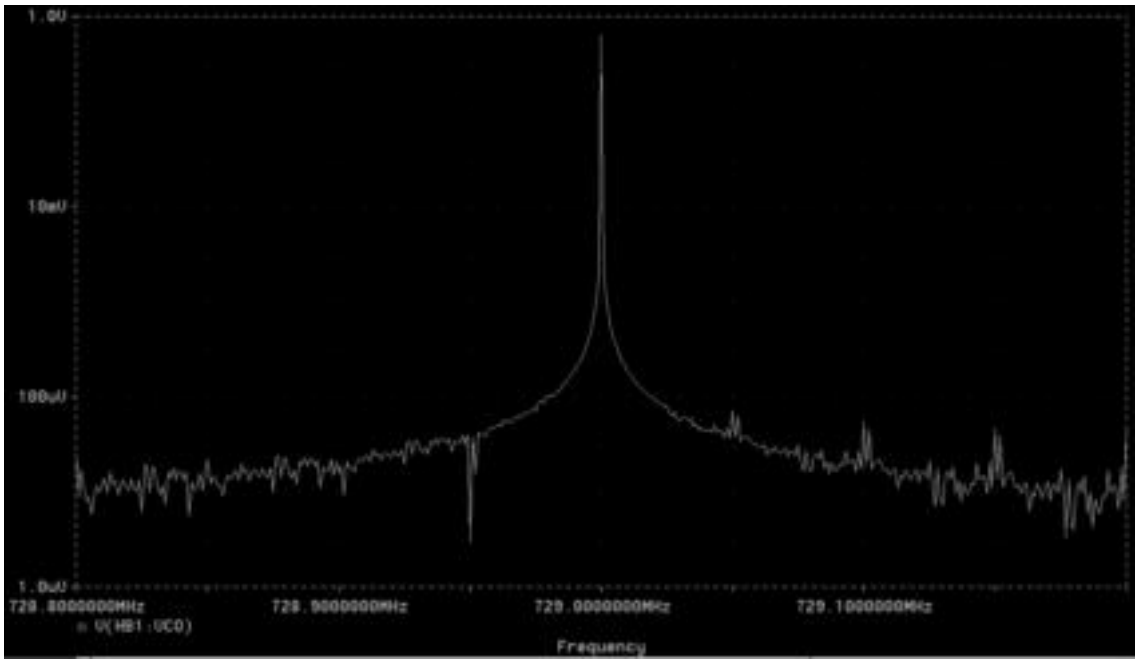
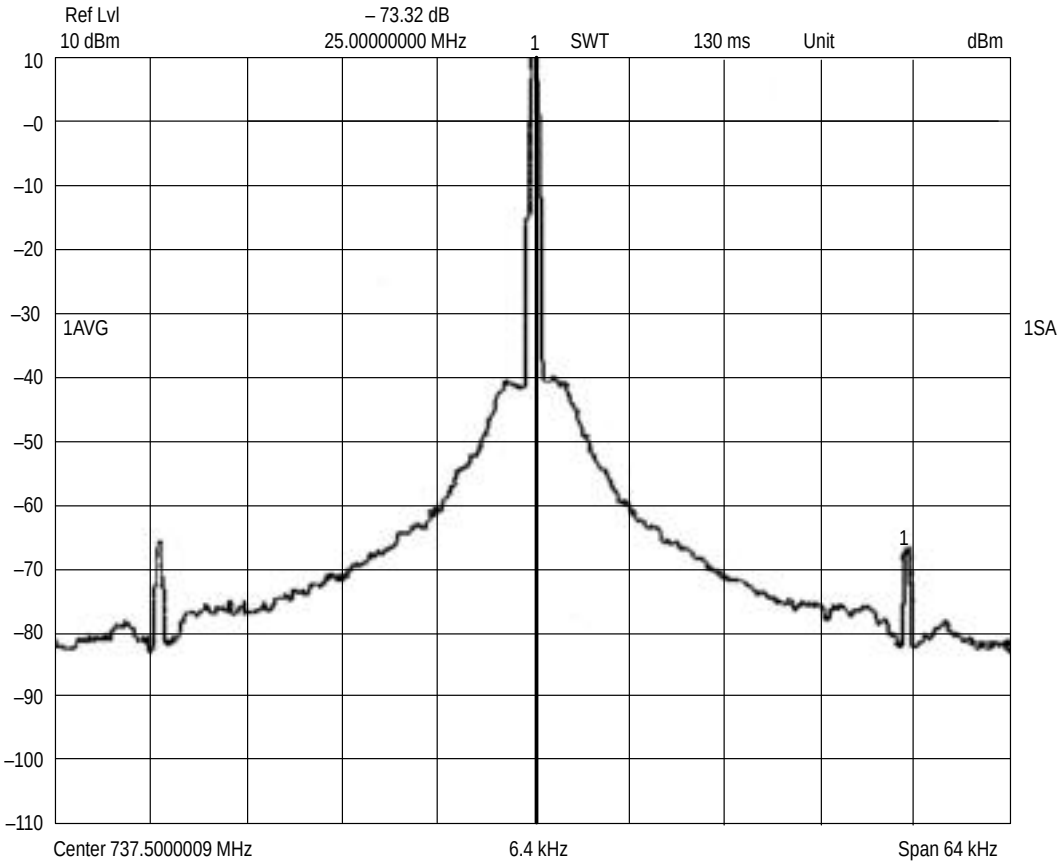


**Figure 49. Sybil EVK Reference Spur Measurements**




It should be noted that the reference spur values obtained from the simulation are lower than the values obtained from the actual EVK. This is because the simulation model is an "ideal" modeling of the PLL. To obtain results closer to the actual implementation, the models should be "massaged" to be more representative of the actual circuit. For example, spur levels more consistent with actual circuitry can be obtained by adding a resistance to ground at the input of the VCO to represent leakage. The value chosen should be consistent with VCO and circuit component performance.

To reduce simulation time, the H value may be used. By reducing the frequency of the VCO output, the number of samples required for simulation can also be reduced. The output shown in Figure 50 shows the result of dividing the VCO output of 730 MHz by 7.3 to produce a 100 MHz output. The reference spurs are better represented since adequate simulation time is possible.

To generate these outputs, the parameter values used were those shown on the top level schematic. The simulator was set to run a transient sweep, with $t_d$ set for a delay that would prevent the 4X frequency from being started. The initial conditions were set to 1 V and the simulation run for 1 ms. VCO was monitored and the probe display button FFT was initiated. The X and Y axis were adjusted to those shown.

Note: These simulations are presented as the result of "ideal" models and may not accurately display real hardware. It would be best to load the VCO input with additional leakage devices such as a large resistance, to accurately display real conditions. These models are starting points for more accurate implementations.

Loop filter analysis is more accurate, since the predominate factors are in the loop filter itself. To simulate the performance of the loop filter, $t_d$ is set for 0, N is set to the desired divider value, and $S_Z$ is set to the desired step. For this example, 733 MHz was chosen.

**NOTE**

These values are for reference only. The maximum operating frequency of the MC145181 is 550 MHz. For VCO frequencies greater than 550 MHz, an added external divider such as a prescaler is necessary.

With the VCO model shown, V(ctrl) = 0 produces an output of 727.6 MHz and at V(ctrl) = 1.35 V, the VCO frequency would be 733 MHz; the minimum MC145230EVK default operating frequency. To show the response of the loop filter to a 10 MHz step at this operating frequency, $S_Z$ = 10 MHz/ 25 kHz = 400. The simulation is run for 1 ms with a step ceiling of 100 ns. The result is shown in Figure 51.

If the simulation is examined over a longer period of time, the long term settling can be compared to the performance of the actual circuitry. The plot shown in Figure 52 shows the VCO control voltage with the display resolution set to 1 mV. This compares to the plot of frequency variation measurements made on the actual EVK. This plot is shown in Figure 53.

Figure 50. H Set to Generate a 100 MHz Output

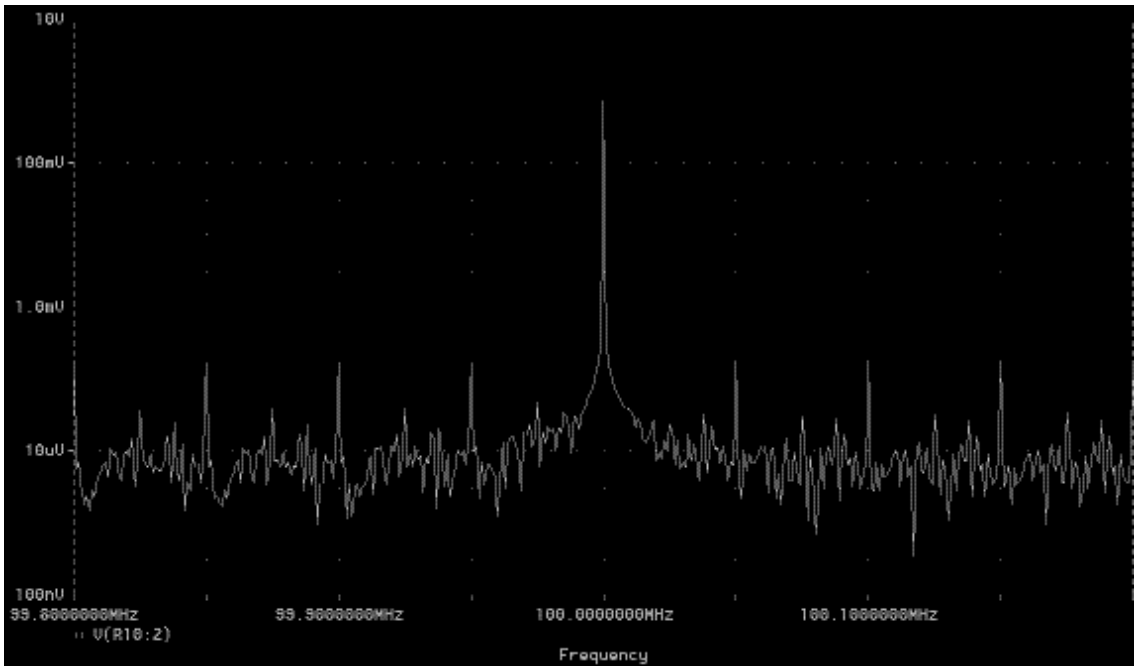



Figure 51. 10 MHz Step for an Operating Frequency of 729 MHz

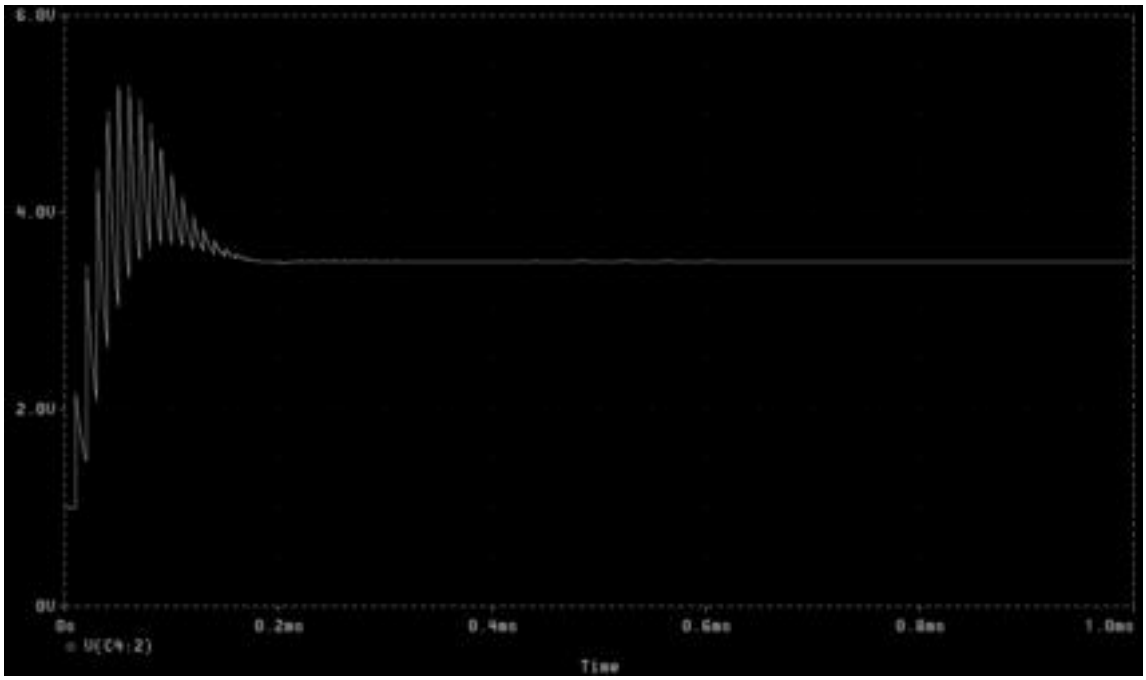


Figure 52. VCO Settling

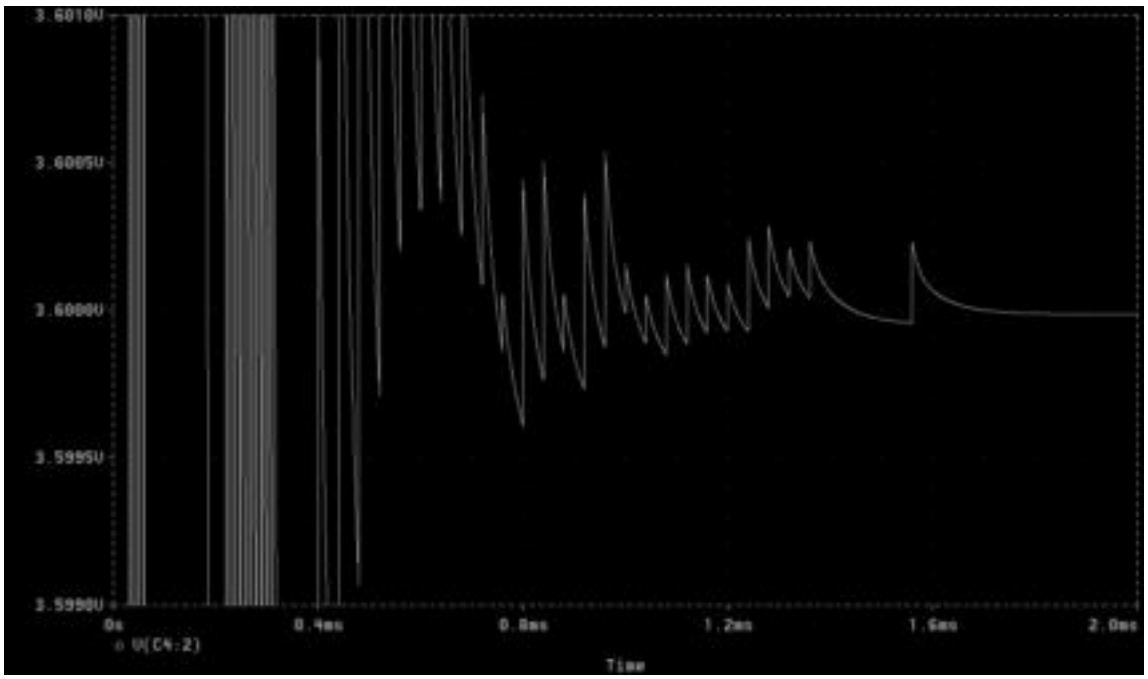
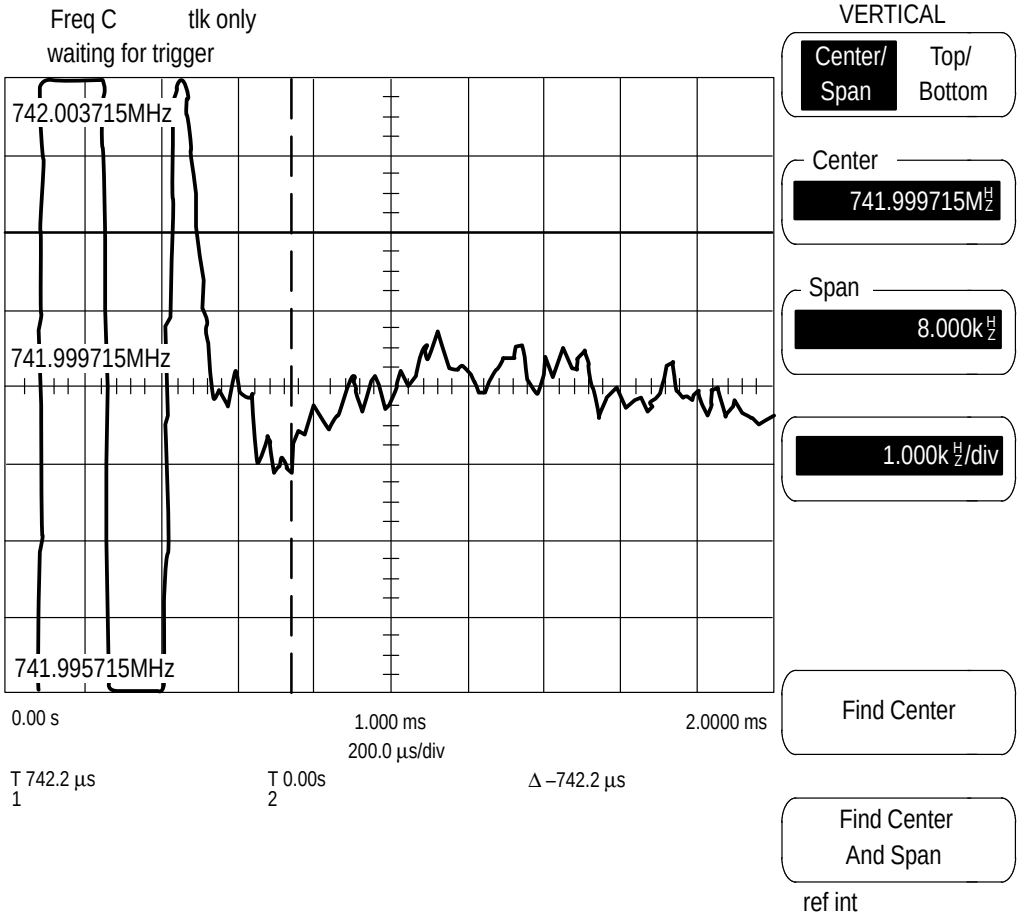



Figure 53. Frequency Settling of the EVK



It is noted that the results obtained from the simulation compare favorably to those obtained from the measurements of the EVK. The simulation display resolution is adjusted to represent the same ±4 kHz deviation as shown in Figure 53. Since variation in VCO control voltage is equal to the VCO frequency divided by the VCO gain, this axis may be redefined to show change in frequency rather than change in control voltage.

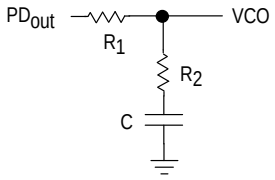
The models shown represent a “skeleton” that may be used to develop extensive and reliable simulations that can greatly reduce actual breadboarding and testing. In addition to the basic simulations shown, PSpice provides a method by which worst case and Monte Carlo evaluation can be performed on all, or selected components. By limiting the circuit to minimum necessary components, simulation can be performed using only the PSpice evaluation copy. In addition, the optional PSpice program Optimizer should allow refining the loop filter more easily.

While PSpice is a powerful tool, it is not without limits. Since it was designed to run on large mainframe computers, the PC is just now becoming powerful enough to make use of the capability of the simulator. A fast Pentium class processor with a large RAM and a hard drive of the Gbyte size is a necessity. Even with the most judicious planning, some simulations will “bump” the limits of the system.

## 7D. SECONDARY LOOP FILTER DESIGN

### Low Pass Filter Design for $PD_{out}'$

The design of low pass filtering for $PD_{out}'$ for the device can be accomplished using the following design information. In addition to the example included here, Motorola Application Note AN1207, also includes examples of active filtering which may be used to supplement this information.




$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NC(R_1 + R_2)}}$$

$$\zeta = 0.5\,\omega_n\left(R_2C + \frac{N}{K_\phi K_{VCO}}\right)$$

$$F(s) = \frac{R_2sC + 1}{(R_1 + R_2)sC + 1}$$

Definitions:
N = Total Division Ratio in Feedback Loop
$K_\phi$ (Phase Detector Gain) = $V_{DD}$/ 4π V/radian for $PD_{out}'$
$K_\phi$ (Phase Detector Gain) = $V_{DD}$/2π V/radian for $\phi_V$ and $\phi_R$

$$K_{VCO}\ (\text{VCO Gain}) = \frac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}$$

For a nominal design starting point, the user might consider a damping factor $\zeta \approx 0.7$ and a natural loop frequency $\omega_n \approx (2\pi f_R/50)$, where $f_R$ is the frequency at the phase detector input. Larger $\omega_n$ values result in faster loop lock times and, for similar sideband filtering, higher $f_R$–related VCO sidebands.

### Recommended Reading:

Gardner, Floyd M., *Phaselock Techniques (second edition).* New York, Wiley–Interscience, 1979.

Manassewitsch, Vadim, *Frequency Synthesizers: Theory and Design (second edition).* New York, Wiley–Interscience, 1980.

Blanchard, Alain, *Phase–Locked Loops: Application to Coherent Receiver Design.* New York, Wiley–Interscience, 1976.

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Rohde, Ulrich L., *Digital PLL Frequency Synthesizers Theory and Design.* Englewood Cliffs, NJ, Prentice–Hall, 1983.

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AR254, Phase–Locked Loop Design Articles, Motorola Semiconductor Products, Inc., Reprinted with permission from *Electronic Design,* 1987.

AN1207, The MC145170 in Basic HF and VHF Oscillators, Motorola Semiconductor Products, Inc., 1992.

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### Example:

Given the following information:

VCO frequency = 45.555 MHz,

Frequency step size = 5 kHz,

VCO gain = 3.4 MHz/V.

Design a loop filter with a damping factor of 0.707.

The VCO is assumed to have a linear response throughout the range used in this example. The gain for the VCO has been given as 3.4 MHz/V and is multiplied by 2π rad/s/Hz for calculating loop filter values.

$K_{VCO}$ = 2π rad/s/Hz x 3.4 MHz/V = 2.136 x $10^7$ rad/s/V .

The gain for the phase detector is defined as

$$K_\phi = \frac{V_{DD}}{4\pi}\ \text{V/rad for } PD_{out}' \ .$$

Using a value for $V_{DD}$ (phase detector supply voltage) of 3.6 V with the output voltage multiplier turned off, the value is

$$K_\phi = \frac{3.6}{4\pi} = 0.2865\ \text{V/rad} \ .$$

Let

$$\omega_n = \frac{2\pi\, f_r}{50} = 628.3\ \text{rad/s}$$

and

$$N = \frac{F_{VCO}}{F_{step\ size}} = \frac{45.555\ \text{MHz}}{5\ \text{kHz}} = 9111 \ .$$

Choosing C = 0.05 μF and calculating R1 + R2,

$$R1 + R2 = \frac{K_\phi\, K_{VCO}}{N\, C\, \omega_n^2} = 34\ \text{k}\Omega \ .$$

With a damping factor of 0.707,

$$R2 = \frac{\dfrac{0.707}{0.5\,\omega_n} - \dfrac{N}{K_\phi\, K_{VCO}}}{C} = 15\ \text{k}\Omega \ ,$$

R1 = (R2 + R1) – R2 = 34 k – 15 k = 19 kΩ ∼ 20 kΩ .

The choice for C is somewhat arbitrary, however, its value does impact the performance of the loop filter. If possible, a range of choices for C should be used to calculate potential loop filters and the resultant filters simulated, as will be shown below, to determine the best balance.

If additional filtering is desired, R1 may be split into two equal resistors and a capacitor to ground inserted. Since the closest resistance to one–half of 9 k is 4.7 kΩ, this value is chosen for $R1_a$ and $R1_b$. The maximum value for the added capacitance is based on the bandwidth of the original loop filter.

The general form for the transfer function for the passive filter shown in Figure 54, can be shown to have the form:

$$F(s) = K_h \left[ \frac{s + \omega_2}{(s + \omega_1)(s + \omega_3)} \right]$$

where

$$\omega_1 = \frac{1}{(R1_a + R1_b + R2)\, C} \quad ,$$

$$\omega_2 = \frac{1}{R2C} \quad ,$$

$$\omega_3 = \frac{1}{\left[ \frac{R1_a\, R1_b + R1_a\, R2}{(R1 + R2)} \right] C_c} \quad ,$$

where

$$R1 = R1_a + R1_b$$

and

$$\omega_3 > \omega_2 \quad .$$

Since splitting R1 into two equal values, $R1_a$ and $R1_b$, and inserting the capacitance between the junction of $R1_a$ and $R1_b$ does not change the position of the pole located at $\omega_1$, the value of $\omega_1$ remains

$$\omega_1 = \frac{1}{(R1_a + R1_b + R2)\, C} = \frac{1}{(R1 + R2)\, C} \quad .$$

The 0 identified at $\omega_2 = 1/R2\ C$ is also unaffected by the addition of $C_c$ if $\omega_3 > \omega_2$.

Since

$$R1_a = R1_b = \frac{R1}{2} \quad .$$

the value of $C_c$ can be determined by specifying the value for $\omega_3$ and using the values already determined for R1 and R2. The rule of thumb is to choose $\omega_3$ to be 10 x $\omega_B$ so as not to impact the original filter. $\omega_B$ can be found as

$$\omega_B = \omega_n \sqrt{[1 + 2\zeta^2 + \sqrt{(2 + 4\zeta^2 + 4\zeta^4)}]}$$

$$\omega_B = 628.3 \text{ rad/s} \sqrt{[1 + 2\,(0.707)^2 + \sqrt{(2 + 4\,(0.707)^2 + 4\,(0.707)^4)}]}$$

$$= 1.293 \times 10^3 \text{ rad/s} \quad .$$

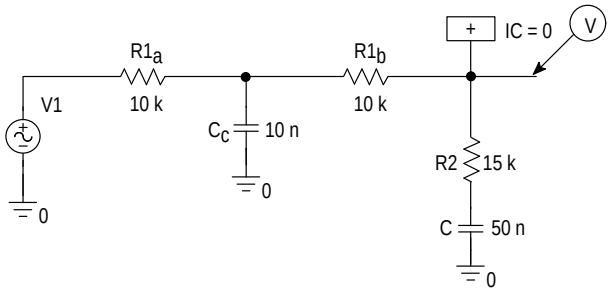
$$10\ \omega_B = 12.93 \times 10^3 \text{ rad/s} \quad .$$

The circuit for the passive loop filter is shown in Figure 54. R1 is split into two equal values and $C_c$ inserted at the junction of $R1_a$ and $R1_b$. Using the values defined above, $C_c$ is determined to be

$$C_c = \frac{1}{\left[ \frac{R1_a\, R1_b + R1_a\, R2}{(R1 + R2)\, \omega_3} \right]}$$

$$= \frac{1}{\left[ \frac{R1_a\, R1_b + R1_a\, R2}{(R1 + R2)\, 10} \right] \omega_B} = 10.83 \text{ nfd} \sim 10 \text{ nfd} \quad .$$

**Figure 54. Passive Loop Filter for $PD_{out}'$**




### Open Loop AC Analysis of the Loop Filter

AC analysis is chosen for the mode of simulation for PSpice and VSIN is chosen for V1 and is set to produce a 1 V peak output signal. The simulation is then run and the result shown in Figure 55.

A Bode plot of the loop filter is obtained which describes the open loop characteristics of the loop filter. The corner frequencies of the filter can be modified and the simulation rerun until the desired wave shape is obtained. Since AC analysis runs much faster than transient analysis, the AC open loop analysis of the loop filter is much quicker and requires less resources than the closed loop transient analysis.

### Closed Loop Filter Simulations Using PSpice

The top level schematic for simulating a simple loop filter for $PD_{out}'$ operating closed loop, is shown in Figure 56. This filter uses the values calculated above.

The schematic represents the PLL function using the internal phase detector, $PD_{out}'$, the loop filter calculated above, and a VCO. The parameter table allows altering the divider value of N, the maximum current obtained from $PD_{out}'$, and $PD_{out}$ charge pump voltage from the top level schematic.

The schematic for the VCO is shown in Figure 57. Analog behavioral modeling is used rather than discrete transistor modeling to reduce component count and improve simulation efficiency.

The behavioral VCO is composed of an integrator that transforms the input ctrl into the voltage control V(int) and a sine wave generator function whose frequency is controlled by V(int). EVALUE and GVALUE functions are used to perform the transforms. The analog behavioral models, ABM and ABMI, can also be used.

Figure 55. Bode Plot of the Passive Loop Filter

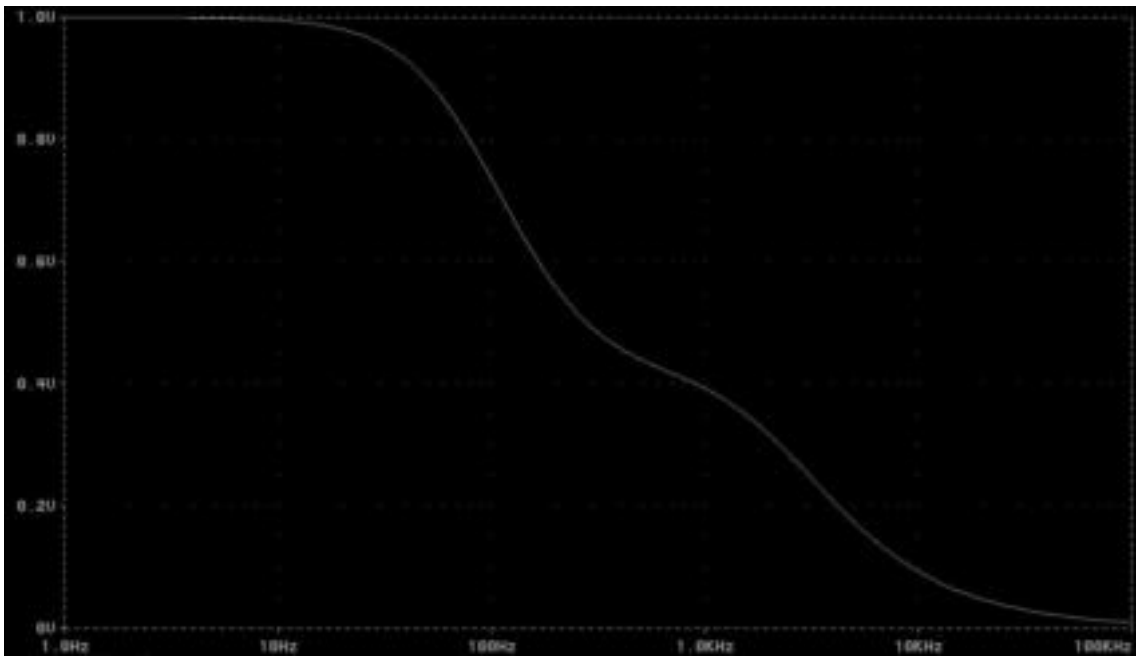



Figure 56. Passive Loop Filter

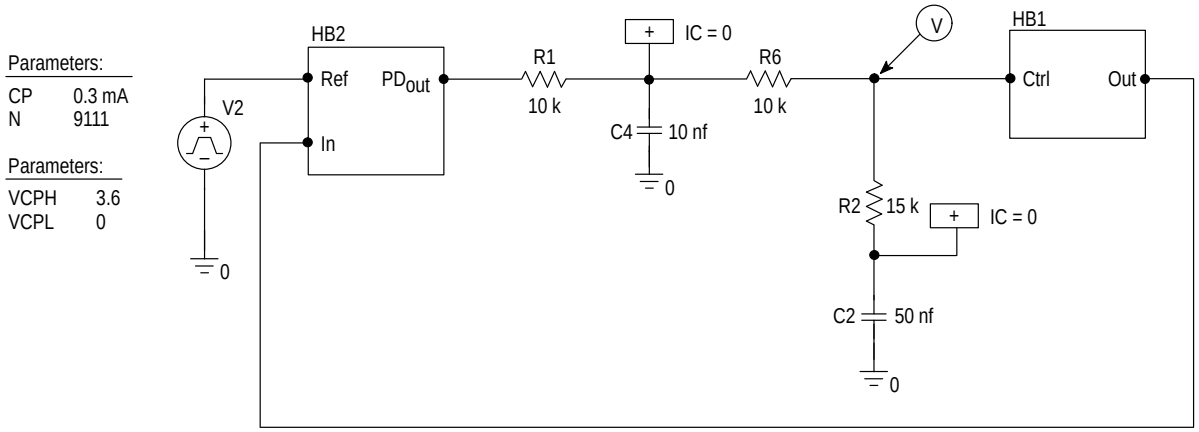
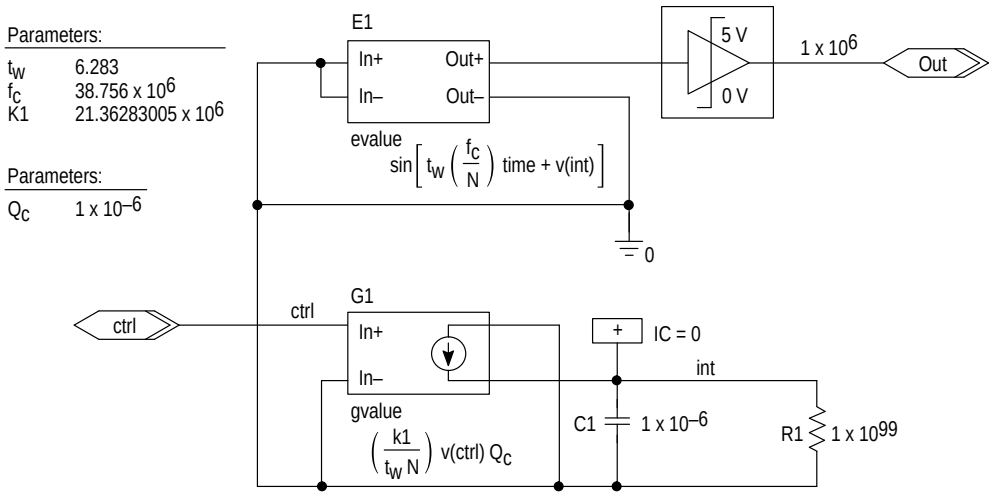


**Figure 57. VCO Behavioral Model**




G1 performs the operation [k1/($t_W$ N)] v(ctrl) $Q_C$. This integrates the input ctrl to produce a voltage ramp used by E1 to produce the desired output. This input is integrated by C1 whose value should equal $Q_C$ for most applications. R1 is required by SPICE to prevent a floating node error.

E1 performs the calculations necessary to generate a sine wave of the desired frequency based on the values listed in the parameter tables and the value of ctrl. The output of E1 is multiplied by 1 x $10^6$ and limited to 0 and 5 to obtain a square wave with a fast rise/fall time. Since I/O_STM is a standard model whose values are 0 and 5, these are used here and in the phase detector rather than modifying the component libraries.

The parameter tables provide a convenient method for setting VCO parameters. $t_W$ is 2π, $f_C$ is the zero control voltage VCO frequency, and K1 is the VCO gain in rad/s/V.

The sub–schematic for the phase/frequency detector section of the drawing is shown in Figure 58. This is composed of two blocks, HB3 and HB4. HB3 performs the $PD_{out}'$ function with HB4 performing the actual phase detector operation.

The circuit for the phase/frequency detector is shown in Figure 59. The model is made up of two pulse generators, two RS flip–flops, and appropriate behavioral gates.

HB1 and HB2 are RS flip–flops. These are constructed from behavioral blocks as shown in Figure 60. A behavioral AND gate with a 5 ns delay completes the three state (±2π) phase/frequency detector. The STP function ensures the RS flip–flops are reset at initiation.

To perform the phase detector function, the Ref and $f_{in}$ inputs of the behavioral RS flip–flops are configured to simulate edge triggered operation. This is achieved by placing a 1 ns delay in the Ref and $f_{in}$ signal paths. The input and output of the delay are compared by the input behavioral block and interpreted as a 1 ns pulse. These pulses are used to set HB1 and HB2. If $f_{in}$ leads Ref, the In flip–flop, HB2, will be set first. When Ref leads $f_{in}$, the Ref flip–flop, HB1, will be set first. The lagging edge drives the second flip–flop output high and the behavioral AND gate then resets both flip–flops. The delay line at the output of the behavioral AND gate prevents PSpice from being confused and also completes the simulation of the phase detector. The outputs of the two RS flip=flops are labeled $R_\phi$ and $V_\phi$. The time between the leading and lagging edges is reflected in the pulse width of the leading edge flip–flop. The lagging edge flip–flop will display a narrow pulse equal in width to the value chosen for the delay at the output of the behavioral AND gate. This should be programmed to the minimum value as specified by the data sheet and is usually 5 ns or less.

Since the outputs $R_\phi$ and $V_\phi$ are pure logic signals, additional circuitry is necessary to produce the output $PD_{out}'$. This output should be high impedance when not driving, and pull either high or low depending on which function ($R_\phi$ or $V_\phi$) is active. The circuitry shown in Figure 61 performs this function.

To eliminate the need for discrete modeling of $PD_{out}'$, analog behavioral modeling is used. Analog behavioral blocks ABMI/2, generate a current source/sink output whenever the appropriate input is high.

A second set of behavioral blocks monitor the output idrive, and switch on the appropriate voltage controlled switch whenever the output rises to the value of $V_{DD}$ (phase detector supply voltage) or drops to 0.

To model $PD_{out}'$, either a model of the transistors used for $PD_{out}'$ must be used or this behavioral arrangement can be used. Since the output is specified by a specific output level and current capability, this arrangement suffices. The output swing becomes VCPH in the schematic and the current capability is CP. If a non–zero value is desired for $V_{lo}$, the value VCPL is adjusted from the parameter table on the top level schematic.

This arrangement allows setting the output voltage swing of $PD_{out}'$ by specifying VCPH, the current drive of $PD_{out}'$ by specifying the desired value for CP, and leakage values can be simulated by setting the appropriate attributes for S1 and S4 or by adding additional resistance.

### Simulation

Figures 62 and 63 are the simulation results of running a transient analysis on the example shown above. The time to lock from power on is simulated by setting the initial condition (IC1) to 0 and running the simulation. Figure 62 is the time versus value of the VCO control voltage. Figure 63 shows the output at the input of the loop filter and can be used to determine lock time.

Figure 58. Phase/Frequency Detector

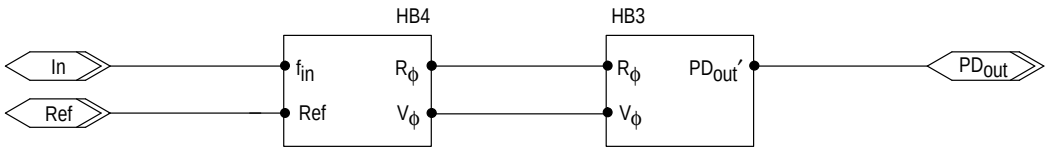



Figure 59. Phase Detector Logic

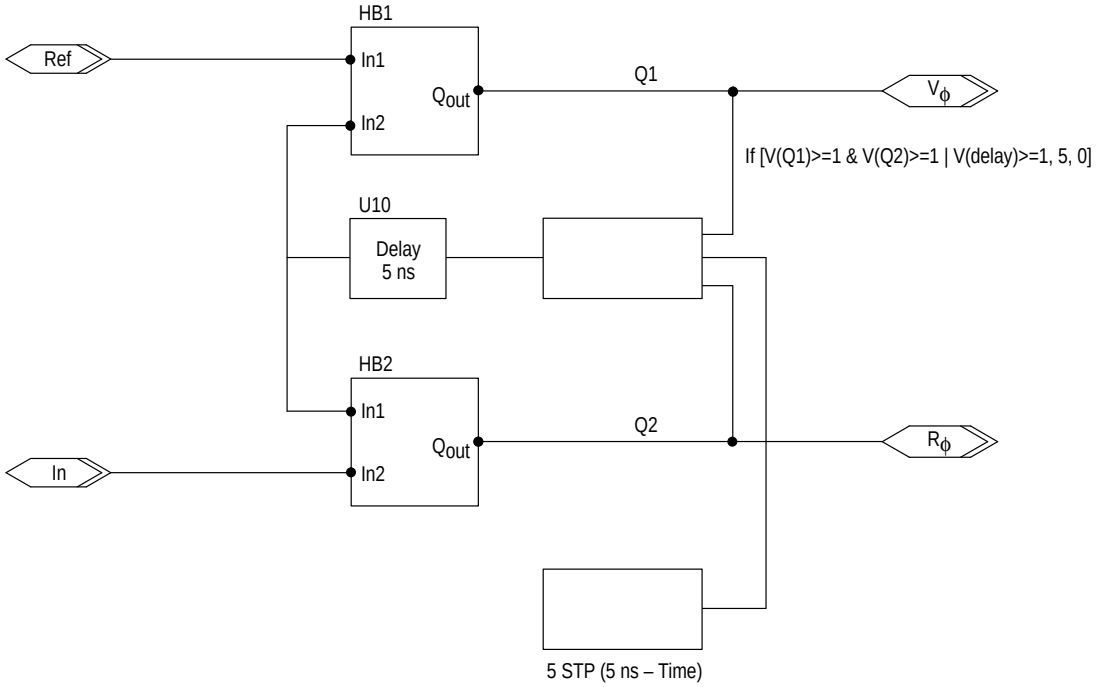



Figure 60. Behavioral RS Flip–flop

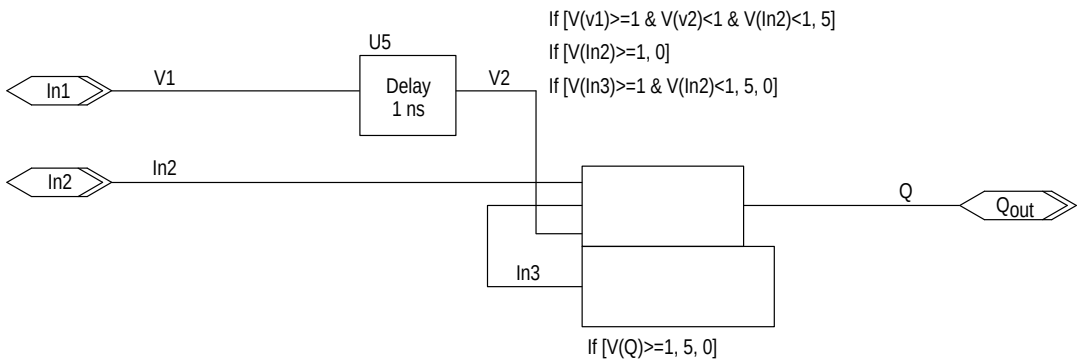


Figure 61. $R_\phi / V_\phi$ to $PD_{out}$′ Conversion

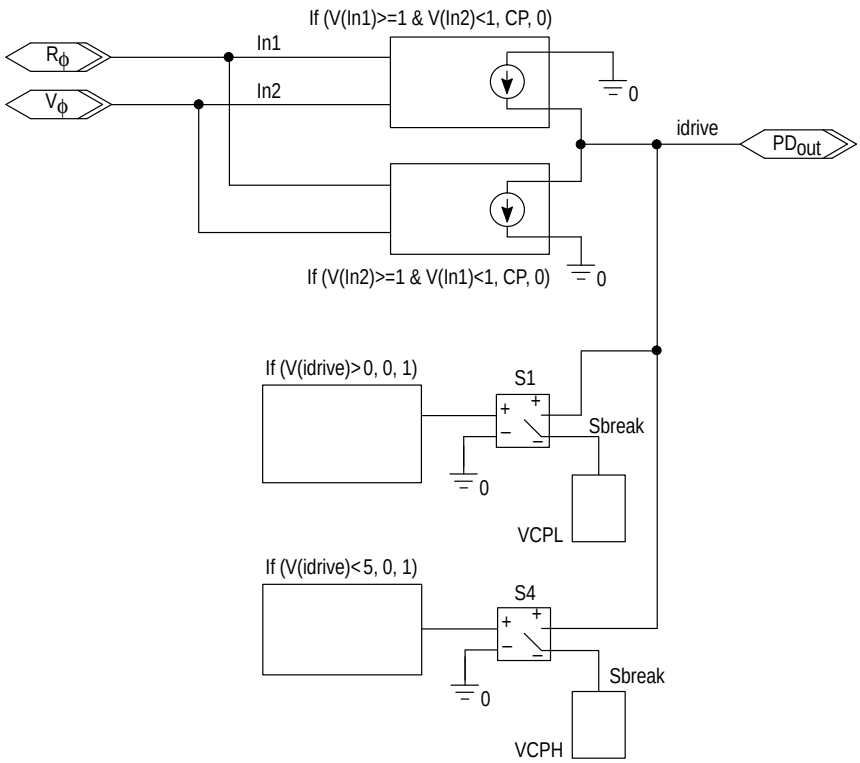



Figure 62. VCO Control Voltage versus Time

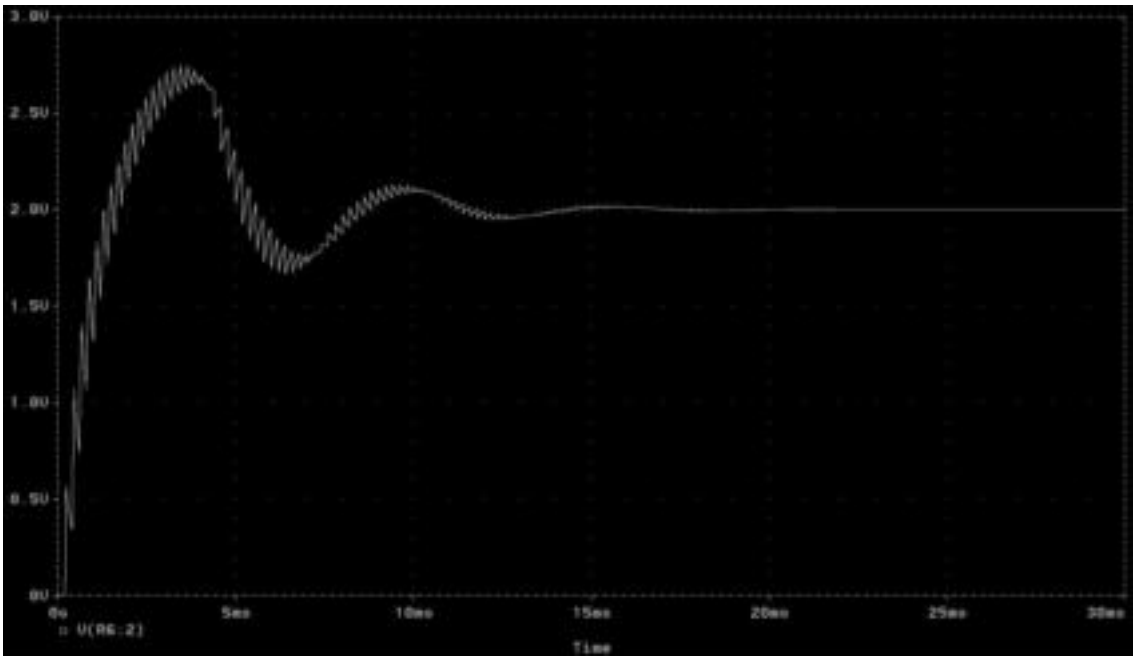
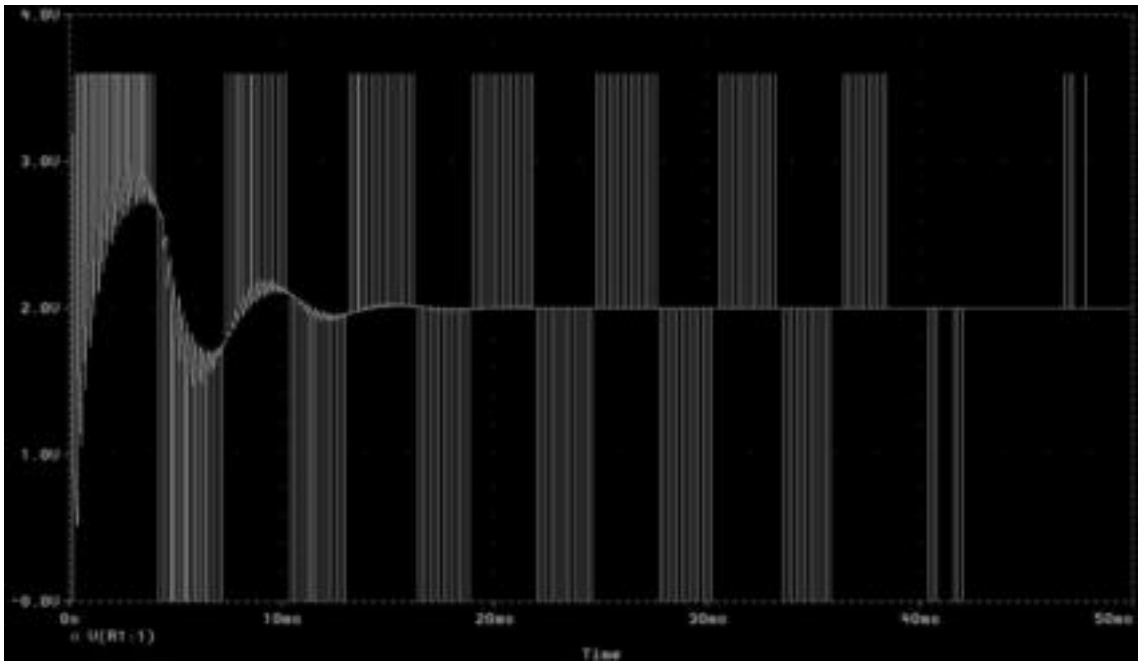


Figure 63. $PD_{out}'$ at Input to Loop Filter




**Summary**

PSpice provides a method by which the performance of PLL circuitry can be simulated prior to, or in addition to, laboratory testing. The use of behavioral modeling allows the creation of simulation circuits that can provide valuable information for loop filter design and adjustment. By judicious attention to VCO modeling, expected output characteristics can be verified prior to laboratory testing. While simulation does not replace laboratory testing, it can be used to find solutions to “what if” questions without the need for extensive empirical data gathering.

## 7E. VOLTAGE MULTIPLIER STALL AVOIDANCE

There are three important criteria to note, highlighted in the following sections: **Allowing for Voltage Build, Ensuring Valid Counter Programming,** and **Allowing for Overshoot.** Violation of any of these may cause the voltage multiplier to collapse. Once the voltage collapses, the loop goes out of lock and can not recover until the voltage is allowed to build up again. For an active loop, the voltage multiplier is designed to *maintain* the multiplied voltage on the phase/frequency detector supply pin ($C_{mult}$). If the main loop is active, the multiplier cannot build the voltage.

### Allowing for Voltage Build

After power up, a sufficient time interval must be provided for the on–chip voltage multiplier to build up the voltage on the $C_{mult}$ pin. During this interval, the phase/frequency detector outputs for the main loop ($PD_{out}$–Hi and $PD_{out}$–Lo) must be inactive (floating outputs). The POR (power–on reset) circuit forces this “float” condition, thus allowing the voltage to build on the $C_{mult}$ pin.

The duration of the interval to build the voltage is determined by the external capacitor size tied to the $C_{mult}$ pin and the charging current which is 100 μA minimum. The following formula may be used:

$$T = CV/I$$

where

T is the interval in seconds,
C is the $C_{mult}$ capacitor size in farads,
V is the desired voltage on $C_{mult}$ in volts, and
I is the charging current, $1 \times 10^{-4}$ amps.

The desired voltage on $C_{mult}$ is 4 V for a nominal 2 V supply and 5 V for any supply above 2.6 V.

After this interval, the chip can maintain the voltage on the $C_{mult}$ pin and the phase detectors may be safely placed in the active state.

The interval above also applies when the voltage multiplier is turned off (with power applied) via bits R′19 R′18 R′17 being 000. After the multiplier is turned back on, sufficient time must be allowed for the voltage to build on $C_{mult}$. In this case, typically an external resistor does not allow the $C_{mult}$ voltage to discharge below approximately $V_{pos}$ (see Section 5E, under **$C_{mult}$**). Note that if the voltage multiplier is NOT turned off (that is, the above bits are unequal to 000), the keep–alive circuit maintains the multiplied voltage on $C_{mult}$.

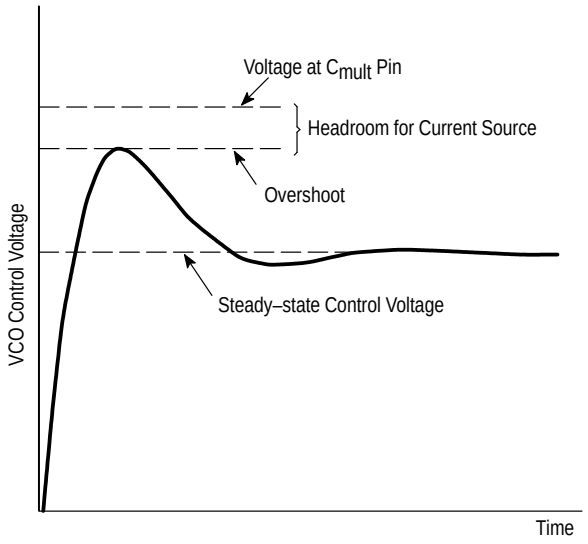
### Ensuring Valid Counter Programming

Before the PLLs and/or phase detectors are taken out of standby, legitimate divide ratios (pertinent to the application) must be loaded in the registers. For example, proper divide ratios must be loaded for the R, N, R′, and N′ counters. Also, proper values for all other bits must be loaded. For example: selection of crystal or external reference mode must be made prior to activation of the loops.

After the IC is initialized with the proper bits loaded, the main loop may then be safely activated via the phase detector float bit and/or the PLL standby bit being programmed to 0.

### Allowing for Overshoot

The VCO control voltage overshoot for the main loop must not be allowed to exceed the capability of the phase/frequency detectors’ maximum output voltage. The detectors’ maximum output voltage is determined by the minimum voltage at $C_{mult}$ and the headroom required for the current source. See the following figure.




For example, if the main supply voltage ($V_{pos}$) is 3 V and the voltage multiplier is utilized, the minimum voltage at $C_{mult}$ is 4.75 V. Then, to allow for current source headroom, the maximum output voltage from the parameter table in Section 3C is approximately $C_{mult}$ – 0.6 V or 4.2 V approximately. Thus, the maximum output overshoot voltage at the phase/frequency detector outputs should be no more than 4.2 V.

Continuing the above example, if the loop is designed with 20% overshoot in the VCO control voltage, then the overshoot must be subtracted off of the 4.2 V shown above. Therefore, the upper end of the control voltage to the VCO must be no more than approximately 3.64 V.

The equations below can be used to determine constraints:

$$\Delta V \leq \frac{V_\phi - 1.2}{2\alpha + 1}$$

$$SSV_{max} = V_\phi - \alpha\,(\Delta V) - 0.6$$

where

ΔV is the VCO control voltage range, the maximum minus the minimum voltage,

$V_\phi$ is the minimum phase detector supply voltage (at the $C_{mult}$ pin) per the following table,

α is the control voltage overshoot in decimal; for example, 20% overshoot is 0.2, and

$SSV_{max}$ is the maximum allowed steady–state VCO control voltage.

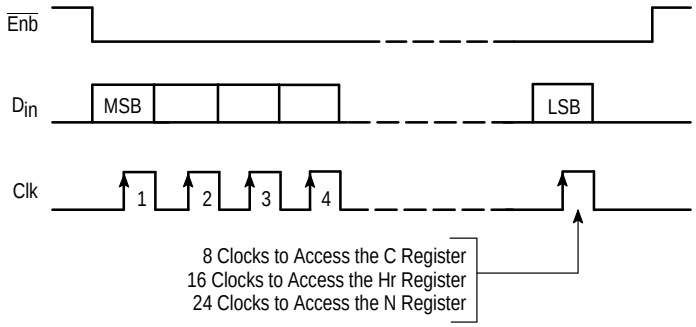
**MINIMUM PHASE DETECTOR VOLTAGE FROM VOLTAGE MULTIPLIER**

| Supply Voltage, $V_{pos}$ | Minimum Phase Detector Voltage, $V_\phi$ |
|---|---|
| 1.8 V | 3.32 V |
| 2.0 V | 3.72 V |
| 2.5 V | 4.75 V |
| 3.6 V | 4.75 V |

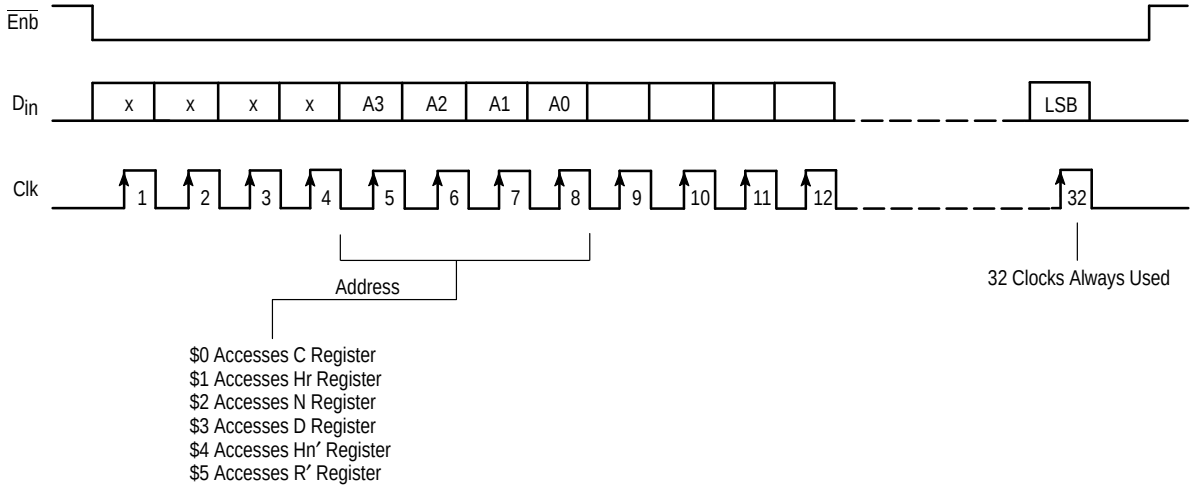
# 8. PROGRAMMER'S GUIDE

## 8A. QUICK REFERENCE

### BitGrabber ACCESS OF THE REGISTERS




### CONVENTIONAL ACCESS OF THE REGISTERS

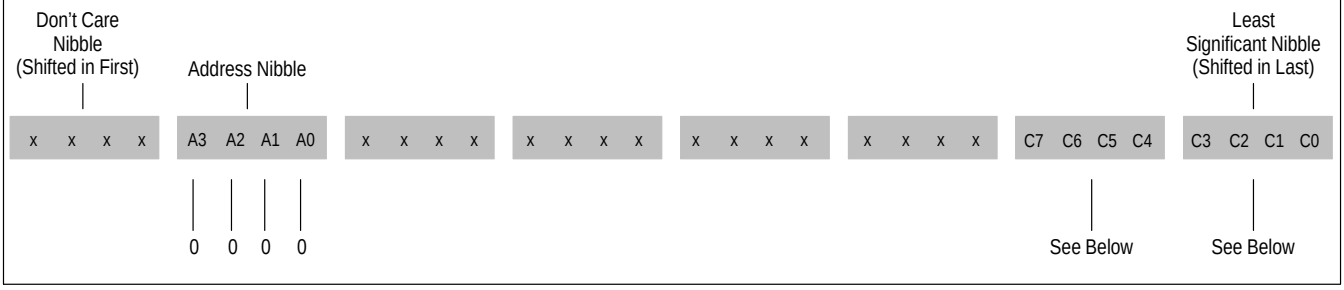



↑ = when the PLL device loads the data bit.

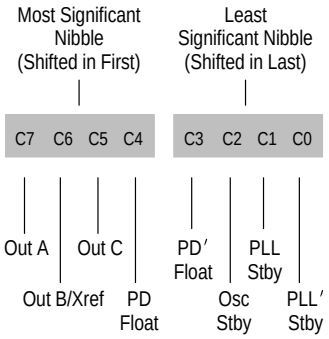
## 8A. QUICK REFERENCE (continued)

### C REGISTER

**Conventional Access**




**BitGrabber Access**




Out A = Output A Pin Logic State
0 = Pin is forced to 0 (power up default)
1 = Pin is forced to 1
See Note 1

Out B/XRef = Output B Pin Logic State/
External Reference Selection
See table below

Out C = Output C Pin Logic State
0 = Pin is forced to 0 (power up default)
1 = Pin is forced to high impedance

PD Float = Phase Detector Float
0 = Active, normal operation (power up default)
1 = $PD_{out}$–Hi/$PD_{out}$–Lo are forced to high impedance

PD′ Float = Phase Detector′ Float
0 = Active, normal operation (power up default)
1 = $PD_{out}$′ is forced to high impedance

Osc Stby = Oscillator Standby
0 = Active, normal operation (power up default)
1 = Oscillator/reference circuit in standby
See Note 2

PLL Stby = PLL Standby
0 = Active, normal operation
1 = Main PLL in standby (power up default)
See table below

PLL′ Stby = PLL′ Standby
0 = Active, normal operation
1 = Secondary PLL in standby (power up default)

**NOTES:** 1. For the Out A bit to control the Output A pin as a port expander, bits R′21 R′20 must be 0 0, which selects Output A as a general–purpose output. If R′21 R′20 are not equal to 0 0, then the Out A bit is a don't care.
2. Whenever Osc Stby = 1, both PLL Stby and PLL′ Stby must be 1, also.

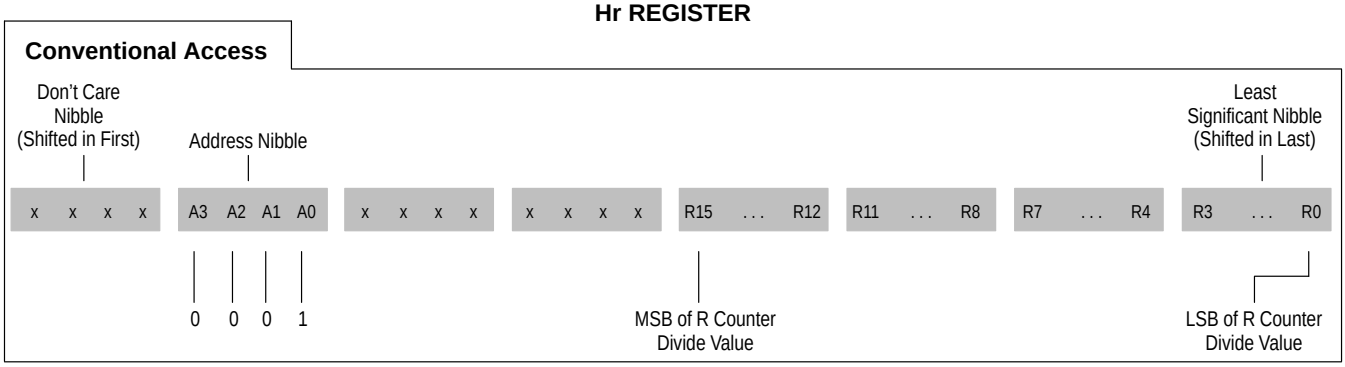
**Mode Pin and Bit Summary**

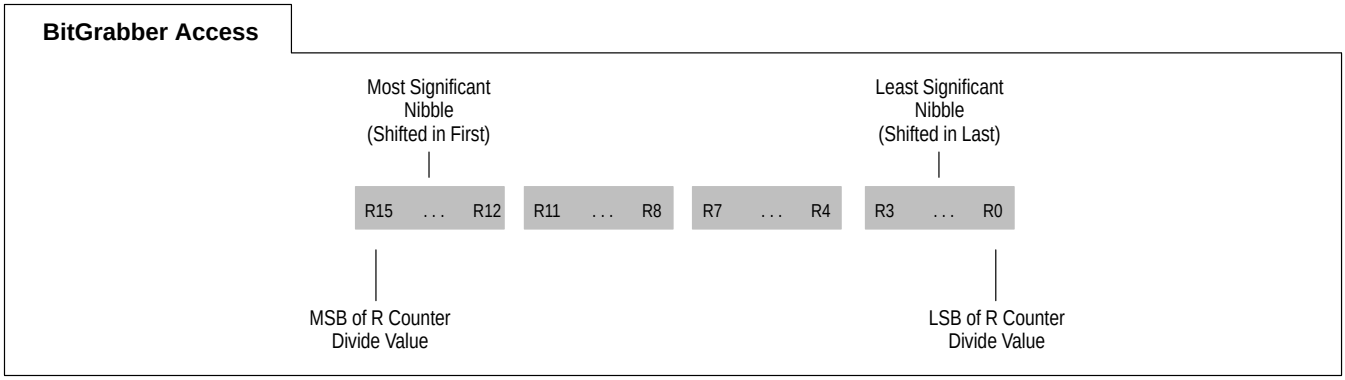
| Mode Pin | Out B/XRef Bit | PLL Stby Bit | Reference Circuit | Output B Pin | Main PLL |
|---|---|---|---|---|---|
| 0 | 0 | 0 | Xtal Osc mode | 0 | Active |
| 0 | 0 | 1 | Xtal Osc mode | Z | Standby |
| 0 | 1 | 0 | Xtal Osc mode | 1 | Active |
| 0 | 1 | 1 | Xtal Osc mode | Z | Standby |
| 1 | 0 | 0 | Xtal Osc mode | 0 | Active |
| 1 | 0 | 1 | Xtal Osc mode | Z | Standby |
| 1 | 1 | 0 | External Reference mode | 1 | Active |
| 1 | 1 | 1 | External Reference mode | Z | Standby |

**NOTES:** Xtal osc = crystal oscillator. Z = high impedance.

## 8A. QUICK REFERENCE (continued)

### Hr REGISTER



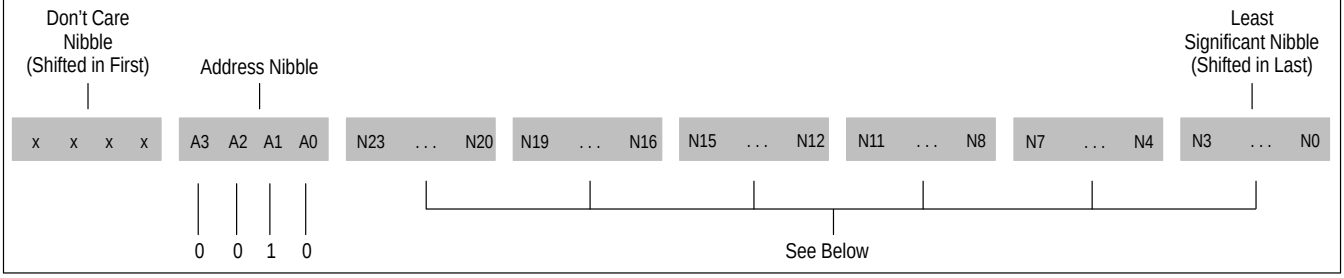

**EXAMPLE:** To program the R counter to divide by 1000 in decimal, first multiply 1000 by 2 which is 2000. Convert 2000 to hexadecimal: $7D0. Then, add leading 0s to form 2 bytes (4 nibbles): $07D0. Finally, load the Hr register bits R15 to R0 with $07D0. When the N register is subsequently loaded, data passes from the first Hr register (buffer) to the second R register (buffer). (Data is still retained in the Hr register.)
With BitGrabber, no address bits are needed. With a conventional load, address bits A3 to A0 must be included.

**NOTE:** Hexadecimal numbers are preceded with a dollar sign. For example: hexadecimal 1234 is shown as $1234.

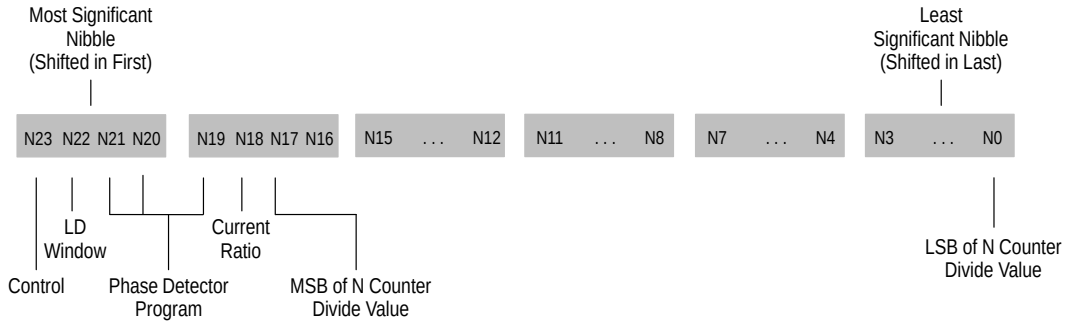
## 8A. QUICK REFERENCE (continued)

### N REGISTER

**Conventional Access**




**BitGrabber Access**




Control = Control for Auxiliary Divider
See Table A

LD Window = Lock Detector Window for Main Loop
0 = 32 $Osc_e$ periods
1 = 128 $Osc_e$ periods

Phase Detector Program = Detector Program for Main Loop
See Table B

Current Ratio = $PD_{out}$–Hi to $PD_{out}$–Lo Current Ratio
0 = 4:1
1 = 8:1

**EXAMPLE:** To program the N counter to divide by 1000 in decimal, first convert to hexadecimal: $3E8. Then, add leading 0s to form 2 leading bits plus 2 bytes (2 bits plus 4 nibbles); this is N17 to N0. Bits N23 to N18 should be appropriate to control the above functions. Finally, load the N register. Loading the N register also causes data to pass from the Hr register to the R register and data from the Hn′ register to pass to the N′ register.
With BitGrabber, no address bits are needed. With a conventional load, address bits A3 to A0 must be included.

**Table A. $Osc_e$ to $f_{out}$ Frequency Ratio, Mode = Low**

| N23 | R′1 | R′0 | $Osc_e$ to $f_{out}$ Frequency Ratio |
|---|---|---|---|
| 0 | 0 | 0 | 10:1 |
| 0 | 0 | 1 | 12.5:1 |
| 0 | 1 | 0 | 12.5:1 |
| 0 | 1 | 1 | 12.5:1 |
| 1 | 0 | 0 | 8:1 |
| 1 | 0 | 1 | 10:1 |
| 1 | 1 | 0 | 10:1 |
| 1 | 1 | 1 | 10:1 |

**NOTE:** When the Mode pin is high, the $f_{out}$ pins are configured as polarity inputs and N23 must be programmed to 1.

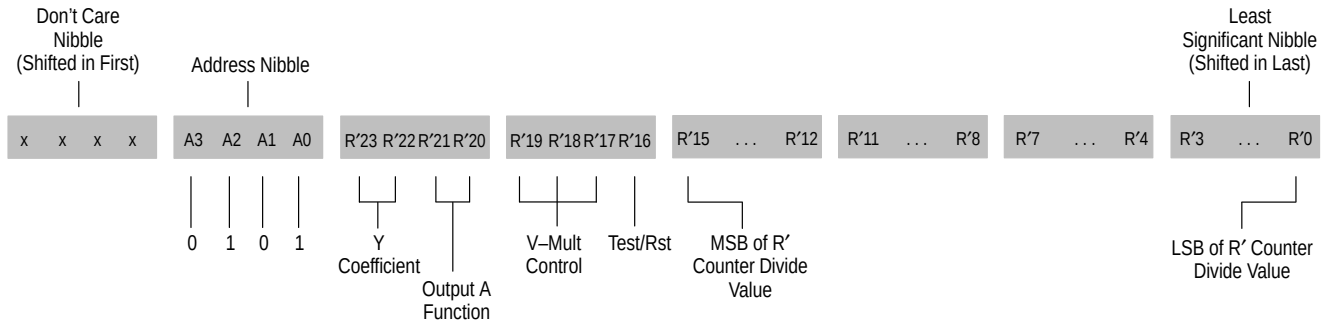
**Table B. Main Phase Detector Control**

| N21 | N20 | N19 | Result |
|---|---|---|---|
| 0 | 0 | 0 | Both $PD_{out}$–Hi and $PD_{out}$–Lo floating |
| 0 | 0 | 1 | $PD_{out}$–Hi floating, $PD_{out}$–Lo enabled |
| 0 | 1 | 0 | $PD_{out}$–Hi enabled, $PD_{out}$–Lo floating |
| 0 | 1 | 1 | Both $PD_{out}$–Hi and $PD_{out}$–Lo enabled |
| 1 | 0 | 0 | $PD_{out}$–Hi enabled and $PD_{out}$–Lo floating for 16 $f_R$ cycles, then $PD_{out}$–Hi floating and $PD_{out}$–Lo enabled |
| 1 | 0 | 1 | $PD_{out}$–Hi enabled and $PD_{out}$–Lo floating for 32 $f_R$ cycles, then $PD_{out}$–Hi floating and $PD_{out}$–Lo enabled |
| 1 | 1 | 0 | $PD_{out}$–Hi enabled and $PD_{out}$–Lo floating for 64 $f_R$ cycles, then $PD_{out}$–Hi floating and $PD_{out}$–Lo enabled |
| 1 | 1 | 1 | $PD_{out}$–Hi enabled and $PD_{out}$–Lo floating for 128 $f_R$ cycles, then $PD_{out}$–Hi floating and $PD_{out}$–Lo enabled |

## 8A. QUICK REFERENCE (continued)

### R′ REGISTER

**Conventional Access only**




Y Coefficient
- 0 0 = Maximum frequency on $f_{in} \leq 550$ MHz
- 0 1 = Maximum frequency on $f_{in} \leq 1.2$ GHz
- 1 0 = Maximum frequency on $f_{in} \leq 2.2$ GHz
- 1 1 = Not used

Output A Function = Controls Output A Mux
- 0 0 = General–Purpose Output
- 0 1 = $f_R$
- 1 0 = $f_{R'}$
- 1 1 = Phase Detector pulse

V–Mult Control = Voltage Multiplier Control
- 0 0 0 = Multiplier OFF, 9 MHz ≤ $Osc_e$ ≤ 80 MHz
- 0 0 1 = Multiplier ON, 9 MHz ≤ $Osc_e$ ≤ 20 MHz
- 0 1 0 = Multiplier ON, 20 MHz < $Osc_e$ ≤ 40 MHz
- 0 1 1 = Multiplier ON, 40 MHz < $Osc_e$ ≤ 80 MHz

Test/Rst = Test/Reset
- 0 = only programming value allowed

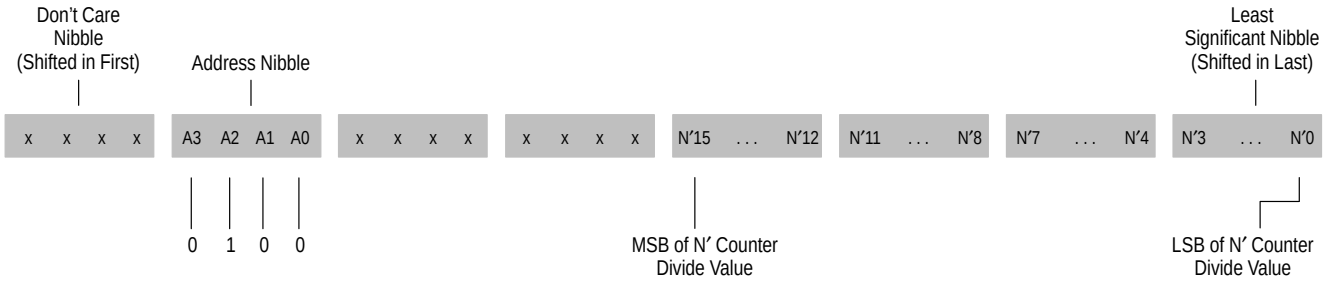
**EXAMPLE:** When the Mode pin is tied low, see Table 21 for R′ counter programming. When the Mode pin is tied high, to program the R′ counter to divide by 1000 in decimal, first multiply 1000 by 2, which is 2000. Convert 2000 to hexadecimal: $7D0. Then, add leading 0s to form 2 bytes (4 nibbles); this becomes bits R′15 to R′0. Bits R′23 to R′16 should be appropriate to control the above functions. Finally, load the R′ register.
With a conventional load, address bits A3 to A0 must be included.

**NOTE:** Hexadecimal numbers are preceded with a dollar sign. For example: hexadecimal 1234 is shown as $1234.

## 8A. QUICK REFERENCE (continued)

### Hn′ REGISTER

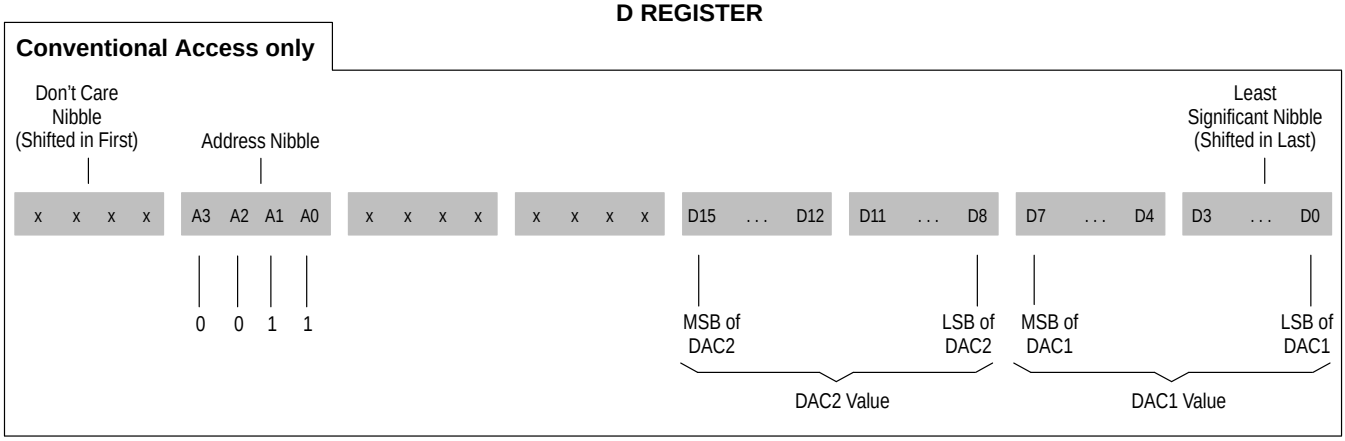
**Conventional Access only**




**EXAMPLE:** To program the N′ counter to divide by 1000 in decimal, first convert 1000 to hexadecimal: $3E8. Then, add leading 0s (if necessary) to form 2 bytes (4 nibbles): $03E8. Finally, configure address bits A3 to A0 and load the Hn′ register. When the N register is subsequently loaded, data passes from the first Hn′ register (buffer) to the second N′ register (buffer). (Data is still retained in the Hn′ register.)

## 8A. QUICK REFERENCE (continued)

### D REGISTER




DAC2 Value = Analog Output Level of DAC2
- $00 = zero output
- $01 = zero + 1 LSB output
- $02 = zero + 2 LSBs output
- $03 = zero + 3 LSBs output
- •
- •
- •
- $FD = full scale – 2 LSBs output
- $FE = full scale – 1 LSB output
- $FF = full scale output

DAC1 Value = Analog Output Level of DAC1
- $00 = zero output
- $01 = zero + 1 LSB output
- $02 = zero + 2 LSBs output
- $03 = zero + 3 LSBs output
- •
- •
- •
- $FD = full scale – 2 LSBs output
- $FE = full scale – 1 LSB output
- $FF = full scale output

## 8B. INITIALIZING THE DEVICE

### Introduction

The registers retain data as long as power is applied to the device. The R and N registers contain counter divide ratios for the main loop, PLL. The R′ and N′ registers contain counter divide ratios for the secondary loop, PLL′. Additional control bits are located in the R′, N, and C registers. The D register controls the DACs. Section 8A is a handy reference for register access and bit definitions.

The C, D, R′, and N registers can be directly written, and have an immediate impact on chip operation. The Hr and Hn′ registers can be directly written, but have no immediate impact on chip operation. This is because the Hr and Hn′ registers are the front–ends of double buffers. The Hr register feeds the R register. The Hn′ register feeds the N′ register. Changing data in the R and/or N′ registers is done with a write to the Hr and/or Hn′ register, respectively, followed by a write to the N register. The transfer of data from the Hr to R and Hn′ to N′ registers is triggered with a write to the N register.

Typically, the Hr and Hn′ registers are written once, during initialization after power up. The Hr and Hn′ registers only need to be accessed if their data is changing.

### An Example

Following is an initialization example for a system with a main loop that covers 1.8 to 2.1 GHz in 30 kHz steps. An external reference of 19.44 MHz is utilized. The secondary loop is selected to run at 200 MHz. Both VCOs are positive polarity meaning that when the input control voltage increases, the output frequency increases. A divided–down reference is not needed ($f_{out}$ and $\overline{f_{out}}$). Therefore, the Mode pin is tied to $V_{pos}$ and the Pol and Pol′ pins are tied to ground.

The following initialization gives serial data examples for BitGrabber access of the C, Hr, and N registers.

### Initialization

Below is the six–step initialization sequence used after power up for the example given above.

Programming the C register first is recommended if the voltage multiplier is utilized. There are three important criteria to note. Violation of any criterion may cause the voltage multiplier to collapse. The first criterion is that after power up, a sufficient time interval must be provided (after the C and R′ registers are initialized) for the on–chip voltage multiplier to build up the voltage on the $C_{mult}$ pin. This interval is determined by the external capacitor size tied to the $C_{mult}$ pin and the charging current which is about 100 μA. After this interval, the chip can maintain the voltage on the $C_{mult}$ pin and the phase/frequency detectors for the main loop may be safely activated. The second criterion is that before the phase/frequency detectors are activated, legitimate divide ratios (pertinent to the application) must be loaded in the registers. The third criterion is a hardware issue. The three criteria are discussed with more detail in Section 7E.

If the voltage multiplier is not used, Step 1 is eliminated and the initialization sequence starts with Step 2.

### Step 1: Load the C Register

The C register is programmed such that the main loop's phase/frequency detector outputs are floating (PD Float bit C4 = 1), the reference circuit is active (Osc Stby bit C2 = 0), and an external reference is accommodated (Out B/Xref bit C6 = 1, with the Mode pin high). When the voltage multiplier is enabled by programming the R′ register, the voltage is allowed to build on the $C_{mult}$ pin such that a voltage higher than the main supply voltage is providing power to the phase/frequency detectors. Both loops are active (PLL Stby bits C1 = C0 = 0). Also, for this example, Output A and Output C are programmed low (Out bits C7 = C5 = 0).

In summary, hexadecimal 58 or $58 is serially transferred (BitGrabber access with no address bits).

### Step 2: Load the R′ Register

For the secondary loop, the 19.44 MHz reference is divided down to 80 kHz by the R′ counter; the divide ratio is 243. Per Section 8A, the value is doubled to 486. The 16 LSBs of the R′ register determine the R′ counter divide ratio. Therefore, 486 is converted to $01E6 and becomes the 16 LSBs (R′15 to R′0) in the R′ register. Test/Rst bit R′16 must be a 0. Bits R′19 to R′17 determine the refresh rate of the voltage multiplier. The frequency at $Osc_e$ is <20 MHz. Therefore, per Section 8A, bits R′19 to R′17 must be 001. If Output A is needed as a MCU port expander, bits R′21 = R′20 = 0. Per Section 8A, Y Coefficient bits R′23 R′22 = 10.

In summary, $058201E6 is serially transferred (conventional access with an address of 0101).

### Step 3: Load the Hr Register

For the main loop, the 19.44 MHz reference must be divided down to 30 kHz by the R counter; the divide ratio is 648. Per Section 8A, the ratio 648 is doubled to 1296 and then converted to $510. The Hr register value is programmed as $0510. When the Hr register contents are transferred to the R register, the R counter divide ratio is determined.

In summary, $0510 is serially transferred (BitGrabber access). This value is transferred from the Hr to the R register when the N register is accessed in Step 5.

### Step 4: Load the Hn′ Register

For the secondary loop, the phase detector is chosen to run at 80 kHz. Therefore, 80 kHz must be multiplied up to 200 MHz which is a factor of 2500. The factor is converted to $9C4. The Hn′ register is programmed as $09C4. When the Hn′ register contents are transferred to the N′ register, the N′ counter divide ratio is determined.

In summary, $040009C4 is serially transferred (conventional access with an address of 0100). The value $09C4 is transferred to the N′ register when the N register is accessed in Step 5.

### Step 5: Load the N Register

For this example, the IC is initialized to tune the lowest end of the main loop. The lowest end of the main loop's frequency range is 1.8 GHz. Therefore, the 30 kHz must be multiplied up to 1.8 GHz which is a factor of 60,000 or $EA60 to be loaded into bits N17 to N0 of the N register. Bit N18 is programmed to 0 for a $PD_{out}$–Hi to $PD_{out}$–Lo current ratio of 4:1. If $PD_{out}$–Lo is used for the main loop, bits N21 to N19 must be 001. ($PD_{out}$–Lo must be used to initialize the device when *adapt* is used, see Section 8D.) Bit N22 = 0 to select a lock detect window of approximately $32 / Osc_e$ = 32/19.44 MHz or 1.6 μs. Bit N23 must be programmed to 1 by the user. (When the Mode pin is high, programming N23 to a 0 is for Motorola use only.)

In summary, $88EA60 is serially transferred (BitGrabber access). The N register access also causes double–buffer transfers of Hr to R and Hn′ to N′.

**Step 6: Load the C Register**

Now that legitimate divide ratios are programmed for the counters, the main loop may be activated. Thus, the PD float bit C4 is now programmed to 0. The standby bits are unchanged: C2 = C1 = C0 = 0. Bit C5 could be used to control Output C to either a low level or high impedance; for a low level, C5 = 0. Whenever an external reference is utilized, bit C6 must be 1. Bit C7 may be used to control Output A to a low or high level because it is selected as “port expander” by bit R′21 and R′20; for a low level, C7 = 0.

In summary, $40 is serially transferred (BitGrabber access). This causes the main loop to tune to 1.8 GHz, the secondary loop to tune to 200 MHz, and both the Output A and Output C pins to be forced low.

The device is now initialized.

## 8C. PROGRAMMING WITHOUT ADAPT

### Tuning the Top of the Band

After initializing the device via steps 1 through 6 in Section 8B, the only register that needs to be loaded to tune the main loop is the N register.

For this example, tuning the upper end of the band (2.1 GHz) requires that the 30 kHz at the phase/frequency detector be multiplied up to 2.1 GHz. This is a loop multiplying factor of 70,000. This value is converted to $11170 and is loaded for bits N17 to N0. Bits N23 to N18 are not changed and are programmed as indicated in Section 8B, step 5.

In summary, $891170 is transferred to tune the main loop. No other registers are loaded.

### Tuning Other Channels

Tuning other channels for the main loop, while keeping the secondary loop at a constant frequency, only requires programming the N register. See Table 22 for example frequencies.

**Table 22. Main Loop Tuning Examples**

| Frequency Desired (MHz) | Multiplying Factor (Decimal) | Multiplying Factor (Hexadecimal) | N Register Data (Hexadecimal) |
|---|---|---|---|
| 1800.000 | 60,000 | $EA60 | $88EA60 |
| 1800.030 | 60,001 | $EA61 | $88EA61 |
| 1800.060 | 60,002 | $EA62 | $88EA62 |
| 1800.090 | 60,003 | $EA63 | $88EA63 |
| 1950.000 | 65,000 | $FDE8 | $88FDE8 |
| 1966.080 | 65,536 | $10000 | $890000 |
| 2088.960 | 69,632 | $11000 | $891000 |
| 2100.000 | 70,000 | $11170 | $891170 |

## 8D. PROGRAMMING UTILIZING HORSESHOE WITH ADAPT

### Introduction

A unique adapt feature can be used with the MC145225 or MC145230 when conventional tuning cannot meet the lock–time requirements of a system and the annoying spurs or noise cannot be tolerated from a fractional–N scheme. The adapt feature is available on the main loop only.

For adapt, a timer is engaged which causes an internal data update of the R and N registers to be delayed. The IC supports the *Horseshoe* scheme for adapt by allowing a fairly–close quickly–tuned *approximate* frequency to be tuned, followed by the tuning of the *exact* frequency. Two sets of R and N data are sent to the device. The first set {R1, N1} is for tuning the approximate frequency. The second set {R2, N2} is for tuning the exact frequency. Use of the timer delays the transfer of {R2, N2} until a programmed interval has elapsed. In addition, after the interval has elapsed, the main loop control switches from $PD_{out}$–Hi to $PD_{out}$–Lo.

### Tuning Near the Top of the Band

Continuing the example, after initializing the device via steps 1 through 6 in Section 8B, Horseshoe with adapt can be used to tune the main loop to obtain fast frequency jumps. Use of the BitGrabber access is recommended to minimize the number of serial data clocks required for sending the four “words”.

In this example, the first phase of adapt utilizes approximate tuning with the phase/frequency detector running at 4x the step size. Therefore, the approximate tuning runs the detector at about 120 kHz. The second phase, with exact tuning, runs the detector at 30 kHz. Horseshoe with adapt requires that two data sets be serially sent to the device for every frequency tuned. The first set is for approximate tuning {R1, N1}; the second set is for exact tuning {R2, N2}.

Approximate tuning with Horseshoe is unique. This method involves two key elements: (1) increasing the phase detector frequency and (2) varying *both* the R and N divide values such that the approximate frequency is within a certain predetermined range. The Horseshoe algorithm contained in the development system software also allows placing a constraint on the loop–gain variation that the user can tolerate.

For example, to tune 1800.270 MHz, the first {R1, N1} data set could contain divide ratios for the R and N counters of 138.5 and 12,826, respectively. With this data set, the phase detector is running at about 140 kHz and the approximate frequency is about 325 Hz from the exact frequency. The second data set contains R and N divide ratios of 648 and 60,009, respectively. This achieves the exact (target) frequency of 1800.270 MHz.

The timer must be programmed to determine the interval that the device is in the approximate–tune mode. For this example, assume this is 32 $f_R$ cycles; thus, bits N21 N20 N19 = 1 0 1 in the first data set. Note that this time interval is 32 cycles of $f_R$, with the phase detector running at about 140 kHz (approximate tune) or about 230 µs plus the MCU

shift time shown in Figure 64. Included in the first data set are N23 = 1 which is required when the Mode pin is high, N22 = 0 for the lock detect window of 1.6 μs, and N18 = 0 for a current ratio of 4:1 (because the phase detector is running at approximately 4x the step size). Note that bits N23, N22, and N18 are unchanged from the initialization values.

For the second data set, bits N23, N22, and N18 are unchanged. Bits N21, N20, and N19 must be programmed as 001. This enables $PD_{out}$–Lo for the exact tune after time out.

In summary, two data sets need to be sent to the device: {R1, N1} and {R2, N2}. They are sent in succession as R1, N1, R2, N2; where R1 is the R register value for the first data set, N1 is the N register value for the first set, etc. For the example, these values are {R1, N1} = {$0115, $A8321A} and {R2, N2} = {$0510, $88EA69}. See Figure 64.

### Tuning Other Channels

Tuning other channels for the main loop, while keeping the secondary loop at a constant frequency, requires sending two data sets to the part {R1, N1} and {R2, N2}. See Table 23.

## 8E. CONTROLLING THE DACs

### Introduction

The two 8–bit DACs are independent circuit blocks on the chip. They have no interaction with other circuits on the chip. A single 16–bit register, called the D register, holds the binary value which controls both DACs.

### Programming the DACs

A DAC programmed for 0 scale is in the low–power mode. The 0 scale is programmed as $00 for each 8–bit DAC.

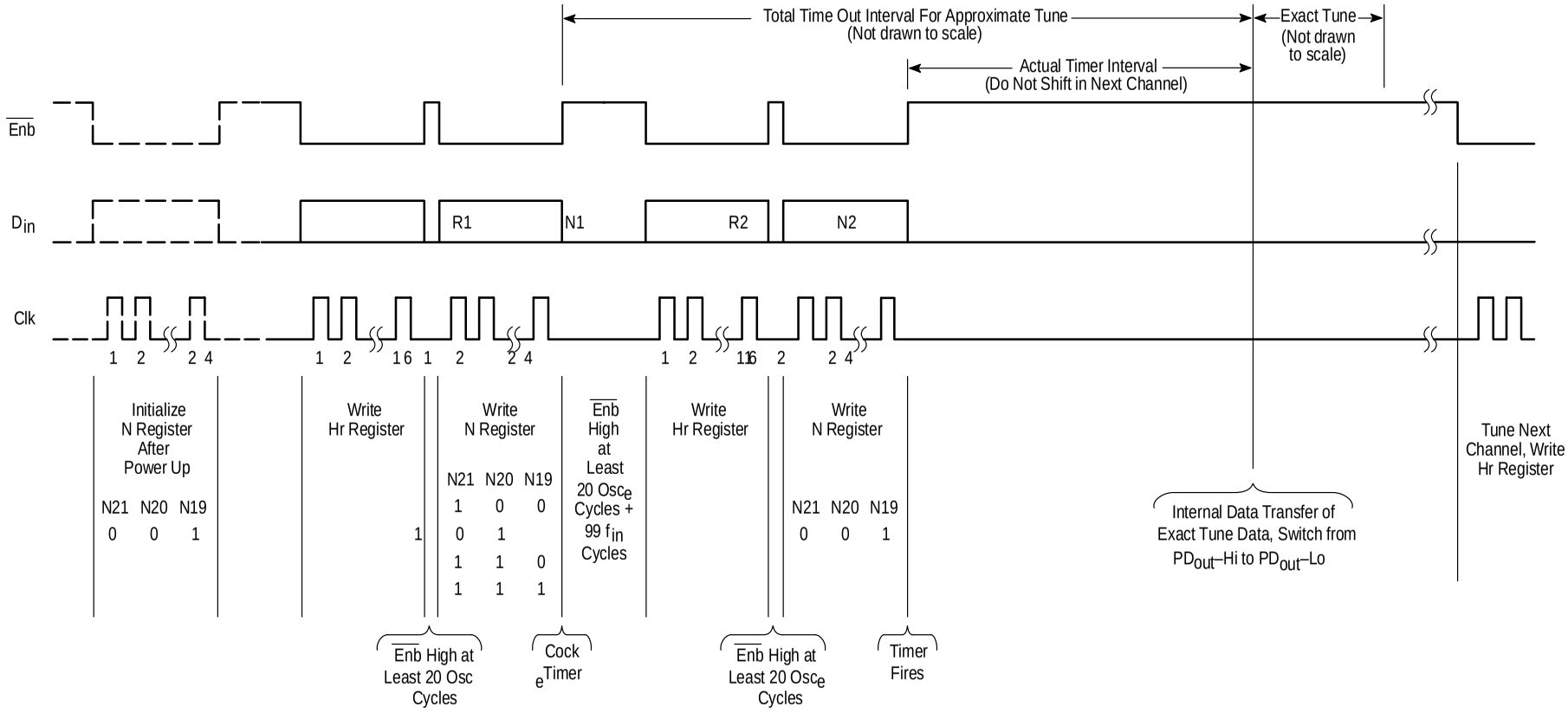
As an example, consider a system that uses just one of the DACs (DAC 1). The other DAC output is unused and is programmed for 0 output. If a condition for a system requires that the DAC have a half–scale output, then DAC 1 is programmed as $80.

In summary, $03000080 is serially transferred (conventional access with an address of 0011).

**Table 23. Main Loop Tuning Using Horseshoe With Adapt**

| Desired Target Frequency (MHz) | Approximate Tuning | | | Exact Tuning | |
|---|---|---|---|---|---|
| | R1 | N1 | Frequency Error (Hz) | R2 | N2 |
| 1800.000 | $0144 | $A83A98 | 0 | $0510 | $88EA60 |
| 1800.270 | $0115 | $A8321A | 325 | $0510 | $88EA69 |
| 1808.220 | $0184 | $A8467D | 619 | $0510 | $88EB72 |
| 2061.300 | $00EC | $A830E0 | 1017 | $0510 | $890C66 |
| 2063.010 | $00F6 | $A830E0 | 732 | $0510 | $890C9F |
| 2100.000 | $0144 | $A8445C | 0 | $0510 | $891170 |

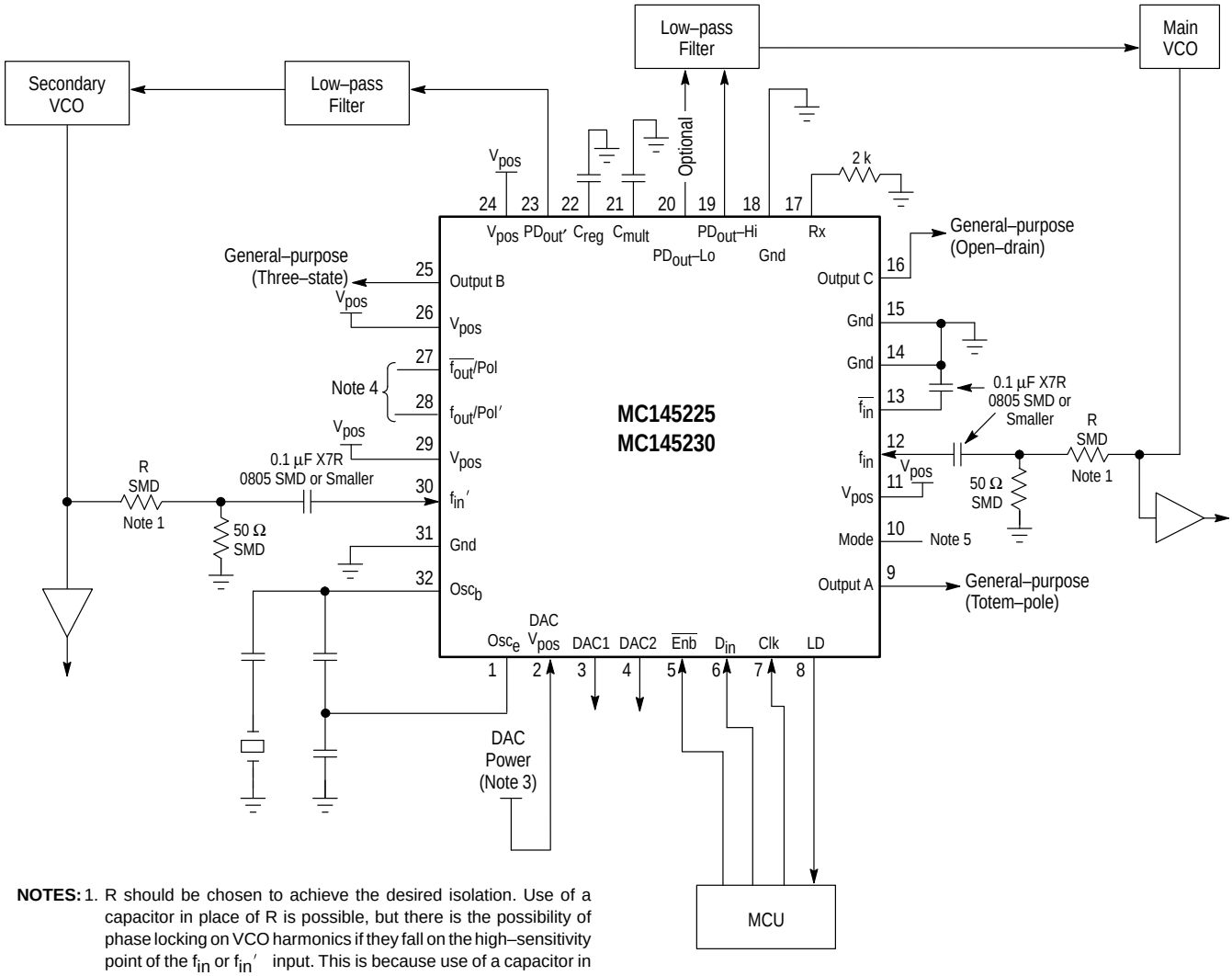
**Figure 64. Serial Data Format for Horseshoe with Adapt**




**NOTE:** The interval for shifting in Exact Tune {R2, N2} data adds to the actual Approximate Tuning time. However, this is usually insignificant. For example, at a data rate of 2 Mbps (2 megabits per second), approximately 20 µs is added to the Approximate Tuning time.

## 9. APPLICATION CIRCUIT

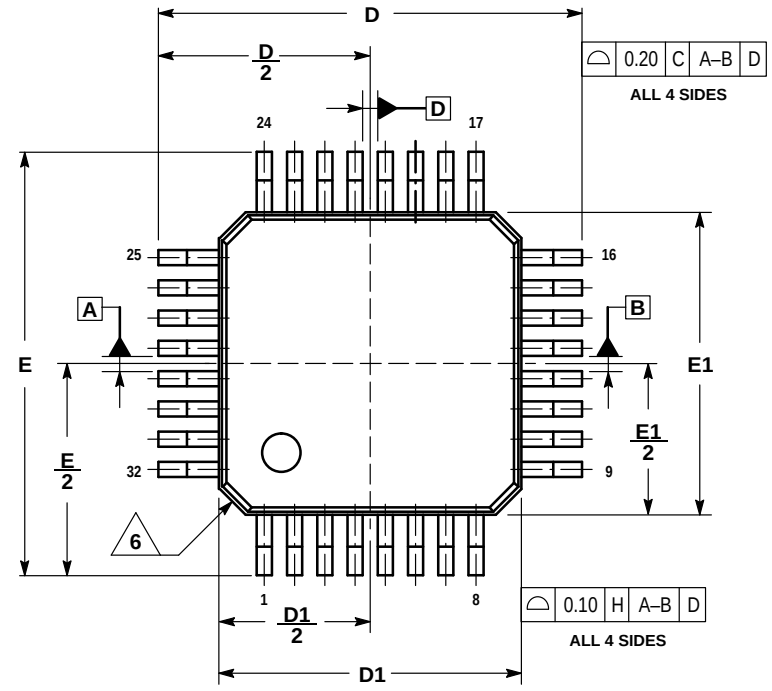
**Figure 65. Application Circuit**

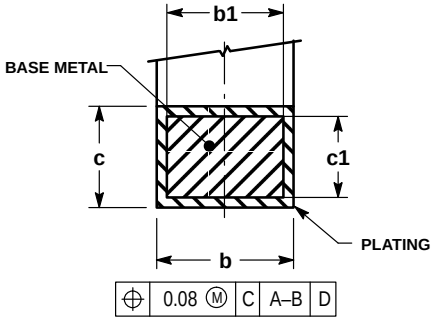



**NOTES:** 1. R should be chosen to achieve the desired isolation. Use of a capacitor in place of R is possible, but there is the possibility of phase locking on VCO harmonics if they fall on the high–sensitivity point of the $f_{in}$ or $f_{in}'$ input. This is because use of a capacitor in place of R forms a high–pass filter.
2. $V_{pos}$ may range from 1.8 to 3.6 V.
3. DAC power may be any potential between 1.8 V and 3.6 V.
4. Configurable pins. See Pin Descriptions.
5. Tie mode to Gnd or $V_{pos}$.

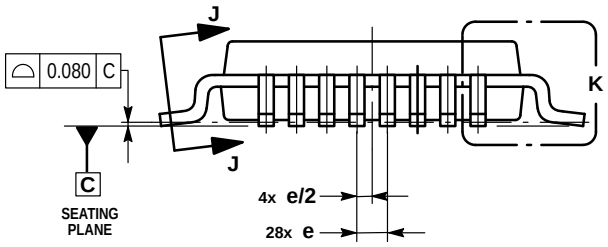
## 10. OUTLINE DIMENSIONS

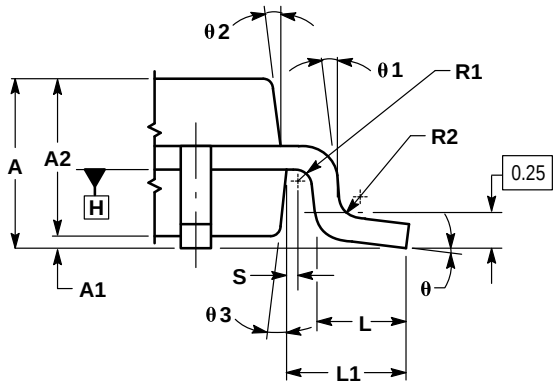
PLASTIC PACKAGE
CASE 873C–01
(LQFP–32)
ISSUE A




SECTION J–J




DETAIL K

NOTES:
1. DIMENSIONS ARE IN MILLIMETERS. AND TOLERANCING PER ASME Y14.5M, 1994.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DATUMS A, B, AND D TO BE DETERMINED WHERE THE LEADS EXIT THE PLASTIC BODY AT DATUM PLANE H.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08 mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN A PROTRUSION AND AN ADJACENT LEAD IS 0.07 mm.
6. EXACT SHAPE OF CORNERS MAY VARY.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | — | 1.60 |
| A1 | 0.05 | 0.15 |
| A2 | 1.35 | 1.45 |
| b | 0.18 | 0.27 |
| b1 | 0.17 | 0.23 |
| c | 0.10 | 0.20 |
| c1 | 0.09 | 0.16 |
| D | 7.00 BSC | |
| D1 | 5.00 BSC | |
| E | 7.00 BSC | |
| E1 | 5.00 BSC | |
| e | 0.50 BSC | |
| L | 0.45 | 0.75 |
| L1 | 1.00 REF | |
| R1 | 0.08 | — |
| R2 | 0.08 | 0.20 |
| S | 0.20 | — |
| θ | 0° | 7° |
| θ1 | 0° | — |
| θ2 | 11° | 13° |
| θ3 | 11° | 13° |

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