MC149570

Advance Information

Multi-Standard Video Processor

The MC149570 multi-standard video processor provides the video compression, decompression, and scaling functions for Qorus® video communication system applications. To support two-way video communications, the video processor can decode and encode H.261 and/or H.263 video bitstream simultaneously. The processor has a direct interface to a NTSC/PAL decoder and encoder. It requires 1 Mbyte EDO DRAMs for frame storing. The MC149570 video processor performs five major independent video functions: Video Pre-Processing, Video Post-Processing, Video Encoding, Video Decoding, and Picture-In-Picture (PIP) Processing. The functional block diagram in **Figure 1** shows the major functional modules that enable the MC149570 to perform these functions.

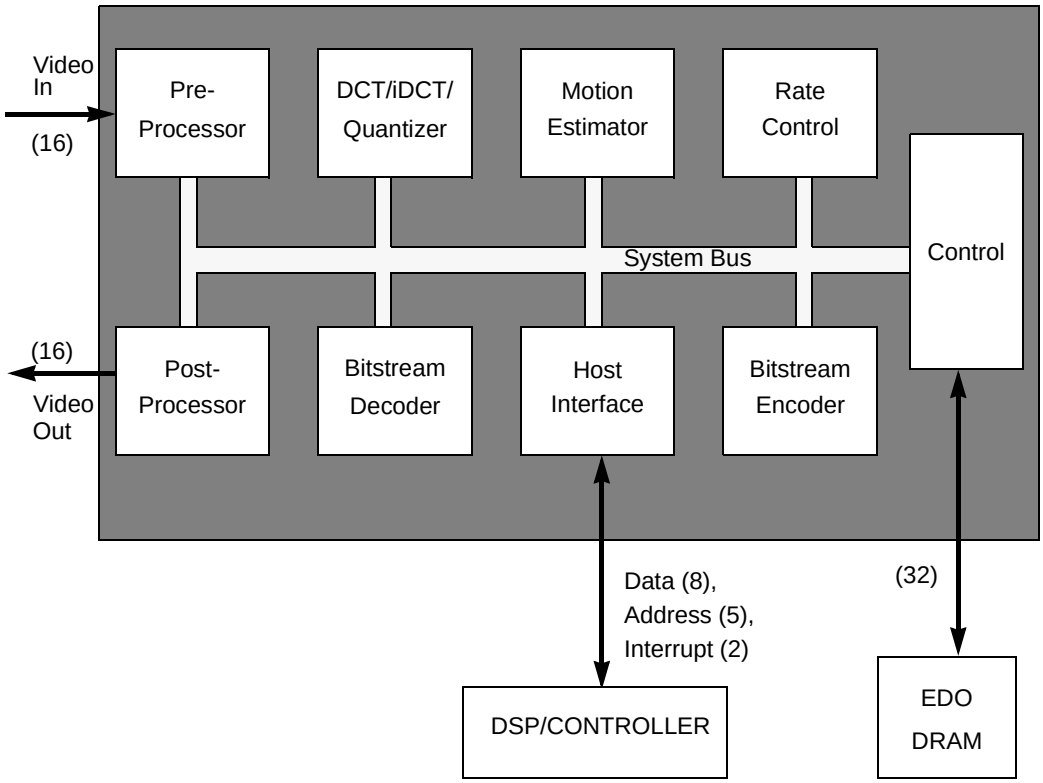

Figure 1. MC149570 Functional Block Diagram

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FOR TECHNICAL ASSISTANCE:

Telephone: 1-800-521-6274

Internet: http://www.mot-sps.com/support/technical/

Data Sheet Conventions

This data sheet uses the following conventions:

PIN_L	Used to indicate a signal that is active when pulled low. (For example, the DCS_L pin is active when low.)
asserted	Means that a high true (active high) signal is high or that a low true (active low) signal is low
deasserted	Means that a high true (active high) signal is low or that a low true (active low) signal is high

Examples:	Signal/Symbol	Logic State	Signal State	Voltage
	PIN_L	True	Asserted	V_{IL}/V_{OL}
	PIN_L	False	Deasserted	V_{IH}/V_{OH}
	PIN	True	Asserted	V_{IH}/V_{OH}
	PIN	False	Deasserted	V_{IL}/V_{OL}

Note: Values for V_{IL}, V_{OL}, V_{IH}, and V_{OH} are defined by individual product specifications.

FEATURES

- Multiple ITU Video Standard support:
  - ITU H.261
  - ITU H.263
- Independent video encode and decode engines
  - Encodes CIF (352 × 288) and QCIF (176 × 144) sized images
  - Decodes CIF, QCIF, and SQCIF (128 × 96) sized images
  - Encodes/decodes CIF up to 15 frames per second and QCIF up to 30 frames per second
- Supports from 16 kbps to 512 kbps video bit rates
- Has video bypass mode for self view
- Video Pre-Processing
  - Accepts NTSC or PAL input video signals
  - Non-linear temporal noise core filter reduces noise and improves coding efficiency
  - Data input stream compliant with 4:2:2 (16-bit) CCIR 601 standard
  - Glueless interface to industry standard NTSC/PAL video decoders
- Video Post-Processing
  - Scales CIF/QCIF/SQCIF video to standard NTSC/PAL
  - Deblocking Filtering and Mosquito Filtering—Reduces visible artifacts from video compression
  - Four positions for Picture-In-Picture (PIP) with mirror option that allows direct display of input video
  - Data output stream compliant with 4:2:2 (16-bit) CCIR 601 standard
  - Local display scaling from CIF, QCIF, and SQCIF to different interlaced display sizes (see **Table 1**)

Table 1. Display Scaling

Type	Input Resolution	Scaled Display Image					
NTSC	CIF	704 × 480	528 × 360	352 × 288	—	—	—
	QCIF	704 × 480	528 × 360	352 × 240	264 × 180	176 × 288	176 × 144
	SubQCIF	512 × 320	384 × 240	256 × 160	192 × 120	128 × 192	128 × 96
PAL	CIF	704 × 576	528 × 432	352 × 576	352 × 288	—	—
	QCIF	704 × 576	528 × 432	352 × 288	264 × 216	176 × 288	176 × 144
	SubQCIF	512 × 384	384 × 288	256 × 192	192 × 144	128 × 192	128 × 96

  - Glueless interface to industry standard NTSC/PAL video encoders
  - Compensation circuitry for display overscan
  - Four selectable colors for border/background
- Motion Estimation
  - Fully supports H.263 Annex F Advanced Prediction Mode
  - Four motion vectors per macroblock generated supports overlapped block motion compression for better picture quality at lower bit rates
  - Unrestricted motion vectors can extend past picture boundaries to improve performance
  - Motion estimation vector range extends to -16 to +15.5 vertical and horizontal pixels
  - 384 full pel motion vector candidates
  - Half-pixel search motion estimation
- Rate Control
  - Intelligent frame rate control
  - Dynamic trade-off between temporal/spatial quality and low latency frame rate adjustment on user input during video calls
  - Minimum delay due to fully pipelined processing
- Other features
  - H.261 and H.263 modes independently configurable for encoder and decoder
  - NTSC/PAL I/O modes independently configurable
  - 8-bit Host Interface provides chip control and bitstream interface
  - Thirty On-chip registers allow the user to program video parameters
  - On-chip DRAM controller interfaces EDO DRAM through a 32-bit Data Bus
  - Programmable on-chip Phase Lock Loop (PLL) that can be programmed to run from 27 MHz to 44 MHz
  - Operating frequency of 44 MHz with video input/output frequency of 13.5 MHz
  - All inputs are 5 V tolerant
  - Optimized for 3.3 V operation from 0°C to 70°C ambient temperature
  - 292-ball PBGA package with 1.27 mil ball pitch

1

Signal Descriptions

1.1 Signal Groupings

The input and output signals of the MC149570 are organized into functional groups, as shown in **Table 1-1** and as illustrated in **Figure 1-1**. The MC149570 is operated from a 3.3 V supply; however, all the input and bidirectional pins can tolerate 5 V.

Table 1-1. MC149570 Functional Signal Groupings

Functional Group	Number of Signals	Detailed Description
Power (VCC_x) and Ground (GND_x)	29	**Table 1-2**
Reset	1	**Table 1-3**
Phase Lock Loop (PLL) and Clock	2	**Table 1-4**
Operation Mode Select	3	**Table 1-5**
Host Interface	18	**Table 1-6**
Video Input	19	**Table 1-7**
Video Output	19	**Table 1-8**
DRAM Interface	45	**Table 1-9**

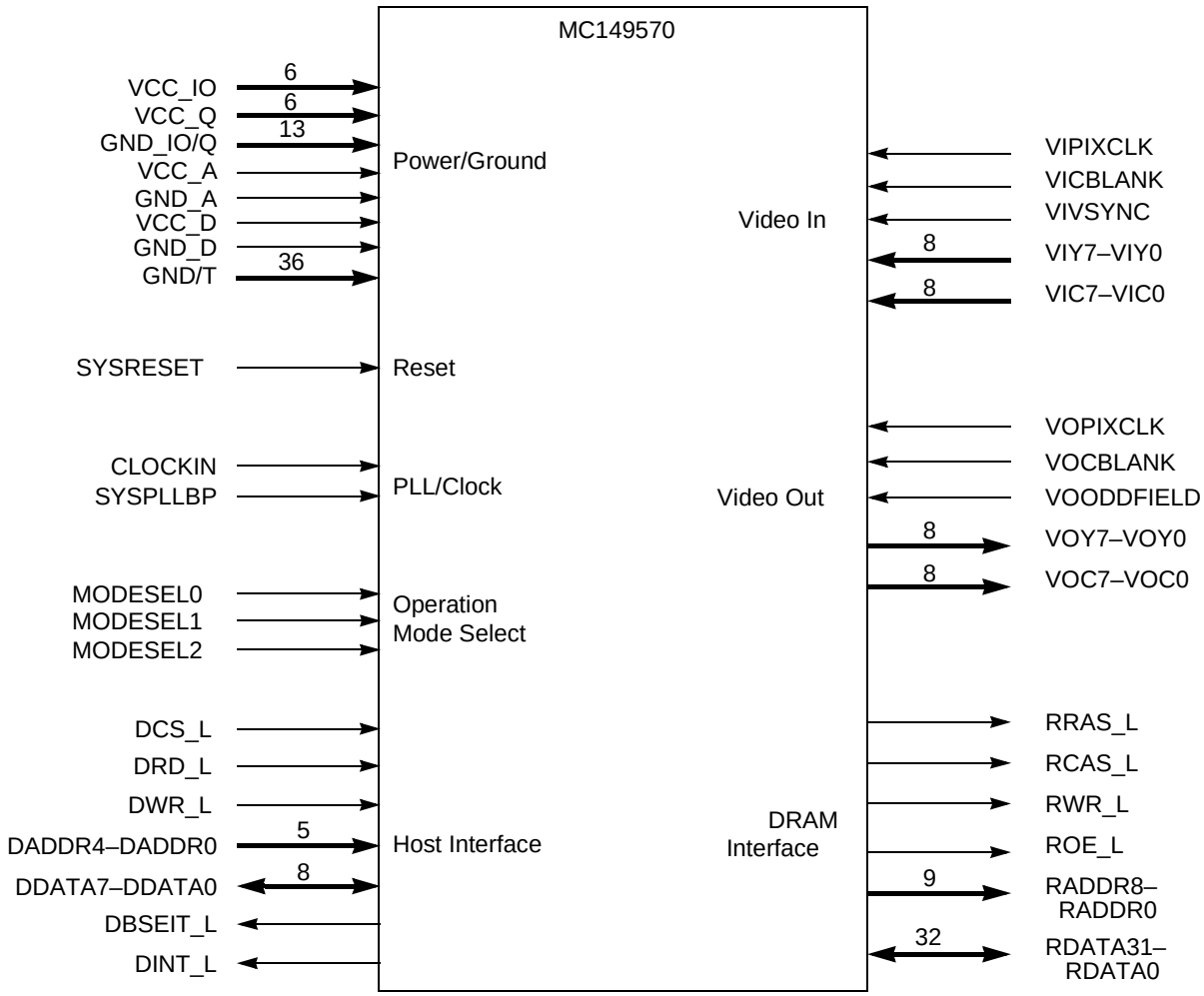


Figure 1-1. MC149570 Signals Identified by Functional Group

1.2 Power and Ground Signals

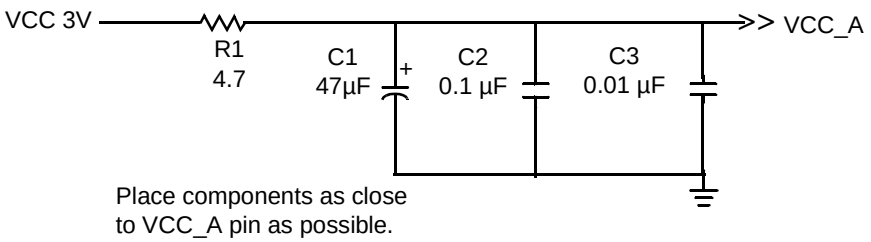
Table 1-2. MC149570 Power and Ground Signals

Signal Name	Description
VCC_IO	I/O Power
VCC_Q	Core Power
GND_IO/Q	I/O and Core Ground
VCC_A	PLL Analog Power
GND_A	PLL Analog Ground
VCC_D	PLL Digital Power
GND_D	PLL Digital Ground
GND/T	Thermal Ground

Notes: 1. VCC_IQ, VCC_Q and VCC_D should be connected together on the PCB to a low impedance power source (i.e., a 3.3V power plane).

2. GND_IO, GND_Q, GND_A, GND_D, and GND/T should be connected together on the PCB to a low impedance path to ground (i.e., a ground plane).

3. VCC_A requires special treatment at the PCB level. The power should be connected thru a small resistor or ferrite bead to minimize coupling of digital noise into this pin. In addition, dedicated decoupling caps should be placed as close to the pin as possible. The PCB trace should be wider than normal (e.g., 40 mil) to minimize inductance. Refer to the schematic below:



1.3 Reset Signals

Table 1-3. MC149570 Reset Signal

Signal Name	Signal Type	Detailed Description
SYSRESET	Input[1]	Chip reset

Notes: 1. All inputs are 5 V tolerant.

1.4 PLL and Clock Signals

Table 1-4. MC149570 PLL and Clock Signals

Signal Name	Signal Type	Detailed Description
CLOCKIN	Input[2]	Clock input to the on-chip PLL (default = 20 MHz)
SYSPLLBP	Input[1,2]	Asserting this signal bypasses the on-chip PLL. This pin must be asserted to bypass the PLL before changing the Operation Mode from Normal to the PLL Programming Mode.

Notes: **1.** See **Section 1.5** for information about selecting the Operation Mode and its effect on PLL operation.
2. All inputs are 5 V tolerant.

1.5 Operation Mode Signals

Table 1-5. MC149570 Operation Mode Signals

Signal Name	Signal Type	Detailed Description
MODESEL0–MODESEL2	Input[1]	The MODESEL signals combine to define eight operational modes for normal operations and diagnostics.[2,3,4]

Notes: **1.** All inputs are 5 V tolerant.
2. Two operation modes are available to users:
- Normal Operation Mode (all three signals = 0), and
- PLL Programming Mode (all three signals = 1).

3. In the Normal Operation Mode, the PLL generates a default internal clock frequency of 2.2 times CLOCKIN. For example, if CLOCKIN = 20 MHz, the internal clock frequency is 44 MHz.
4. To change the ratio between CLOCKIN and the internal clock, select the PLL Programming Mode. See the *MC149570 Programming Manual* for information about programming the PLL ratio.

1.6 Host Interface Signals

Table 1-6. MC149570 Host Interface Signals

Signal Name	Signal Type	Detailed Description
DCS_L	Input[1]	Chip select from DSP/controller
DRD_L	Input[1]	Read enable from DSP/controller
DWR_L	Input[1]	Write enable from DSP/controller
DADDR4–DADDR0	Input[1]	DSP/Controller Address bus
DDATA7–DDATA0	Bidirectional[2]	DSP/Controller Interface data bus
DBSEIT_L	Output	DSP/Controller BSE Interrupt
DINT_L	Output	DSP/Controller Interrupt

Notes: 1. All inputs are 5 V tolerant.
2. Bidirectional inputs are 5 V tolerant; bidirectional outputs conform to **Table 3-3**.

1.7 Video Input Signals

Table 1-7. MC149570 Video Input Signals

Signal Name	Signal Type	Detailed Description
VIPIXCLK	Input[1]	Pixel clock
VICBLANK	Input[1]	Composite BLANK
VIVSYNC	Input[1]	Vertical Sync
VIY7–VIY0	Input[1]	Luma data Y in 4:2:2
VIC7–VIC0	Input[1]	Chroma data Cb/Cr

Notes: 1. All inputs are 5 V tolerant.

1.8 Video Output Signals

Table 1-8. MC149570 Video Output Signals

Signal Name	Signal Type	Detailed Description
VOPIXCLK	Input[1]	Pixel clock
VOCBLANK	Input[1]	Composite BLANK
VOODDFIELD	Input[1]	Odd field select
VOY7–VOY0	Output	Luma data Y in 4:2:2
VOC7–VOC0	Output	Chroma data in 4:2:2

Notes: 1. All inputs are 5 V tolerant.

1.9 DRAM Interface Signals

Table 1-9. MC149570 DRAM Interface Signals

Signal Name	Signal Type	Detailed Description
RRAS_L	Output	Row address strobe to EDO DRAMs
RCAS_L	Output	Column address strobe to EDO DRAMs
RWR_L	Output	Write enable to EDO DRAMs
ROE_L	Output	Output enable for EDO DRAMs
RADDR8–RADDR0	Output	Address bus to EDO DRAMs
RDATA31–RDATA0	Bidirectional[1]	Memory data bus

Notes: 1. Bidirectional inputs are 5 V tolerant; bidirectional outputs conform to **Table 3-3**.

2

Signal and Packaging Information

2.1 Introduction

This section provides information on packaging, including a diagram of the package with signals, and a table showing how the signals described in **Section 1** are allocated. See **Figure 2-1** for the signal name and location information. The MC149570 is available in a 292-position Plastic Ball Grid Array (PBGA) package. See **Figure 2-2** for package details.

Detailed package drawing for this device is also available on the Motorola web page at:

http://mot-sps.com/cgi-bin/cases

Use package 1135C-01 for the search.

2.2 PBGA Package Description

A PBGA package top view is shown in **Figure 2-1** with signal and location designators.

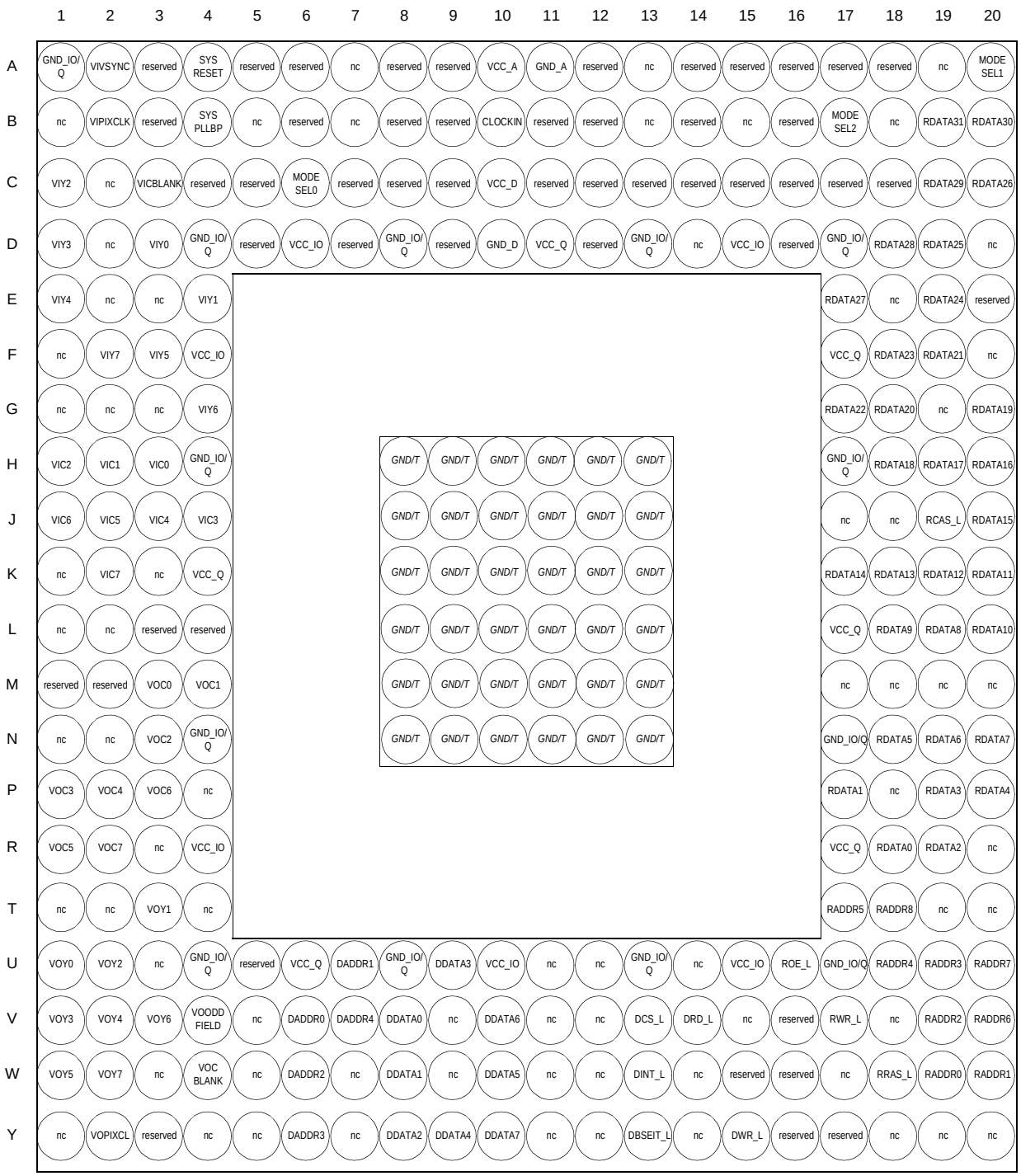


Figure 2-1. MC149570 292-Position PBGA Diagram

NOTE: Locations marked as *reserved* must not be connected.

Table 2-1. MC149570 292-Position PBGA Package Signal List

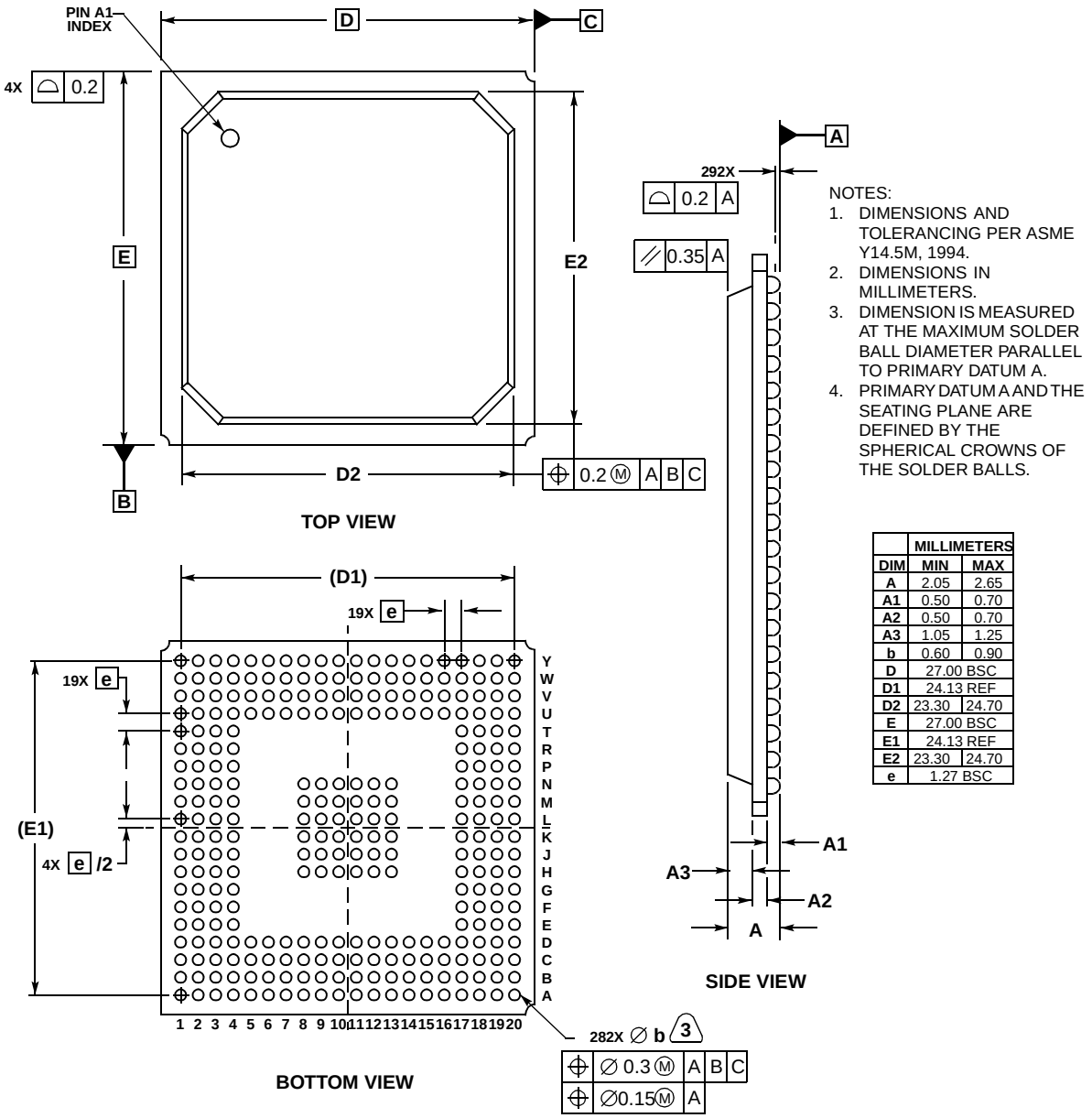
Location	Signal Name	Location	Signal Name	Location	Signal Name	Location	Signal Name
A1	GND_IO/Q	B1	nc	C1	VIY2	D1	VIY3
A2	VIVSYNC	B2	VIPIXCLK	C2	nc	D2	nc
A3	reserved	B3	reserved	C3	VICBLANK	D3	VIY0
A4	SYSRESET	B4	SYSPLLBP	C4	reserved	D4	GND_IO/Q
A5	reserved	B5	nc	C5	reserved	D5	reserved
A6	reserved	B6	reserved	C6	MODESEL0	D6	VCC_IO
A7	nc	B7	nc	C7	reserved	D7	reserved
A8	reserved	B8	reserved	C8	reserved	D8	GND_IO/Q
A9	reserved	B9	reserved	C9	reserved	D9	reserved
A10	VCC_A	B10	CLOCKIN	C10	VCC_D	D10	GND_D
A11	GND_A	B11	reserved	C11	reserved	D11	VCC_Q
A12	reserved	B12	reserved	C12	reserved	D12	reserved
A13	nc	B13	nc	C13	reserved	D13	GND_IO/Q
A14	reserved	B14	reserved	C14	reserved	D14	nc
A15	reserved	B15	nc	C15	reserved	D15	VCC_IO
A16	reserved	B16	reserved	C16	reserved	D16	reserved
A17	reserved	B17	MODESEL2	C17	reserved	D17	GND_IO/Q
A18	reserved	B18	nc	C18	reserved	D18	RDATA28
A19	nc	B19	RDATA31	C19	RDATA29	D19	RDATA25
A20	MODESEL1	B20	RDATA30	C20	RDATA26	D20	nc

Table 2-1. MC149570 292-Position PBGA Package Signal List (Continued)

Location	Signal Name	Location	Signal Name	Location	Signal Name	Location	Signal Name
E1	VIY4	H9	GND/T	K10	GND/T	M11	GND/T
E2	nc	H10	GND/T	K11	GND/T	M12	GND/T
E3	nc	H11	GND/T	K12	GND/T	M13	GND/T
E4	VIY1	H12	GND/T	K13	GND/T	M17	nc
E17	RDATA27	H13	GND/T	K17	RDATA14	M18	nc
E18	nc	H17	GND_IO/Q	K18	RDATA18	M19	nc
E19	RDATA24	H18	RDATA18	K19	RDATA12	M20	nc
E20	reserved	H19	RDATA17	K20	RDATA11	N1	nc
F1	nc	H20	RDATA16	L1	nc	N2	nc
F2	VIY7	J1	VIC6	L2	nc	N3	VOC2
F3	VIY5	J2	VIC5	L3	reserved	N4	GND_IO/Q
F4	VCC_IO	J3	VIC4	L4	reserved	N8	GND/T
F17	VCC_Q	J4	VIC3	L8	GND/T	N9	GND/T
F18	RDATA23	J8	GND/T	L9	GND/T	N10	GND/T
F19	RDATA21	J9	GND/T	L10	GND/T	N11	GND/T
F20	nc	J10	GND/T	L11	GND/T	N12	GND/T
G1	nc	J11	GND/T	L12	GND/T	N13	GND/T
G2	nc	J12	GND/T	L13	GND/T	N17	GND_IO/Q
G3	nc	J13	GND/T	L17	VCC_Q	N18	RDATA5
G4	VIY6	J17	nc	L18	RDATA9	N19	RDATA6
G17	RDATA22	J18	nc	L19	RDATA8	N20	RDATA7
G18	RDATA20	J19	RCAS_L	L20	RDATA10	P1	VOC3
G19	nc	J20	RDATA15	M1	reserved	P2	VOC4
G20	RDATA19	K1	nc	M2	reserved	P3	VOC6
H1	VIC2	K2	VIC7	M3	VOC0	P4	nc
H2	VIC1	K3	nc	M4	VOC1	P17	RDATA1
H3	VIC0	K4	VCC_Q	M8	GND/T	P18	nc
H4	GND_IO/Q	K8	GND/T	M9	GND/T	P19	RDATA3
H8	GND/T	K9	GND/T	M10	GND/T	P20	RDATA4

Table 2-1. MC149570 292-Position PBGA Package Signal List (Continued)

Location	Signal Name	Location	Signal Name	Location	Signal Name	Location	Signal Name
R1	VOC5	U9	DDATA3	V13	DCS_L	W17	nc
R2	VOC7	U10	VCC_IO	V14	DRD_L	W18	RRAS_L
R3	nc	U11	nc	V15	nc	W19	RADDR0
R4	VCC_IO	U12	nc	V16	reserved	W20	RADDR1
R17	VCC_Q	U13	GND_IO/Q	V17	RWR_L	Y1	nc
R18	RDATA0	U14	nc	V18	nc	Y2	VOPIXCL
R19	RDATA2	U15	VCC_IO	V19	RADDR2	Y3	reserved
R20	nc	U16	ROE_L	V20	RADDR6	Y4	nc
T1	nc	U17	GND_IO/Q	W1	VOY5	Y5	nc
T2	nc	U18	RADDR4	W2	VOY7	Y6	DADDR3
T3	VOY1	U19	RADDR3	W3	nc	Y7	nc
T4	nc	U20	RADDR7	W4	VOCBLANK	Y8	DDATA2
T17	RADDR5	V1	VOY3	W5	nc	Y9	DDATA4
T18	RADDR8	V2	VOY4	W6	DADDR2	Y10	DDATA7
T19	nc	V3	VOY6	W7	nc	Y11	nc
T20	nc	V4	VOODD FIELD	W8	DDATA1	Y12	nc
U1	VOY0	V5	nc	W9	nc	Y13	DBSEIT_L
U2	VOY2	V6	DADDR0	W10	DDATA5	Y14	nc
U3	nc	V7	DADDR4	W11	nc	Y15	DWR_L
U4	GND_IO/Q	V8	DDATA0	W12	nc	Y16	reserved
U5	reserved	V9	nc	W13	DINT_L	Y17	reserved
U6	VCC_Q	V10	DDATA6	W14	nc	Y18	nc
U7	DADDR1	V11	nc	W15	reserved	Y19	nc
U8	GND_IO/Q	V12	nc	W16	reserved	Y20	nc



NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO PRIMARY DATUM A.
4. PRIMARY DATUM A AND THE SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	2.05	2.65
A1	0.50	0.70
A2	0.50	0.70
A3	1.05	1.25
b	0.60	0.90
D	27.00 BSC	
D1	24.13 REF	
D2	23.30	24.70
E	27.00 BSC	
E1	24.13 REF	
E2	23.30	24.70
e	1.27 BSC	

CASE 1135C-01
ISSUE O

DATE 11/06/97

Figure 2-2. 292-Pin PBGA Package Details

3

Specifications

3.1 Introduction

The MC149570 specifications are preliminary and are from design simulations. They may not be fully tested or guaranteed at this early stage of the product life cycle. Finalized specifications will be published after full characterization and device qualifications are complete.

3.2 Maximum Ratings

Table 3-1. Power and Temperature Ratings

Rating	Symbol	Value	Unit
Supply voltage	V_{CC}	–0.3 to +4.0	V
All input voltage	V_{IN}	0 to 5.5	V
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature	T_{STG}	–55 to +150	°C

Note: Absolute maximum ratings are stress ratings only and functional operation at the maximum limits is not guaranteed. Stress beyond the maximum rating may affect device reliability or cause permanent damage to the device.

3.3 Thermal Characteristics

Table 3-2. Package Thermal Characteristics

Characteristic	Symbol	Value	Unit
Junction to Ambient Thermal Resistance	θ_{JA}	24	°C/W

3.4 DC Electrical Characteristics

Table 3-3. DC Electrical Characteristics

Characteristics	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Input High Voltage	V_{IH}	2.0	—	5.5	V
Input Low Voltage	V_{IL}	0	—	0.8	V
Output High Voltage • DDATA7–DDATA0, RCAS_L (I_{OH} = -8mA) • RDATA31–RDATA0, RADDR8–RADDR0, ROE_L, RRAS_L, RWR_L (I_{OH} = -4 mA) • VOC7–VOC0, VOY7–VOY0, DBSEIT_L, DINT_L (I_{OH} = -2 mA)	V_{OH}	2.4	—	VCC	V
Output Low Voltage • DDATA7–DDATA0, RCAS_L (I_{OL} = 8mA) • RDATA31–RDATA0, RADDR8–RADDR0, ROE_L, RRAS_L, RWR_L (I_{OL} = 4 mA) • VOC7–VOC0, VOY7–VOY0, DBSEIT_L, DINT_L (I_{OL} = 2 mA)	V_{OL}	0	—	0.4	V
Input Leakage Current (@ 5.5V / Maximum V_{CC} / 0.0V)	I_{IN}	–10	—	10(1)	µA
Input Leakage Current (2)(@ Maximum V_{CC} / 0.0V)	I_{IN}	–10	—	100	µA
High Impedance Input Current	I_{tsi}	–10	—	10	µA
Icc in Normal Operation Mode	I_{CC}	—	—	450	mA
Input Capacitance	—	—	9		pF

Notes: **1.** Not including the following 5 input pins with internal pull down resistor:
Mode Select 0, Mode Select 1, Mode Select 2, SYSRESET, SYSPLLBP
2. Input Leakage Current for:
Mode Select 0, Mode Select 1, Mode Select 2, SYSRESET, SYSPLLBP

3.5 AC Electrical Characteristics

The timing waveforms shown in this section are tested with a V_{il} maximum of 0.0 V and V_{ih} minimum of 3.0V for all pins. AC timing specifications, which are referenced to a device input signal, are measured in production with respect to the 50% point of the respective input signal's transition. Output levels are measured with the production test machine V_{ol} and V_{oh} reference levels set at 1.2V and 1.6V, respectively.

3.5.1 MC149570 Chip Reset

MC149570 supports a level-sensitive reset. To generate a chip-level reset, assert the SYSRESET signal. This resets the registers associated with the PLL control. Then, 1 ms later, deassert SYSRESET. Given a 20 MHz CLOCKIN and the default setting for the PLL programming register (F/R register), the MC149570 accepts programmed values 22 CLOCKIN cycles after the falling edge of SYSRESET.

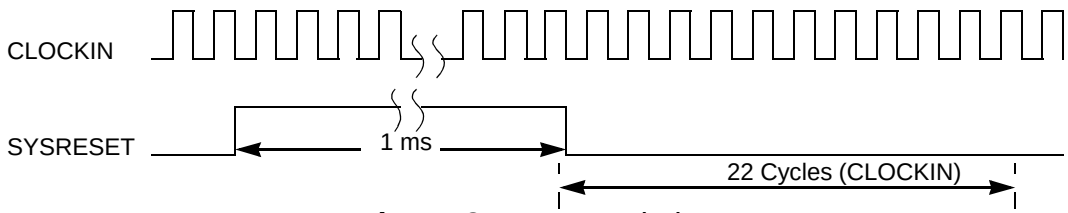


Figure 3-1. *Reset Timing*

3.5.2 PLL Programming Mode

MC149570 enters the PLL Programming mode when the three mode pins (MODESEL0, MODELSEL1, and MODESEL2) are set to all ones (111). In the PLL programming mode, the on-chip PLL is automatically by-passed and the MC149570 runs at half the frequency of CLOCKIN. The on-chip PLL can then be programmed by writing a desired ratio value into the PLL_R_F register ($1F). Note that the ratio of F/R can not be less than 1. Due to a settle time requirement for the PLL, the PLL must stay in this mode for at least 1 mSec after writing to the PLL_R_F register. An internal reset is triggered as soon as MC149570 exits the PLL Programming mode. The internal reset performs the same function as the normal system reset while reserving the new R and F values.

Warning: Performing a normal system reset after exiting the PLL programming mode returns the MC149570 to the default values**.**

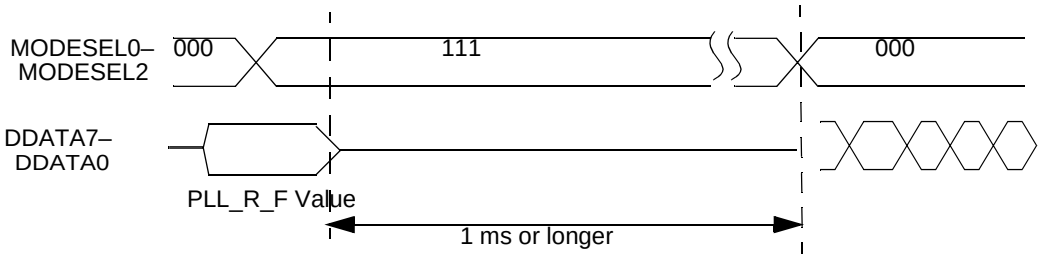


Figure 3-2. *PLL ProgrammingTiming*

3.5.3 Host Interface Write Timings

Table 3-4. Host Interface Write Timings (Host Writes to MC149570)

No.	Characteristics	Min Delay	Max Delay	Units
1	Address valid to Write Enable Deassertion	9	-	ns
2	Write Enable Cycle Time	35	-	ns
3	Write Enable Deassertion Time	3	-	ns
4	Write Data Setup Time w.r.t Write Enable Deassertion	5	-	ns
5	Write Data Hold Time w.r.t. Write Enable Deassertion	2	-	ns
6	Previous Read Enable Deassertion to Write Enable Deassertion	35	-	ns
7	Write Enable Deassertion to Address Not Valid	2	-	ns
8	Chip Select to Write Enable Assertion	0.1	-	ns
9	Write Enable Deassertion to Chip Select Inactive	2	-	ns

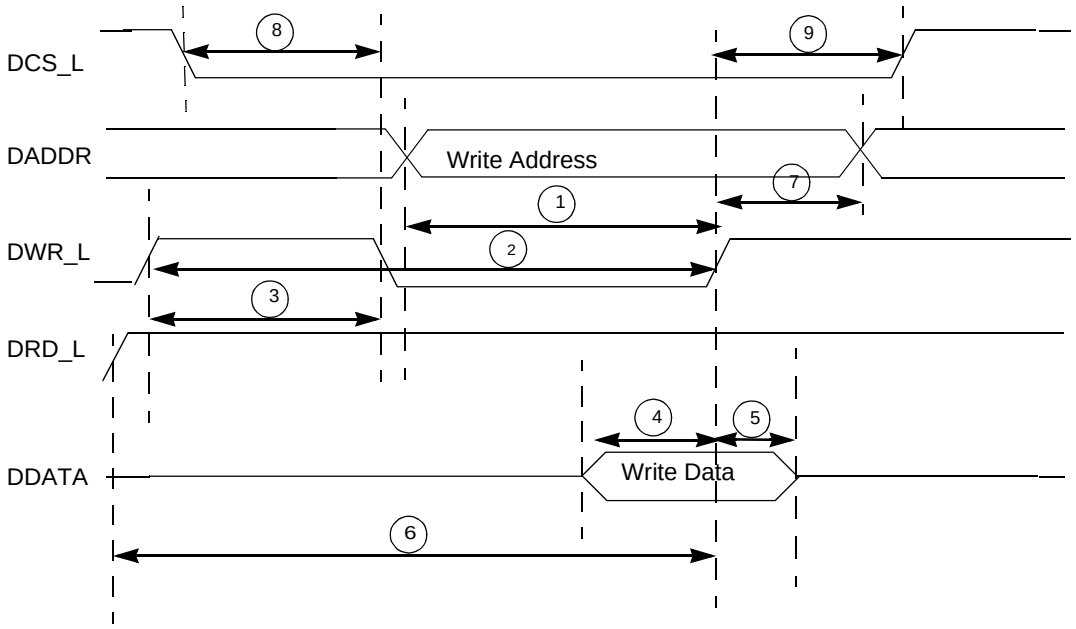


Figure 3-3. *Host Interface Write Timings*

3.5.4 Host Interface Read Timings

Table 3-5. Host Interface Read Timings (Host Read from MC149570)

No.	Characteristics	Min	Max	Units
10	Address valid to Data Active		9	ns
11	Read Enable Cycle Time	35	-	ns
12	Read Enable Deassertion Time	3	-	ns
13	Read Enable Assertion to Data Active		8	ns
14	Read Data Hold Time w.r.t. Read Enable Deassertion	1	6	ns
15	Previous Write Enable Deassertion to Read Enable Deassertion	35	-	ns
16	Read Enable Deassertion to Address Invalid	2	-	ns
17	Chip Select to Read Enable Assertion	0.1	-	ns
18	Read Enable De-assertion to Chip Select Inactive	2	-	ns

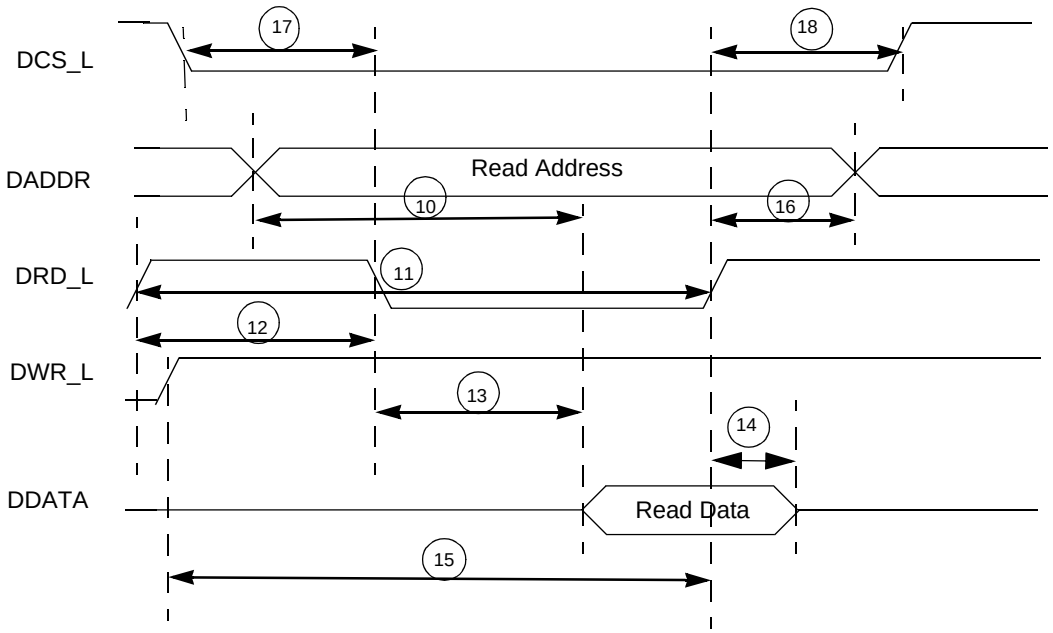


Figure 3-4. *Host Interface Read Timings*

3.5.5 Interrupt Timings

Table 3-6. Periodic Interrupt Latency Timings

Periodical Interrupts	Max. Host Response Time after an Interrupt Request	Minimum Time Between Interrupts	Units
Request for transmit of encoded bitstream (DBSEIT_L)	9	25.7	µs
Request for bits transmitted over channel (DINT_L)	1	33	ms
Request for incoming bitstream(DINT_L)	not limited	25.7	µs

There are no defined limits for non-periodic interrupts, such as:

- Unsupported H.263 options:
  - Unrestricted motion Vectors
  - CPM
  - PB frame
  - Arithmetic coding
- H.261/H.263 errors
  - Invalid Picture Type
  - Illegal Variable Length Code
  - More than 64 coefficients for run-length decode
  - Unexpected start code
  - Incorrect # Macroblocks
- Buffer Underflow/Overflow
  - Bitstream receive buffer
  - Bitstream transmit buffer

3.5.6 Video Signal Timing

Table 3-7. Video Timing

Clock Signals	Frequency	Units
VIPIXCLK, VOPIXCLK	13.5	MHz

Table 3-8. Video Input Timings

No.	Characteristics	Min	Max	Units
19	VIVSYNCH Set-up Time	3	—	ns
20	VIVSYNCH Hold Time	3	—	ns
21	VICBLANK Active and Inactive Set-upTime	6	—	ns
22	VICBLANK Hold Time	3	—	ns
23	Data Set-up Time	3	—	ns
24	Data Hold Time	3	—	ns

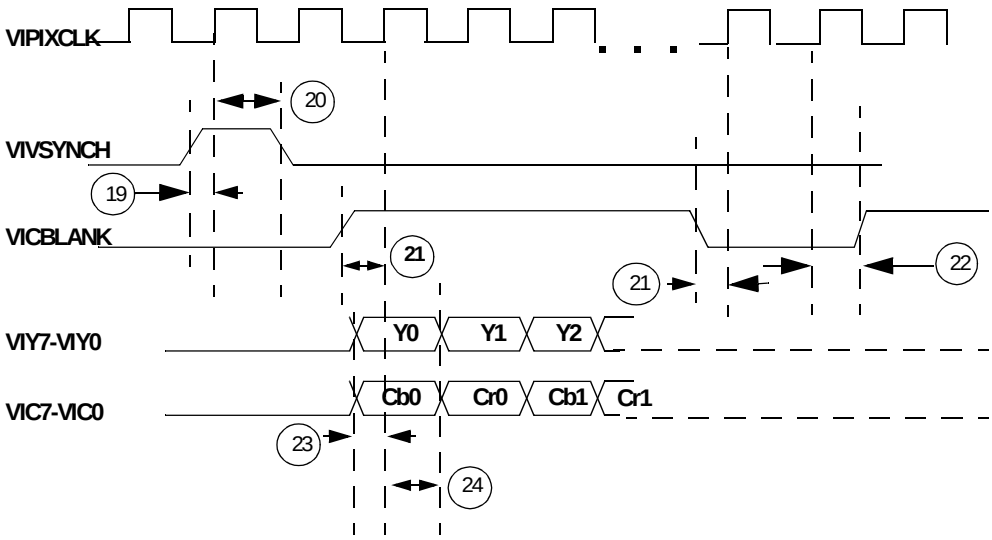


Figure 3-5. *Input Video Signals*

Table 3-9. Video Output Timings

No.	Characteristics	Min Delay	Max Delay	Units
25	VOODDFIELD Set-up Time	13	-	ns
26	VOODDFIELD Hold Time	3	-	ns
27	VOCBLANK Active and Inactive Set-up Time	9		ns
28	VOCBLANK Hold Time	3	-	ns
29	Video Out Data Delay	-	22	ns
30	Video Out Data Hold Time	4	-	ns

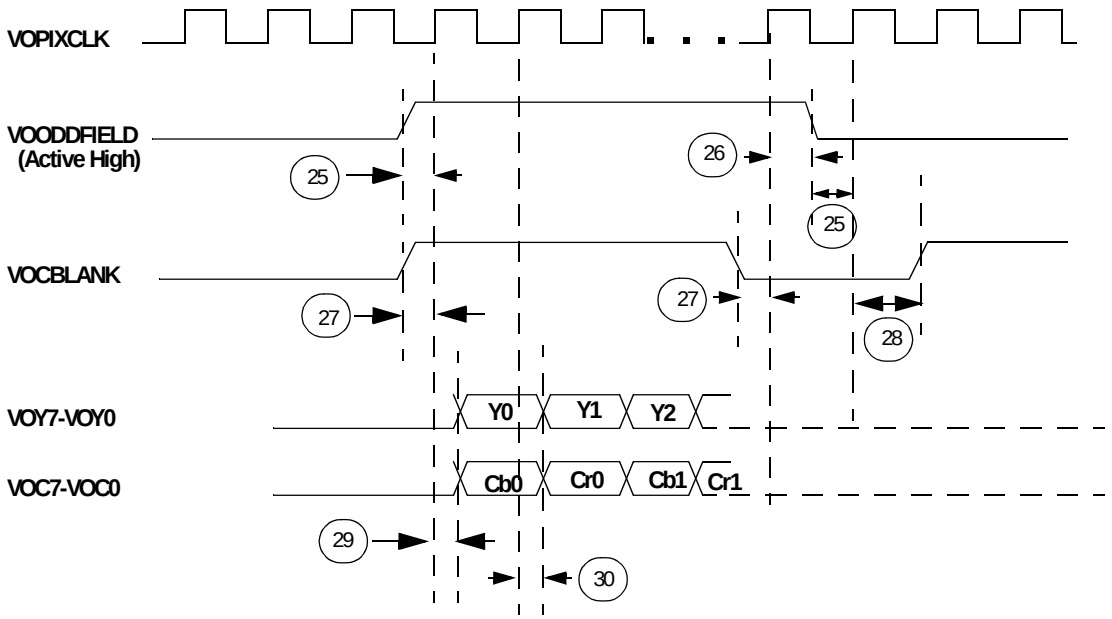


Figure 3-6. *Output Video Signals*

Table 3-10. NTSC/PAL Decode Parameters

Characteristic	Value
VIVSYNC minimum pulse width	1 VIPIXCLK
VICBLANK active video width	720 VIPIXCLKs
NTSC line width	858 VIPIXCLKs
PAL line width	864 VIPIXCLKs
NTSC active lines	240 lines
PAL active lines	288 lines

Table 3-11. NTSC/PAL Encoder Parameters

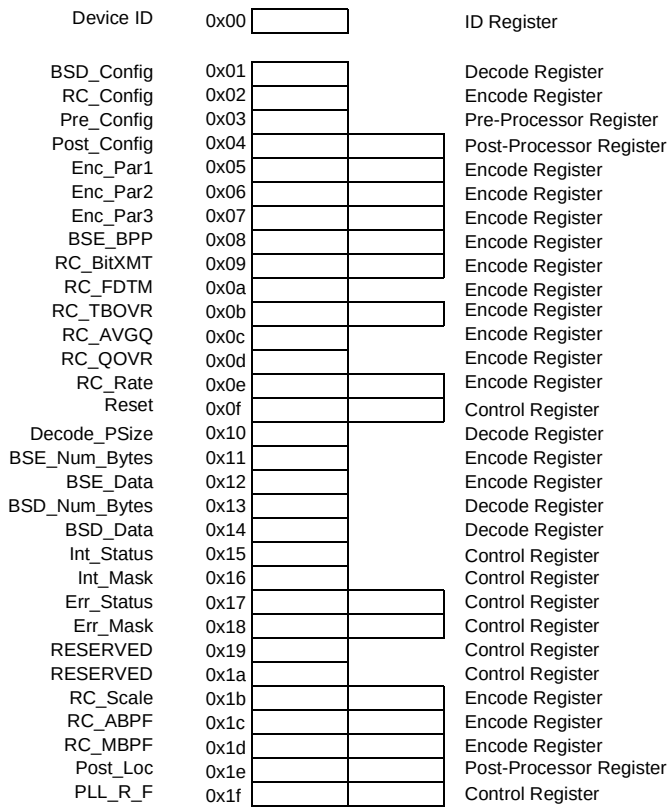
Characteristic	Value
VOCBLANK active video width	720 VOPIXCLKs
NTSC active lines	240 lines
PAL active lines	288 lines

4

Programmability

4.1 Programming Registers

MC149570 has programmable registers as shown in **Figure 4-1**. The registers provide system configurability for the supported major video functions.



For information on programming details, refer to the *MC149570 Programming Manual*

Figure 4-1. MC149570 Configuration Register Layout

4.2 Programmable Features

Table 4-1. MC149570 Programmable Features

Video Processing	Feature	Value
Pre-Processing	Noise Core Filtering	On or Off
	Picture Format to be captured	NTSC or PAL
Post-Processing	Display Format	NTSC or PAL
	Picture Size	*NTSC resolutions:* • CIF: 704 x 480, 528 x 360, 352 x 288 • QCIF: 704 x 480, 528 x 360, 352 x 240, 264 x 180, 176 x 288, 176 x 144 • SubQCIF: 512 x 320, 384 x 240, 256 x 160, 192 x 120, 128 x 192, 128 x 96 *PAL resolutions:* • CIF: 704 x 576, 528 x 432, 352 x 576, 352 x 288 • QCIF: 704 x 576, 528 x 432, 352 x 288, 264 x 216, 176 x 288, 176 x 144 • SubQCIF: 512 x 384, 384 x 288, 256 x 192, 192 x 144, 128 x 192, 128 x 96
	Mosquito Filter Threshold	0–7
	Deblocking Filter	On or Off
	Picture Location Horizontal Adjustment	0–126 pixels move horizontally to the left or right in increments of 2
	Picture Location Vertical Adjustment	0–62 pixels move vertically up or down in increments of 2
	PIP Location	Four locations: upper right, upper left, lower left, and lower right
	Background Color	Four Options: Black, Green, Blue, and Purple
	PIP mirror	On or Off
	Video Bypass/Selfview	On or Off

Table 4-1. MC149570 Programmable Features (Continued)

Video Processing	Feature	Value
Encoding	Encode Resolution	CIF or QCIF
	Bitstream Syntax	H.261 or H.263
	BCH Framing	On or Off
	Advanced Prediction Mode (APM)	On or Off
	Freeze Picture Release	On or Off
	Number of GOB Headers	Four options: every other, every fourth, all, and none
	Adjusted Quantization Target	1–31
	Minimum Picture Interval	0–31
	Intraframe Count	0–31
	Channel Bit Rate	(0–8191) * 64
Decoding	Decoded Picture Resolution[1]	CIF, QCIF, or SubQCIF
	Decoded Picture Bitstream Syntax[1]	H.261 or H.263
	Stop Display on Error	On or Off
	Picture Freeze	On or Off
PLL Programming	Clock Scalability	27 MHz–44 MHz

Notes: 1. *Determined by incoming encoded video bitstream*

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