freescale™ semiconductor

MC34016

Cordless Universal Telephone Interface

The MC34016 is a telephone line interface meant for use in cordless telephone base stations for CT0, CT1, CT2 and DECT. The circuit forms the interface towards the telephone line and performs all speech and line interface functions like dc and ac line termination, 2–4 wire conversion, automatic gain control and hookswitch control. Adjustment of transmission parameters is accomplished by two 8–bit registers accessible via the integrated serial bus interface and by external components.

- DC Masks for Voltage and Current Regulation
- Supports Passive or Active AC Set Impedance Applications
- Double Wheatstone Bridge Sidetone Architecture
- Symmetrical Inputs and Outputs with Large Signal Swing Capability
- Gain Setting and Mute Function for T_X and R_X Amplifiers
- Very Low Noise Performance
- Serial Bus Interface SPI Compatible
- Operation from 3.0 to 5.5 V

FEATURES

Line Driver Architecture

- Two DC Masks for Voltage Regulation
- Two DC Masks for Current Regulation
- Passive or Active Set Impedance Adjustment
- Double Wheatstone Bridge Architecture
- Automatic Gain Control Function

Transmit Channel

- Symmetrical Inputs Capable of Handling Large Voltage Swing
- Gain Select Option via Serial Bus Interface
- Transmit Mute Function, Programmable via Bus
- Large Voltage Swing Capability at the Telephone Line

Receive Channel

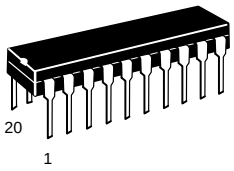
- Double Sidetone Architecture for Optimum Line Matching
- Symmetrical Outputs Capable of Producing High Voltage Swing
- Gain Select Option via Serial Bus Interface
- Receive Mute Function, Programmable via Serial Bus

Serial Bus Interface

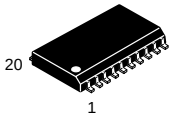
- 3–Wire Connection to Microcontroller
- One Programmable Output Meant for Driving a Hookswitch
- Two Programmable Outputs Capable of Driving Low Ohmic Loads
- Two 8–Bit Registers for Parameter Adjustment

CORDLESS UNIVERSAL TELEPHONE INTERFACE

SEMICONDUCTOR TECHNICAL DATA

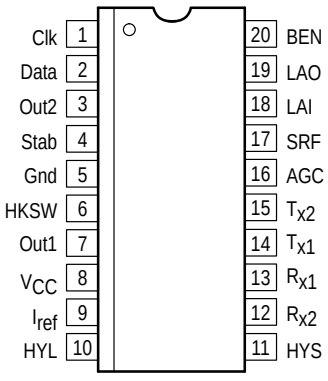


P SUFFIX
PLASTIC PACKAGE
CASE 738



DW SUFFIX
PLASTIC PACKAGE
CASE 751D

PIN CONNECTIONS



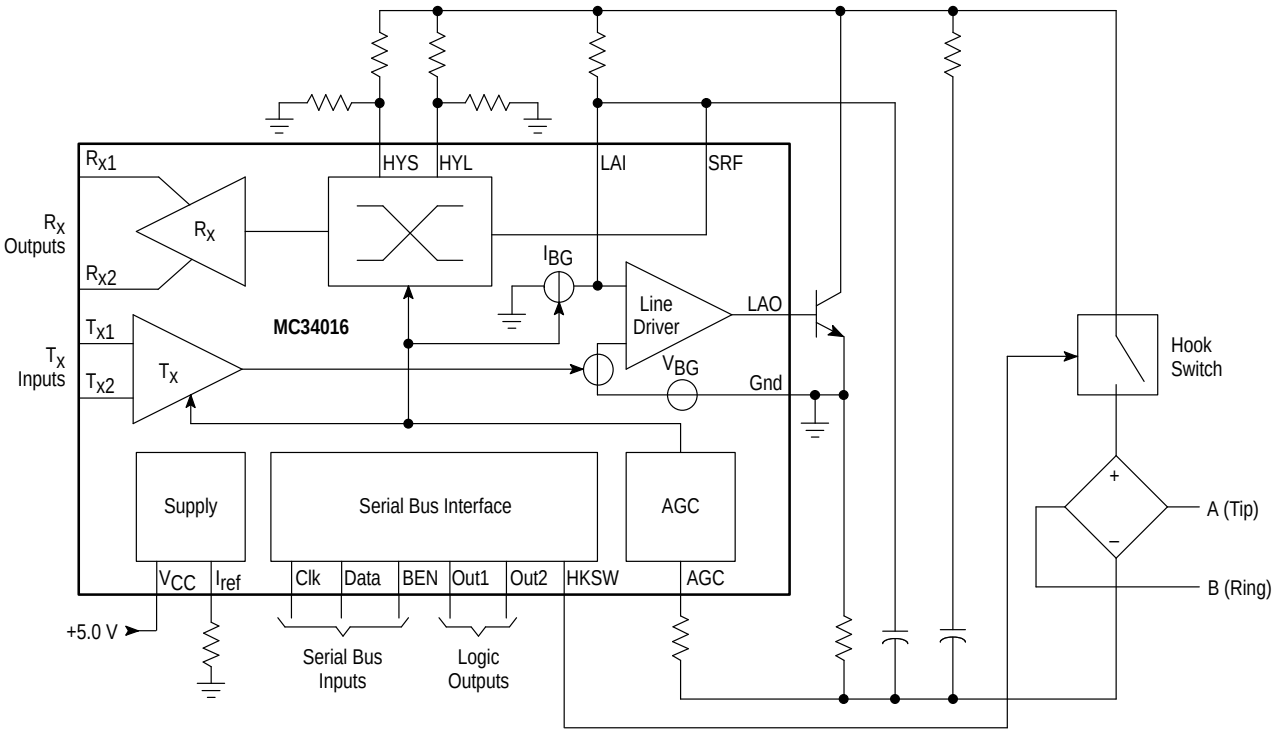
(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC34016P	T_A = –20° to +70°C	DIP
MC34016DW		SO–20

Rev 1

Representative Block Diagram



This device contains 610 active transistors + 242 gates.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Operation Supply Voltage	V_{CC}	–0.5, 6.5	V
All Other Inputs	V_{in}	–0.5, V_{CC} +0.5	V
Operating Ambient Temperature	T_A	–20 to +70	°C
Junction Temperature	T_J	+150	°C

NOTE: ESD data available upon request.

DC ELECTRICAL CHARACTERISTICS (All parameters are specified with Bit 0 of Register 1 set to 1, the rest of the bits in both registers set to 0, T_A = 25°C, V_{CC} = 5.0 V, I_{line} = 15 mA, f = 1.0 kHz, Test Circuit in Figure 9, unless otherwise noted.)

Parameter	Condition	Min	Typ	Max	Unit
VOLTAGE REGULATION					
Line Voltage V_{line}	I_{line} = 5.0 mA I_{line} = 15 mA I_{line} = 60 mA	3.7 4.2 6.6	4.0 4.5 6.85	4.3 4.8 7.1	V
CURRENT REGULATION (Bit 4, Reg.1 = 1; Bit 1, Reg. 2 = 1; R_{AGC} = 47 kΩ)					
Line Voltage V_{line}	I_{line} = 15 mA	4.2	4.5	4.8	V
Line Current I_{line}	V_{line} = 10 V V_{line} = 35 V	– –	35 56	– –	mA
Line Current I_{line} in Protection Mode	V_{line} = 70 V	–	28	–	mA
DC BIASING					
Operating Supply Voltage V_{CC}	–	3.0	–	5.5	V
Current Consumption from V_{CC}	V_{CC} = 3.0 V, all Bits to 0 V_{CC} = 5.0 V, all Bits to 0	– –	3.0 3.5	4.0 4.5	mA
Source Capabiltiy Pin LAO in Speech Mode	V_{LAO} = 0.7 V	–	–	–2.0	mA
Source Capability Pin LAO in Dialing Mode (Bit 5, Reg. 1 = 1)	V_{LAO} = 0.7 V	–	–	–5.0	mA
Internal Pull Down Resistor at Pin LAO	–	–	11	–	kΩ
Bias Voltage at Pins HYL, HYS and LAI	–	–	1.3	–	V
Bias Voltage at Pins T_{x1} and T_{x2}	–	–	1.5	–	V
Bias Voltage at Pins R_{x1} and R_{x2}	–	–	1.3	–	V
LOGIC INPUTS					
Logic Low Level Pins Clk, Data, BEN	–	–	–	0.6	V
Logic High Level Pins Clk, Data, BEN	–	2.2	–	–	V
LOGIC OUTPUTS					
Source Capability from Pins HKSW, Out1, Out2	Output Voltage at V_{CC} – 1.3 V	–	–	–1.0	mA
Sink Capability into Pins HKSW, Out1, Out2	Output Voltage at 0.5 V	5.0	–	–	mA

AC ELECTRICAL CHARACTERISTICS (All parameters are specified with Bit 0 of Register 1 set to 1, the rest of the bits in both registers set to 0, T_A = 25°C, V_{CC} = 5.0 V, I_{line} = 15 mA, f = 1.0 kHz, Test Circuit in Figure 9, unless otherwise noted.)

Parameter	Condition	Min	Typ	Max	Unit
TRANSMIT CHANNEL					
Transmit Gain from VT_X to V_{line}	MC34016P MC34016DW VT_X = 0.1 Vrms	–1.0 –1.25	0.25 –0.20	1.5 0.85	dB
Gain Variation with Line Current Referred to I_{line} = 15 mA with the AGC Function Switched "Off"	I_{line} = 70 mA, Bit 0, Reg. 2 = 1	–0.7	–	0.7	dB
Gain Increase in 6.0 dB Mode	Bit 4, Reg. 2 = 1	5.3	6.0	6.7	dB
Gain Reduction in Mute Condition	Bit 2, Reg. 2 = 1	65	–	–	dB
Input Impedance at T_{x1} or T_{x2}	–	–	30	–	kΩ
Maximum Input Swing for VT_X	THD ≤ 2%	–	4.0	–	Vpp
THD at the Line (V_{line})	VT_X = 3.0 dBm	–	1.0	2.0	%
Psophometrically Weighted Noise Level at the Line (V_{line})	200 Ω Between T_{x1} and T_{x2}	–	–79	–	dBmp
RECEIVE CHANNEL					
Receive Gain from V_{line} to VR_X	V_{line} = 0.1 Vrms	–1.0	0	1.0	dB
Gain Variation with Line Current Referred to I_{line} = 15 mA with the AGC Function Switched "Off"	I_{line} = 70 mA, Bit 0, Reg. 2 = 1	–0.7	–	0.7	dB

AC ELECTRICAL CHARACTERISTICS (continued) (All parameters are specified with Bit 0 of Register 1 set to 1, the rest of the bits in both registers set to 0, T_A = 25°C, V_{CC} = 5.0 V, I_{line} = 15 mA, f = 1.0 kHz, Test Circuit in Figure 9, unless otherwise noted.)

Parameter	Condition	Min	Typ	Max	Unit
RECEIVE CHANNEL					
Gain Increase in 6.0 dB Mode	Bit 5, Reg. 2 = 1	5.3	6.0	6.7	dB
Gain Reduction in Mute Condition	Bit 3, Reg. 2 = 1	70	–	–	dB
Input Impedance at HYL or HYS	–	–	30	–	kΩ
Output Impedance at R_{X1} or R_{X2}	–	–	150	–	Ω
Maximum Input Swing at HYL or HYS	for THD ≤ 2%	–	800	–	mVpp
Maximum Output Swing VR_X	for THD ≤ 10%	–	3.5	–	Vpp
Total Harmonic Distortion at VR_X	V_{line} = 3.0 dBm	–	1.0	2.0	%
Psophometrically Weighted Noise Level at VR_X	200 Ω Between T_{X1} and T_{X2}	–	80	–	µVrms
AUTOMATIC GAIN CONTROL					
Gain Reduction in Transmit and Receive Channel with Respect to I_{line} = 15 mA	I_{line} = 70 mA	5.0	6.0	7.0	dB
Highest Line Current for Maximum Gain	–	–	20	–	mA
Lowest Line Current for Minimum Gain	–	–	60	–	mA
Gain Reduction in Transmit and Receive Channel with Respect to I_{line} = 35 mA	I_{line} = 85 mA, Bit 1, Reg. 2 = 1	5.0	6.0	7.0	dB
Highest Line Current for Maximum Gain	Bit 1, Reg. 2 = 1	–	40	–	mA
Lowest Line Current for Minimum Gain	Bit 1, Reg. 2 = 1	–	80	–	mA
BALANCE RETURN LOSS					
Balance Return Loss with Respect to 600Ω	f = 1.0 kHz	20	–	–	dB
SIDETONE					
Voltage Gain from VT_X to VR_X	I_{line} = 15 mA, Bit 0, Reg. 2 = 1	–	–	–20	dB
SERIAL BUS					
Clock Frequency	–	–	–	550	kHz
BEN Rising Edge Setup Time Before First Clk Rising Edge	See t1 in Timing Diagram	500	–	–	ns
Data Setup Time Before Clk Rising Edge	See t2 in Timing Diagram	500	–	–	ns
Data Hold Time After Clk Rising Edge	See t3 in Timing Diagram	500	–	–	ns
BEN Falling Edge Delay Time After Last Clk Rising Edge	See t4 in Timing Diagram	1.5	–	–	µs
BEN Rising Edge Delay Time After Last BEN Falling Edge	See t5 in Timing Diagram	6.0	–	–	µs
Power Supply Reset Voltage V_{CC}	–	–	2.5	–	V

PIN FUNCTION DESCRIPTION

Pin	Symbol	Description
1	Clk	Serial bus clock input
2	Data	Serial bus data input
3	Out2	Logic output 2
4	Stab	Line driver compensation
5	Gnd	Ground
6	HKSW	Logic output for the hook switch
7	Out1	Logic output 1
8	V_{CC}	Supply input (+5.0 V)
9	I_{ref}	Reference current adjustment
10	HYL	Hybrid input for long lines
11	HYS	Hybrid input for short lines
12	R_{x2}	Receive output 2
13	R_{x1}	Receive output 1
14	T_{x1}	Transmit input 1
15	T_{x2}	Transmit input 2
16	AGC	Automatic gain control input
17	SRF	Sidetone reference input
18	LAI	Line amplifier input
19	LAO	Line amplifier output
20	BEN	Serial bus enable input

DESCRIPTION OF THE CIRCUIT

Throughout this part, please refer to the typical application of Figure 10. The data given in this chapter refers to typical data of the characteristics.

DC OPERATION

For dc, the MC34016 incorporates four different masks which can be selected via the serial bus interface:

Bit 4, Reg. 1 'DC Mask'	Bit 5, Reg. 1 'DC Mode'	Bit 1, Reg. 2 'AGC Ratio'	DC Mask Selected
0	0	X	Voltage Regulation Mask
X	1	X	Pulse Dial Mask
1	0	0	Current Regulation Mask with AGC Ratio 1:2
1	0	1	Current Regulation Mask with AGC Ratio 3:5

X = don't care

Voltage Regulation Mask

The voltage regulation mask is the default setting of the MC34016 after power–up. In this mode, the circuit behaves as a zener with a series resistor. The line voltage can be expressed as:

$$V_{line} = V_{BG} + (I_{BG} \times R_{DC1}) + (I_{line} \times R_S)$$

with: V_{BG} =1.3 V

I_{BG} = 5.2 µA

R_{DC1} = DC setting resistor of 470 kΩ in the typical application

I_{line} = Line current

R_S = Slope resistor of 50 Ω in the typical application

thus: $V_{line} = 3.75 + (50 \times I_{line})$

By choosing different values of R_{DC1}, the zener voltage can be adjusted to fit country specific requirements. In Figure 1, a curve shows V_{line} versus I_{line} for different R_{DC1} values.

Pulse Dial Mask

In this mask, the circuit is forced into a very low voltage drop mode meant for pulse dialing (e.g. make period during pulse dialing). Pin LAO of the MC34016 sources a current of 5.0 mA in this mode, saturating output transistor Q1. The line voltage V_{line} is now determined by the saturation voltage of Q1 and the dc slope resistor R_S:

$$V_{line} = V_{CE(sat)Q1} + (R_S \times I_{line}) \cong 0.1 + (50 \times I_{line})$$

Figure 2 shows V_{line} versus I_{line}.

Current Regulation Masks

These masks are equal to the voltage regulation mask up to a knee current. Above this current, the dc slope changes to a higher value fulfilling requirements such as those in France.

$$V_{line} = 3.75 + (R_S \times I_{line}) \quad \text{for } I_{AGC} < I_{knee}$$

$$V_{line} = [I_{BG} + (2.5 \times (I_{AGC} - I_{knee}))] \times R_{DC1} + [V_{BG} + (R_S \times I_{line})] \quad \text{for } I_{AGC} > I_{knee}$$

with : $I_{AGC} = I_{line} \times \frac{R_S}{R_{AGC}}$

I_{knee} = 21 µA for AGC ratio 1:2
I_{knee} = 31 µA for AGC ratio 3:5

With R_S = 50 Ω and R_{AGC} = 47 kΩ, and the AGC ratio set to 3:5, I_{AGC} will equal I_{knee} at a line current of 29 mA. With the AGC ratio set to 1:2, the knee occurs at 20 mA. Above these line currents, it can be derived that the dc slope of the circuit changes to:

$$R_{Slope} = 2.5 \times \frac{R_S \times R_{DC1}}{R_{AGC}} + R_S$$

With the component values mentioned, a slope of 1300 Ω will occur. Figures 3 and 4 shows V_{line} versus I_{line} in the two current regulation masks for different values of R_{DC1}.

When I_{AGC} reaches 62 µA for AGC ratio 3:5 or 52 µA in case of AGC ratio 1:2, the MC34016 will enter protection mode after about 800 ms. In practice this mode occurs only under overload conditions. In protection mode, the MC34016 decreases the power dissipation in Q1 by drastically increasing the dc slope starting from I_{knee}. This results in a reduced line current which remains practically constant over line voltage. With the equation for Iagc it can be derived that:

AGC ratio	Line Current to Enter Protection Mode	Line Current in Protection Mode
3:5	58 mA	29 mA
1:2	49 mA	20 mA

Once the MC34016 enters protection mode, it remains there until the output HKSW is toggled via Bit 0 of Register 1 (on–hook, off–hook).

Supply Voltage V_{CC}

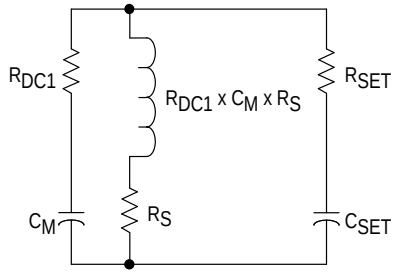
The MC34016 operates from an external supply within a voltage range of 3.0 to 5.5 V. The current consumption with all bits set to 0, equals 3.0 mA at 3.0 V and 3.5 mA at 5.5 V.

AC SET IMPEDANCE

The MC34016 offers two possibilities for the adjustment of the ac set impedance. Either a passive or an active set impedance can be obtained.

Passive Set Impedance

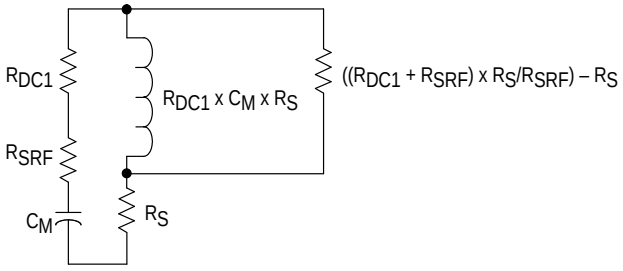
In this application, the set impedance is formed by the ac impedance of the circuit itself in parallel with resistor R_{SET} and capacitor C_{SET}. An equivalent network equals:



With the component values of the typical application, the inductor has a value of about 2.4 H and R_{DC1} equals 470 kΩ. In the audio range of 300–3400 Hz, these components form a fairly large parallel impedance to R_{SET} and C_{SET}. Therefore, the set impedance is mainly determined by the passive network R_{SET} and C_{SET}. In the typical application, R_{SET} is 600 Ω, but it can easily be replaced by a complex network to obtain a complex set impedance.

Active Set Impedance

An active set impedance can be obtained by placing a resistor between pin LAI and SRF (R_{SRF}) as shown in Figure 11. By doing so, the MC34016 itself generates the ac set impedance and R_{SET} and C_{SET} can be omitted. An equivalent network now equals:



Ignoring the effect of the inductor and the parallel path R_{DC1} + R_{SRF} again for audio frequencies, the set impedance is now determined by:

$$Z_{SET} = \frac{R_S}{R_{SRF}} \times (R_{DC1} + R_{SRF})$$

With R_S = 50 Ω and R_{DC1} = 470 kΩ, R_{SRF} should be 43 kΩ to obtain a 600 Ω set impedance. To obtain a complex set impedance, R_{DC1} can be made complex. In such case, the dc mask can be adjusted with the dc value of R_{DC1} and the set impedance can be adjusted with the ac value of R_{DC1}. An application with an active set impedance is interesting, particularly in countries like France, where with the dc current regulation mask, rather high line voltages can be reached. With a passive set impedance, this would result in a high cost for capacitor C_{SET}.

TRANSMIT CHANNEL

Inputs

The inputs T_{X1} and T_{X2} are designed to handle large signal levels of up to +3.0 dBm. The input impedance for both T_{X1} and T_{X2} equals 30 kΩ. The inputs are designed for symmetrical as well as asymmetrical use. In asymmetrical drive, one input can be tied to Gnd via an external capacitor.

Gain

The gain from inputs T_{X1} and T_{X2} to the line is dependent on the set impedance, the line load impedance and dc slope resistor R_S in the following way:

$$A_{TX} = \frac{1}{6 \times R_S} \times \frac{Z_{SET} \times Z_{line}}{Z_{SET} + Z_{line}}$$

With Z_{SET} = 600 Ω, Z_{line} = 600 Ω and R_S = 50 Ω the gain equals 0 dB. By setting Bit 4 of Register 2 to 1, the gain is raised by 6.0 dB.

Outputs

In order to transmit signals to the line, the output stage of the MC34016 (line driver) modulates the zener previously described. To guarantee stability of the output stage capacitor C_{STB} of 100 pF is required

SIDETONE

The MC34016 is equipped with a double Wheatstone bridge architecture to optimize sidetone. One sidetone network is used for short lines and one for long lines. Switchover between both networks is dependent on line current and is described in the automatic gain control section. Different sidetone equations apply depending on whether a passive or an active set impedance is set.

Sidetone Cancellation with Passive Set Impedance

In a passive set impedance application, the set impedance is a part of the equations for optimum sidetone. For short lines optimum cancellation occurs if:

$$Z_{HS1} = \frac{R_{HS2}}{R_S} \times \frac{Z_{SET} \times Z_{lineshort}}{Z_{SET} + Z_{lineshort}}$$

with: $Z_{lineshort}$ = impedance of a short telephone line

and for long lines:

$$Z_{HL1} = \frac{R_{HL2}}{R_S} \times \frac{Z_{SET} \times Z_{linelong}}{Z_{SET} + Z_{linelong}}$$

with: $Z_{linelong}$= impedance of a long telephone line

Sidetone Cancellation with Active Set Impedance

In the active set impedance application, the set impedance does not appear in the equations for optimum sidetone cancellation as it does in the passive application. For short lines, optimum cancellation occurs if:

$$Z_{HS1} = \frac{R_{HS2}}{R_S} \times Z_{lineshort}$$

and for long lines:

$$Z_{HL1} = \frac{R_{HL2}}{R_S} \times Z_{linelong}$$

RECEIVE CHANNEL

Inputs

The inputs HYS and HYL have an input resistance of 30 kΩ and can handle signals up to 800 mVpp. This corresponds to a signal at the telephone line of about 8.0 dBm in the typical application. The switchover from HYS to HYL is dependent on line current and described in the automatic gain control section.

Gain

The overall gain from the line to the outputs R_{X1} and R_{X2} for short lines and passive impedance equals:

$$A_{RX} = 7.6 \times \frac{R14'}{R14' + Z_{HYS}}$$

For active impedance it follows:

$$A_{RX} = 7.6 \times \frac{R14'}{R14' + Z_{HYS}} \times \left(1 + \frac{R1 \times Z_{HYS}}{R14 \times Z_{SET}}\right)$$

In these relations, R14′ is the resistor R14 in parallel with the input impedance at HYS of 30 kΩ. The gain for long lines can be derived by replacing Z_{HYS} and R14 by Z_{HYL}

and R17. With R14 = 3.0 kΩ and Z_{HYS} = 18 kΩ the receive gain equals 0 dB for the passive impedance application.

Outputs

The outputs R_{X1} and R_{X2} of the receive channel have an output impedance of 150 Ω and are designed to drive a 10 kΩ resistive load or a 47 nF capacitive load with a 3.5 Vpp swing.

AUTOMATIC GAIN CONTROL

The automatic gain control function (AGC) controls the transmit and receive gains and the switchover for the sidetone networks for short and long lines according to the line current (which represents line length). The effect of AGC on the transmit and receive amplifiers is 6.0 dB at default and it can be disabled via the serial bus. The switchover for the sidetone networks tracks the AGC curves for the transmit and receive amplifier gain. This feature can also be disabled via the serial bus:

Bit 6, Reg. 2 'PABX Mode'	Bit 0, Reg. 2 'AGC Range'	Description
0	0	AGC Gain Range of 6.0 dB, Sidetone Switchover Enabled
0	1	No AGC Gain Range, Sidetone Switchover Enabled
1	0	AGC Range of 6.0 dB, only HYS Input Active, HYL Muted
1	1	No AGC Gain Range, only HYS Input Active, HYL Muted

The ratio between start and stop current for the AGC curves is programmable for both voltage and current regulation mode:

Bit 4, Reg. 1 'DC Mask'	Bit 1, Reg. 2 'AGC Ratio'	AGC Ratio Selected	$I_{AGCstart}$ (μA)	$I_{AGCstop}$ (μA)
0	0	Voltage Regulation, AGC Ratio 1:3	10	31
0	1	Voltage Regulation, AGC Ratio 1:2	21	42
1	0	Current Regulation, AGC Ratio 1:2	21	42
1	1	Current Regulation, AGC Ratio 3:5	31	52

The relation between line current and I_{start} and I_{stop} is given by:

$$I_{linestart} = \frac{R_{AGC}}{R_S} \times I_{AGCstart}$$

$$I_{linestop} = \frac{R_{AGC}}{R_S} \times I_{AGCstop}$$

Figures 5, 6, 7 and 8 show the AGC curves for both voltage regulation and current regulation. In current regulation, the start point for the AGC curves is coupled to the knee point of the dc characteristic, or: $I_{knee} = I_{AGCstart}$.

LOGIC OUTPUT DRIVERS

The MC34016 is equipped with three logic outputs meant to interface to the front end of a telephone. The outputs can be controlled via the serial bus interface. As shown in the characteristics, the logic outputs are capable of sourcing at least 1.0 mA and sinking at least 5.0 mA.

Output HKSW

Output HKSW is dedicated to drive the hookswitch. With HKSW low, the line is opened via Q2 and Q3 and automatically switches off the line driver transistor Q1. This feature guarantees fast dc settling after line breaks occurring during pulse dialing.

Outputs Out1 and Out2

Outputs Out1 and Out2 may be used for any logic function, such as control of an earth switch and/or a shunt wire.

SERIAL BUS INTERFACE

The serial interface of the MC34016 enables a simple three wire connection to a micro controller.

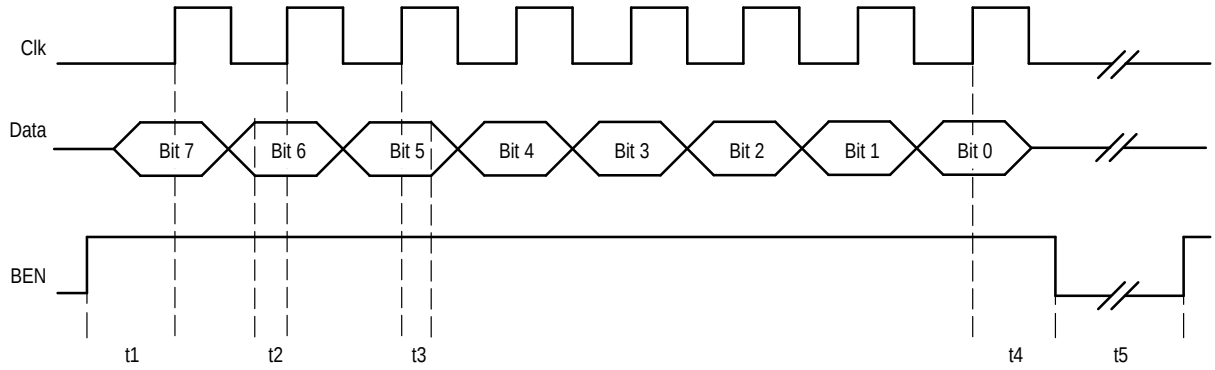
Timing

Times t1, t2, t3, t4 and t5 are specified in the electrical characteristics.

With BEN high, data can be clocked into the serial port by using Data and Clk lines. On the rising edge of the Clk, the data enters the MC34016. The last 8–bits of data entered are shifted into the registers when BEN is forced low. With BEN low, the serial port of the MC34016 is disabled. BEN must be kept low until the next register update is needed. Data should be written by entering the most significant bit first (Bit 7) and the least significant bit (Bit 0) last.

With BEN low, the Data and Clk lines may be used to control other devices in the application.

Timing Diagram



Registers

The MC34016 is equipped with two 8–bit registers which are selected by the value of the most significant bit (Bit 7). If the supply voltage of the MC34016 drops below 2.5 V, all registers are set to 0. This RESET function enables a smooth power–up of the device. The registers are as follows:

Register 1 (Bit 7 = 0)

Bit	Function	Operation	Default
0	Output HKSW	0: HKSW is Low 1: HKSW is High	0
1	Output Out1	0: Out1 is Low 1: Out1 is High	0
2	Output Out2	0: Out2 is Low 1: Out2 is High	0
3	Not Used	–	–
4	DC Mask	0: Voltage Regulation Mask 1: Current Regulation Mask for France	0
5	DC Mode	0: Speech Mode/Normal Operation 1: Dialing Mode for Low Voltage Drop	0
6	Test Mode	Only Used During Manufacturing	0

Register 2 (Bit 7 = 1)

Bit	Function	Operation		Default
0	AGC Range	0: AGC Range 6.0 dB 1: AGC Range 0 dB (Switched “Off”)		0
1	AGC Ratio	Voltage Regulation: (Bit 4, Reg. 1 = 0) 0: Ratio 1:3 1: Ratio 1:2	Current Regulation: (Bit 4, Reg. 1 = 1) 0: Ratio 1:2 1: Ratio 3:5	0
2	Transmit Mute	0: Transmit Channel Active 1: Transmit Channel Muted		0
3	Receive Mute	0: Receive Channel Active 1: Receive Channel Muted		0
4	Transmit Gain	0: Transmit Channel Gain = 0 dB 1: Transmit Channel Gain = 6.0 dB		0
5	Receive Gain	0: Receive Channel Gain = 0 dB 1: Receive Channel Gain = 6.0 dB		0
6	PABX Mode	0: Normal Mode 1: PABX Mode (only Input HYS Selected)		0

Figure 1. Line Voltage versus Line Current
(Voltage Regulation Mask)

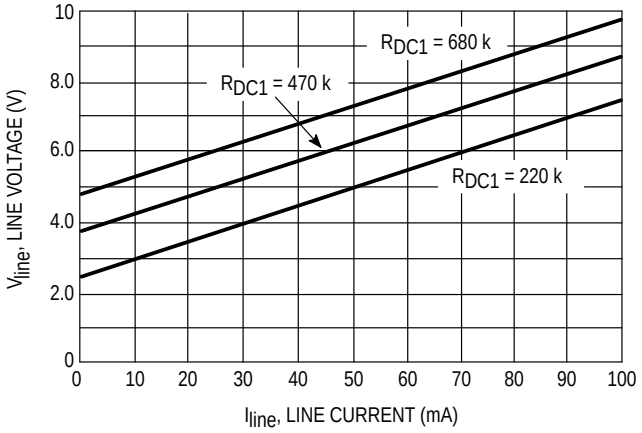


Figure 2. Line Voltage versus Line Current
(Pulse Dial Mask)

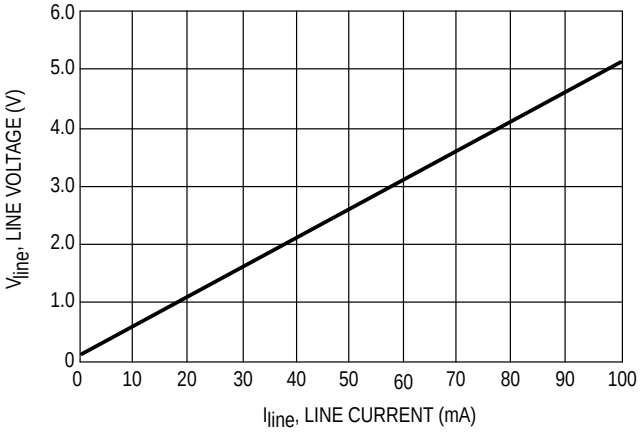


Figure 3. Line Voltage versus Line Current
(Current Regulation Mask)

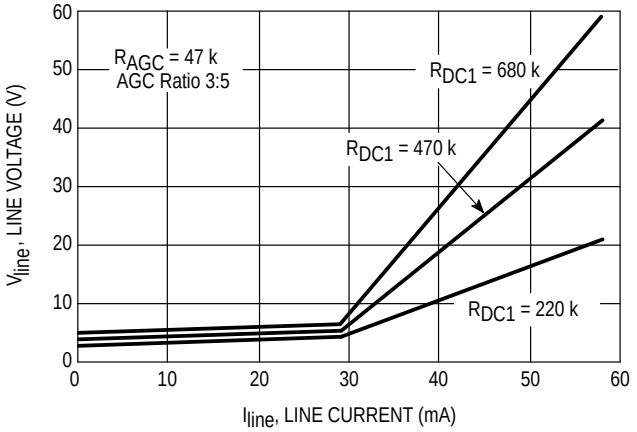


Figure 4. Line Voltage versus Line Current
(Current Regulation Mask)

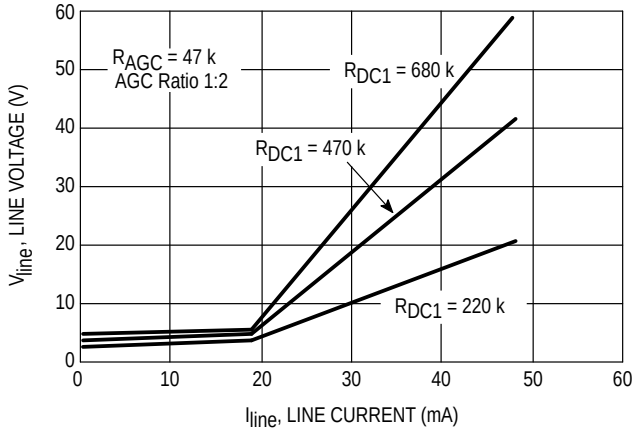


Figure 5. AGC Weighting Factor versus I_{line}
(Voltage Regulation Mask)

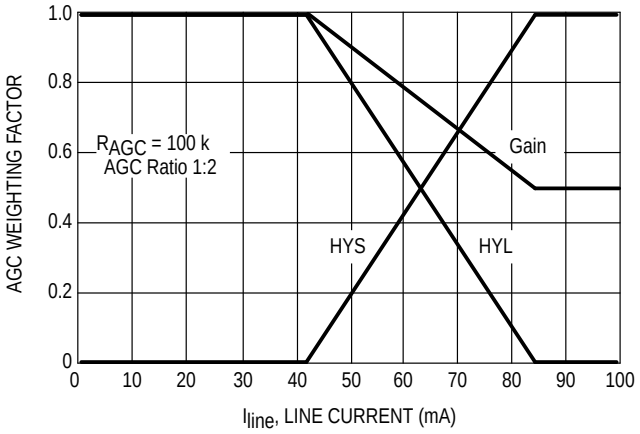


Figure 6. AGC Weighting Factor versus I_{line}
(Voltage Retulation Mask)

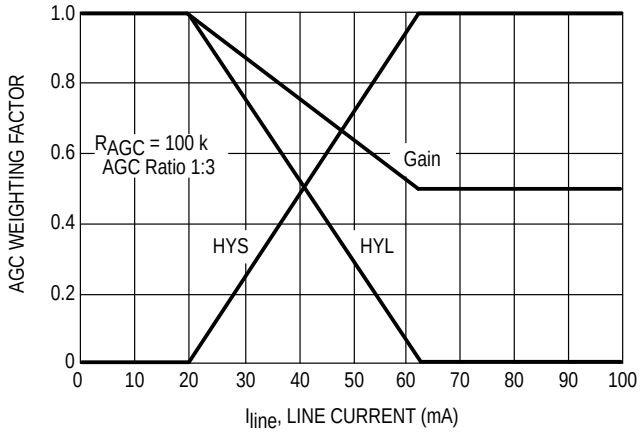


Figure 7. AGC Weighting Factor versus I_{line}
(Current Regulation Mask)

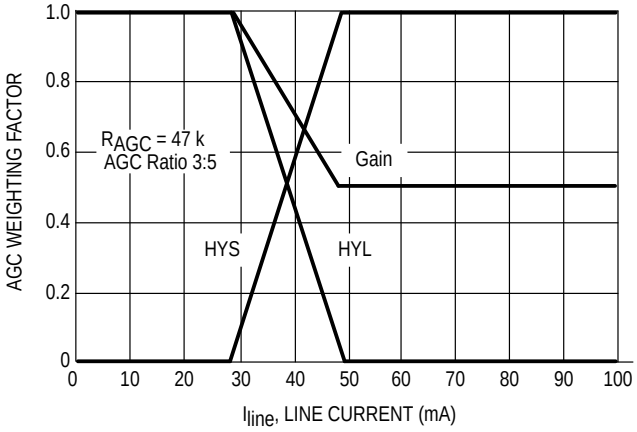


Figure 8. AGC Weighting Factor versus I_{line}
(Currrent Regulation Mask)

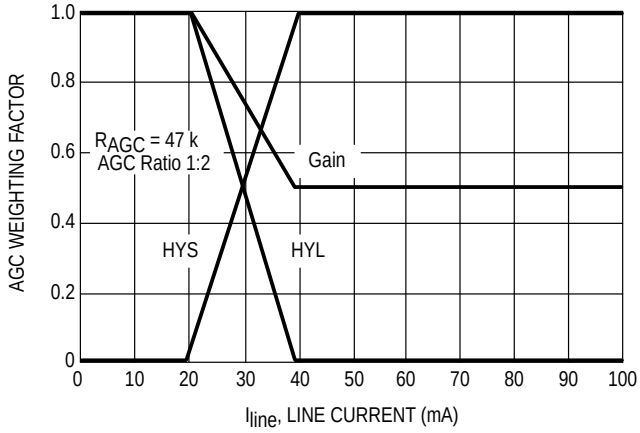


Figure 9. Test Diagram

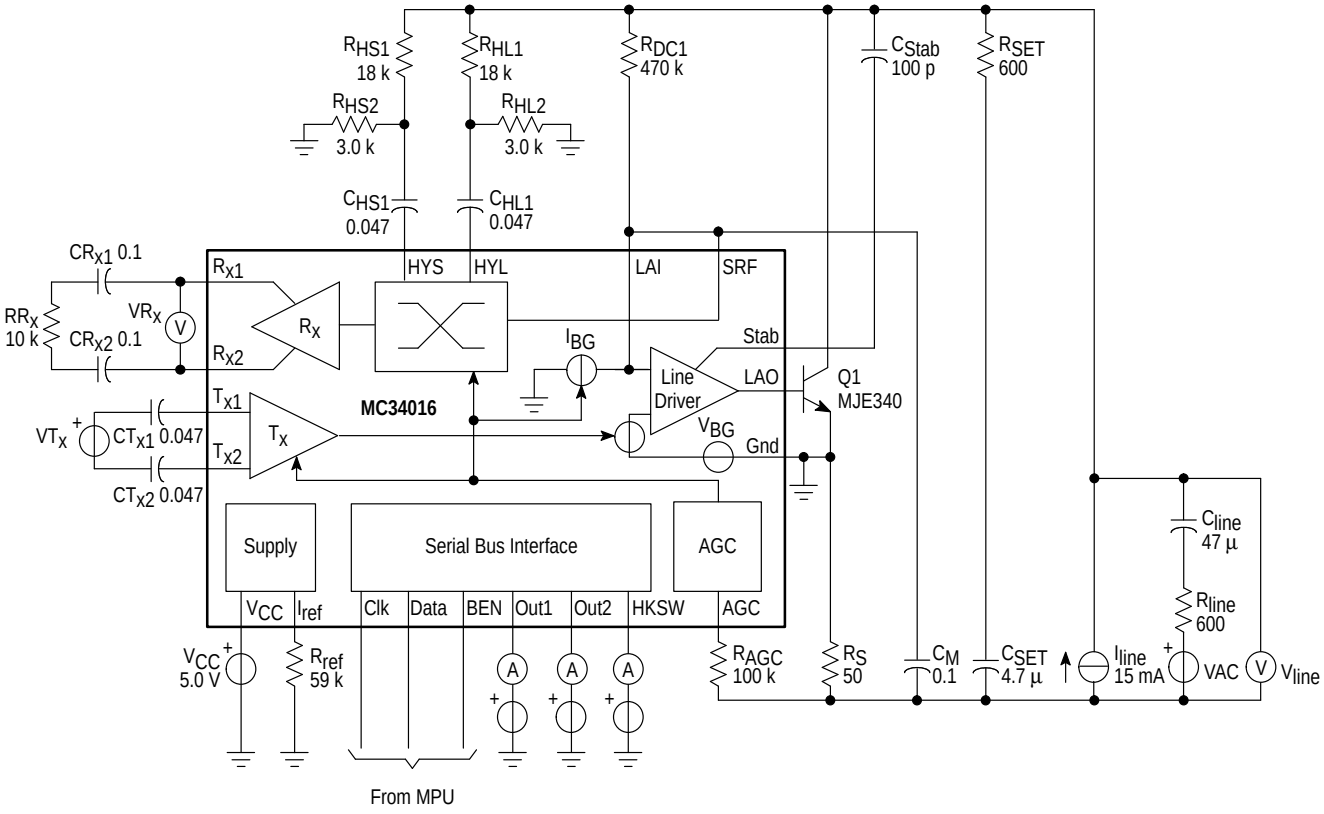
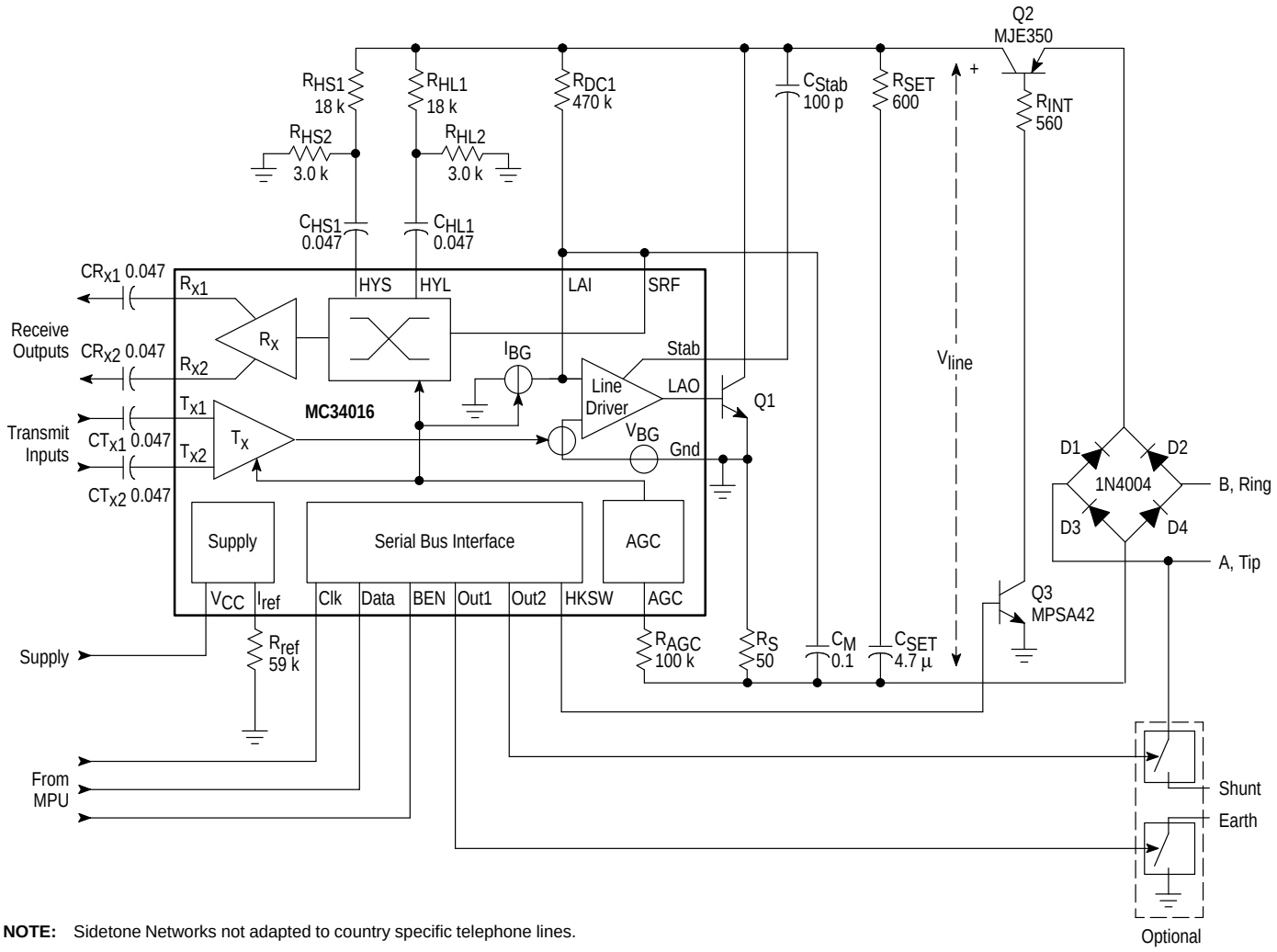
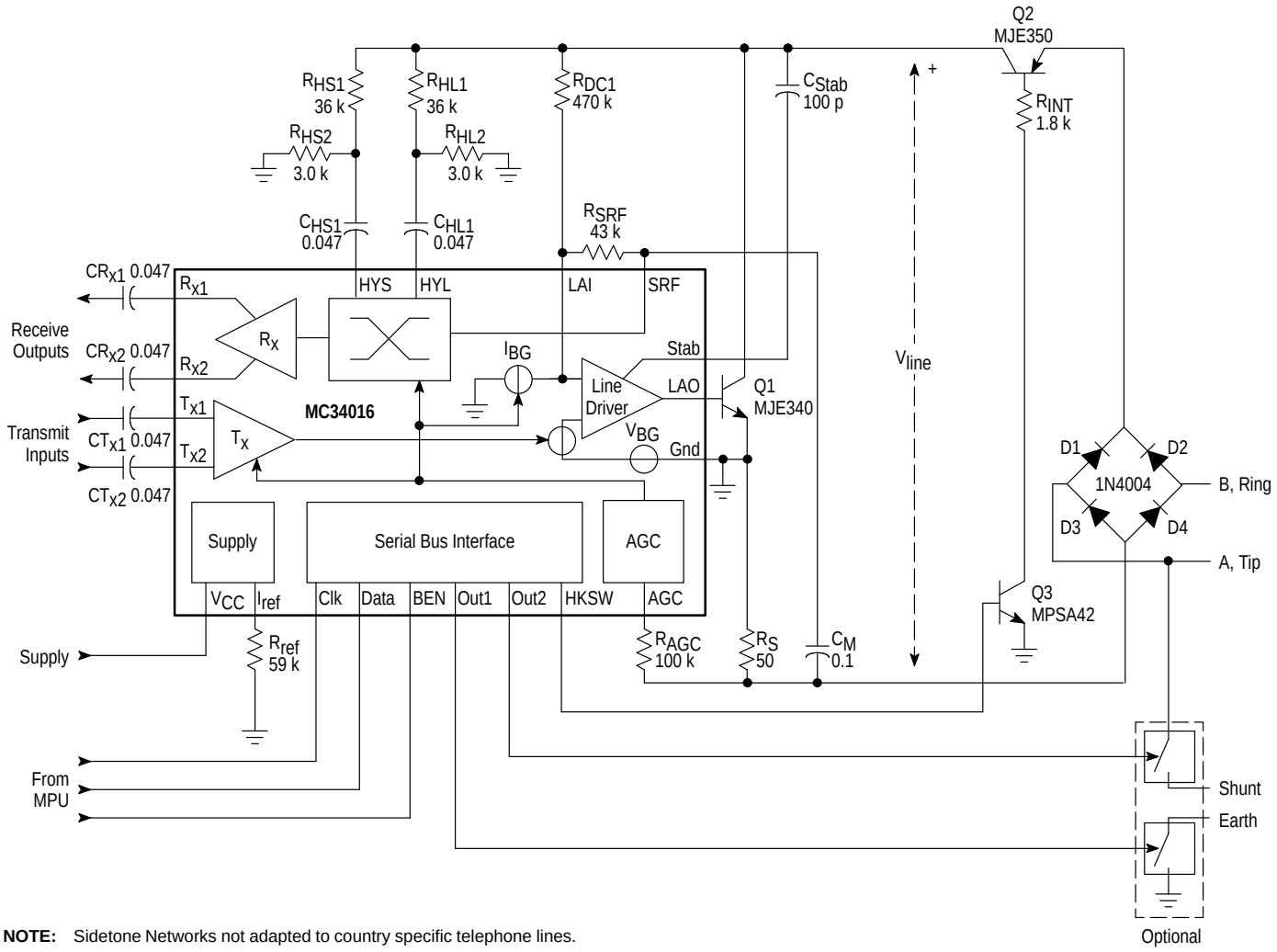


Figure 10. Typical Application with Passive Impedance and Voltage Regulation



NOTE: Sidetone Networks not adapted to country specific telephone lines.

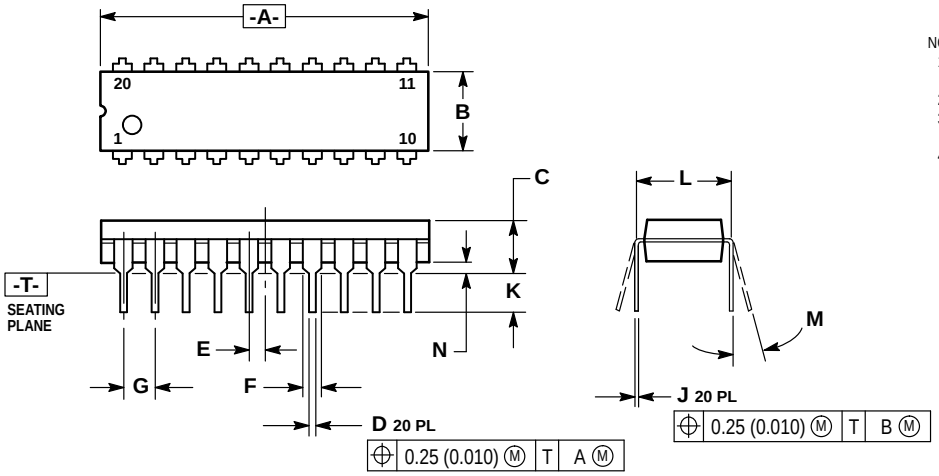
Figure 11. Typical Application with Active Impedance and Current Regulation



NOTE: Sidetone Networks not adapted to country specific telephone lines.

OUTLINE DIMENSIONS

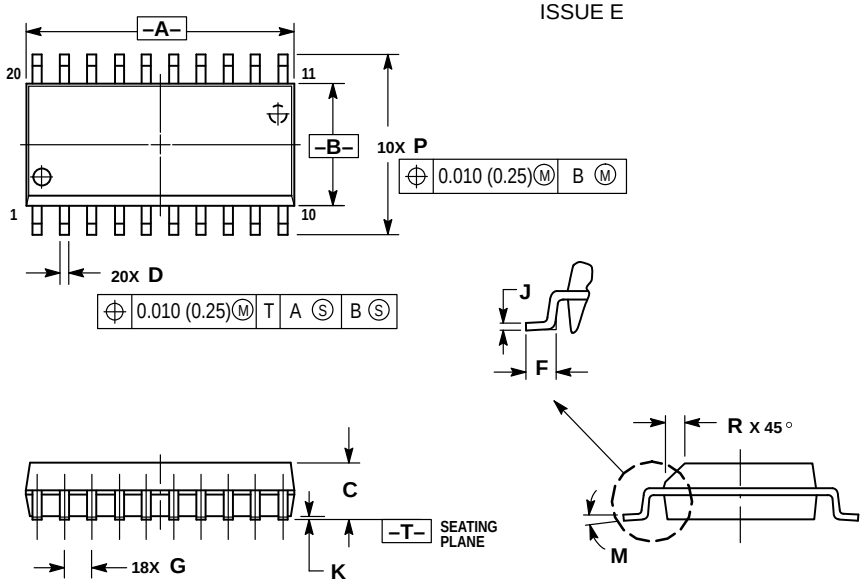
P SUFFIX
PLASTIC PACKAGE
CASE 738–03
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.010	1.070	25.66	27.17
B	0.240	0.260	6.10	6.60
C	0.150	0.180	3.81	4.57
D	0.015	0.022	0.39	0.55
E	0.050 BSC		1.27 BSC	
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

DW SUFFIX
PLASTIC PACKAGE
CASE 751D–04
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.150 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.65	12.95	0.499	0.510
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

NOTES

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