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MC68331
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Technical Supplement

Electrical Characteristics

The M68300 Modular Microcontroller Family includes a number of 32-bit devices built up from a selection of functional modules. MC68331, MC68332, and MC68334 microcontrollers contain the same central processing unit (CPU32) and system integration module (SIM), and thus have similar electrical characteristics.

This supplement consists of a new electrical characteristics appendix (Appendix A) that replaces Section 8 of the *MC68331 User's Manual* (MC68331UM/AD) and Section 10 of the *MC68332 User's Manual* (MC68332UM/AD). The *MC68334 User's Manual* (MC68334UM/AD) will include Appendix A when it is published.

Appendix A contains specification tables and timing diagrams. Each timing diagram has an individual key table of parameters abstracted from the specification tables. Pertinent notes have been included in the key tables. Because the MC68331 has no on-chip RAM and no time processing unit (TPU), there is a separate DC characteristics table (Table A–4) for this device.

Improved specifications contained in this supplement include:

- System clock timing and stability parameters
- Device and clock synthesizer current parameters
- Power consumption parameters
- Data bus mode select and reset timing parameters
- Fast termination bus cycle timing parameters
- Background debugging mode (BDM) timing parameters
- ECLK bus timing parameters
- Chip-select timing parameters
- Queued serial peripheral interface (QSPI) timing parameters

Table A–1. Maximum Ratings

Rating	Symbol	Value	Unit
Supply Voltage[1, 2, 6]	V_{DD}	–0.3 to +6.5	V
Input Voltage[1, 2, 3, 6]	V_{in}	–0.3 to +6.5	V
Instantaneous Maximum Current Single pin limit (applies to all pins)[1, 4, 5, 6]	I_D	25	mA
Operating Maximum Current Digital input disruptive current [4, 5, 7] $V_{SS} - 0.3 \le V_{IN} \le V_{DD} + 0.3$	I_{iD}	–500 to 500	µA
Operating Temperature Range MC68332 "C" Suffix MC68332 "V" Suffix MC68332 "M" Suffix	T_A	T_L to T_H –40 to 85 –40 to 105 –40 to 125	°C
Storage Temperature Range	T_{stg}	–55 to 150	°C

NOTES:

1. Permanent damage can occur if maximum ratings are exceeded. Exposure to voltages or currents in excess of recommended values affects device reliability. Device modules may not operate normally while being exposed to electrical extremes.
2. Although sections of the device contain circuitry to protect against damage from high static voltages or electrical fields, take normal precautions to avoid exposure to voltages higher than maximum-rated voltages.
3. All pins except $\overline{\text{TSTME}}$/TSC.
4. All functional non-supply pins are internally clamped to V_{SS}. All functional pins except EXTAL, $\overline{\text{TSTME}}$/TSC, and XFC are internally clamped to V_{DD}.
5. Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions.
6. This parameter is periodically sampled rather than 100% tested.
7. Total input current for all digital input-only and all digital input/output pins must not exceed 10 mA. Exceeding this limit can cause disruption of normal operation.

Table A–2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance Plastic 132-Pin Surface Mount	Θ_{JA}	38	°C/W

NOTES:

The average chip-junction temperature (T_J) in C can be obtained from:

$$T_J = T_A + (P_D \times \Theta_{JA}) \quad (1)$$

where

T_A = Ambient Temperature, °C

Θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

P_D = $P_{INT} + P_{I/O}$

P_{INT} = $I_{DD} \times V_{DD}$, Watts — Chip Internal Power

$P_{I/O}$ = Power Dissipation on Input and Output Pins — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D + (T_A + 273°C) + \Theta_{JA} \times P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

Table A–3. Clock Control Timing

(V_{DD} and V_{DDSYN} = 5.0 Vdc ±10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H, 32.768 kHz reference)

Characteristic	Symbol	Min	Max	Unit
PLL Reference Frequency Range	f_{ref}	25	50	kHz
System Frequency[1] On-Chip PLL System Frequency External Clock Operation	f_{sys}	dc 0.131 dc	16.78 16.78 16.78	MHz
PLL Lock Time[2]	t_{lpll}	—	20	ms
Limp Mode Clock Frequency[3] SYNCR X bit = 0 SYNCR X bit = 1	f_{limp}	— —	f_{sys} max/2 f_{sys} max	MHz
CLKOUT Stability[4, 5] Short term Long term	C_{stab}	–1.0 –0.5	1.0 0.5	%

NOTES:

1. All internal registers retain data at 0 Hz.
2. Assumes that stable V_{DDSYN} is applied, that an external filter capacitor with a value of 0.1 µF is attached to the XFC pin, and that the crystal oscillator is stable. Lock time is measured from power-up to RESET release. This specification also applies to the period required for PLL lock after changing the W and Y frequency control bits in the synthesizer control register (SYNCR) while the PLL is running, and to the period required for the clock to lock after LPSTOP.
3. Determined by the internal reference voltage applied to the on-chip VCO. The X bit in SYNCR controls a divide by two prescaler on the system clock output.
4. Short-term CLKOUT stability is the average deviation from programmed frequency measured over a 2 µs interval at maximum f_{sys}. Long-term CLKOUT stability is the average deviation from programmed frequency measured over a 1 ms interval at maximum f_{sys}. Stability is measured with a stable external clock input applied — variation in crystal oscillator frequency is additive to this figure.
5. This parameter is periodically sampled rather than 100% tested.

Table A–4a. MC68331 DC Characteristics

(V_{DD} and V_{DDSYN} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)

Characteristic	Symbol	Min	Max	Unit
Input High Voltage	V_{IH}	0.7 (V_{DD})	V_{DD} + 0.3	V
Input Low Voltage	V_{IL}	V_{SS} – 0.3	0.2 (V_{DD})	V
Input Hysteresis[1]	V_{HYS}	0.5	—	V
Input Leakage Current[2] V_{in} = V_{DD} or V_{SS} Input-only pins	I_{in}	–2.5	2.5	µA
High Impedance (Off-State) Leakage Current[2] V_{in} = V_{DD} or V_{SS} All input/output and output pins	I_{OZ}	–2.5	2.5	µA
CMOS Output High Voltage[2, 3] I_{OH} = –10.0 µA Group 1, 2, 4 input/output and all output pins	V_{OH}	V_{DD} – 0.2	—	V
CMOS Output Low Voltage[2] I_{OL} = 10.0 µA Group 1, 2, 4 input/output and all output pins	V_{OL}	—	0.2	V
Output High Voltage[2, 3] I_{OH} = –0.8 mA Group 1, 2, 4 input/output and all output pins	V_{OH}	V_{DD} – 0.8	—	V
Output Low Voltage[2] I_{OL} = 1.6 mA Group 1 I/O Pins, CLKOUT, FREEZE/QUOT, $\overline{IPIPE}$ I_{OL} = 5.3 mA Group 2 and Group 4 I/O Pins, $\overline{CSBOOT}$, BG/$\overline{CS}$ I_{OL} = 12 mA Group 3	V_{OL}	— — —	0.4 0.4 0.4	V
Three State Control Input High Voltage	V_{IHTSC}	1.6 (V_{DD})	9.1	V
Data Bus Mode Select Pull-up Current[5] V_{in} = V_{IL} DATA[15:0] V_{in} = V_{IH} DATA[15:0]	I_{MSP}	— –15	–120 —	µA
V_{DD} Supply Current[6] RUN[4] LPSTOP, 32.768 kHz crystal, VCO Off (STSIM = 0) LPSTOP (External clock input frequency = maximum f_{sys})	I_{DD} S_{IDD} S_{IDD}	— — —	124 350 5	mA µA mA
Clock Synthesizer Operating Voltage	V_{DDSYN}	4.5	5.5	V
V_{DDSYN} Supply Current[6] 32.768 kHz crystal, VCO on, maximum f_{sys} External Clock, maximum f_{sys} LPSTOP, 32.768 kHz crystal, VCO off (STSIM = 0) 32.768 kHz crystal, V_{DD} powered down	I_{DDSYN} I_{DDSYN} S_{IDDSYN} I_{DDSYN}	— — — —	1 5 150 100	mA mA µA µA

Table A–4a. MC68331 DC Characteristics (Continued)

(V_{DD} and V_{DDSYN} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)

Characteristic	Symbol	Min	Max	Unit
Power Dissipation[7]	P_D	—	690	mW
Input Capacitance[2, 8] All input-only pins All input/output pins	C_{in}	— —	10 20	pF
Load Capacitance[2] Group 1 I/O Pins and CLKOUT, FREEZE/QUOT, IPIPE Group 2 I/O Pins and CSBOOT, BG/CS Group 3 I/O pins Group 4 I/O pins	C_L	— — — —	90 100 130 200	pF

NOTES:

1. Applies to:
   Port D [7:0]
   Port E [7:3]
   Port F [7:0]
   TSTME/TSC, BKPT, RESET, IFETCH, RXD
2. Input-Only Pins: TSTME/TSC, BKPT, RXD
   Output-Only Pins: CSBOOT, BG/CS, CLKOUT, FREEZE/QUOT, IPIPE
   Input/Output Pins:
   Group 1: DATA[15:0], IFETCH
   Group 2: Port C (ADDR23/ECLK, ADDR[22:19]/CS[9:6], FC[2:0]/CS[5:3])
   Port D (PCS[3:1],TXD, PCS0/SS)
   Port E (DSACK[1:0], AVEC, RMC, DS, AS, SIZ[1:0])
   Port F (IRQ[7:1], MODCLK)
   ADDR[18:0], R/W, BERR, BR/CS0, BGACK/CS2
   Group 3: HALT, RESET
   Group 4: MISO, MOSI, SCK
3. Does not apply to HALT and RESET because they are open drain pins. Does not apply to Port D (MISO, MOSI, SCK, PCS0/SS, PCS[3:1], TXD) in wired-OR mode.
4. Current measured with system clock frequency of 16.78 MHz, all modules active.
5. Use of an active pulldown device is recommended.
6. Total operating current is the sum of the appropriate V_{DD} supply and V_{DDSYN} supply current.
7. Power dissipation measured with system clock frequency of 16.78 MHz, all modules active. Power dissipation is calculated using the following expression:

$$P_D = \text{Maximum } V_{DD} (I_{DDSYN} + I_{DD})$$

8. Input capacitance is periodically sampled rather than 100% tested.

Table A–4b. MC68332/MC68334 DC Characteristics

(V_{DD} and V_{DDSYN} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)

Characteristic	Symbol	Min	Max	Unit
Input High Voltage	V_{IH}	0.7 (V_{DD})	V_{DD} + 0.3	V
Input Low Voltage	V_{IL}	V_{SS} – 0.3	0.2 (V_{DD})	V
Input Hysteresis[1]	V_{HYS}	0.5	—	V
Input Leakage Current[2] V_{in} = V_{DD} or V_{SS} Input-only pins	I_{in}	–2.5	2.5	µA
High Impedance (Off-State) Leakage Current[2] V_{in} = V_{DD} or V_{SS} All input/output and output pins	I_{OZ}	–2.5	2.5	µA
CMOS Output High Voltage[2, 3] I_{OH} = –10.0 µA Group 1, 2, 4 input/output and all output pins	V_{OH}	V_{DD} – 0.2	—	V
CMOS Output Low Voltage[2] I_{OL} = 10.0 µA Group 1, 2, 4 input/output and all output pins	V_{OL}	—	0.2	V
Output High Voltage[2, 3] I_{OH} = –0.8 mA Group 1, 2, 4 input/output and all output pins	V_{OH}	V_{DD} – 0.8	—	V
Output Low Voltage[2] I_{OL} = 1.6 mA Group 1 I/O Pins, CLKOUT, FREEZE/QUOT, $\overline{IPIPE}$ I_{OL} = 5.3 mA Group 2 and Group 4 I/O Pins, $\overline{CSBOOT}$, $\overline{BG}$/$\overline{CS}$ I_{OL} = 12 mA Group 3	V_{OL}	— — —	0.4 0.4 0.4	V
Three State Control Input High Voltage	V_{IHTSC}	1.6 (V_{DD})	9.1	V
Data Bus Mode Select Pull-up Current[5] V_{in} = V_{IL} DATA[15:0] V_{in} = V_{IH} DATA[15:0]	I_{MSP}	— –15	–120 —	µA
V_{DD} Supply Current[6] RUN[4] RUN, TPU emulation mode LPSTOP, 32.768 kHz crystal, VCO Off (STSIM = 0) LPSTOP (External clock input frequency = maximum f_{sys})	 I_{DD} I_{DD} S_{IDD} S_{IDD}	 — — — —	 124 134 350 5	 mA mA µA mA
Clock Synthesizer Operating Voltage	V_{DDSYN}	4.5	5.5	V
V_{DDSYN} Supply Current[6] 32.768 kHz crystal, VCO on, maximum f_{sys} External Clock, maximum f_{sys} LPSTOP, 32.768 kHz crystal, VCO off (STSIM = 0) 32.768 kHz crystal, V_{DD} powered down	 I_{DDSYN} I_{DDSYN} S_{IDDSYN} I_{DDSYN}	 — — — —	 1 5 150 100	 mA mA µA µA
RAM Standby Voltage[7] Specified V_{DD} applied Standby mode, V_{DD} = V_{SS}	V_{SB}	0.0 3.0	5.5 5.5	V
RAM Standby Current Specified V_{DD} applied Standby mode, V_{DD} = V_{SS}	I_{SB} I_{SB}	— —	10 50	µA µA

Table A–4b. MC68332/MC68334 DC Characteristics (Continued)

(V_{DD} and V_{DDSYN} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)

Characteristic	Symbol	Min	Max	Unit
Power Dissipation[8]	P_D	—	690	mW
Input Capacitance[2, 9] All input-only pins All input/output pins	C_{in}	— —	10 20	pF
Load Capacitance[2] Group 1 I/O Pins and CLKOUT, FREEZE/QUOT, IPIPE Group 2 I/O Pins and CSBOOT, BG/CS Group 3 I/O pins Group 4 I/O pins	C_L	— — — —	90 100 130 200	pF

NOTES:

1. Applies to:
   TP[15:0]
   Port D [7:0]
   Port E [7:3]
   Port F [7:0]
   TSTME/TSC, BKPT, RESET, IFETCH, T2CLK, RXD
2. Input-Only Pins: TSTME/TSC, BKPT, T2CLK, RXD
   Output-Only Pins: CSBOOT, BG/CS, CLKOUT, FREEZE/QUOT, IPIPE
   Input/Output Pins:
   Group 1: DATA[15:0], IFETCH, TP[15:0]
   Group 2: Port C (ADDR23/ECLK, ADDR[22:19]/CS[9:6], FC[2:0]/CS[5:3])
   Port D (PCS[3:1],TXD, PCS0/SS)
   Port E (DSACK[1:0], AVEC, RMC, DS, AS, SIZ[1:0])
   Port F (IRQ[7:1], MODCLK)
   ADDR[18:0], R/W, BERR, BR/CS0, BGACK/CS2
   Group 3: HALT, RESET
   Group 4: MISO, MOSI, SCK
3. Does not apply to HALT and RESET because they are open drain pins. Does not apply to Port D (MISO, MOSI, SCK, PCS0/SS, PCS[3:1], TXD) in wired-OR mode.
4. Current measured with system clock frequency of 16.78 MHz, all modules active.
5. Use of an active pulldown device is recommended.
6. Total operating current is the sum of the appropriate V_{DD} supply and V_{DDSYN} supply current.
7. The SRAM module will not switch into standby mode as long as V_{SB} does not exceed V_{DD} by more than 0.5 Volt. The SRAM array cannot be accessed while the module is in standby mode.
8. Power dissipation measured with system clock frequency of 16.78 MHz, all modules active. Specification does not include TPU emulation mode. Power dissipation is calculated using the following expression:

$$P_D = \text{Maximum } V_{DD} (I_{DDSYN} + I_{DD})$$

9. Input capacitance is periodically sampled rather than 100% tested.

Table A–5. AC Timing

(V_{DD} and V_{DDSYN} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)

Num	Characteristic	Symbol	Min	Max	Unit
F1[2]	Frequency of Operation (32.768 kHz crystal)	f	0.13	16.78	MHz
1	Clock Period	t_{cyc}	59.6	—	ns
1A	ECLK Period	t_{Ecyc}	476	—	ns
1B[3]	External Clock Input Period	t_{Xcyc}	59.6	—	ns
2, 3	Clock Pulse Width	t_{CW}	24	—	ns
2A, 3A	ECLK Pulse Width	t_{ECW}	236	—	ns
2B, 3B[3]	External Clock Input High/Low Time	t_{XCHL}	29.8	—	ns
4, 5	Clock Rise and Fall Time	t_{Crf}	—	5	ns
4A, 5A	Rise and Fall Time — All Outputs except CLKOUT	t_{rf}	—	8	ns
4B, 5B	External Clock Rise and Fall Time	t_{XCrf}	—	5	ns
6	Clock High to Address, FC, SIZE, $\overline{RMC}$ Valid	t_{CHAV}	0	29	ns
7	Clock High to Address, Data, FC, SIZE, $\overline{RMC}$ High Impedance	t_{CHAZx}	0	59	ns
8	Clock High to Address, FC, SIZE, $\overline{RMC}$ Invalid	t_{CHAZn}	0	—	ns
9	Clock Low to $\overline{AS}$, $\overline{DS}$, $\overline{CS}$ Asserted	t_{CLSA}	2	25	ns
9A[4]	$\overline{AS}$ to $\overline{DS}$ or $\overline{CS}$ Asserted (Read)	t_{STSA}	–15	15	ns
9C	Clock Low to $\overline{IFETCH}$, $\overline{IPIPE}$ Asserted	t_{CLIA}	2	22	ns
11	Address, FC, SIZE, $\overline{RMC}$ Valid to $\overline{AS}$, $\overline{CS}$ (and $\overline{DS}$ Read) Asserted	t_{AVSA}	15	—	ns
12	Clock Low to $\overline{AS}$, $\overline{DS}$, $\overline{CS}$ Negated	t_{CLSN}	2	29	ns
12A	Clock Low to $\overline{IFETCH}$, $\overline{IPIPE}$ Negated	t_{CLIN}	2	22	ns
13	$\overline{AS}$, $\overline{DS}$, $\overline{CS}$ Negated to Address, FC, SIZE Invalid (Address Hold)	t_{SNAI}	15	—	ns
14	$\overline{AS}$, $\overline{CS}$ (and $\overline{DS}$ Read) Width Asserted	t_{SWA}	100	—	ns
14A	$\overline{DS}$, $\overline{CS}$ Width Asserted (Write)	t_{SWAW}	45	—	ns
14B	$\overline{AS}$, $\overline{CS}$ (and $\overline{DS}$ Read) Width Asserted (Fast Write Cycle)	t_{SWDW}	40	—	ns
15[5]	$\overline{AS}$, $\overline{DS}$, $\overline{CS}$ Width Negated	t_{SN}	40	—	ns
16	Clock High to $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$ High Impedance	t_{CHSZ}	—	59	ns
17	$\overline{AS}$, $\overline{DS}$, $\overline{CS}$ Negated to R/$\overline{W}$ High	t_{SNRN}	15	—	ns
18	Clock High to R/$\overline{W}$ High	t_{CHRH}	0	29	ns
20	Clock High to R/$\overline{W}$ Low	t_{CHRL}	0	29	ns
21	R/$\overline{W}$ High to $\overline{AS}$, $\overline{CS}$ Asserted	t_{RAAA}	15	—	ns
22	R/$\overline{W}$ Low to $\overline{DS}$, $\overline{CS}$ Asserted (Write)	t_{RASA}	70	—	ns
23	Clock High to Data Out Valid	t_{CHDO}	—	29	ns

Table A–5. AC Timing (Continued)

(V_{DD} and V_{DDSYN} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)

Num	Characteristic	Symbol	Min	Max	Unit
24	Data Out Valid to Negating Edge of $\overline{AS}$, $\overline{CS}$ (Fast Write Cycle)	t_{DVASN}	15	—	ns
25	$\overline{DS}$, $\overline{CS}$ Negated to Data Out Invalid (Data Out Hold)	t_{SNDOI}	15	—	ns
26	Data Out Valid to $\overline{DS}$, $\overline{CS}$ Asserted (Write)	t_{DVSA}	15	—	ns
27	Data In Valid to Clock Low (Data Setup)	t_{DICL}	5	—	ns
27A	Late $\overline{BERR}$, $\overline{HALT}$ Asserted to Clock Low (Setup Time)	t_{BELCL}	20	—	ns
28	$\overline{AS}$, $\overline{DS}$ Negated to $\overline{DSACK[1:0]}$, $\overline{BERR}$, $\overline{HALT}$, $\overline{AVEC}$ Negated	t_{SNDN}	0	80	ns
29[6]	$\overline{DS}$, $\overline{CS}$ Negated to Data In Invalid (Data In Hold)	t_{SNDI}	0	—	ns
29A[6, 7]	$\overline{DS}$, $\overline{CS}$ Negated to Data In High Impedance	t_{SHDI}	—	55	ns
30[6]	CLKOUT Low to Data In Invalid (Fast Cycle Hold)	t_{CLDI}	15	—	ns
30A[6]	CLKOUT Low to Data In High Impedance	t_{CLDH}	—	90	ns
31[8]	$\overline{DSACK[1:0]}$ Asserted to Data In Valid	t_{DADI}	—	50	ns
33	Clock Low to $\overline{BG}$ Asserted/Negated	t_{CLBAN}	—	29	ns
35[9]	$\overline{BR}$ Asserted to $\overline{BG}$ Asserted ($\overline{RMC}$ Not Asserted)	t_{BRAGA}	1	—	t_{cyc}
37	$\overline{BGACK}$ Asserted to $\overline{BG}$ Negated	t_{GAGN}	1	2	t_{cyc}
39	$\overline{BG}$ Width Negated	t_{GH}	2	—	t_{cyc}
39A	$\overline{BG}$ Width Asserted	t_{GA}	1	—	t_{cyc}
46	R/$\overline{W}$ Width Asserted (Write or Read)	t_{RWA}	150	—	ns
46A	R/$\overline{W}$ Width Asserted (Fast Write or Read Cycle)	t_{RWAS}	90	—	ns
47A	Asynchronous Input Setup Time $\overline{BR}$, $\overline{BGACK}$, $\overline{DSACK[1:0]}$, $\overline{BERR}$, $\overline{AVEC}$, $\overline{HALT}$	t_{AIST}	5	—	ns
47B	Asynchronous Input Hold Time	t_{AIHT}	15	—	ns
48[10]	$\overline{DSACK[1:0]}$ Asserted to $\overline{BERR}$, $\overline{HALT}$ Asserted	t_{DABA}	—	30	ns
53	Data Out Hold from Clock High	t_{DOCH}	0	—	ns
54	Clock High to Data Out High Impedance	t_{CHDH}	—	28	ns
55	R/$\overline{W}$ Asserted to Data Bus Impedance Change	t_{RADC}	40	—	ns
56	$\overline{RESET}$ Pulse Width (Reset Instruction)	t_{HRPW}	512	—	t_{cyc}
57	$\overline{BERR}$ Negated to $\overline{HALT}$ Negated (Rerun)	t_{BNHN}	0	—	ns
70	Clock Low to Data Bus Driven (Show)	t_{SCLDD}	0	29	ns
71	Data Setup Time to Clock Low (Show)	t_{SCLDS}	15	—	ns
72	Data Hold from Clock Low (Show)	t_{SCLDH}	10	—	ns
73	$\overline{BKPT}$ Input Setup Time	t_{BKST}	15	—	ns

Table A–5. AC Timing (Continued)

(V_{DD} and V_{DDSYN} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)

Num	Characteristic	Symbol	Min	Max	Unit
74	$\overline{BKPT}$ Input Hold Time	t_{BKHT}	10	—	ns
75	Mode Select Setup Time	t_{MSS}	20	—	t_{cyc}
76	Mode Select Hold Time	t_{MSH}	0	—	ns
77	$\overline{RESET}$ Assertion Time[11]	t_{RSTA}	4	—	t_{cyc}
78	$\overline{RESET}$ Rise Time[12, 13]	t_{RSTR}	—	10	t_{cyc}

NOTES:

1. All AC timing is shown with respect to 20% V_{DD} and 70% V_{DD} levels unless otherwise noted.
2. Minimum system clock frequency is four times the crystal frequency, subject to specified limits.
3. Minimum external clock high and low times are based on a 50% duty cycle. The minimum allowable t_{XCYC} period will be reduced when the duty cycle of the external clock signal varies. The relationship between external clock input duty cycle and minimum t_{XCYC} is expressed:

   Minimum t_{XCYC} period = minimum t_{XCHL} / (50% – external clock input duty cycle tolerance).

   To achieve maximum operating frequency (f_{sys}) while using an external clock input, adjust clock input duty cycle to obtain a 50% duty cycle on CLKOUT.
4. Specification 9A is the worst-case skew between $\overline{AS}$ and $\overline{DS}$ or $\overline{CS}$. The amount of skew depends on the relative loading of these signals. When loads are kept within specified limits, skew will not cause $\overline{AS}$ and $\overline{DS}$ to fall outside the limits shown in specification 9.
5. If multiple chip selects are used, $\overline{CS}$ width negated (specification 15) applies to the time from the negation of a heavily loaded chip select to the assertion of a lightly loaded chip select. The $\overline{CS}$ width negated specification between multiple chip selects does not apply to chip selects being used for synchronous ECLK cycles.
6. These hold times are specified with respect to $\overline{DS}$ or $\overline{CS}$ on asynchronous reads and with respect to CLKOUT on fast cycle reads. The user is free to use either hold time.
7. Maximum value is equal to (t_{cyc} / 2) + 25 ns.
8. If the asynchronous setup time (specification 47A) requirements are satisfied, the $\overline{DSACK[1:0]}$ low to data setup time (specification 31) and $\overline{DSACK[1:0]}$ low to $\overline{BERR}$ low setup time (specification 48) can be ignored. The data must only satisfy the data-in to clock low setup time (specification 27) for the following clock cycle. $\overline{BERR}$ must satisfy only the late $\overline{BERR}$ low to clock low setup time (specification 27A) for the following clock cycle.
9. To ensure coherency during every operand transfer, $\overline{BG}$ will not be asserted in response to $\overline{BR}$ until after all cycles of the current operand transfer are complete and $\overline{RMC}$ is negated.
10. In the absence of $\overline{DSACK[1:0]}$, $\overline{BERR}$ is an asynchronous input using the asynchronous setup time (specification 47A).
11. After external $\overline{RESET}$ negation is detected, a short transition period (approximately 2 t_{cyc}) elapses, then the SIM drives $\overline{RESET}$ low for 512 t_{cyc}.
12. External assertion of the $\overline{RESET}$ input can overlap internally-generated resets. To insure that an external reset is recognized in all cases, $\overline{RESET}$ must be asserted for at least 590 CLKOUT cycles.
13. External logic must pull $\overline{RESET}$ high during this period in order for normal MCU operation to begin.
14. Address access time = (2.5 + WS) t_{cyc} – t_{CHAV} – t_{DICL}
    Chip select access time = (2 + WS) t_{cyc} – t_{CLSA} – t_{DICL}
    Where: WS = number of wait states. When fast termination is used (2 clock bus) WS = –1.

Table A–6. Background Debugging Mode Timing

(V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = T_L to T_H)

Num	Characteristic	Symbol	Min	Max	Unit
B0	DSI Input Setup Time	t_{DSISU}	15	—	ns
B1	DSI Input Hold Time	t_{DSIH}	10	—	ns
B2	DSCLK Setup Time	t_{DSCSU}	15	—	ns
B3	DSCLK Hold Time	t_{DSCH}	10	—	ns
B4	DSO Delay Time	t_{DSOD}	—	25	ns
B5	DSCLK Cycle Time	t_{DSCCYC}	2	—	t_{cyc}
B6	CLKOUT High to FREEZE Asserted/Negated	t_{FRZAN}	—	50	ns
B7	CLKOUT High to $\overline{\text{IFETCH}}$ High Impedance	t_{IFZ}	—	50	ns
B8	CLKOUT High to $\overline{\text{IFETCH}}$ Valid	t_{IF}	—	50	ns
B9	DSCLK Low Time	t_{DSCLO}	1	—	t_{cyc}

NOTES:
1. All AC timing is shown with respect to 20% V_{DD} and 70% V_{DD} levels unless otherwise noted.

Table A–7. ECLK Bus Timing

(V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = T_L to T_H)

Num	Characteristic	Symbol	Min	Max	Unit
E1[2]	ECLK Low to Address Valid	t_{EAD}	—	60	ns
E2	ECLK Low to Address Hold	t_{EAH}	10	—	ns
E3	ECLK Low to $\overline{\text{CS}}$ Valid ($\overline{\text{CS}}$ delay)	t_{ECSD}	—	150	ns
E4	ECLK Low to $\overline{\text{CS}}$ Hold	t_{ECSH}	15	—	ns
E5	$\overline{\text{CS}}$ Negated Width	t_{ECSN}	30	—	ns
E6	Read Data Setup Time	t_{EDSR}	30	—	ns
E7	Read Data Hold Time	t_{EDHR}	15	—	ns
E8	ECLK Low to Data High Impedance	t_{EDHZ}	—	60	ns
E9	$\overline{\text{CS}}$ Negated to Data Hold (Read)	t_{ECDH}	0	—	ns
E10	$\overline{\text{CS}}$ Negated to Data High Impedance	t_{ECDZ}	—	1	t_{cyc}
E11	ECLK Low to Data Valid (Write)	t_{EDDW}	—	2	t_{cyc}
E12	ECLK Low to Data Hold (Write)	t_{EDHW}	5	—	ns
E13	$\overline{\text{CS}}$ Negated to Data Hold (Write)	t_{ECHW}	0	—	ns
E14[3]	Address Access Time (Read)	t_{EACC}	386	—	ns
E15[4]	Chip Select Access Time (Read)	t_{EACS}	296	—	ns
E16	Address Setup Time	t_{EAS}	1/2	—	t_{cyc}

NOTES:
1. All AC timing is shown with respect to 20% V_{DD} and 70% V_{DD} levels unless otherwise noted.
2. When the previous bus cycle is not an ECLK cycle, the address may be valid before ECLK goes low.
3. Address access time = $t_{Ecyc} - t_{EAD} - t_{EDSR}$.
4. Chip select access time = $t_{Ecyc} - t_{ECSD} - t_{EDSR}$.

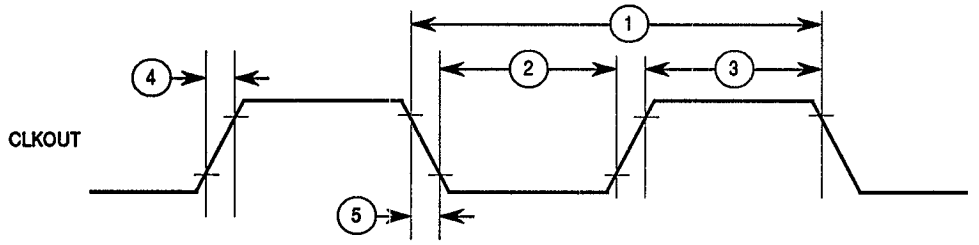
Table A–8. QSPI Timing

(V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = T_L to T_H, 200 pF load on all QSPI pins)

Num	Function	Symbol	Min	Max	Unit
	Operating Frequency Master Slave	f_{op}	DC DC	1/4 1/4	System Clock Frequency System Clock Frequency
1	Cycle Time Master Slave	t_{qcyc}	4 4	510 —	t_{cyc} t_{cyc}
2	Enable Lead Time Master Slave	t_{lead}	2 2	128 —	t_{cyc} t_{cyc}
3	Enable Lag Time Master Slave	t_{lag}	— 2	1/2 —	SCK t_{cyc}
4	Clock (SCK) High or Low Time Master Slave[2]	t_{sw}	2 t_{cyc} – 60 2 t_{cyc} – n	255 t_{cyc} —	ns ns
5	Sequential Transfer Delay Master Slave (Does Not Require Deselect)	t_{td}	17 13	8192 —	t_{cyc} t_{cyc}
6	Data Setup Time (Inputs) Master Slave	t_{su}	30 20	— —	ns ns
7	Data Hold Time (Inputs) Master Slave	t_{hi}	0 20	— —	ns ns
8	Slave Access Time	t_a	—	1	t_{cyc}
9	Slave MISO Disable Time	t_{dis}	—	2	t_{cyc}
10	Data Valid (after SCK Edge) Master Slave	t_v	— —	50 50	ns ns
11	Data Hold Time (Outputs) Master Slave	t_{ho}	0 0	— —	ns ns
12	Rise Time Input Output	t_{ri} t_{ro}	— —	2 30	µs ns
13	Fall Time Input Output	t_{fi} t_{fo}	— —	2 30	µs ns

NOTES:

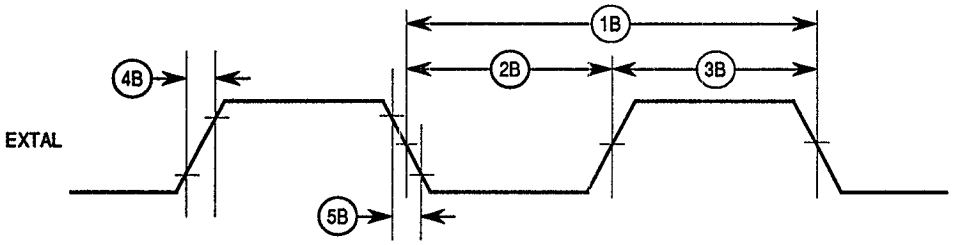
1. All AC timing is shown with respect to 20% V_{DD} and 70% V_{DD} levels unless otherwise noted.
2. In formula, n = External SCK rise + External SCK fall time



68300 CLKOUT TIM

NOTE: Timing shown with respect to 20% and 70% V_{DD}.

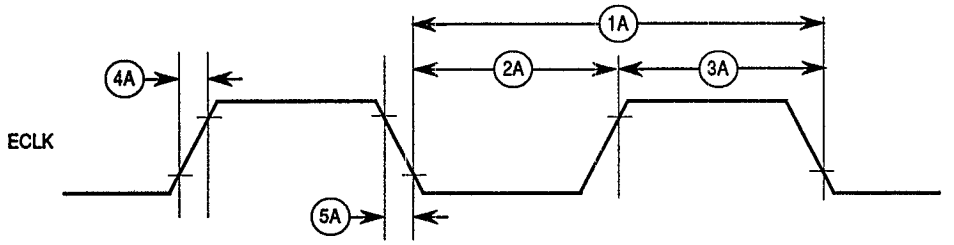
Figure A–1. CLKOUT Output Timing Diagram



68300 EXT CLK INPUT TIM

NOTE: Timing shown with respect to 20% and 70% V_{DD}. Pulse width shown with respect to 50% V_{DD}.

Figure A–2. External Clock Input Timing Diagram



68300 ECLK OUTPUT TIM

NOTE: Timing shown with respect to 20% and 70% V_{DD}.

Figure A–3. ECLK Output Timing Diagram

Key to Figures A–1, A–2, A–3

(Abstracted from Table A–5; see table for complete notes)

Num	Characteristic	Symbol	Min	Max	Units
1	Clock Period	t_{cyc}	59.6	—	ns
1A	ECLK Period	t_{Ecyc}	476	—	ns
1B[3]	External Clock Input Period	t_{Xcyc}	59.6	—	ns
2, 3	Clock Pulse Width	t_{CW}	24	—	ns
2A, 3A	ECLK Pulse Width	t_{ECW}	236	—	ns
2B,3B[3]	External Clock Input High/Low Time	t_{XCHL}	29.8	—	ns
4, 5	Clock Rise and Fall Time	t_{Crf}	—	5	ns
4A, 5A	ECLK Rise and Fall Time	t_{Erf}	—	8	ns
4B, 5B	External Clock Rise and Fall Time	t_{XCrf}	—	5	ns

NOTES:

1. All AC timing is shown with respect to 20% V_{DD} and 70% V_{DD} levels unless otherwise noted.
3. Minimum external clock high and low times are based on a 50% duty cycle. The minimum allowable t_{XCYC} period will be reduced when the duty cycle of the external clock signal varies. The relationship between external clock input duty cycle and minimum t_{XCYC} is expressed:

   Minimum t_{XCYC} period = minimum t_{XCHL} / (50% – external clock input duty cycle tolerance).

   To achieve maximum operating frequency (f_{sys}) while using an external clock input, adjust clock input duty cycle to obtain a 50% duty cycle on CLKOUT.

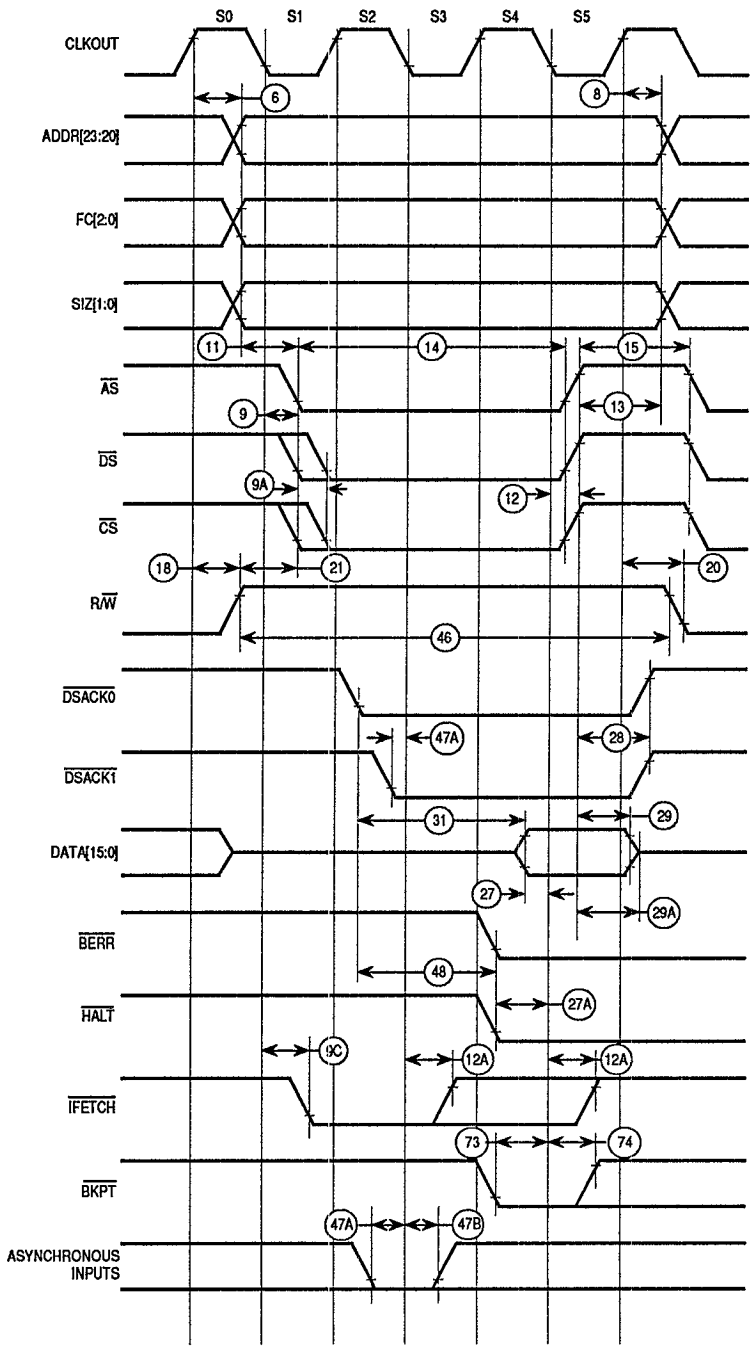


Figure A–4. Read Cycle Timing Diagram

Key to Figure A–4
(Abstracted from Table A–5; see table for complete notes)

Num	Characteristic	Symbol	Min	Max	Units
6	Clock High to Address, FC, SIZE, RMC Valid	t_{CHAV}	0	29	ns
8	Clock High to Address, FC, SIZE, RMC Invalid	t_{CHAZn}	0	—	ns
9	Clock Low to AS, DS, CS Asserted	t_{CLSA}	2	25	ns
9A[4]	AS to DS or CS Asserted (Read)	t_{STSA}	–15	15	ns
9C	Clock Low to IFETCH, IPIPE Asserted	t_{CLIA}	2	22	ns
11	Address, FC, SIZE, RMC Valid to AS, CS (and DS Read) Asserted	t_{AVSA}	15	—	ns
12	Clock Low to AS, DS, CS Negated	t_{CLSN}	2	29	ns
12A	Clock Low to IFETCH, IPIPE Negated	t_{CLIN}	2	22	ns
13	AS, DS, CS Negated to Address, FC, SIZE Invalid (Address Hold)	t_{SNAI}	15	—	ns
14	AS, CS (and DS Read) Width Asserted	t_{SWA}	100	—	ns
15[5]	AS, DS, CS Width Negated	t_{SN}	40	—	ns
18	Clock High to R/W High	t_{CHRH}	0	29	ns
20	Clock High to R/W Low	t_{CHRL}	0	29	ns
21	R/W High to AS, CS Asserted	t_{RAAA}	15	—	ns
27	Data In Valid to Clock Low (Data Setup)	t_{DICL}	5	—	ns
27A	Late BERR, HALT Asserted to Clock Low (Setup Time)	t_{BELCL}	20	—	ns
28	AS, DS Negated to DSACK[1:0], BERR, HALT, AVEC Negated	t_{SNDN}	0	80	ns
29[6]	DS, CS Negated to Data In Invalid (Data In Hold)	t_{SNDI}	0	—	ns
29A[6, 7]	DS, CS Negated to Data In High Impedance	t_{SHDI}	—	55	ns
31[8]	DSACK[1:0] Asserted to Data In Valid	t_{DADI}	—	50	ns
46	R/W Width Asserted (Write or Read)	t_{RWA}	150	—	ns
47A	Asynchronous Input Setup Time BR, BGACK, DSACK[1:0], BERR, AVEC, HALT	t_{AIST}	5	—	ns
47B	Asynchronous Input Hold Time	t_{AIHT}	15	—	ns
48[10]	DSACK[1:0] Asserted to BERR, HALT Asserted	t_{DABA}	—	30	ns
73	BKPT Input Setup Time	t_{BKST}	15	—	ns
74	BKPT Input Hold Time	t_{BKHT}	10	—	ns

NOTES:

1. All AC timing is shown with respect to 20% V_{DD} and 70% V_{DD} levels unless otherwise noted.
4. Specification 9A is the worst-case skew between AS and DS or CS. The amount of skew depends on the relative loading of these signals. When loads are kept within specified limits, skew will not cause AS and DS to fall outside the limits shown in specification 9.
5. If multiple chip selects are used, CS width negated (specification 15) applies to the time from the negation of a heavily loaded chip select to the assertion of a lightly loaded chip select. The CS width negated specification between multiple chip selects does not apply to chip selects being used for synchronous ECLK cycles.
6. These hold times are specified with respect to DS or CS on asynchronous reads and with respect to CLKOUT on synchronous reads. The user is free to use either hold time.
7. Maximum value is equal to (t_{cyc} / 2) + 25 ns.
8. If the asynchronous setup time (specification 47A) requirements are satisfied, the DSACK[1:0] low to data setup time (specification 31) and DSACK[1:0] low to BERR low setup time (specification 48) can be ignored. The data must only satisfy the data-in to clock low setup time (specification 27) for the following clock cycle. BERR must satisfy only the late BERR low to clock low setup time (specification 27A) for the following clock cycle.
10. In the absence of DSACK[1:0], BERR is an asynchronous input using the asynchronous setup time (specification 47A).

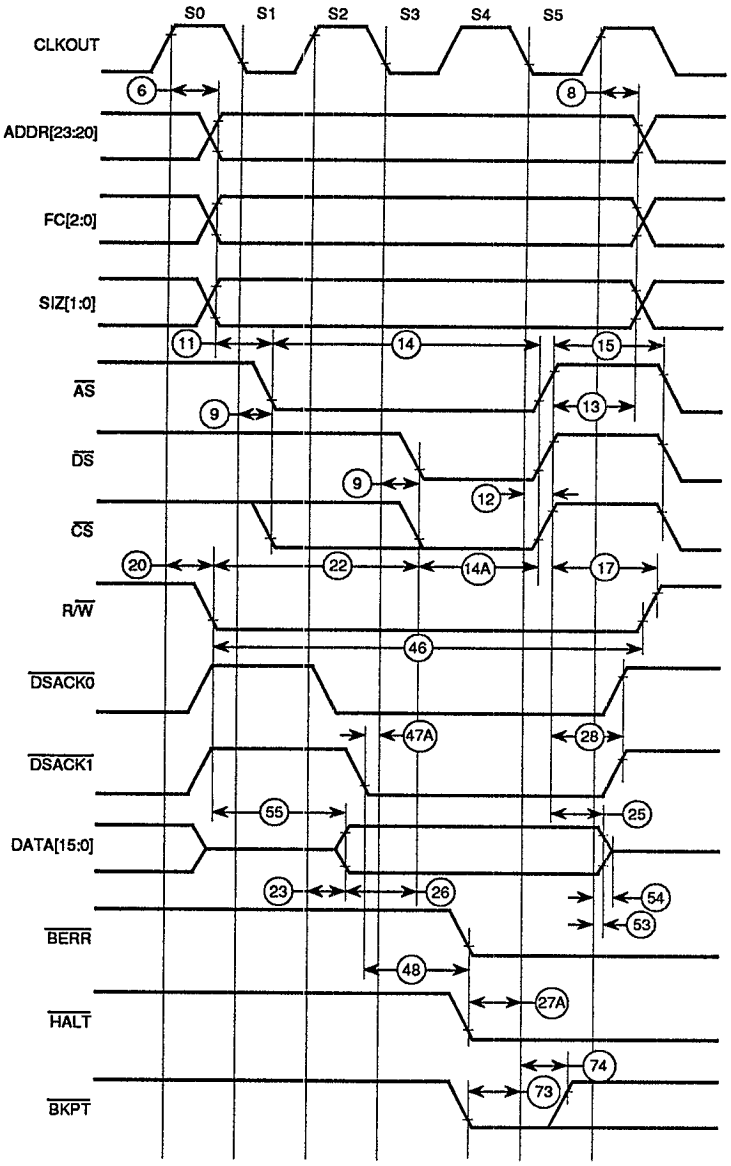


Figure A–5. Write Cycle Timing Diagram

Key to Figure A–5

(Abstracted from Table A–5; see table for complete notes)

Num	Characteristic	Symbol	Min	Max	Units
6	Clock High to Address, FC, SIZE, RMC Valid	t_{CHAV}	0	29	ns
8	Clock High to Address, FC, SIZE, RMC Invalid	t_{CHAZn}	0	—	ns
9	Clock Low to AS, DS, CS Asserted	t_{CLSA}	2	25	ns
11	Address, FC, SIZE, RMC Valid to AS, CS (and DS Read) Asserted	t_{AVSA}	15	—	ns
12	Clock Low to AS, DS, CS Negated	t_{CLSN}	2	29	ns
13	AS, DS, CS Negated to Address, FC, SIZE Invalid (Address Hold)	t_{SNAI}	15	—	ns
14	AS, CS (and DS Read) Width Asserted	t_{SWA}	100	—	ns
14A	DS, CS Width Asserted Write	t_{SWAW}	45	—	ns
15[5]	AS, DS, CS Width Negated	t_{SN}	40	—	ns
17	AS, DS, CS Negated to R/W High	t_{SNRN}	15	—	ns
20	Clock High to R/W Low	t_{CHRL}	0	29	ns
22	R/W Low to DS, CS Asserted (Write)	t_{RASA}	70	—	ns
23	Clock High to Data Out Valid	t_{CHDO}	—	29	ns
25	DS, CS Negated to Data Out Invalid (Data Out Hold)	t_{SNDOI}	15	—	ns
26	Data Out Valid to DS , CS Asserted (Write)	t_{DVSA}	15	—	ns
27A	Late BERR, HALT Asserted to Clock Low (Setup Time)	t_{BELCL}	20	—	ns
28	AS, DS Negated to DSACK[1:0], BERR, HALT, AVEC Negated	t_{SNDN}	0	80	ns
46	R/W Width Asserted (Write or Read)	t_{RWA}	150	—	ns
47A	Asynchronous Input Setup Time BR, BGACK, DSACK[1:0], BERR, AVEC, HALT	t_{AIST}	5	—	ns
48[10]	DSACK[1:0] Asserted to BERR, HALT Asserted	t_{DABA}	—	30	ns
53	Data Out Hold from Clock High	t_{DOCH}	0	—	ns
54	Clock High to Data Out High Impedance	t_{CHDH}	—	28	ns
73	BKPT Input Setup Time	t_{BKST}	15	—	ns
74	BKPT Input Hold Time	t_{BKHT}	10	—	ns

NOTES:

1. All AC timing is shown with respect to 20% V_{DD} and 70% V_{DD} levels unless otherwise noted.
5. If multiple chip selects are used, CS width negated (specification 15) applies to the time from the negation of a heavily loaded chip select to the assertion of a lightly loaded chip select. The CS width negated specification between multiple chip selects does not apply to chip selects being used for synchronous ECLK cycles.
10. In the absence of DSACK[1:0], BERR is an asynchronous input using the asynchronous setup time (specification 47A).

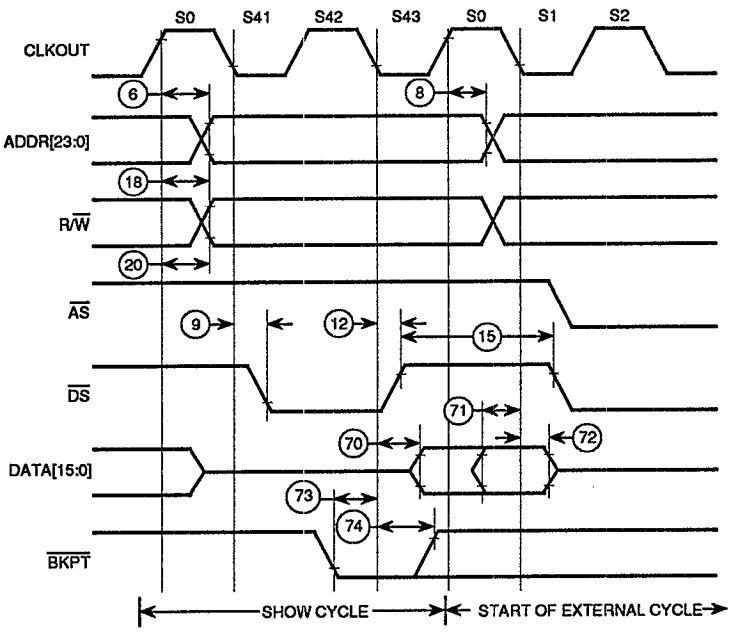


Figure A–6. Show Cycle Timing Diagram

Key to Figure A–6

(Abstracted from Table A–5; see table for complete notes)

Num	Characteristic	Symbol	Min	Max	Units
6	Clock High to Address, FC, SIZE, $\overline{RMC}$ Valid	t_{CHAV}	0	29	ns
8	Clock High to Address, FC, SIZE, $\overline{RMC}$ Invalid	t_{CHAZn}	0	—	ns
9	Clock Low to $\overline{AS}$, $\overline{DS}$, $\overline{CS}$ Asserted	t_{CLSA}	2	25	ns
12	Clock Low to $\overline{AS}$, $\overline{DS}$, $\overline{CS}$ Negated	t_{CLSN}	2	29	ns
15[5]	$\overline{AS}$, $\overline{DS}$, $\overline{CS}$ Width Negated	t_{SN}	40	—	ns
18	Clock High to R/$\overline{W}$ High	t_{CHRH}	0	29	ns
20	Clock High to R/$\overline{W}$ Low	t_{CHRL}	0	29	ns
70	Clock Low to Data Bus Driven (Show)	t_{SCLDD}	0	29	ns
71	Data Setup Time to Clock Low (Show)	t_{SCLDS}	15	—	ns
72	Data Hold from Clock Low (Show)	t_{SCLDH}	10	—	ns
73	$\overline{BKPT}$ Input Setup Time	t_{BKST}	15	—	ns
74	$\overline{BKPT}$ Input Hold Time	t_{BKHT}	10	—	ns

NOTES:

1. All AC timing is shown with respect to 20% V_{DD} and 70% V_{DD} levels unless otherwise noted.
5. If multiple chip selects are used, $\overline{CS}$ width negated (specification 15) applies to the time from the negation of a heavily loaded chip select to the assertion of a lightly loaded chip select. The $\overline{CS}$ width negated specification between multiple chip selects does not apply to chip selects being used for synchronous ECLK cycles.

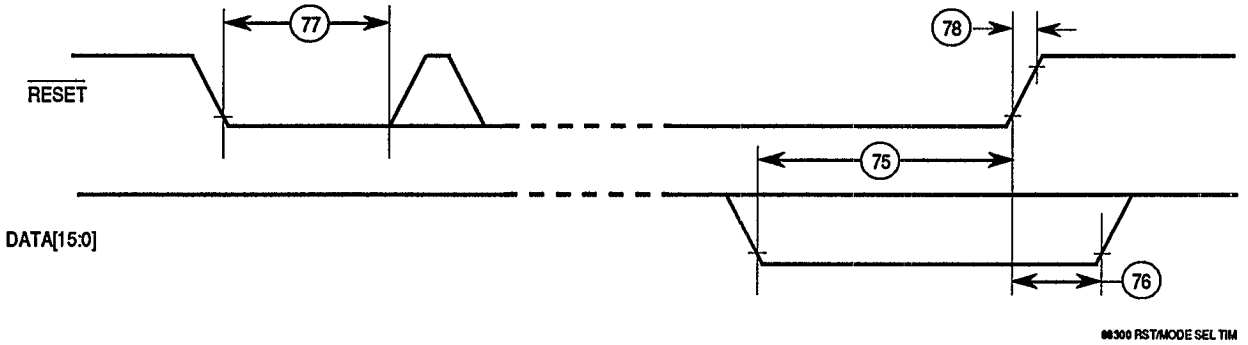


Figure A–7. Reset and Mode Select Timing Diagram

Key to Figure A–7

(Abstracted from Table A–5; see table for complete notes)

Num	Characteristic	Symbol	Min	Max	Units
75	Mode Select Setup Time	t_{MSS}	20	—	t_{cyc}
76	Mode Select Hold Time	t_{MSH}	0	—	ns
77	$\overline{\text{RESET}}$ Assertion Time[11, 12]	t_{RSTA}	4	—	t_{cyc}
78	$\overline{\text{RESET}}$ Rise Time[13]	t_{RSTR}	—	10	t_{cyc}

NOTES:

1. All AC timing is shown with respect to 20% V_{DD} and 70% V_{DD} levels unless otherwise noted.
11. After external $\overline{\text{RESET}}$ negation is detected, a short transition period (approximately 2 t_{cyc}) elapses, then the SIM drives $\overline{\text{RESET}}$ low for 512 t_{cyc}.
12. External assertion of the $\overline{\text{RESET}}$ input can overlap internally-generated resets. To insure that an external reset is recognized in all cases, $\overline{\text{RESET}}$ must be asserted for at least 590 CLKOUT cycles.
13. External logic must pull $\overline{\text{RESET}}$ high during this period in order for normal MCU operation to begin.

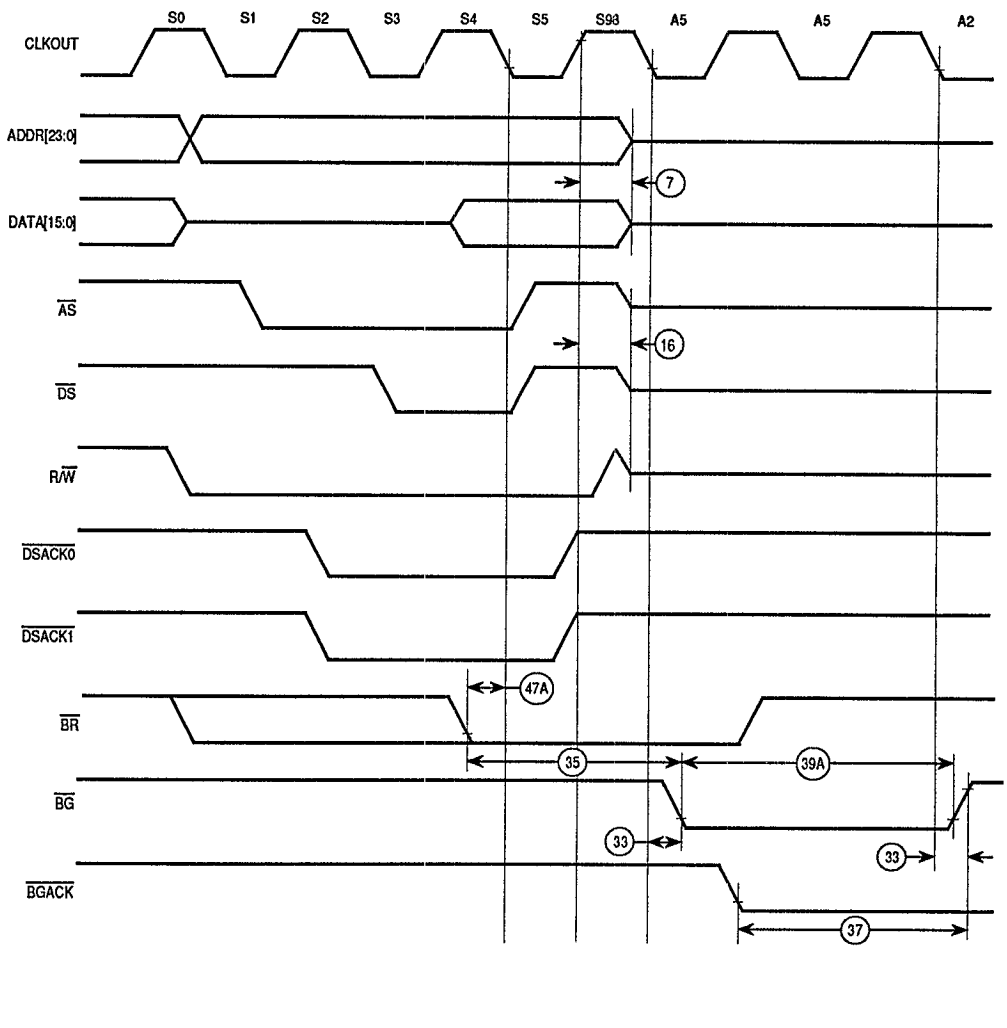


Figure A–8. Bus Arbitration Timing Diagram — Active Bus Case

Key to Figure A–8

(Abstracted from Table A–5; see table for complete notes)

Num	Characteristic	Symbol	Min	Max	Units
7	Clock High to Address, Data, FC, SIZE, $\overline{RMC}$ High Impedance	t_{CHAZx}	0	59	ns
16	Clock High to $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$ High Impedance	t_{CHSZ}	—	59	ns
33	Clock Low to $\overline{BG}$ Asserted/Negated	t_{CLBA}	—	29	ns
35[9]	$\overline{BR}$ Asserted to $\overline{BG}$ Asserted ($\overline{RMC}$ Not Asserted)	t_{BRAGA}	1	—	t_{cyc}
37	$\overline{BGACK}$ Asserted to $\overline{BG}$ Negated	t_{GAGN}	1	2	t_{cyc}
39A	$\overline{BG}$ Width Asserted	t_{GA}	1	—	t_{cyc}
47A	Asynchronous Input Setup Time $\overline{BR}$, $\overline{BGACK}$, $\overline{DSACK[1:0]}$, $\overline{BERR}$, $\overline{AVEC}$, $\overline{HALT}$	t_{AIST}	5	—	ns

NOTES:

1. All AC timing is shown with respect to 20% V_{DD} and 70% V_{DD} levels unless otherwise noted.
9. To ensure coherency during every operand transfer, $\overline{BG}$ will not be asserted in response to $\overline{BR}$ until after all cycles of the current operand transfer are complete and $\overline{RMC}$ is negated.

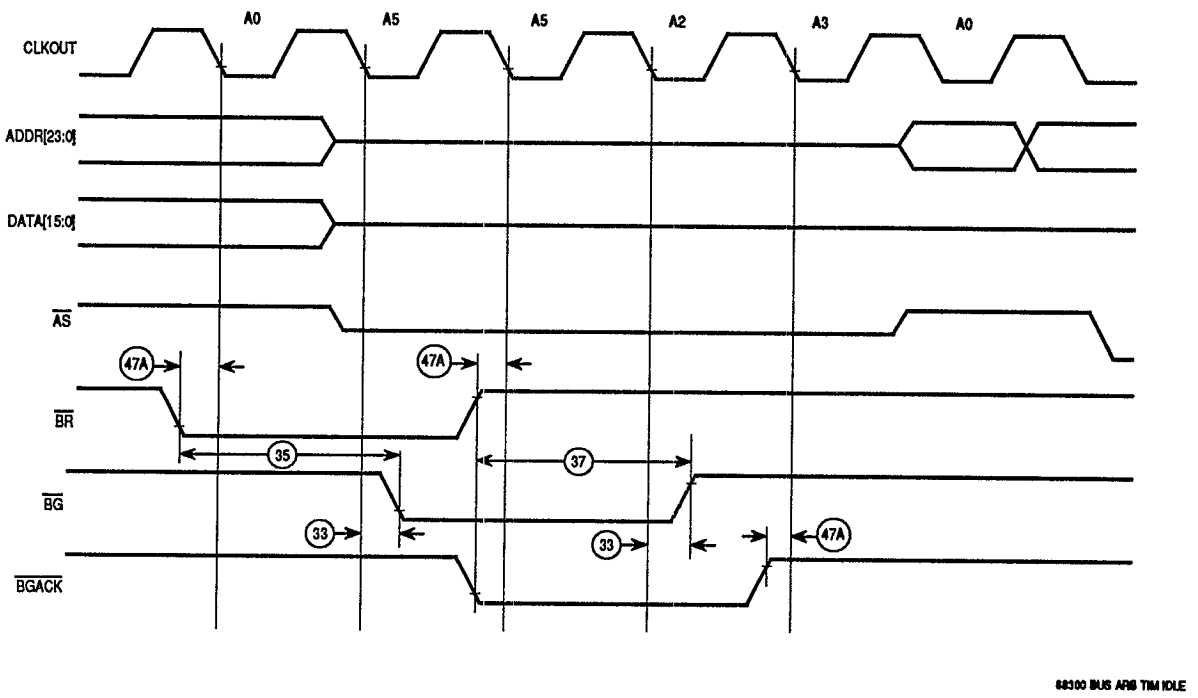


Figure A–9. Bus Arbitration Timing Diagram — Idle Bus Case

Key to Figure A–9

(Abstracted from Table A–5; see table for complete notes)

Num	Characteristic	Symbol	Min	Max	Units
33	Clock Low to $\overline{BG}$ Asserted/Negated	t_{CLBA}	—	29	ns
35[9]	$\overline{BR}$ Asserted to $\overline{BG}$ Asserted ($\overline{RMC}$ Not Asserted)	t_{BRAGA}	1	—	t_{cyc}
37	$\overline{BGACK}$ Asserted to $\overline{BG}$ Negated	t_{GAGN}	1	2	t_{cyc}
47A	Asynchronous Input Setup Time $\overline{BR}$, $\overline{BGACK}$, $\overline{DSACK[1:0]}$, $\overline{BERR}$, $\overline{AVEC}$, $\overline{HALT}$	t_{AIST}	5	—	ns

NOTES:

1. All AC timing is shown with respect to 20% V_{DD} and 70% V_{DD} levels unless otherwise noted.
9. To ensure coherency during every operand transfer, $\overline{BG}$ will not be asserted in response to $\overline{BR}$ until after all cycles of the current operand transfer are complete and $\overline{RMC}$ is negated.

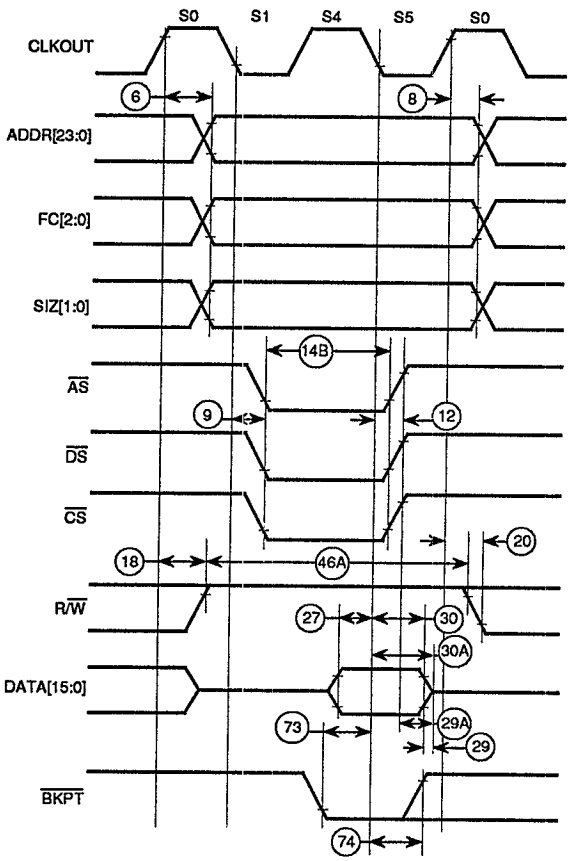


Figure A–10. Fast Termination Read Cycle Timing Diagram

Key to Figure A–10

(Abstracted from Table A–5; see table for complete notes)

Num	Characteristic	Symbol	Min	Max	Units
6	Clock High to Address, FC, SIZE, $\overline{RMC}$ Valid	t_{CHAV}	0	29	ns
8	Clock High to Address, FC, SIZE, $\overline{RMC}$ Invalid	t_{CHAZn}	0	—	ns
9	Clock Low to $\overline{AS}$, $\overline{DS}$, $\overline{CS}$ Asserted	t_{CLSA}	2	25	ns
12	Clock Low to $\overline{AS}$, $\overline{DS}$, $\overline{CS}$ Negated	t_{CLSN}	2	29	ns
14B	$\overline{AS}$, $\overline{CS}$ (and $\overline{DS}$ Read) Width Asserted	t_{SWDW}	40	—	ns
18	Clock High to R/$\overline{W}$ High	t_{CHRH}	0	29	ns
20	Clock High to R/$\overline{W}$ Low	t_{CHRL}	0	29	ns
27	Data In Valid to Clock Low (Data Setup)	t_{DICL}	5	—	ns
29[6]	$\overline{DS}$, $\overline{CS}$ Negated to Data In Invalid (Data In Hold)	t_{SNDI}	0	—	ns
29A[6, 7]	$\overline{DS}$, $\overline{CS}$ Negated to Data In High Impedance	t_{SHDI}	—	55	ns
30[6]	CLKOUT Low to Data In Invalid	t_{CLDI}	15	—	ns
30A[6]	CLKOUT Low to Data In High Impedance	t_{CLDH}	—	90	ns
46A	R/$\overline{W}$ Width Asserted	t_{RWAS}	90	—	ns
73	$\overline{BKPT}$ Input Setup Time	t_{BKST}	15	—	ns
74	$\overline{BKPT}$ Input Hold Time	t_{BKHT}	10	—	ns

NOTES:

1. All AC timing is shown with respect to 20% V_{DD} and 70% V_{DD} levels unless otherwise noted.
6. These hold times are specified with respect to $\overline{DS}$ or $\overline{CS}$ on asynchronous reads and with respect to CLKOUT on synchronous reads. The user is free to use either hold time.
7. Maximum value is equal to (t_{cyc} / 2) + 25 ns.

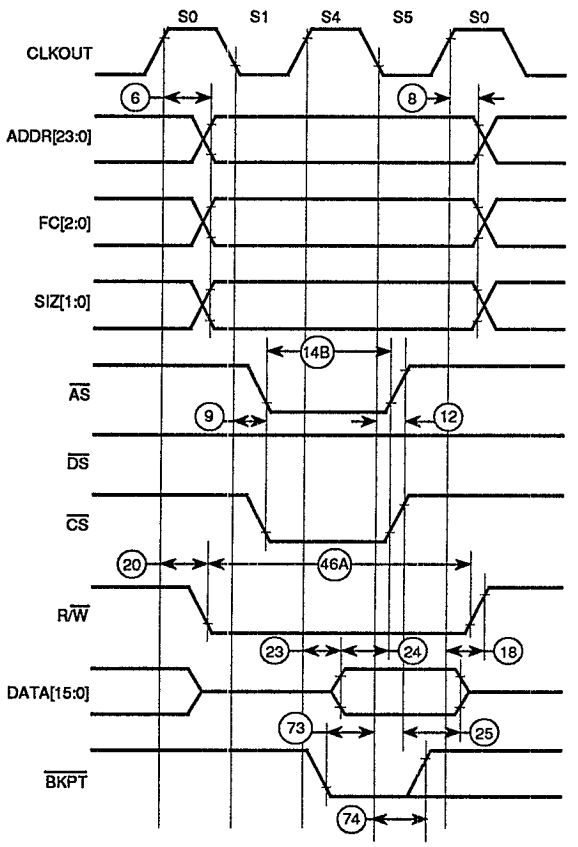


Figure A–11. Fast Termination Write Cycle Timing Diagram

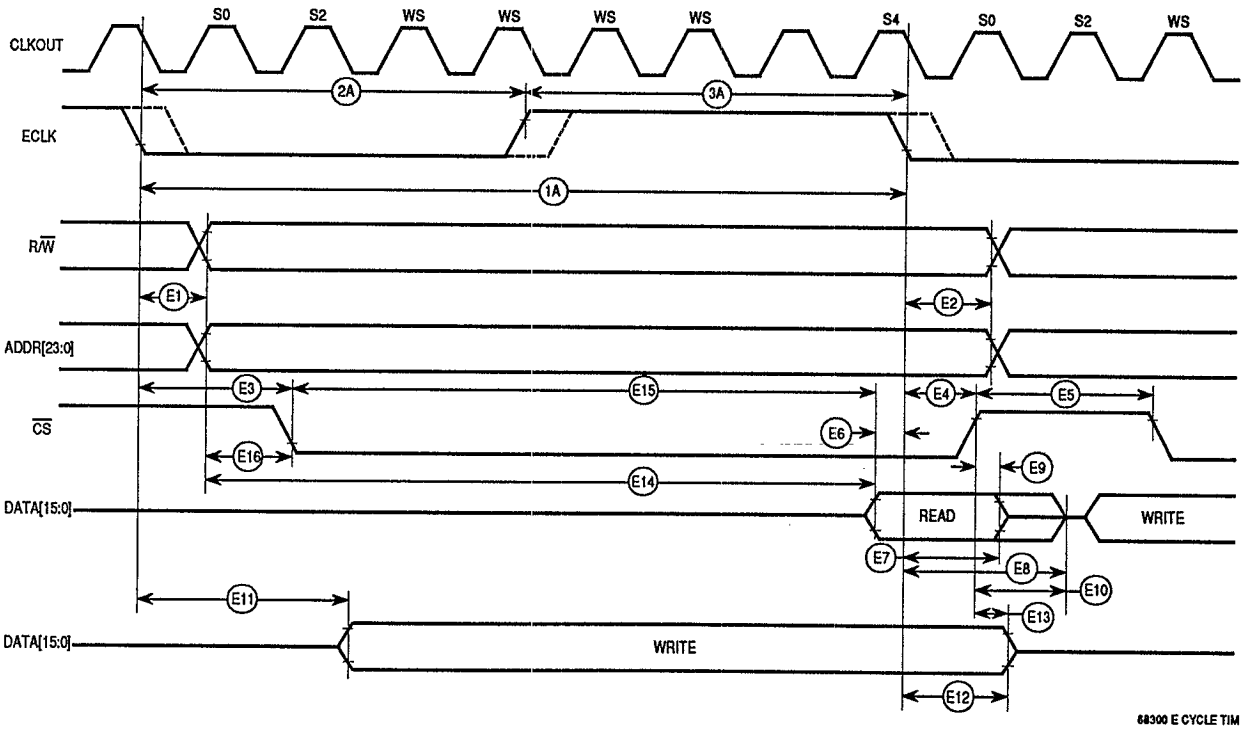
Key to Figure A–11

(Abstracted from Table A–5; see table for complete notes)

Num	Characteristic	Symbol	Min	Max	Units
6	Clock High to Address, FC, SIZE, $\overline{RMC}$ Valid	t_{CHAV}	0	29	ns
8	Clock High to Address, FC, SIZE, $\overline{RMC}$ Invalid	t_{CHAZn}	0	—	ns
9	Clock Low to $\overline{AS}$, $\overline{DS}$, $\overline{CS}$ Asserted	t_{CLSA}	2	25	ns
12	Clock Low to $\overline{AS}$, $\overline{DS}$, $\overline{CS}$ Negated	t_{CLSN}	2	29	ns
14B	$\overline{AS}$, $\overline{CS}$ (and $\overline{DS}$ Read) Width Asserted	t_{SWDW}	40	—	ns
18	Clock High to R/$\overline{W}$ High	t_{CHRH}	0	29	ns
20	Clock High to R/$\overline{W}$ Low	t_{CHRL}	0	29	ns
23	Clock High to Data Out Valid	t_{CHDO}	—	29	ns
24	Data Out Valid to Negating Edge of $\overline{AS}$, $\overline{CS}$	t_{DVASN}	15	—	ns
25	$\overline{DS}$, $\overline{CS}$ Negated to Data Out Invalid (Data Out Hold)	t_{SNDOI}	15	—	ns
46A	R/$\overline{W}$ Width Asserted	t_{RWAS}	90	—	ns
73	$\overline{BKPT}$ Input Setup Time	t_{BKST}	15	—	ns
74	$\overline{BKPT}$ Input Hold Time	t_{BKHT}	10	—	ns

NOTES:

1. All AC timing is shown with respect to 20% V_{DD} and 70% V_{DD} levels unless otherwise noted.



NOTE: Shown with ECLK = system clock/8 — EDIV bit in clock synthesizer control register (SYNCR) = 0.

Figure A–12. ECLK Timing Diagram

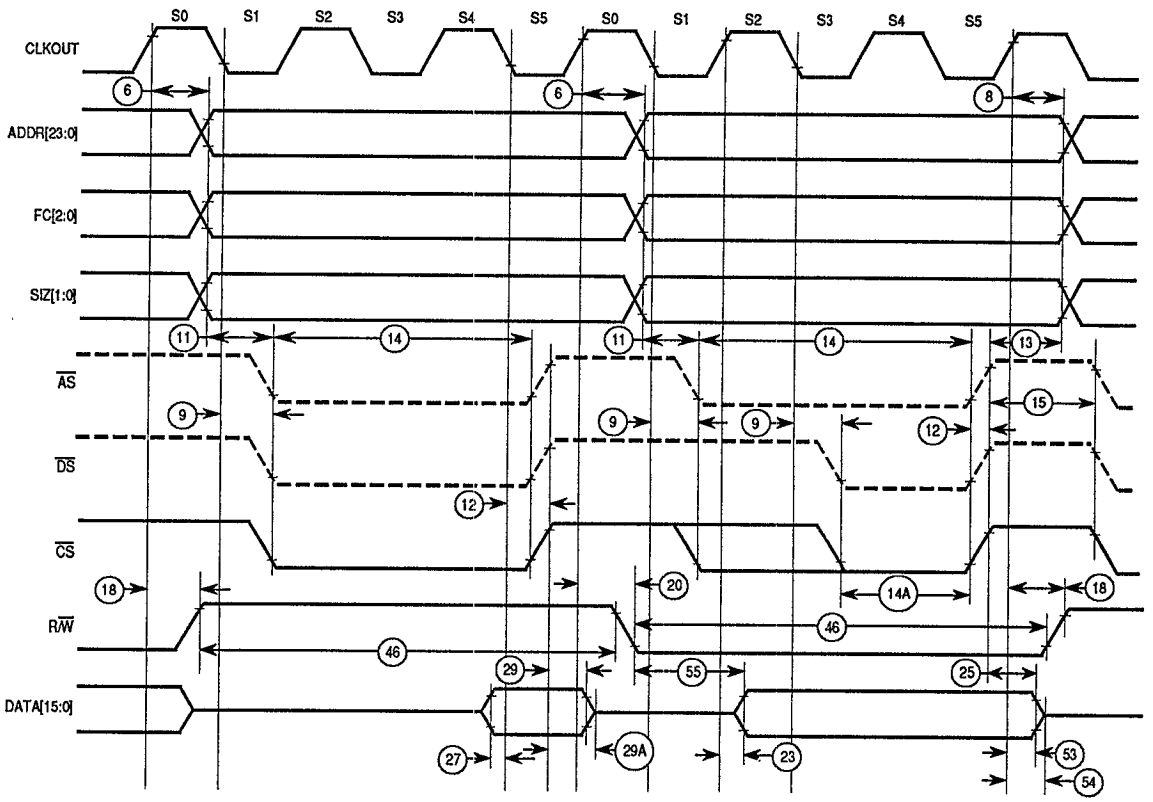
Key to Figure A–12

(Abstracted from Table A–7; see table for complete notes)

Num	Characteristic	Symbol	Min	Max	Units
1A	ECLK Period	t_{Ecyc}	476	—	ns
2A, 3A	ECLK Pulse Width	t_{ECW}	236	—	ns
4A, 5A	Rise and Fall Time — All Outputs except CLKOUT	t_{Erf}	—	8	ns
E1[2]	ECLK Low to Address and R/$\overline{W}$ Valid	t_{EAD}	—	60	ns
E2	ECLK Low to Address and R/$\overline{W}$ Hold	t_{EAH}	10	—	ns
E3	ECLK Low to $\overline{CS}$ Valid ($\overline{CS}$ delay)	t_{ECSD}	—	150	ns
E4	ECLK Low to $\overline{CS}$ Hold	t_{ECSH}	15	—	ns
E5	$\overline{CS}$ Negated Width	t_{ECSN}	30	—	ns
E6	Read Data Setup Time	t_{EDSR}	30	—	ns
E7	Read Data Hold Time	t_{EDHR}	15	—	ns
E8	ECLK Low to Data High Impedance	t_{EDHZ}	—	60	ns
E9	$\overline{CS}$ Negated to Data Hold (Read)	t_{ECDH}	0	—	ns
E10	$\overline{CS}$ Negated to Data High Impedance	t_{ECDZ}	—	1	t_{cyc}
E11	ECLK Low to Data Valid (Write)	t_{EDDW}	—	2	t_{cyc}
E12	ECLK Low to Data Hold (Write)	t_{EDHW}	5	—	ns
E13	$\overline{CS}$ Negated to Data Hold (Write)	t_{ECHW}	0	—	ns
E14[3]	Address Access Time (Read)	t_{EACC}	386	—	ns
E15[4]	Chip Select Access Time (Read)	t_{EACS}	296	—	ns
E16	Address Setup Time	t_{EAS}	1/2	—	t_{cyc}

NOTES:

1. All AC timing is shown with respect to 20% V_{DD} and 70% V_{DD} levels unless otherwise noted.
2. When the previous bus cycle is not a synchronous ECLK bus cycle, the address may be valid before ECLK goes low.
3. Address access time = $t_{Ecyc} - t_{EAD} - t_{EDSR}$.
4. Chip select access time = $t_{Ecyc} - t_{ECSD} - t_{EDSR}$.



NOTE: AS and DS timing shown for reference only.

Figure A–13. Chip Select Timing Diagram

Key to Figure A–13

(Abstracted from Table A–5; see table for complete notes)

Num	Characteristic	Symbol	Min	Max	Units
6	Clock High to Address, FC, SIZE, $\overline{RMC}$ Valid	t_{CHAV}	0	29	ns
8	Clock High to Address, FC, SIZE, $\overline{RMC}$ Invalid	t_{CHAZn}	0	—	ns
9	Clock Low to $\overline{AS}$, $\overline{DS}$, $\overline{CS}$ Asserted	t_{CLSA}	2	25	ns
11	Address, FC, SIZE, $\overline{RMC}$ Valid to $\overline{AS}$, $\overline{CS}$ (and $\overline{DS}$ Read) Asserted	t_{AVSA}	15	—	ns
12	Clock Low to $\overline{AS}$, $\overline{DS}$, $\overline{CS}$ Negated	t_{CLSN}	2	29	ns
13	$\overline{AS}$, $\overline{DS}$, $\overline{CS}$ Negated to Address, FC, SIZE Invalid (Address Hold)	t_{SNAI}	15	—	ns
14	$\overline{AS}$, $\overline{CS}$ (and $\overline{DS}$ Read) Width Asserted	t_{SWA}	100	—	ns
14A	$\overline{DS}$, $\overline{CS}$ Width Asserted Write	t_{SWAW}	45	—	ns
15[5]	$\overline{AS}$, $\overline{DS}$, $\overline{CS}$ Width Negated	t_{SN}	40	—	ns
18	Clock High to R/$\overline{W}$ High	t_{CHRH}	0	29	ns
20	Clock High to R/$\overline{W}$ Low	t_{CHRL}	0	29	ns
23	Clock High to Data Out Valid	t_{CHDO}	—	29	ns
25	$\overline{DS}$, $\overline{CS}$ Negated to Data Out Invalid (Data Out Hold)	t_{SNDOI}	15	—	ns
29[6]	$\overline{DS}$, $\overline{CS}$ Negated to Data In Invalid (Data In Hold)	t_{SNDI}	0	—	ns
29A[6, 7]	$\overline{DS}$, $\overline{CS}$ Negated to Data In High Impedance	t_{SHDI}	—	55	ns
46	R/$\overline{W}$ Width Asserted (Write or Read)	t_{RWA}	150	—	ns
53	Data Out Hold from Clock High	t_{DOCH}	0	—	ns
54	Clock High to Data Out High Impedance	t_{CHDH}	—	28	ns
55	R/$\overline{W}$ Asserted to Data Bus Impedance Change	t_{RADC}	40	—	ns

NOTES:

1. All AC timing is shown with respect to 20% V_{DD} and 70% V_{DD} levels unless otherwise noted.
5. If multiple chip selects are used, $\overline{CS}$ width negated (specification 15) applies to the time from the negation of a heavily loaded chip select to the assertion of a lightly loaded chip select. The $\overline{CS}$ width negated specification between multiple chip selects does not apply to chip selects being used for synchronous ECLK cycles.
6. These hold times are specified with respect to $\overline{DS}$ or $\overline{CS}$ on asynchronous reads and with respect to CLKOUT on synchronous reads. The user is free to use either hold time.
7. Maximum value is equal to (t_{cyc} / 2) + 25 ns.

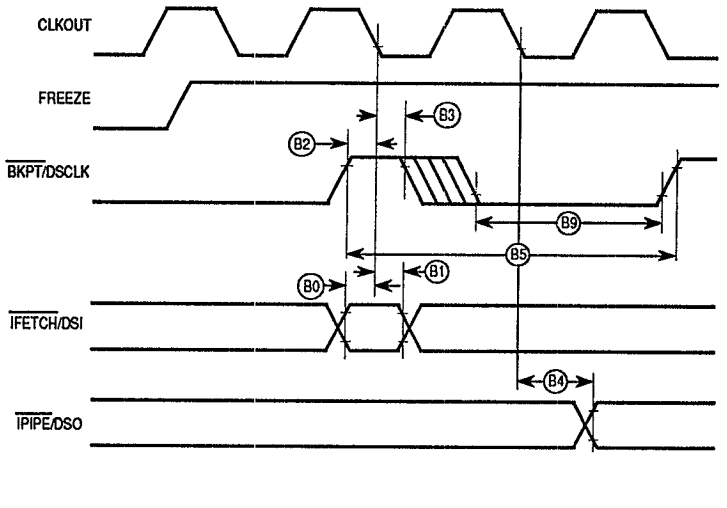


Figure A–14. Background Debugging Mode Timing Diagram — Serial Communication

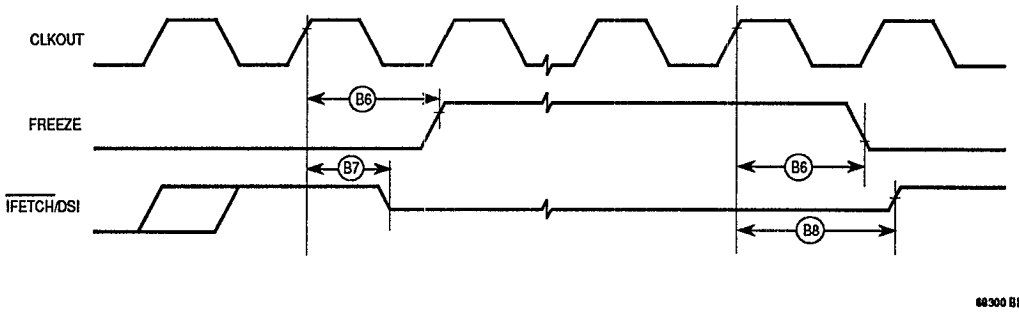


Figure A–15. Background Debugging Mode Timing Diagram — Freeze Assertion

Key to Figures A–14 and A–15

(Abstracted from Table A–6; see table for complete notes)

Num	Characteristic	Symbol	Min	Max	Unit
B0	DSI Input Setup Time	t_{DSISU}	15	—	ns
B1	DSI Input Hold Time	t_{DSIH}	10	—	ns
B2	DSCLK Setup Time	t_{DSCSU}	15	—	ns
B3	DSCLK Hold Time	t_{DSCH}	10	—	ns
B4	DSO Delay Time	t_{DSOD}	—	t_{cyc} + 25	ns
B5	DSCLK Cycle Time	t_{DSCCYC}	2	—	t_{cyc}
B6	CLKOUT High to FREEZE Asserted/Negated	t_{FRZAN}	—	50	ns
B7	CLKOUT High to $\overline{\text{IFETCH}}$ High Impedance	t_{IFZ}	—	50	ns
B8	CLKOUT High to $\overline{\text{IFETCH}}$ Valid	t_{IF}	—	50	ns
B9	DSCLK Low Time	t_{DSCLO}	1	—	t_{cyc}

NOTES:

1. All AC timing is shown with respect to 20% V_{DD} and 70% V_{DD} levels unless otherwise noted.

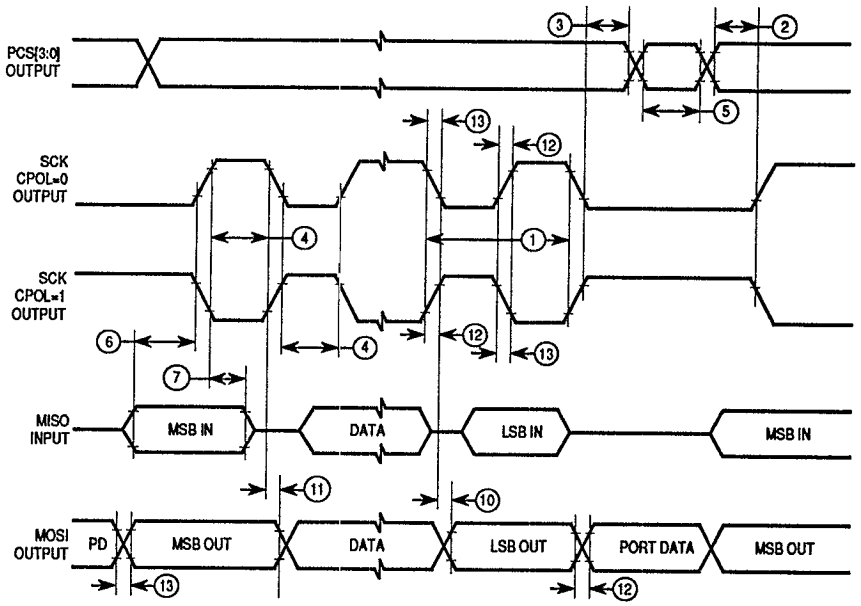


Figure A–16. QSPI Timing — Master, CPHA = 0

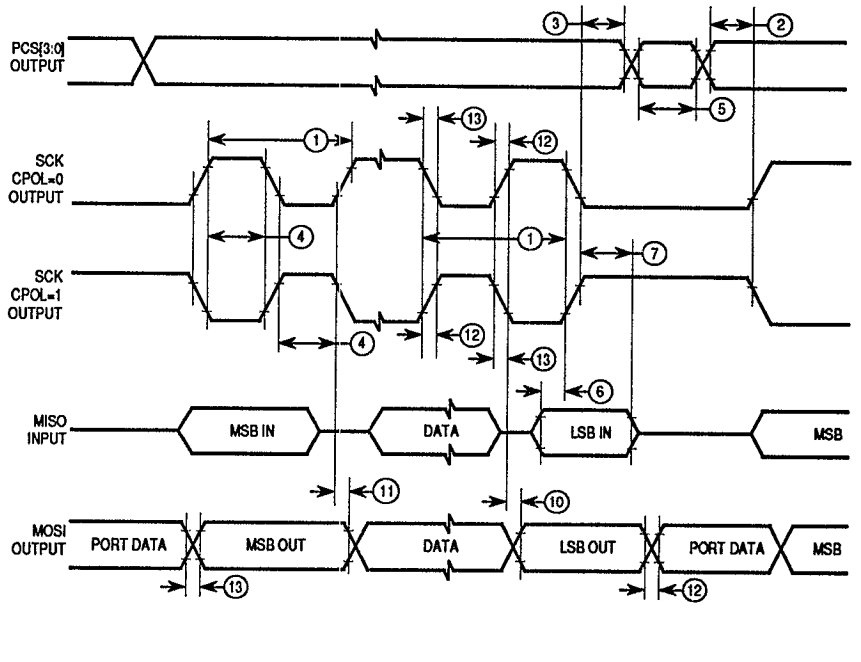


Figure A–17. QSPI Timing — Master, CPHA = 1

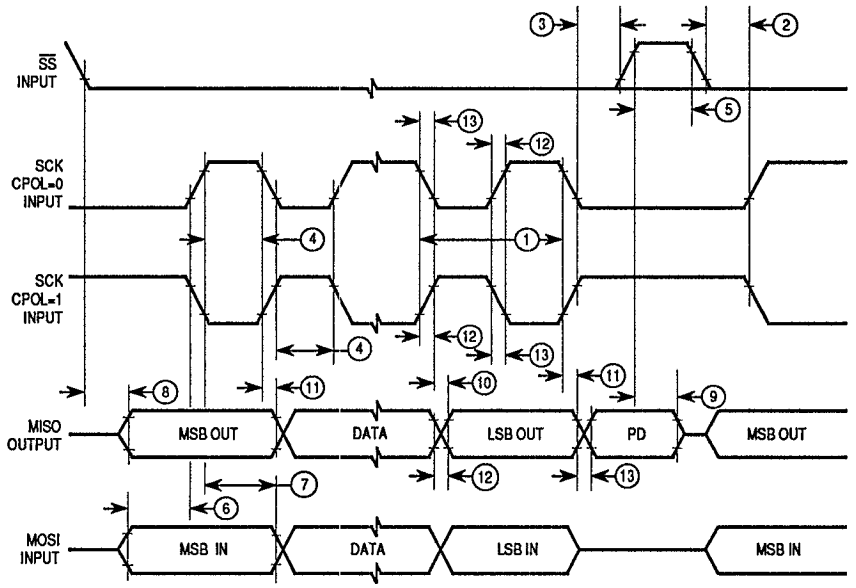
Key to Figures A–16 and A–17

(Abstracted from Table A–8)

Num	Function	Symbol	Min	Max	Unit
1	Master Cycle Time	t_{qcyc}	4	510	t_{cyc}
2	Master Enable Lead Time	t_{lead}	2	128	t_{cyc}
3	Master Enable Lag Time	t_{lag}	—	1/2	SCK
4	Master Clock (SCK) High or Low Time	t_{sw}	2 t_{cyc} – 60	255 t_{cyc}	ns
5	Master Sequential Transfer Delay	t_{td}	17	8192	t_{cyc}
6	Master Data Setup Time (Inputs)	t_{su}	30	—	ns
7	Master Data Hold Time (Inputs)	t_{hi}	0	—	ns
10	Master Data Valid (after SCK Edge)	t_v	—	50	ns
11	Master Data Hold Time (Outputs)	t_{ho}	0	—	ns
12	Rise Time Input Output	 t_{ri} t_{ro}	 — —	 2 30	 µs ns
13	Fall Time Input Output	 t_{fi} t_{fo}	 — —	 2 30	 µs ns

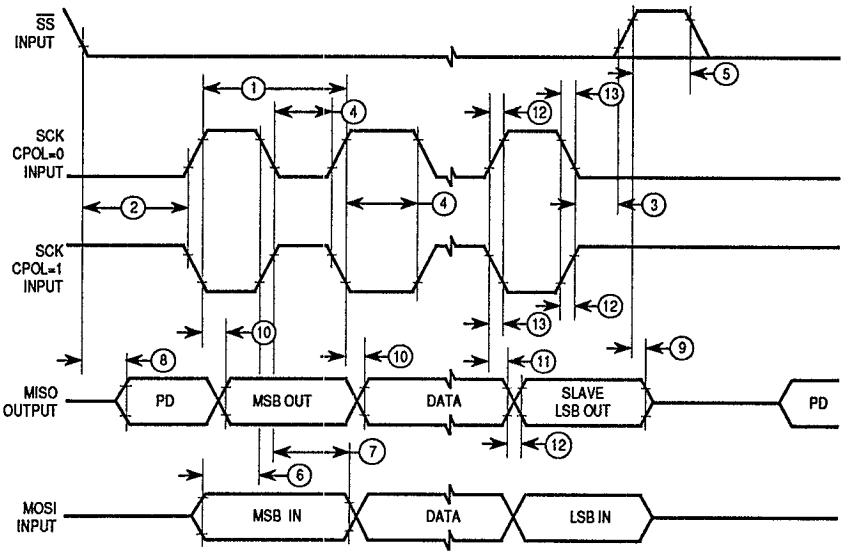
NOTES:

1. All AC timing is shown with respect to 20% V_{DD} and 70% V_{DD} levels unless otherwise noted.



68306 QSPI T SLV CPHA0

Figure A–18. QSPI Timing — Slave, CPHA = 0



68300 QSPI T SLV CPHA1

Figure A–19. QSPI Timing — Slave, CPHA = 1

Key to Figures A–18 and A–19

(Abstracted from Table A–8)

Num	Function	Symbol	Min	Max	Unit
1	Slave Cycle Time	t_{qcyc}	4	—	t_{cyc}
2	Slave Enable Lead Time	t_{lead}	2	—	t_{cyc}
3	Slave Enable Lag Time	t_{lag}	2	—	t_{cyc}
4	Slave Clock (SCK) High or Low Time[2]	t_{sw}	2 t_{cyc} – n	—	ns
5	Slave Sequential Transfer Delay (Does Not Require Deselect)	t_{td}	13	—	t_{cyc}
6	Slave Data Setup Time (Inputs)	t_{su}	20	—	ns
7	Slave Data Hold Time (Inputs)	t_{hi}	20	—	ns
8	Slave Access Time	t_a	—	1	t_{cyc}
9	Slave MISO Disable Time	t_{dis}	—	2	t_{cyc}
10	Slave Data Valid (after SCK Edge)	t_v	—	50	ns
11	Slave Data Hold Time (Outputs)	t_{ho}	0	—	ns
12	Rise Time Input Output	 t_{ri} t_{ro}	 — —	 2 30	 µs ns
13	Fall Time Input Output	 t_{fi} t_{fo}	 — —	 2 30	 µs ns

NOTES:

1. All AC timing is shown with respect to 20% V_{DD} and 70% V_{DD} levels unless otherwise noted.
2. In formula, n = External SCK rise + External SCK fall time

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