HC05

MC68HC05L11

TECHNICAL
DATA

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APPLICATION NOTE

Designing with the MC68HC05L11

Data Flow for DDIR=1 in LCD Interface

When designing with the MC68HC05L11, please note the following on the silicon with mask set no. 0E29D relating to the LCD interface.

When the DDIR bit is set, and the lower segment bank is selected, the least significant bit of the Horizontal Shift register ($2D & $2E) will be shifted out first at LD2 during the sequential W/R operation. However, it is found that the data coming out of LD2 is inverted. That is, if the Horizontal Shift register is loaded with $00, the data coming out of LD2 will be $FF. This is inconsistent to section 10.5.2 of the MC68HC05L11 Technical Data.

If the DDIR bit is set and the lower segment bank is selected, invert the data once before shifting out from LD2.

Choosing DDIR=1 is not necessary in most cases. Most designs do not need to choose this option.

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MC68HC05L11

High-density Complementary Metal Oxide Semiconductor (HCMOS) Microcontroller Unit

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TABLE OF CONTENTS

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LIST OF FIGURES

LIST OF TABLES

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1
GENERAL DESCRIPTION

The MC68HC05L11 HCMOS microcontroller is a member of the M68HC05 family of microcontrollers. This 8-bit microcontroller unit (MCU) contains a HC05 CPU core, RAM, ROM, I/O ports, a timer, a serial communications interface, a serial peripheral interface, a liquid crystal display control circuitry with auto display off feature, a real time clock with alarm, external parallel address & data bus for external memory access, two on-chip oscillators, and two tone generators. The MC68HC05L11 is particularly suitable for hand-held applications that require a LCD display of various sizes; e.g. PDA organizers.

1.1 Features

The following are some of the hardware and software features of the 100-pin MC68HC05L11 single-chip microcontroller.

Hardware Features

- 8-bit architecture
- Power saving Stop and Wait modes
- 448 bytes of on-chip RAM (including 64 bytes for stack)
- 3600 bytes of on-chip user ROM
- 38 bidirectional I/O lines
- LCD control circuitry with selection of multiplexing ratio from 32 to 256
- Capable of connecting to LCD drivers to increase LCD segment drive lines to 640
- Special hardware for graphics manipulation
- Memory Management Unit (MMU) to increase address bus from 16 to 23 bits for large memory systems
- 4 programmable chip-selects for small memory systems which has addressable locations up to 1 M-byte

- 8-bit bidirectional data bus
- Internal 16-bit timer
- Serial Communications Interface (SCI)
- Serial Peripheral Interface (SPI)
- 2 Programmable tone generators for melody generation or DTMF auto-dialling application
- 2 on-chip oscillators - 1 PLL oscillator for MCU, 1 crystal oscillator for real time clock and LCD driver
- 100 pins QFP or in die form
- 3.69 MHz bus speed at 5V supply
- Self-check mode

Software Features

- Similar to MC6800
- 8 x 8 unsigned multiply instruction
- Efficient use of program space
- Versatile interrupt handling
- True bit manipulation
- Addressing modes with index addressing for tables
- Efficient instruction set
- Memory mapped I/O
- Two power-saving standby modes
- Upward software compatible with the M146805 CMOS family

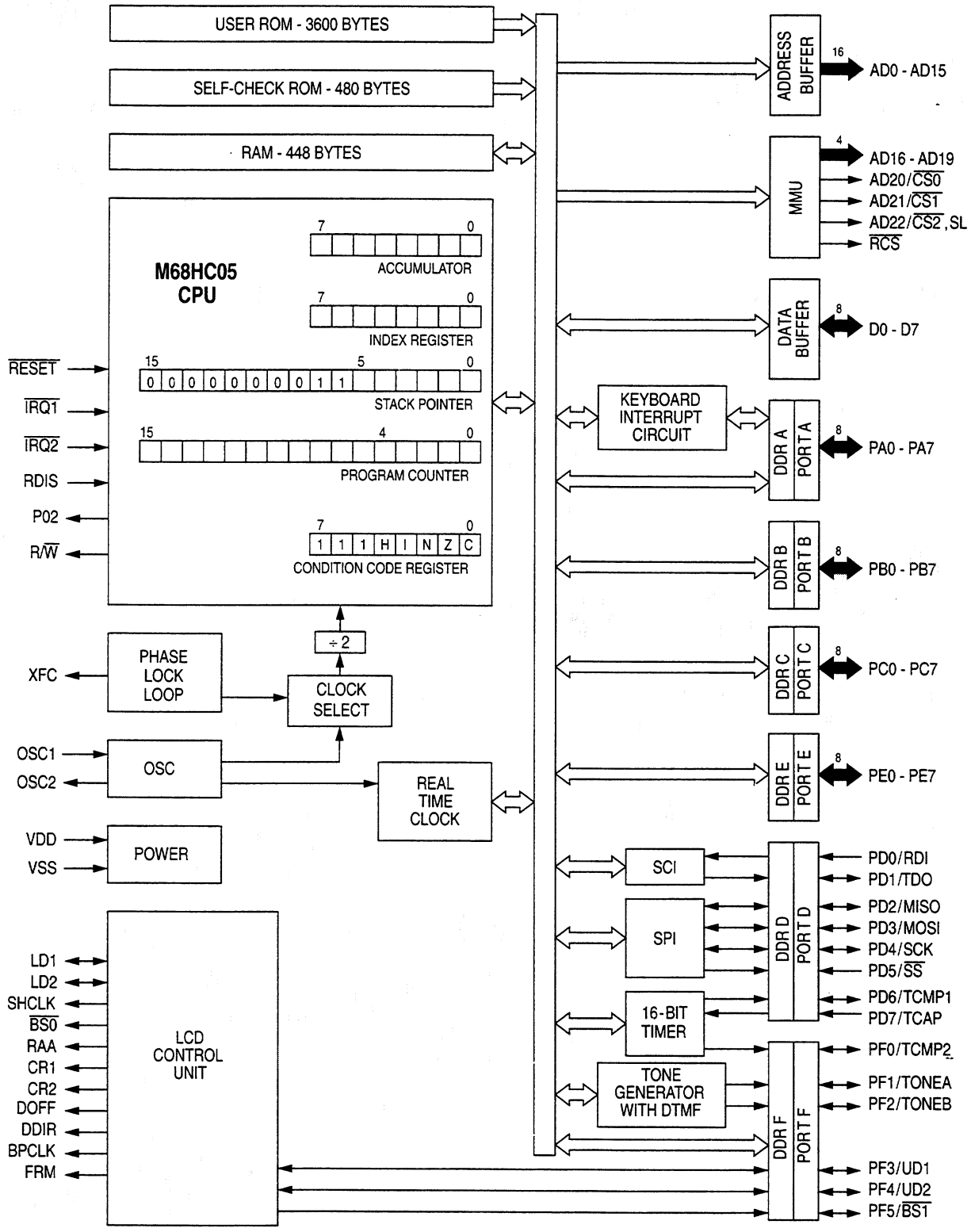

Figure 1-1 MC68HC05L11 Microcontroller Block Diagram

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2
PIN DESCRIPTIONS

This section provides a description of the functional pins of the MC68HC05L11 microcontroller.

2.1 Functional Pin Descriptions

PIN NAME	PIN No.	DESCRIPTION
VSS, VDD	25, 24	Power is supplied to the MCU using these two pins. VDD is power and VSS is ground.
$\overline{IRQ1}$, $\overline{IRQ2}$	20, 19	$\overline{IRQ1}$ and $\overline{IRQ2}$ are external interrupt inputs, and are software programmable to provide two interrupt triggering sensitivities. 1) Negative edge-sensitive triggering only, or 2) Negative edge-sensitive and level-sensitive triggering. See section 4.2.3.
$\overline{RESET}$	18	The active low $\overline{RESET}$ input is not required for start-up but can be used to reset the MCU internal state and provide an orderly software start-up procedure. See section 4.1.1.
OSC1, OSC2	16, 17	These pins provide connections to the on-chip oscillator. The crystal frequency is 32.768KHz. OSC1 may be driven by an external oscillator if an external crystal circuit is not used. See section 5.1.
PA0-PA7	75-82	These eight I/O lines comprise port A. The state of any pin is software programmable and all port A lines are configured as input during power on or external reset. See section 2.2 - Input/Output Programming.
PB0-PB7	67-74	These eight I/O lines comprise port B. The state of any pin is software programmable and all port B lines are configured as input during power on or external reset. See section 2.2 - Input/Output Programming.
PC0-PC7	100-7	These eight I/O lines comprise port C. The state of any pin is software programmable and all port C lines are configured as input during power on or external reset. See section 2.2 - Input/Output Programming.

PIN NAME	PIN No.	DESCRIPTION
PD0-PD7	59-66	These eight lines comprise port D. These port lines perform either as input ports or as peripheral I/O ports, depending on whether the SCI, the SPI and the Timer are activated. Each can be activated by the MCU individually. When the sub-systems are disabled, the corresponding lines become input port lines. A read of port D with sub-system enabled will always read as zero. See section 2.2 - Input/Output Programming.
RDI TDO	59 60	PD0 & PD1 become RDI & TDO lines respectively when the SCI is used. Refer to section 8 for detailed operation.
MISO MOSI SCK $\overline{SS}$	61 62 63 64	PD2-PD5 become MISO, MOSI, SCK & $\overline{SS}$ respectively when the Serial Peripheral Interface is activated by setting the SPE bit of the Serial Peripheral Control register (bit 6 of address $22).
TCMP1 TCAP	65 66	PORTI & TIMI bits of the General Control register (Bits 3 & 7 of address $25) configure PD6 & PD7 as TCMP1 & TCAP respectively for the programmable timer. See also definition for TCMP2. See section 7.1.
PE0-PE7	15-8	These eight I/O lines comprise port E. The state of any pin is software programmable and all port E lines are configured as input during power on or external reset. See section 2.2 - Input/Output Programming.
PF0-PF5	83-88	These six I/O lines comprise port F. The state of any pin is software programmable and all port F lines are configured as input during power on or external reset. See section 2.2 - Input /Output Programming.
TCMP2	83	If PORTI & TIMI bits of the General Control register (bits 3 & 7 of address $25 respectively) are set, PF0 is configured as TCMP2 for the 16-bit free running timer. See Section 7.1.
TONEA	84	If the TENA bit of Programmable TONEA register (bit 7 of address $26) is set, PF1 is configured for the programmable tone generator A output. See Section 7.2.1.
TONEB	85	If the TENB bit of Programmable TONEB register (bit 7 of address $27) is set, PF2 is configured for the programmable tone generator B output. See Section 7.2.2.
UD1 UD2 $\overline{BS1}$	86 87 88	If the DPAN bit of Control Miscellaneous register (bit 7 of address $32) is set, lines PF3 to PF5 are configured to serve a LCD split panel system. See Section 6.2.4. See also $\overline{BS0}$ & $\overline{BS1}$, and UD1 & UD2 definitions.
RDIS	22	This pin can be hard-wired to specify whether users choose to use the internal ROM and its vector sets or external memory and vectors. When this pin is pulled high, the internal 4K ROM (3.5K User ROM + self-check + vectors) are disabled. The MCU then accesses the external memory for both data and vectors. The internal ROM and vectors are enabled if this pin is pulled low. Similar to the SL pin, this pin is sampled once at the power-up or after an external reset.
P02	23	This is a bus clock output of the processor which indicates when the data on the external data bus is to be accessed by either the processor or peripherals. This clock is held low during Stop mode.

PIN NAME	PIN No.	DESCRIPTION
R/$\overline{W}$	21	R/$\overline{W}$ is a processor output which indicates the peripherals in which direction the data is to be passed over through the data bus. When R/$\overline{W}$ is high and the address bus is addressing memory beyond the first 512 bytes, the processor is reading data from external peripherals or memory. When R/$\overline{W}$ is low, the processor is writing data to its external peripherals or memory. R/$\overline{W}$ always stays high if the processor is accessing the lowest 512 bytes of the memory map (except location $31 with bit 7 of $32 clear, where the processor treats this location as an external peripheral). R/$\overline{W}$ also stays high if the processor is in the Stop mode.
AD0-AD22	35-57	AD0-AD22 is a 23-bit wide address bus from the processor AD0-AD19 are dedicated address lines while AD20-AD22 can be used as programmable chip-selects $\overline{CS0}$-$\overline{CS2}$ for small systems. These address lines will stay low if the CPU accesses the internal 512 bytes memory.
$\overline{CS0}$-$\overline{CS2}$	55-57	These pins are programmable chip selects for a small system configuration. These pins will stay high if the CPU enters Stop mode.
SL	57	This pin is sampled once at power-up or after an external reset. If this pin was found high, a small system is defined, with support for 1M-bytes of memory. If sampled low, a large system is defined, with support for 8M-bytes of memory.
$\overline{RCS}$	58	This is a dedicated programmable chip-select for external memory access, e.g. for static RAM. See section 11 for more details. This chip-select will stay high if the CPU is in the Stop mode (see section 6).
D0-D7	27-34	D0-D7 is an 8-bit bidirectional data bus used for the transfer of data between external peripherals/memory and the processor. They will be in high impedance when R/$\overline{W}$ is high or when the address bus is selecting the internal locations of the MCU. However, there is an exception for location $31, the processor treats this location as an external peripheral if bit 7 of address $32 is clear (MSW of Control Miscellaneous register). In this case, valid data may be found on D0-D7 when the processor is accessing location $31.
BPCLK	97	This is a periodic signal for dot row display synchronization to the LCD drivers. See Section 10.6.
FRM	98	This is a periodic reset signal for frame display synchronization to the LCD drivers. See section 10.6.
LD1, LD2	89, 90	Together with UD1 and UD2, these are the bidirectional serial lines which carry LCD data to and from the segment driver(s). See Section 10.3.
$\overline{BS0}$	91	Together with $\overline{BS1}$, these are active low output strobes for selecting banks of segment drivers. Bits 4, 5, & 6 of address $32 (BS0, BS1 & DPAN of Control Miscellaneous register) are the control bits. These strobe pins are asserted only during transfers. See Section 10.5.2.
SHCLK	92	This is an output signal for serial LCD data synchronization. Together with LD1, LD2 and $\overline{BS0}$ these pins exercise an SPI like communication protocol with the segment drivers, with SHCLK as the synchronization signal. SHCLK also exercises the same protocol with UD1, UD2 and $\overline{BS1}$ if the upper panel is selected. See Section 10.
RAA	93	This is an output strobe to the segment driver(s) indicating that a valid data is on D0-D7. (For detailed timing, refer to Appendix B).
CR1, CR2	95, 94	These output signals specify that the valid data on D0-D7 is either a row address or a control code for the segment drivers. (See Appendix B)

2

PIN NAME	PIN No.	DESCRIPTION
DDIR	99	This is an output signal to the segment driver to set the direction of data flow in the bidirectional lines UD2, UD1, LD2 and LD1. If this pin is low, the data enters the MCU from UD1 or LD1 and exits at UD2 or LD2. The flow direction is reversed if this pin is high. This pin is controlled by the DDIR bit in the Control Miscellaneous register (bit 3 of address $32).
DOFF	96	This is an output pin to turn off LCD display. It is the complement of bit DON at address $32. The LCD Timing Generator is also turned off as soon as the DON bit found cleared. See section10.
XFC	26	This pin provides connection between an external capacitor and the internal phase lock loop circuit. See Section 5.1.

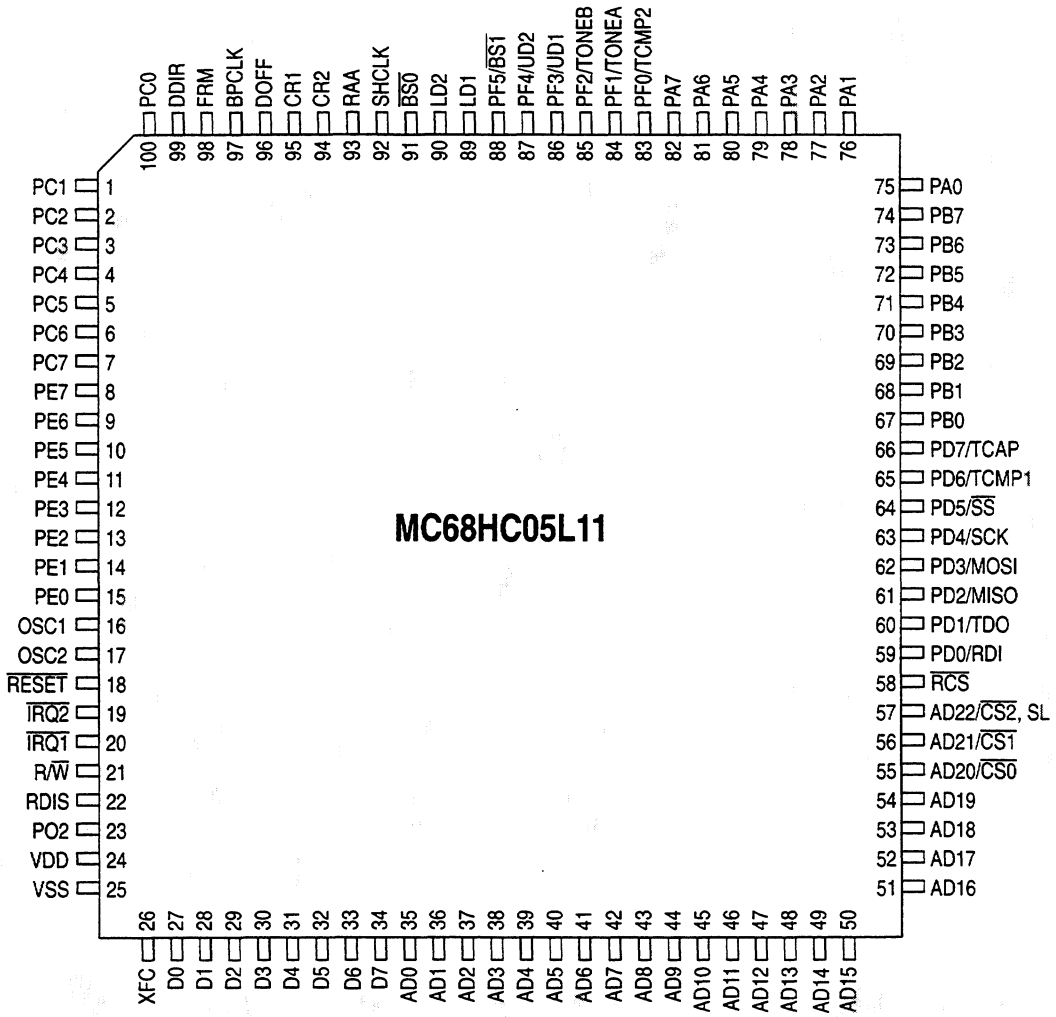


Figure 2-1 100-pin QFP Pin Assignment

2.2 Input/Output Programming

2.2.1 Parallel Ports

Individual pin of ports A#, B, C, E and F* may be programmed as an input or an output under software control. The direction of the pins is determined by the state of corresponding bit in the port data direction register (DDR). Each 8-bit port has an associated 8-bit data direction register. Any port A, B, C, E or F (PF0-PF5) pin is configured as an output if its corresponding DDR bit is set to a logic one. A pin is configured as an input if its corresponding DDR bit is cleared to a logic zero. At power-on or reset, all DDRs are cleared, which configure all port A, B, C, E and F pins as inputs. The data direction registers are capable of being written to or read by the processor. Table 2-1 shows the read write operation on an I/O pin with different DDR. Notice that during the programmed output state, a read of the data register actually reads the value of the output data latch and not the I/O pin.

When KEYE (bit 6 of $25) is set and port A is configured as an input, there will be approx. 250KΩ pull-up resistor associated with each pin of port A and this implies port A DDR bit set to one to become an output port will override the KEYE bit.

* PF3-PF5 become pins to serve the LCD split panel if bit DPAN of address $32 is set. PF1 and PF2 become pins to output audio tones if bits TENA and TENB of addresses $26 and $27 are set respectively. PF0 becomes TCMP2 for the 16-bit free running timer if bits TIMI and PORTI are set.

2.2.2 Fixed Ports

Port D (PD0-PD7) is an 8-bit fixed input that continually monitors the external pins whenever the SCI, SPI, TIMER systems are disabled. During power-on reset or external reset all eight bits become valid input ports because all special function output drivers are disabled. No data register is associated with PD0-PD7 when it is used as an input.

PD0-PD7 will perform as sub-systems' (Timer, SCI, SPI) functional pins when the corresponding sub-systems are selected. Refer to section 7 for Programmable Timer, section 9 for Serial Peripheral Interface, and section 8 for Serial Communications Interface.

It is recommended that all unused input pins be tied to an appropriate logic level (e.g., either V_{DD} or V_{SS}).

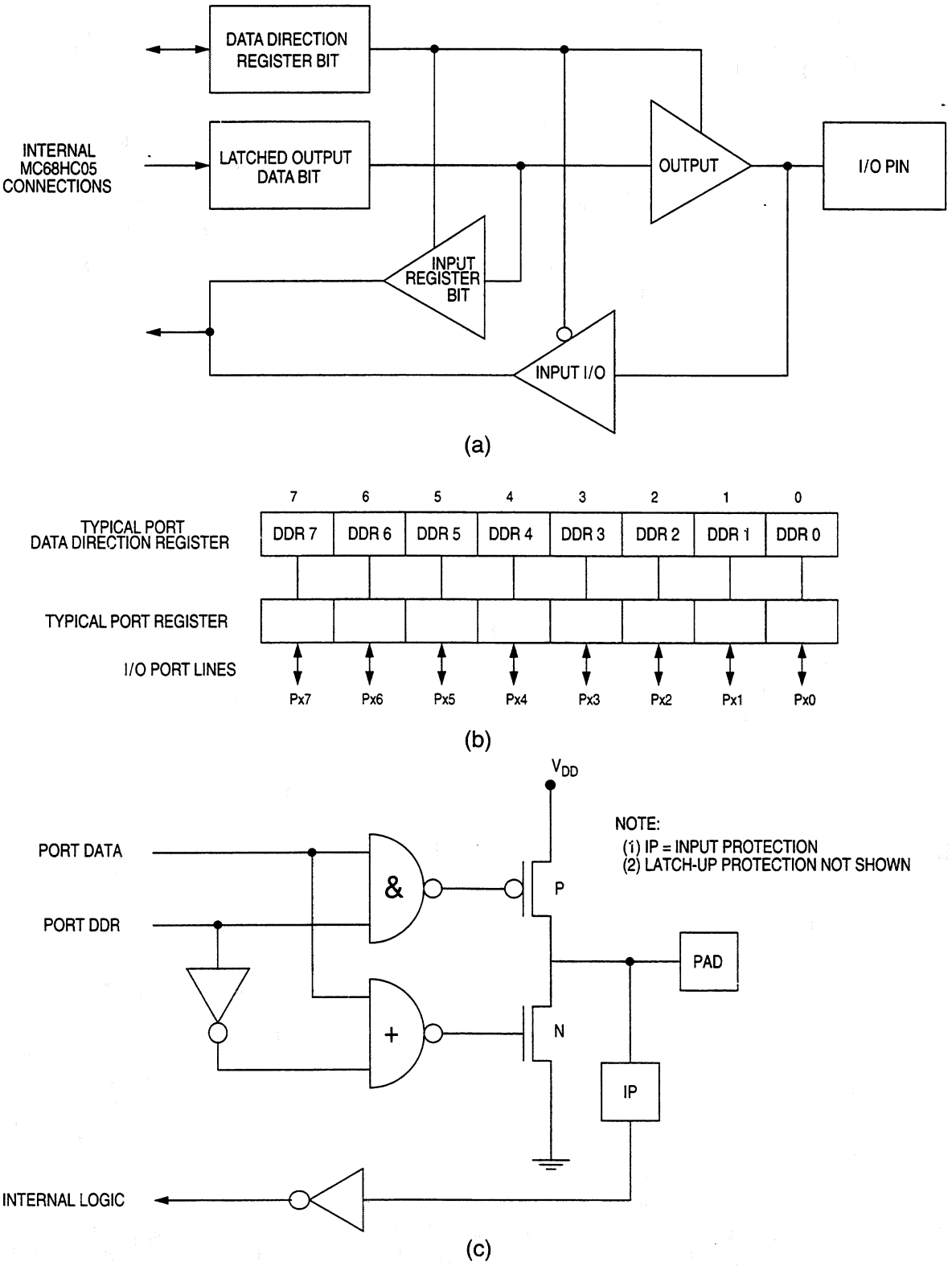


Figure 2-2 Parallel Port I/O Circuitry

3

3 MEMORY

This section describes the organization of the on-chip memory and miscellaneous control registers.

3.1 Memory Map

The CPU can address 1 M-bytes of memory space and up to 8 M-bytes with MMU enabled. The ROM portion of memory holds the program instructions, fixed data, user-defined vectors, and interrupt service routines. The RAM portion of memory holds variable data. I/O registers are memory-mapped so that the CPU can access their locations in the same way that it accesses all other memory locations. Figure 3-1 shows the Memory Map for the MC68HC05L11.

3.2 Input/Output Section

The first 64 addresses of memory space, $0000-$003F, are the I/O section. These are the addresses of the I/O control registers, status registers, and data registers.

3.3 RAM

The 448 addresses from $0040-$01FF are RAM locations. The CPU uses 64 RAM addresses, $00C0-$00FF, as the stack. Before processing an interrupt, the CPU uses five bytes of the stack to save the contents of the CPU registers. During a subroutine call, the CPU uses two bytes of the stack to store the return address. The stack pointer decrements during pushes and increments during pulls.

Note: Be careful when using nested subroutines or multiple interrupt levels. Once the stack pointer passes $00C0, it wraps round back to $00FF.

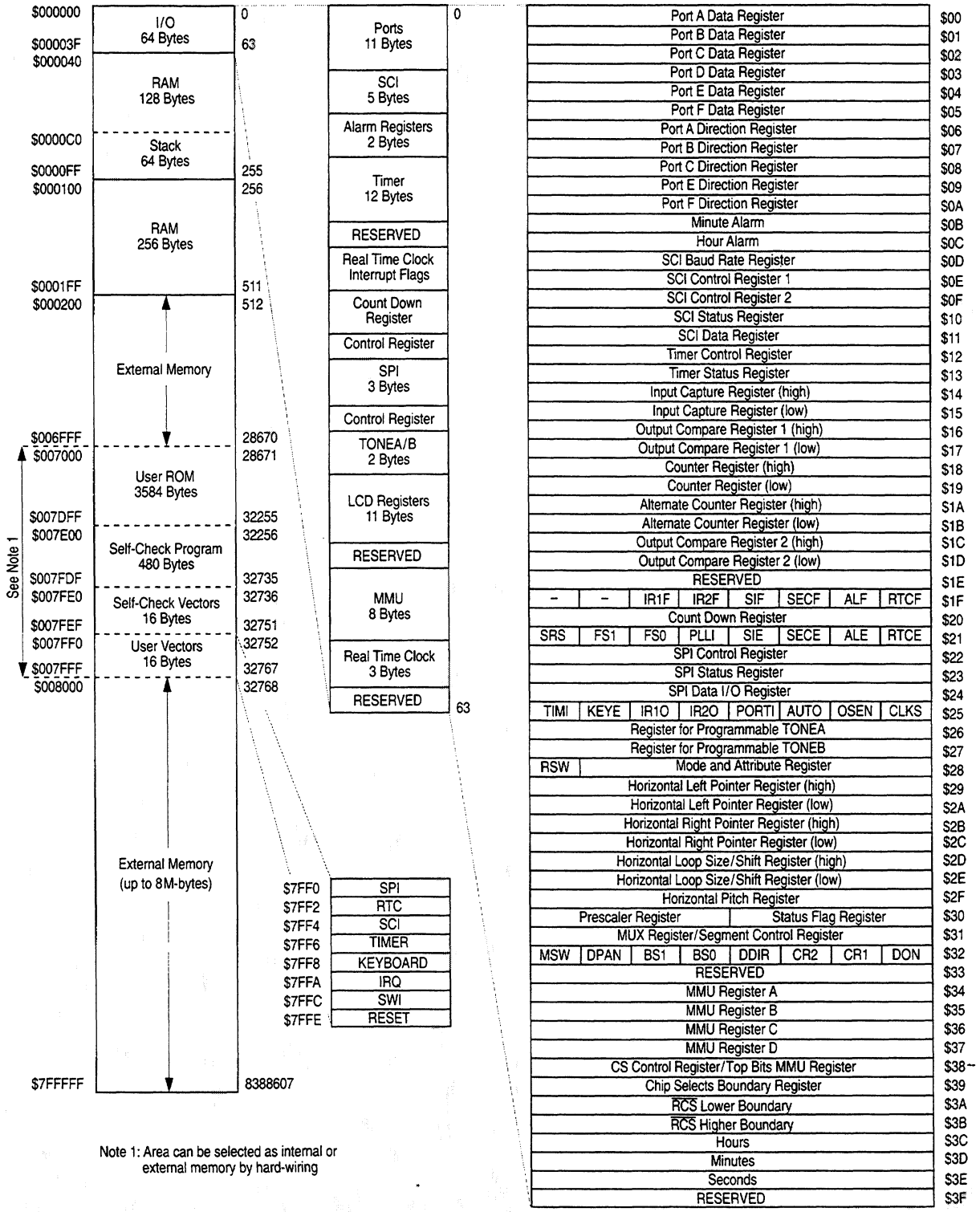


Figure 3-1 MC68HC05L11 Memory Map

3.4 Miscellaneous Registers

Address $21, $25, and $1F are the miscellaneous registers of the MC68HC05L11 MCU. They are described below.

3.4.1 General Control Register

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on Reset
$25	TIMI	KEYE	IR1O	IR2O	PORTI	AUTO	OSEN	CLKS	0000 0000

CLKS

1 (set) – PLL clock for CPU

0 (clear) – 16.384 KHz clock from 32 KHz oscillator

OSEN

1 (set) – Keep the 32 KHz oscillator on during Stop mode for non-interrupt Real Time Clock operation

0 (clear) – Disable 32 KHz oscillator during Stop mode

AUTO

1 (set) – Enable auto display off feature

0 (clear) – Disable auto display off feature

IR2O

1 (set) – Negative edge-sensitive triggering only for IRQ2

0 (clear) – Both negative edge-sensitive and level-sensitive triggering for IRQ2

IR1O

1 (set) – Negative edge-sensitive triggering only for IRQ1

0 (clear) – Both negative edge-sensitive and level-sensitive triggering for IRQ1

KEYE

1 (set) – Keyboard interrupt enable

0 (clear) – Keyboard interrupt disable

BIT 7	BIT 3				
TIMI	PORTI	TIMER	PD6	PD7	PF0
0	0	Disabled	INPUT	INPUT	INPUT
0	1	Enabled	NPUT	NPUT	NPUT
1	0	Enabled	TCAP	TCMP1	INPUT
1	1	Enabled	TCAP	TCMP1	TCMP2

3.4.2 Clock Status and Control Register

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on Reset
$21	SRS	FS1	FS0	PLLI	SIE	SECE	ALE	RTCE	0000 0000

RTCE

1 (set) – Real time clock once a day interrupt enable

0 (clear) – Real time clock once a day interrupt disable

ALE

1 (set) – Alarm interrupt enable

0 (clear) – Alarm interrupt disable

SECE

1 (set) – Real time clock once a second interrupt enable

0 (clear) – Real time clock once a second interrupt disable

PLLI

1 (set) – Indicate PLL is locked (clock from PLL is stable)

0 (clear) – Indicate PLL is unlocked

FS1, FS0

00 = 0.3072 MHz internal bus frequency
01 = 1.2288 MHz internal bus frequency
10 = 2.4576 MHz internal bus frequency
11 = 3.6864 MHz internal bus frequency

SIE, SRS

0X = 1/64 or 1/128 second Interrupt disable
10 = 64 times per second interrupt enable
11 = 128 times per second interrupt enable

3.4.3 Interrupt Status Register

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on Reset
$1F	–	–	IR1F	IR2F	SIF	SECF	ALF	RTCF	0000 0000

RTCF

1 (set) – Indicates once a day interrupt has occurred. After serving this interrupt, it is the user's responsibility to clear this bit, otherwise the CPU will keep on serving this once a day interrupt when a new RTC interrupt occurs (even there is no once a day interrupt occurs).

0 (clear) – Indicates once a day interrupt has not occurred.

ALF

1 (set) – Indicates alarm interrupt has occurred. After serving this interrupt, it is the user's responsibility to clear this bit, otherwise the CPU will keep on serving this alarm interrupt when a new RTC interrupt occurs (even there is no alarm interrupt occurs).

0 (clear) – Indicates alarm interrupt has not occurred.

SECF

1 (set) – Indicates once a second interrupt has occurred. After serving this interrupt, it is responsibility to clear this bit, otherwise the CPU will keep on serving this once a second interrupt when a new RTC interrupt occurs (even there is no once a second interrupt occurs).

0 (clear) – Indicates once a second interrupt has not occurred.

SIF

1 (set) – Indicates a 64 times or 128 times per second interrupt has occurred. After serving this interrupt, it is the user's responsibility to clear this bit, otherwise the CPU will keep on serving this interrupt when a new RTC interrupt occurs.

0 (clear) – Indicates 64 times or 128 times per second interrupt has not occurred.

IR2F

1 (set) – Indicates IRQ2 interrupt has occurred. After serving this interrupt, it is the user's responsibility to clear this bit, otherwise the CPU will keep on serving IRQ2 interrupt when a new IRQ interrupt occurs (even there is no IRQ2 interrupt occurs).

0 (clear) – Indicates IRQ2 interrupt has not occurred.

IR1F

1 (set) – Indicates IRQ1 interrupt has occurred. After serving this interrupt, it is the user's responsibility to clear this bit, otherwise the CPU will keep on serving IRQ1 interrupt when a new IRQ interrupt occurs (even there is no IRQ1 interrupt occurs).

0 (clear) – Indicates IRQ1 interrupt has not occurred.

Flags in location $1F will be set if the corresponding events occur, irrespective of their interrupt enable bit settings. Writing "0" to these bits in $1F will reset their states; while their states remain unchanged if "1" are written to them. E.g. The RTCF flag can be cleared by writing 11111110 binary to $1F without altering other flags. Notice that the BCLR instruction should not be used to manipulate flags of $1F because this may accidentally clear other flags. Since the BCLR instruction will read in the corresponding register content, modify the designated bit and write it back to the register, any flags set within this small time frame will be cleared by the latter write.

All bits in addresses $1F, $21 and $25 are readable and writable, except bit 4 of address $21 (PLLI of Timer Status and Control Register), which is read-only. All bits are cleared during power-up or after an external reset.

4
RESETS AND INTERRUPTS

4.1 RESETS

The MC68HC05L11 has two hardware resets - an active low external reset pin ($\overline{\text{RESET}}$) and a power-on reset function.

4.1.1 $\overline{\text{RESET}}$ Pin

The $\overline{\text{RESET}}$ input pin is used to reset the MCU to provide an orderly software start-up procedure. When using the external reset, the $\overline{\text{RESET}}$ pin must stay low for a minimum of 1.5tcyc. The $\overline{\text{RESET}}$ pin contains an internal Schmitt Trigger as part of its input to improve noise immunity.

4.1.2 Power-On Reset (POR)

The power-on reset occurs when a positive transition is detected on the supply voltage, V_{DD}. The power-on reset is used strictly for power-up conditions, and should not be used to detect any drops in the power supply voltage. There is no provision for a power-down reset. The power-on circuitry provides a 1024 tcyc delay from the time that the oscillator becomes active. If the external $\overline{\text{RESET}}$ pin is low at the end of the 1024 tcyc time out, the processor remains in the reset condition until $\overline{\text{RESET}}$ goes high. The user must ensure that V_{DD} has risen to a point where the MCU can operate properly prior to the time the 1024 POR cycles have elapsed. If there is doubt, the external $\overline{\text{RESET}}$ pin should remain low until such time that V_{DD} has risen to the minimum operating voltage specified.

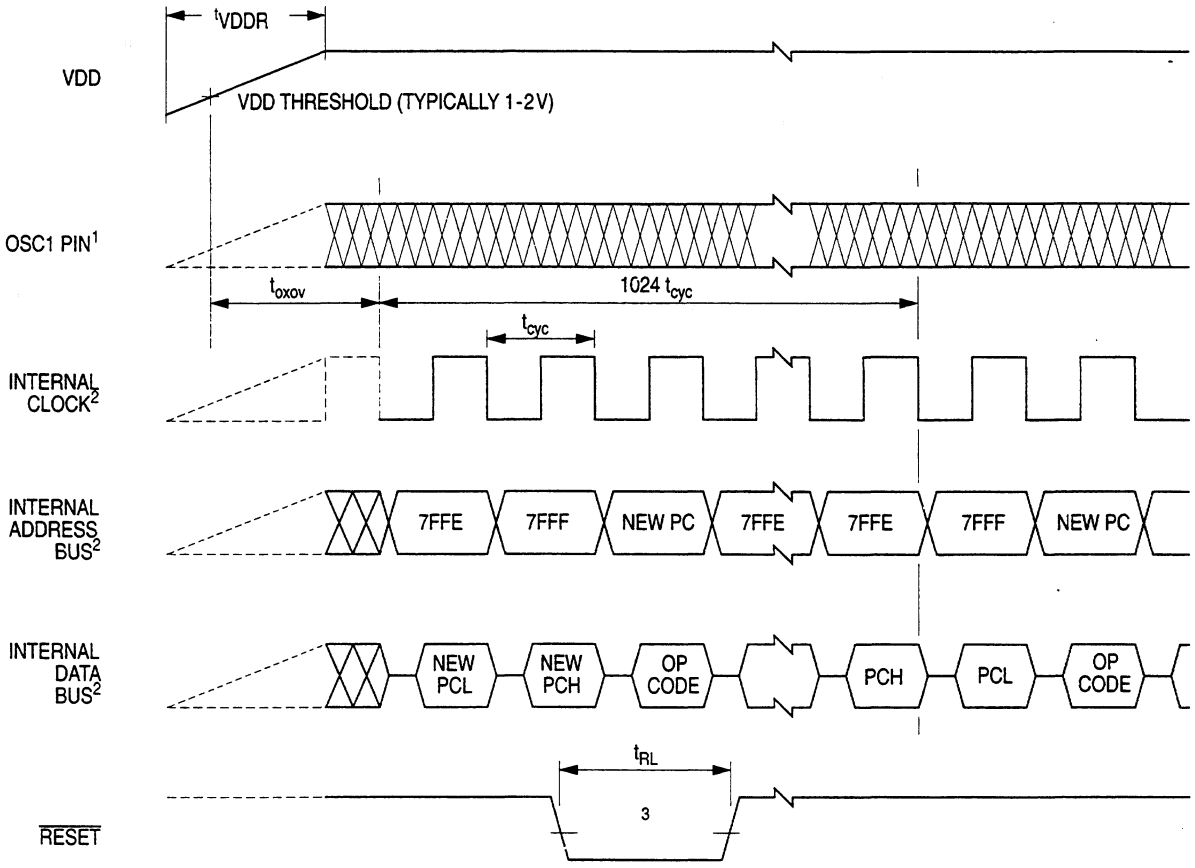
Table 4-1 shows the internal circuit actions on reset, but not necessary in order of occurrence.

Table 4-1 Reset Action on Internal Circuit

	DEFAULT CONDITIONS AFTER RESET
1	Timer prescaler resets to zero state.
2	Timer counter configures to $FFFC.
3	Timer output compare 1 and 2 (TCMP1 & TCMP2) bits resets to zero.
4	All timer interrupt enable bits cleared (ICIE1, OCIE1, ICIE2 and TOIE) to disable timer interrupts. The OLVL1 and OLVL2 timer bits are also cleared by reset.
5	All data direction registers cleared to zero (default as inputs).
6	Count down register is set to 3.
7	Stack pointer configured to $00FF.
8	Internal address bus forced to restart vector ($7FFE-$7FFF).
9	I bit of condition code register set to logic 1.
10	STOP latch cleared.
11*	External interrupt latch cleared.
12	WAIT latch cleared.
13	SCI disabled (serial control bits TE=0 and RE=0). Other SCI bits cleared by reset include: TIE, TCIE, RIE, ILIE, RWU, SBK, RDRF, IDLE, OR, NF, and FE.
14	Set serial status bits TDRE and TC.
15	Cleared all serial interrupt enable bits (TIE and TCIE).
16	SCI prescaler rate control bits are cleared (SCP0 and SCP1).
17	Keyboard interrupt enable bit is cleared.
18	RTC interrupt enable bit is cleared. Other RTC bits cleared are RTCF, ALF, and SECF.
19	SPI disabled (serial output enable control bit SPE=0). Other SPI bits cleared are SPIE, MSTR, SPIF, WCOL, and MODF.
20	Serial interrupt enable bit cleared (SPIE).
21	SPI system configured to slave mode.
22	All bits in address $1F, $21, and $22 are cleared.
23	The following addresses are set: $34=$04, $35=$05, $36=$06, $37=$07.
24	Programmable TONEA and TONEB registers ($26 & $27) are cleared.
25	SL and RDIS pins are sampled.
26	MMU registers are set to point at the upper 32K memory map.
27	All LCD registers except the segment control register are cleared.
28	Lower boundary for $\overline{CS0}$ and all other higher boundaries are cleared.
29	Higher boundary for $\overline{CS0}$ set to $7 and all other lower boundaries to $FF.
30	Addresses $3A and $3B set to $FF.

* time-out still occurs

listed numbers do not represent order of occurrence.



NOTES:
1. OSC1 is not meant to represent frequency. It is only used to represent time.
2. Internal clock, internal address bus, and internal data bus signals are not available externally.
3. Next rising edge of internal clock after rising edge of $\overline{\text{RESET}}$ initiates reset sequence.

Figure 4-1 Power-On Reset and $\overline{\text{RESET}}$ Timing

4.2 INTERRUPTS

The MC68HC05L11 is capable of handling eight types of interrupt, seven hardware and one software. The interrupt mask bit ("I" bit in the Condition Code register), if set, blocks all interrupts except the software interrupt, SWI. Interrupts such as Timer, RTC, SCI and SPI have several flags which will cause the interrupt. Generally, interrupt flags are found in "read only" status registers (except RTC) while their enables are in associated control registers. They are never mixed in the same register. If the enable bit is "0", it blocks the interrupt from occurring but does not inhibit the flag from being set. RESET clears all enable bits. The general sequence for clearing an interrupt is a software sequence of reading the status register while the flag is set followed by a read or write of an associated register (except RTC and IRQs). When any of these interrupts occur, and if enabled, normal processing is suspended at the end of the current instruction execution. The state of the machine is pushed onto the stack (see Figure 4-2 for stacking order) and the appropriate vector points to the starting address of the interrupt service routine (see Table 4-2). Also, the interrupt mask bit in the condition code register is set. This masks further interrupts. At the completion of the service routine, the software normally contains an RTI instruction which, when executed, restores the machine state and continues executing the interrupted program. Figure 4-3 shows the program flow for hardware interrupts.

Note: The interrupt mask bit (I bit) will be cleared if and only if the corresponding bit stored on the stack is zero.

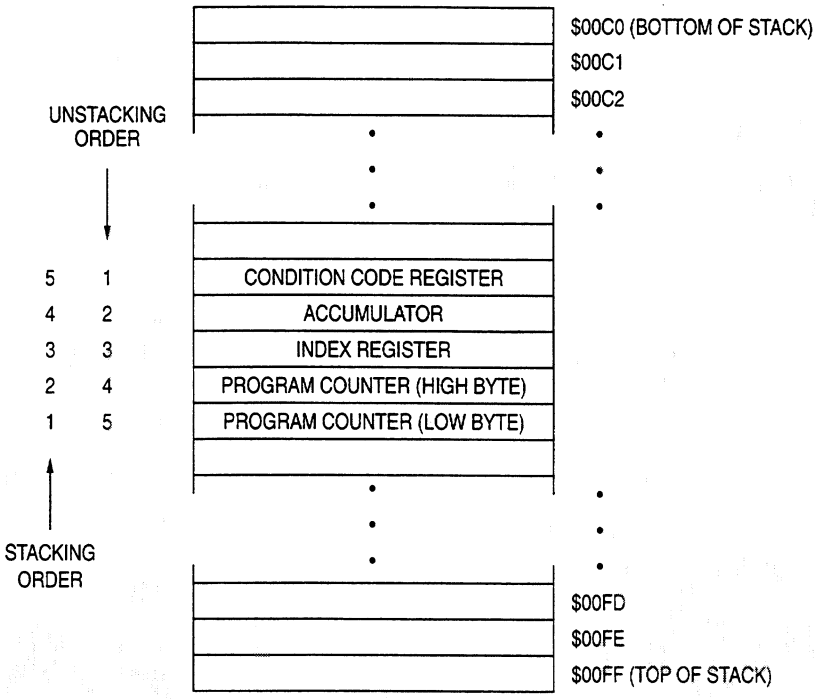


Figure 4-2 Interrupt Stacking Order

Table 4-2 Reset/Interrupt Vector Addresses

Register	Flag Name	Interrupt	CPU Interrupt	Vector Address
–	–	Reset	$\overline{\text{RESET}}$	$7FFE-$7FFF
–	–	Software	SWI	$7FFC-$7FFD
Interrupt Status	IR1F, IR2F	External Interrupt	$\overline{\text{IRQ}}$	$7FFA-$7FFB
General Control	X	Keyboard	KEYBOARD	$7FF8-$7FF9
Timer Status	ICF	Input Capture	TIMER	$7FF6-$7FF7
	OCF1, OCF2	Output Compare 1, 2		
	TOF	Timer Overflow		
SCI Status	TDRE	Transmit Buffer Empty	SCI	$7FF4-$7FF4
	TC	Transmit Complete		
	RDRF	Receive Buffer Full		
	IDLE	Idle Line Detect		
	ORO	Overrun		
RTC Status	SECF	Per Second	RTC	$7FF2-$7FF3
	ALF	Alarm		
	RTCF	Per Day		
	SIF	1/64 or 1/128 Second		
SPI Status	SPIF	Data Transfer Complete	SPI	$7FF0-$7FF1
	MODF	Mode Fault		

4.2.1 Hardware Controlled Sequences

The following three functions are not strictly interrupts, however, they are tied very closely to the interrupts. These functions are $\overline{\text{RESET}}$, STOP, WAIT.

1) $\overline{\text{RESET}}$ The $\overline{\text{RESET}}$ input pin causes the program to go to its starting address. This address is specified by the contents of memory locations $7FFE and $7FFF. The interrupt mask of the condition code register is also set. Much of the MCU is configured to some known state as described in Table 4-1.

2) STOP If the user chooses to use an interrupted RTC, the STOP instruction causes the oscillator to be turned off and the processor "sleeps" until an external interrupt ($\overline{\text{IRQ}}$), Keyboard interrupt or $\overline{\text{RESET}}$ occurs. If non-interrupted RTC is used, only the internal processor clock is turned off. See section 6 on Low Power Modes.

3) WAIT The WAIT instruction causes all processor clocks to stop, but leaves the RTC, Timer, SCI and SPI clocks running. This "rest" state of the processor can be cleared by $\overline{\text{RESET}}$, an external interrupt ($\overline{\text{IRQ1}}$ or $\overline{\text{IRQ2}}$), RTC, Keyboard, Timer, SCI or SPI interrupt. There are no special wait vectors for these individual interrupts. See section 6 on Low Power Modes.

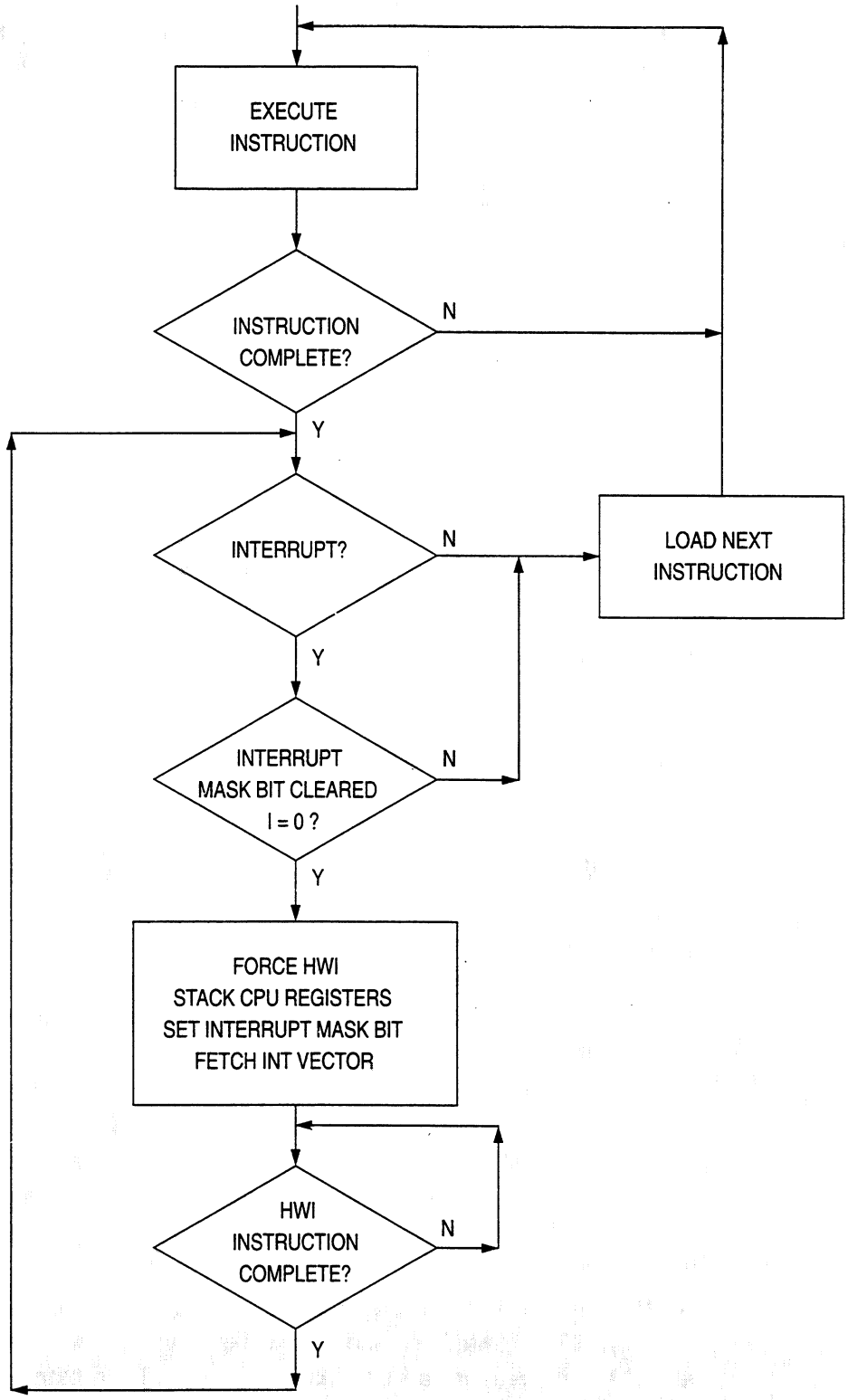


Figure 4-3 Hardware Interrupt Flowchart

4.2.2 Software Interrupt (SWI)

The software interrupt is an executable instruction. The action of the SWI instruction is similar to the hardware interrupts. The SWI is executed regardless of the state of the interrupt mask in the condition code register. The service routine address is specified by the contents of memory location $7FFC and $7FFD.

4.2.3 External Interrupt ($\overline{IRQ1}$ & $\overline{IRQ2}$)

When the signals of the external interrupt pins ($\overline{IRQ1}$, $\overline{IRQ2}$) satisfy the condition selected by the IR1O and IR2O in the general control register (bits 4 & 5 of location $25) then an external interrupt occurs. The actual processor interrupt is generated only if the interrupt mask bit of the condition code register is also cleared. When the interrupt is recognized, the current state of the processor is pushed onto the stack and the interrupt mask bit in the condition code register is set. This masks further interrupts until the present one is serviced. The service routine address is specified by the contents of $7FFA and $7FFB. The interrupt logic recognizes negative edge transitions and pulses (special case of negative edges) on the external interrupt lines. Figure 4-4 shows both a block diagram and timing for the interrupt lines ($\overline{IRQ1}$, $\overline{IRQ2}$) to the processor. This method is used as if pulses on the interrupt line spaced far enough apart to be serviced. The minimum time between pulses is equal to the number of cycles required to execute the interrupt service routine plus 21 cycles. Once a pulse occurs, the next pulse should not occur until the MCU software has exited the routine (an RTI occurs). Users are responsible to clear the interrupt flag IR1F or IR2F before exit from this service routine. Otherwise the same interrupt will cause the MCU to enter this service routine again as soon as it exits from the routine.

Note: The internal interrupt latch is cleared in the first part of the service routine; therefore, one (and only one) external interrupt pulse could be latched during t_{ILIL} and serviced as soon as the I bit is cleared.

4.2.4 Timer Interrupt

Four timer interrupt flags are found in the four most significant bits of the Timer Status register (TSR) at location $13. All four interrupts will vector to the same address at location $7FF6-$7FF7.

Timer Status Register

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on Reset
$13	ICF	OCF1	TOF	OCF2	0	0	0	0	uuuu 0000

Each flag bit is defined as follows:

OCF2 - Output Compare Flag 2

OCF2 is set when the Output Compare register 2 matches the Counter register. It is cleared by reading the TSR (with OCF2 set) and then accessing the least significant byte of the Output Compare register 2 ($1D). Reset does not affect this bit.

TOF - Timer Overflow Flag

TOF is set during the Counter transition of $FFFF to $0000. It is cleared by reading the TSR (with TOF set) followed by reading the least significant byte of the counter ($19). Reset does not affect this bit.

OCF1 - Output Compare Flag 1

OCF1 is set when the Output Compare register 1 matches the Counter register. It is cleared by reading the TSR (with OCF1 set) and then accessing the least significant byte of the Output Compare register 1 ($17). Reset does not affect this bit.

ICF - Input Capture Flag

ICF is set when a proper edge has been sensed by the input capture edge detector. It is cleared by a CPU read of the TSR (with ICF set) followed by accessing the least significant byte of the Input Capture register ($15). Reset does not affect this bit.

All four timer interrupt flags have corresponding enable bits (OCIE2, ICIE, OCIE1, and TOIE) found in the Timer Control register (TCR) at location $12. Reset clears all enable bits preventing an interrupt from occurring. The actual processor interrupt is generated only if the interrupt mask bit of the condition code register is also cleared. When the interrupt is recognized, the current state of the machine is pushed onto the stack and the interrupt mask bit in the condition code register is set. This masks further interrupts until the present one is serviced. The service routine address is specified by the contents of $7FF6 and $7FF7.

Refer to section 7.1 for detailed description of the Programmable Timer

4.2.5 SCI Interrupts

An interrupt in the SCI system will occur when one of the interrupt bits in the SCI Status register (SCSR) is set, provided the interrupt mask bit of the condition code register is cleared and the enable bit in the SCI Control register 2 (SCCR2) is enabled. When the interrupt is recognized, the current state of the machine is pushed onto the stack and the interrupt mask bit in the condition code register is set. This masks further interrupts until the present one is serviced. The interrupt causes the program counter to vector to memory location $7FF4-$7FF5, in which the service routine's starting address is stored. Software in the serial interrupt service routine must determine the priority and cause of the SCI interrupt by examining the interrupt flags and status bits located in the SCI Status register. The general sequence for clearing an interrupt is a software sequence of reading the status register while the flag is set followed by a read or write of an associated register.

Refer to section 8 for detailed description of the Serial Communication Interface.

4.2.6 Keyboard Interrupt

A keyboard interrupt is enabled when the KEYE bit in the general control register ($25) is set, provided the interrupt mask bit of the condition code register is cleared. An interrupt is recognized upon the falling edge of any port A pins. When it is recognized, the current state of the machine is pushed onto the stack and the interrupt mask bit in the condition code register is set. This masks further interrupts until the present one is serviced. The interrupt causes the program counter to vector to memory location $7FF8 - $7FF9 in which it stored the service routine's starting address. When the KEYE bit is set and port A's data direction register is configured as an input port, a pull-up resistor of approx. 250KΩ is associated with each port A pins. A write to port A resets the keyboard interrupt.

A high to low transition on any PORT A pins will cause a keyboard interrupt. This interrupt will be latched internally and will not be cleared even if the KEYE bit is reset to zero. The interrupt flag can only be cleared by performing a 'write' to PORT A. It is advised when writing the keyboard interrupt routine, the CPU should perform a 'write' to PORT A before it clears the interrupt mask flag or execute a RTI instruction.

Users may find an interrupt is pending as soon as KEYE is enabled. It is caused by the internal switching corresponding to the pull-up resistors.

4.2.7 RTC Interrupt

An RTC interrupt is enabled when either the RTCE, ALE or SECE bit in the general control register ($21) is set, provided the interrupt mask bit in the condition code register is cleared. When RTCE bit is set, real time clock will interrupt the CPU once a day. This will occur when the hours register in real time clock register changes from twenty-three to zero. When the SECE bit is set, the real time clock will interrupt CPU once a second. When ALE bit is set, RTC interrupt will occur when

the value of hour alarm and hours are equal, and the value of minute alarm and minutes are equal. When the interrupt is recognized, the current state of the machine is pushed onto the stack and the interrupt mask bit in the condition code register is set. This mask further interrupts until the present one is serviced. The interrupt causes the program counter to vector to $7FF2 - $7FF3 in which is stored the service routine's starting address. Interrupt per day, per second or alarm interrupt can be distinguished by the RTCF, SECF and ALF flags. In order to reset the interrupt, users are responsible for clearing the appropriate flags when executing the interrupt routine.

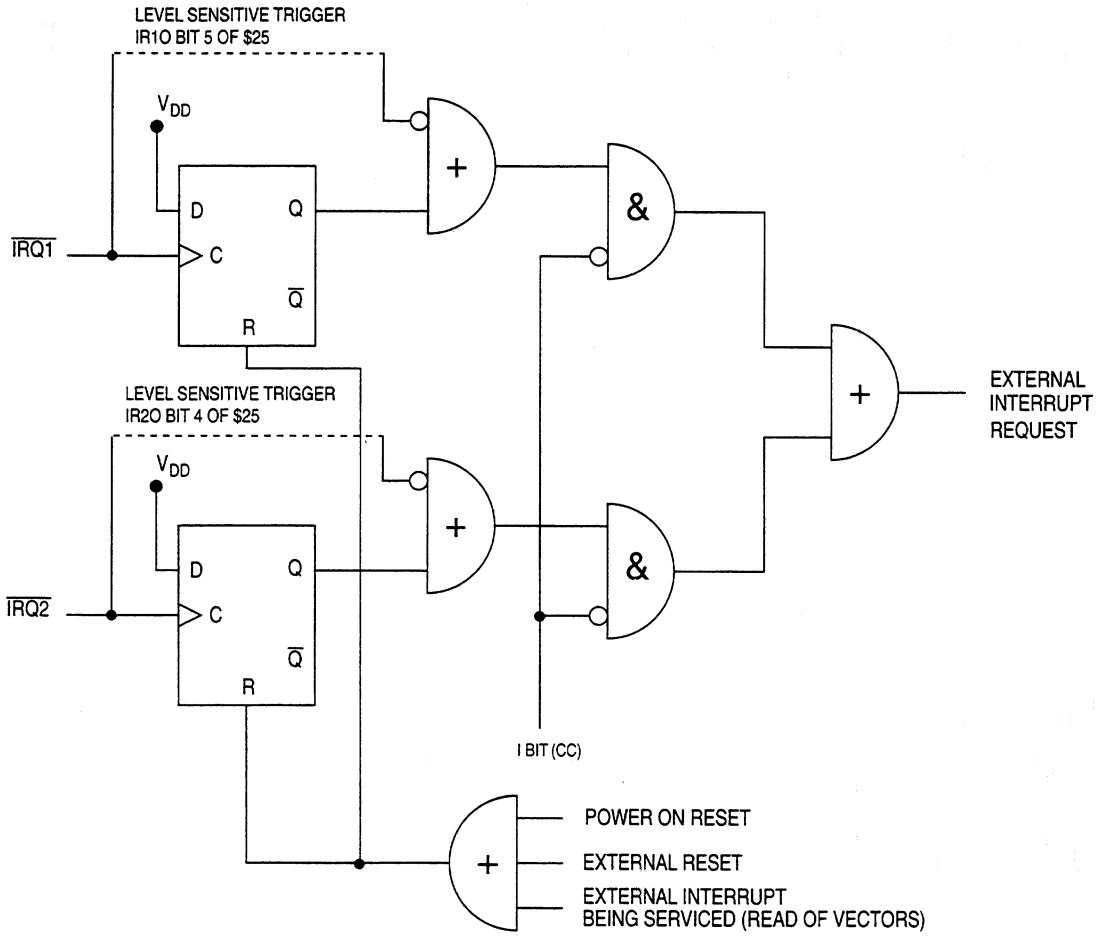
Notice that ALF is set as long as the values of the both hour alarm and hour, minute alarm and minutes are qual. Therefore, users may found ALF is still set even after the MCU performs an ALF flag clearance. To avoid the same alarm interrupt from further interrupting the MCU, users can assign a different values to the alarm register and then ALF can be cleared as a result.

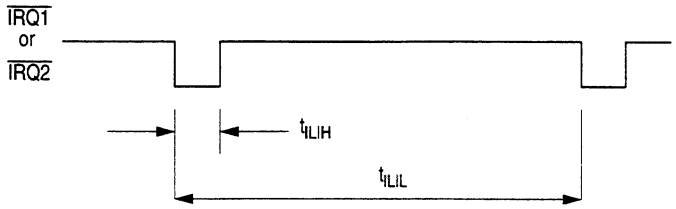
Refer to section 5.2 for detailed description of the Real Time Clock.

4.2.8 SPI Interrupt

An interrupt in the serial peripheral interface (SPI) occurs when one of the interrupt flag in the serial peripheral status register ($23) is set, provided the interrupt mask bit in the condition code register is cleared and the enable bit in the serial peripheral control register ($22) is enabled. When the interrupt is recognized, the current state of the machine is pushed onto the stack and the interrupt mask bit in the condition code register is set. This masks any further interrupt until the present one is serviced. The SPI interrupt causes the program counter to vector to memory location $7FF0 and $7FF1 which contains the starting address of the interrupt's service routine. Software in the serial peripheral interrupt service routine must determine the priority and the cause of the SPI interrupt by examining the interrupt flags located in the SPI status register. The general sequence of clearing an interrupt is a software sequence of accessing the status register while the flag is set, followed by a read or write of an associated register.

Refer to section 9 for detailed description of the Serial Peripheral Interface.





EDGE SENSITIVE TRIGGER CONDITION

The minimum pulse width t_{ILIH} is either 125ns (V_{DD}=5V) or 250ns (V_{DD}=3V). The period t_{ILIL} should not be less than the number of tcyc cycles it takes to execute the interrupt service routine plus 21 tcyc cycles.

Figure 4-4 External Interrupt

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5
CLOCKS

This section describes the Phase Lock Loop and Real Time Clock.

5.1 PHASE LOCK LOOP

System clock can be obtained from either the 32KHz oscillator or from PLL. During power-up or external reset, CPU system clock is 16.384KHz, from 32.768KHz divided by 2. Setting the CLKS bit in the General Control register (bit 0 of address $25) selects PLL clock for the CPU. PLL clock frequency depends on FS1 & FS0 in the Clock Status and Control register (bits 6 & 5 of address $21); see table 5-1. When FS1 and FS0 are set, a 7.3728MHz clock is output from the PLL. This is further divided by 2 before feeding into the MCU as the system clock. Phase Lock Loop Indicator, PLLI in the Clock Status and Control register (bit 4 of address $21), is a read only bit which indicates an accurate clock is ready when set. However, owing to the finite delay in updating this PLLI, it may still be set after FS1 & FS0 are modified and the PLL clock frequency is not yet stabled. FS1 & FS0, and CLKS are cleared during power-up or external reset. It is recommended not to update video data stored in segment drivers if the CLKS bit is cleared. Also, both tone generators A and B will give incorrect frequencies if CLKS is cleared.

Clock Status and Control Register

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on Reset
$21	SRS	FS1	FS0	PLLI	SIE	SECE	ALE	RTCE	0000 0000

General Control Register

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on Reset
$25	TIMI	KEYE	IR1O	IR2O	PORTI	AUTO	OSEN	CLKS	0000 0000

Table 5-1 Phase Lock Loop Output Freqencies

FS1	FS0	PLL Output Clock Frequency	PO2 (Internal Bus Frequency)
0	0	0.6144MHz	0.3072MHz
0	1	2.4576MHz	1.2288MHz
1	0	4.9152MHz	2.4576MHz
1	1	7.3728MHz	3.6864MHz

CLKS is the bit to select CPU clock either coming from the phase lock loop or from the 32KHz clock. During power-up or external reset, this bit is cleared to indicate that CPU clock is from the 32KHz clock. The following is an example of how to use the PLL to obtain an accurate CPU clock.

```
BSET   0,$25        Select PLL clock for CPU.
BSET   5,$21        Select 1.2288 MHz as internal bus frequency.
BRSET  4,$21,*      Wait unitl PLLI is updatedto indicate the
                    unstable state
BRCLR  4,$21,*      Wait until PLL clock is stable.
JMP    SERVE        Go to perform jobs that require accurate
                    frequency (such as SCI and Timer).
```

The PLL consists of an on-chip VCO, a phase comparator and a programmable divide-by-N counter. A filter is required to filter the phase comparator output to provide a DC signal to control the VCO frequency; see figure 5-1.

The phase comparator compares the rising edge of an 8KHz reference signal derived from the 32KHz crystal clock to the rising edge of the VCO clock after being divided by the divide-by-N counter. When there is phase different between the two signals, the phase comparator output will adjust the DC level input to the VCO to change the VCO frequency; see figure 5-2. The divide-by-N counter can be programmed to divide by different rates to obtain 4 different VCO frequencies of 614.4KHz, 2.4576MHz, 4.9152MHz and 7.3728MHz.

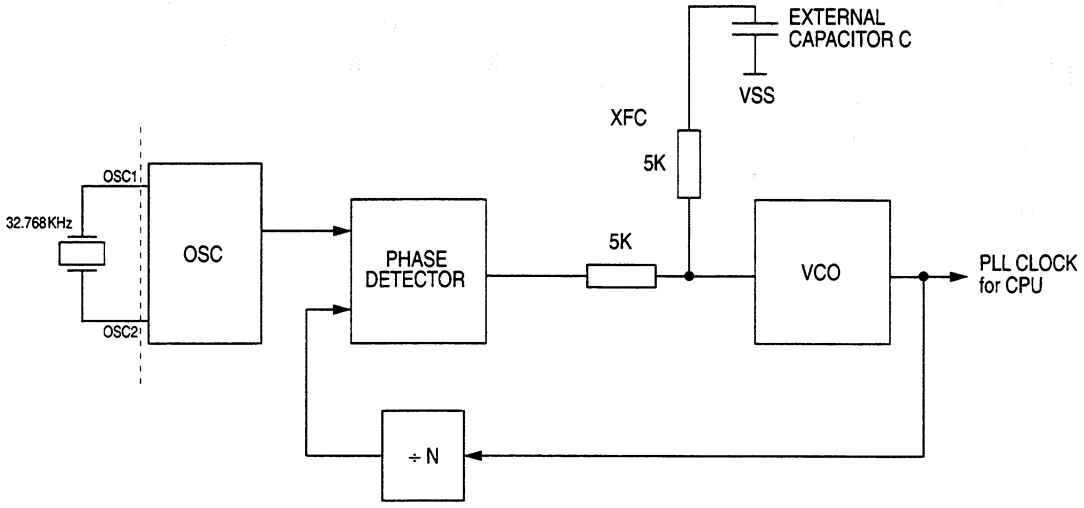

Figure 5-1 Phase Lock Loop Block Diagram

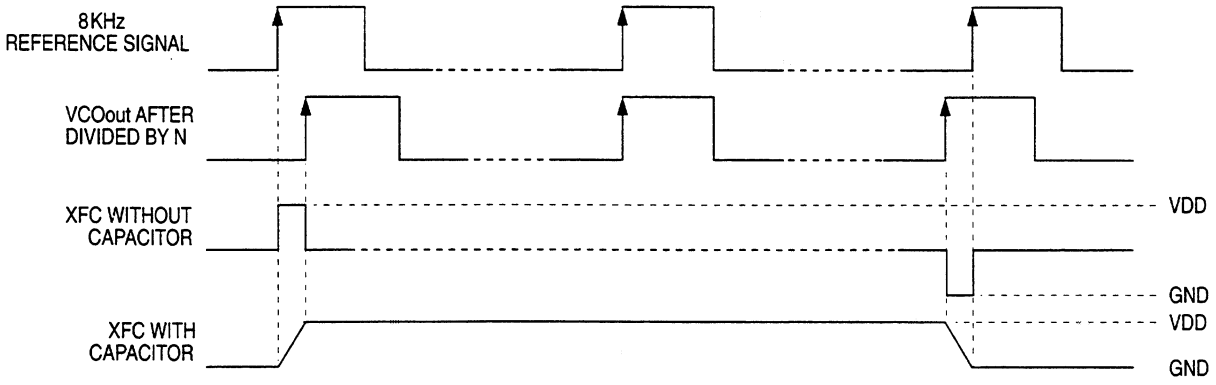

Figure 5-2 Typical Waveform for PLL

5.2 REAL TIME CLOCK

Continuous or non-continuous RTC operation can be selected by programming the OSEN bit in the General Control register (bit 1 of address $25). Real time clock consists of three binary counters which is divided down from the 32.768KHz oscillator. There are four bits in the Clock Status and Control register (address $21) and three bits in the interrupt status register (address $1F) where the operation of the real time clock is controlled. In addition, three locations are reserved for real time clock operation; they are:

RTC Hours Register

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on Reset
$3C	–	–	–						

RTC Minutes Register

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on Reset
$3D	–	–							

RTC Seconds Register

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on Reset
$3E	–	–							

Users should set these RTC registers to the desired value after a reset.

There are two locations associated with the RTC alarm registers. They are:

RTC Minutes Alarm Register

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on Reset
$0B	–	–							0000 0000

RTC Hours Alarm Register

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on Reset
$0C	–	–	–						0000 0000

There are four interrupts associated with the real time clock, their flags are in the Interrupt Status register ($1F), and their respective enable bits are the Clock Status and Control register ($21).

Interrupt Status Register

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on Reset
$1F	–	–	IR1F	IR2F	SIF	SECF	ALF	RTCF	0000 0000

Clock Status and Control Register

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on Reset
$21	SRS	FS1	FS0	PLLI	SIE	SECE	ALE	RTCE	0000 0000

Refer to sections 3.4.2 and 3.4.3 for register definitions.

It should be noted that the flags in the interrupt status register will be set if the corresponding event is detected, irrespective of the setting of the interrupt enable bits.

The following is an example showing how to use the real time clock interrupt:

```
*Main program
        BSET   1,$25        Enable continuous RTC operation.
        BCLR   0,$1F        Clear once a day interrupt flag
        BCLR   1,$1F        Clear alarm interrupt flag
        BCLR   2,$1F        Clear once a second interrupt flag
        BSET   0,$21        Enable RTC (once a day) interrupt.
        BSET   1,$21        Enable RTC (alarm) interrupt.
        BSET   2,$21        Enable RTC (once a second) interrupt.
        STOP                CPU execute STOP instruction for power
                            conservation.
*Real time clock interrupt service routine
        BRSET 0,$1F,ODAY    This bit is set indicating this is an once a
                            day RTC interrupt.
        BRSET 1,$1F,ALINT   This bit is set indicating this is a RTC
                            interruptcausedbyamatchofalarmregisters
                            and real time clock registers.
        BRSET 2,$1F,OSEC    This bit is set indicating this is an once a
                            second RTC interrupt.
        BRA    RTCR
ODAY    LDA    #%11111110
        STA    $1F          Clear bit 0 so that this once a day interrupt
                            will not be recognised as a new one on next
                            RTC interrupt.
        JSR    OADAY        Once a day interrupt service routine
        BRSET 1,$1F,ALINT   This bit is set indicating alarm interrupt
                            also occurs at the same time.
```

```
        BRSET 2,$1F,OSEC    This bit is set indicating once a second RTC
                            interrupt also occurs at the same time.
        RTCR  RTI
ALINT   LDA   #%11111101
        STA   $1F           Clear bit 1 so that this alarm interrupt will
                            not be recognised as a new one on next RTC
                            interrupt.
        JSR   ALARM         Alarm service interrupt routine.
        BRSET 2,$1F,OSEC    This bit is set indicating once a second
                            interrupt also occurs at the same time.
        BRA   RTCR          Return from interrupt.
OSEC    LDA   #%11111011
        STA   $1F           Clear bit 2 so that this once a second
                            interrupt will not be recognised as a new one
                            on next RTC interrupt.
        JSR   OASEC         Once a second interrupt service routine.
        BRA   RTCR          Return from interrupt.
```

5

6
LOW POWER MODES

The MC68HC05L11 has two low power modes, Stop and Wait. These two modes have different effects on the Programmable Timer, Real Time Clock, Serial Communications Interface and Serial Peripheral Interface.

STOP and WAIT executions will cause AD0 to AD21 and PO2 to go low. R/$\overline{W}$ is forced high. All programmable chip selects except $\overline{CS2}$ are forced high. $\overline{CS2}$/AD22 is high impedance (see section 11 on Chip Select for Small Systems). All other address lines are forced low and all data lines are high impedance. It is recommended to tie all high impedance pins to an appropriate logic level (e.g. V_{DD} or V_{SS}) to avoid possible leakage.

6.1 Stop Mode

The Stop mode is entered when the processor executes the STOP instruction. This places the MC68HC05L11 in its lowest power consumption mode. In Stop mode the internal processor clock is turned off, causing all internal processing to halt (see Stop mode flowchart in figure 6-1). Entering Stop mode, the I bit (interrupt mask) in the condition code register is cleared to enable external interrupts $\overline{IRQ1}$ & $\overline{IRQ2}$, RTC and keyboard interrupt. All other registers and memory remain unaltered and all input/output lines remain unchanged. If the user chooses to have a non-interrupted RTC by setting the OSEN bit, the 32KHz oscillator will keep running. Clearing the OSEN bit before entering Stop mode, the RTC will stop after the auto-display feature is served. Stop mode is exited by an external interrupt ($\overline{IRQ1}$/$\overline{IRQ2}$), a RTC interrupt, a keyboard interrupt, or an external $\overline{RESET}$. On exit, the internal processor clock is then turned on and the MCU will wait for 16 cycles of 32KHz/2 clock if the 32KHz oscillator has been kept running continuously. If the exit interrupt is an external reset, the 32KHz oscillator is turned on and, like Power-On-Reset, the MCU operation is halted for 1024 cycles of the 32KHz/2 clock to ensure a stable crystal oscillation. The program counter is vectored to memory locations containing the start address of the interrupt or reset service routine.

The effects of Stop mode on each of the peripherals i.e. Timer, RTC, SCI and SPI are described below.

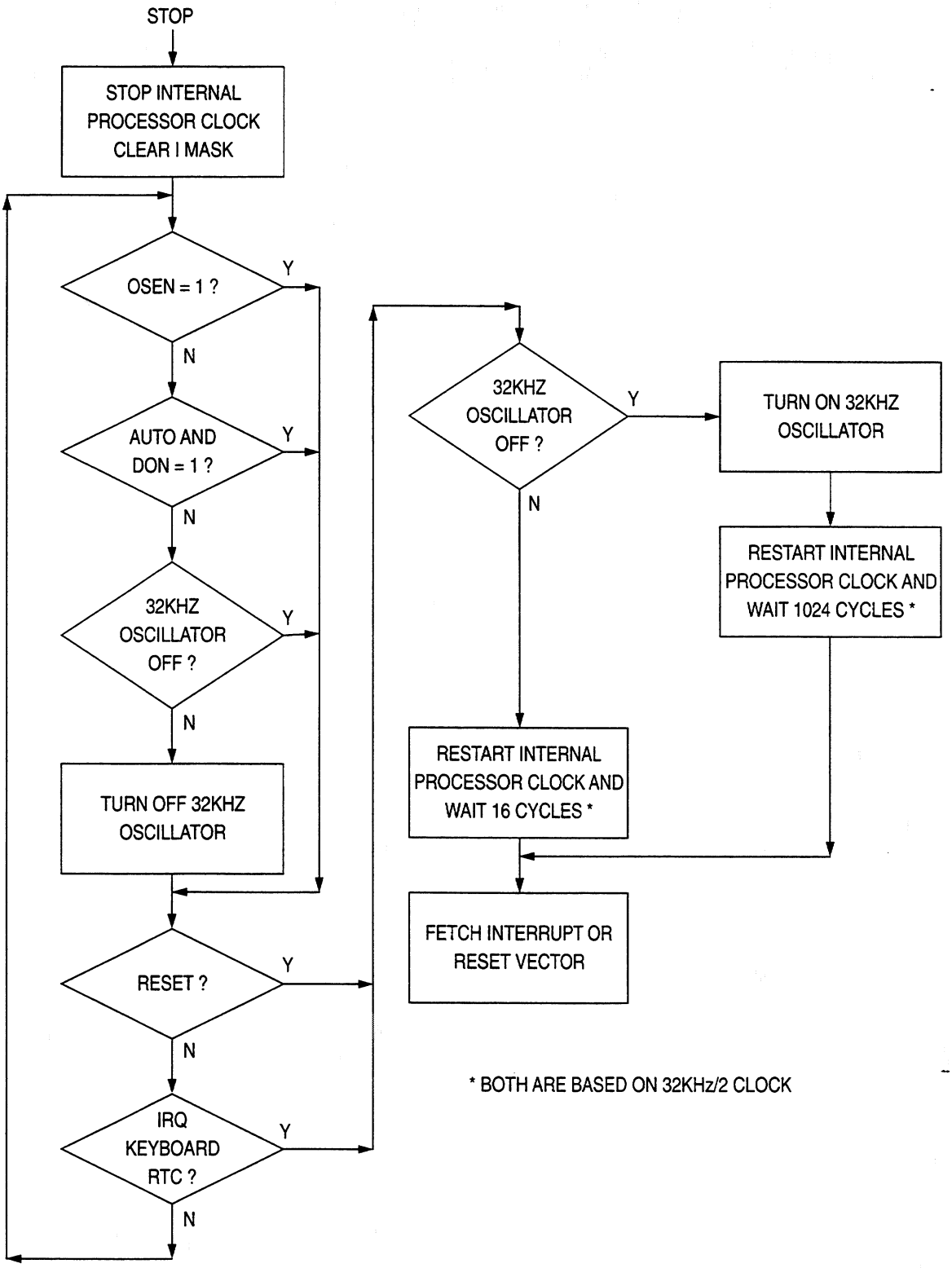

Figure 6-1 Stop Flowchart

6.1.1 Programmable Timer during Stop Mode

When the MCU enters Stop mode, the timer counter stops counting (the internal processor clock is stopped) and remains at that particular count value until the Stop mode is exited by an interrupt, the counter then resumes counting. If the Stop mode is exited by reset, the counter is forced to $FFFC. Another feature of the programmable timer in Stop mode is that if at least one valid input capture edge occurs at the TCAP pin, the input capture detect circuitry is armed. This action does not set any timer flags or "wake up" the MCU, but when the MCU does "wake up" there will be an active input capture flag (and data) from that first valid edge which occurred during Stop mode. If the Stop mode is exited by an external reset (logic low on $\overline{\text{RESET}}$ pin), then no such input capture flag or data action takes place even if there was a valid input capture edge (at the TCAP pin) during MCU Stop mode.

6.1.2 RTC during Stop Mode

The RTC runs at 32.768KHz. The STOP instruction has no effect on the RTC if the OSEN bit in the general control register ($25) is set. If the OSEN bit is cleared, the RTC will stop operation during Stop mode because the 32.768KHz crystal oscillator is disabled after auto-display off.

6.1.3 SCI during Stop Mode

When the MCU enters Stop mode, the baud rate generator which drives the receiver and transmitter is shut down. This essentially stops all SCI activities, i.e. the receiver is unable to receive and the transmitter is unable to transmit. If the STOP instruction is executed during a transmitter transfer, that transfer is halted, and resumes again when the MCU exits Stop mode (this is undesirable). If the receiver is receiving data when the STOP instruction is executed, received data sampling is stopped and the rest of the data is lost. Therefore, to avoid data lost, the SCI should be idle when the STOP instruction is executed.

6.1.4 SPI during Stop Mode

When the MCU enters Stop mode, the baud rate generator which drives the SPI shuts down. This essentially stops all master mode SPI operation, thus the master SPI is unable to transmit or receive any data. If the STOP instruction is executed during an SPI transfer, that transfer is halted until the MCU exits Stop mode. If Stop mode is exited by a reset, then the appropriate control/status bits are cleared and the SPI is disabled. If the device is in the slave mode when the STOP instruction is executed, the slave SPI will still operate. It can still accept data and clock information in addition to transmitting its own data back to a master device.

6.2 Wait Mode

The WAIT instruction places the MC68HC05L11 in a low power consumption mode.In Wait mode, all CPU activities are stopped, but the internal clock, programmable timer, serial communications interface, serial peripheral interface and real time clock remain active. Refer to Figure 6-2 for Wait flowchart. On entering Wait mode, the I bit in the condition code register is cleared to enable all interrupts. In Wait mode all registers and memory remain unaltered and all parallel input/output lines remain unchanged. In additions to interrupts from external $\overline{IRQ1}$ & $\overline{IRQ2}$, keyboard, RTC, interrupts from either timer, SCI, or SPI, will cause the processor to exit Wait mode. If a non-reset exit from Wait mode is performed (e.g. timer overflow interrupt exit), the system will resume from the state before it entered Wait mode. If a reset exit from Wait mode is performed, all the systems revert to the disabled reset state.

In Wait mode, the device power consumption depends on how many systems are active. The power consumption will be the lowest when the SCI, SPI and the Timer are disabled (the RTC cannot be disabled in Wait mode).

6.2.1 Programmable Timer during Wait Mode

The timer system is not affected by the Wait mode and continues regular operation. Any valid timer interrupt will wake up the system.

6.2.2 RTC during Wait Mode

The RTC system is not affected by the Wait mode and continues regular operation. Any valid RTC interrupt will wake up the system.

6.2.3 SCI during Wait Mode

The SCI system is not affected by the Wait mode and continues regular operation. Any valid SCI interrupt will wake up the system.

6.2.4 SPI during Wait Mode

The SPI system is not affected by the Wait mode and continues regular operation. Any valid SPI interrupt will wake up the system.

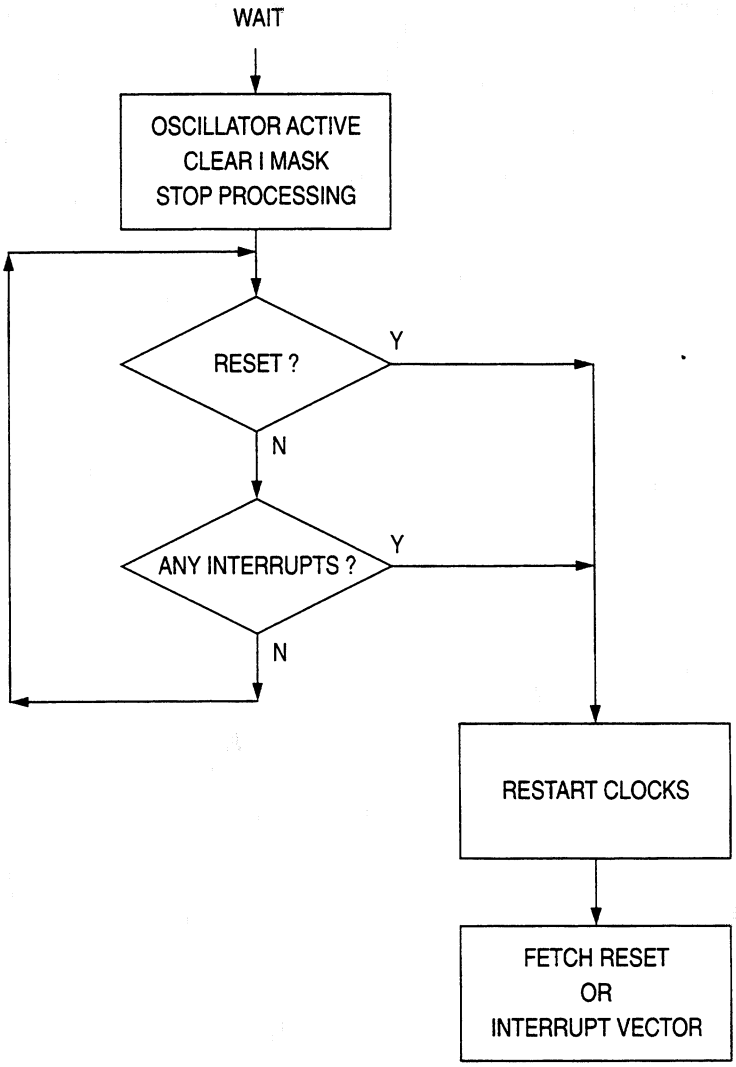

Figure 6-2 Wait Flowchart

6.3 Data Retention Modes

The contents of RAM and CPU registers can be retained at supply voltages as low as 2.0 Vdc. This is referred to as the data retention mode, where the data is held, but the device is not guaranteed to operate.

6

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7
PROGRAMMABLE TIMER & TONE GENERATORS

This section describes the Programmable Timer and Tone Generators.

7.1 PROGRAMMABLE TIMER

The timer consists of a 16-bit free-running counter driven by a fixed divide-by-four prescaler. This timer can be used for many purposes, including input waveform measurements while simultaneously generating an output waveform. Pulse widths can vary from several microseconds to many seconds. Figure 9-1 shows a block diagram for the Programmable Timer.

Because the timer has a 16-bit architecture, the I/O registers for the input capture and output compare functions are pairs of 8-bit registers (high byte and low byte). Generally, assessing the low byte of a specific timer function allows full control of that function. An access of the high byte inhibits that specific timer function until the low byte is also accessed.

Note: The I bit in the condition code register should be set while manipulating both the high and low byte register of a specific timer function to ensure that an interrupt does not occur.

Twelve 8-bit registers are associated with the programmable timer.

- Timer Control Register (TCR) $12
- Timer Status Register (TSR) $13
- Input Capture Register High byte - $14, Low byte - $15
- Output Compare Register 1 High byte - $16, Low byte - $17
- Output Compare Register 2 High byte - $1C Low byte - $1D
- Counter Register High byte - $18, Low byte - $19
- Alternate Counter Register High byte - $1A Low byte - $1B

A description of each register is provided in the following paragraphs.

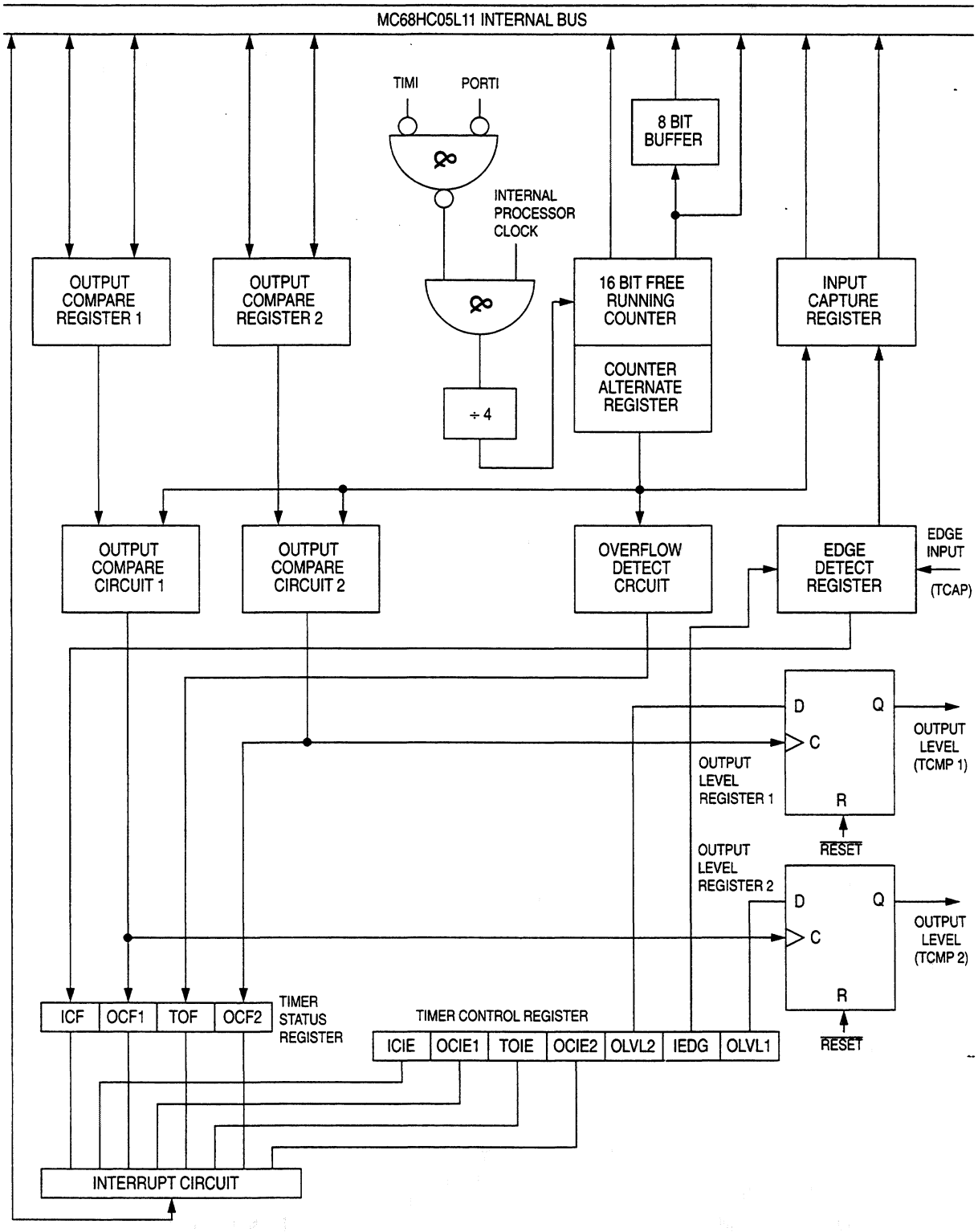


Figure 7-1 Programmable Timer Block Diagram

7.1.1 Counter

- Counter Register location — High byte - $18, Low byte - $19
- Alternate Counter Register — High byte - $1A Low byte - $1B

The key element in the programmable timer is a 16-bit, free-running counter or Counter register, preceded by a prescaler that divides the internal processor clock by four. The prescaler gives the timer a resolution of 1.085µs if the internal bus clock is 3.6864MHz. The counter is incremented during the low portion of the internal bus clock. Software can read the counter at any time without affecting its value.

The double-byte, free-running counter can be read from either of two locations, $18 & $19 (Counter register) or $1A & $1B (counter Alternate register). Reading only the least significant byte (LSB) of the free-running counter ($19 or $1B) receives the count value at the time of the read. If the most significant byte (MSB) ($18 or $1A) is read first, the LSB ($19 or $1B) is latched to a buffer. This buffer value remains fixed after the first MSB read, even if the MSB is read several times. This buffer is accessed when the LSB ($19 or $1B) is read, and thus, completes a read sequence of the complete counter value.

Reading the timer Counter register low byte after reading the Timer Status register clears the timer overflow flag (TOF), but reading the Counter Alternate register does not affect TOF. Therefore, the Counter Alternate register can be read any time without risk of missing timer overflow interrupts due to a cleared TOF.

The free-running counter is preset to $FFFC during reset and is always a read-only register. During a power-on reset, the counter is also preset to $FFFC and begins running after the oscillator start-up delay. The value in the free-running counter repeats every 262144 internal bus clock cycles. TOF is set when the counter overflows (from $FFFF to $0000); this will cause an interrupt if TOIE (bit 5 of Timer Control register).

In some timing control applications it may be desirable to reset the counter under software control. When the low byte of the counter ($19 or $1B) is written to, the counter is set to its reset value of $FFFC. The divide-by-4 prescaler is also reset and the counter resumes normal counting operation. All of the flags and enable bits remain unaltered by this operation. If access has previously been made to the high byte of the free-running counter ($18 or $1A), then the reset counter operation terminates the access sequence.

7.1.2 Output Compare Registers

There are two 16-bit Output Compare registers:

- Output Compare Register 1 — High byte - $16 Low byte - $17
- Output Compare Register 2 — High byte - $1C Low byte - $1D

Each 16-bit Output Compare register is made up of two 8-bit registers. These Output Compare registers are used for several purposes, such as indicating when a period of time has elapsed. All

bits are readable and writable and are not affected by the timer hardware or reset. If the compare function is not needed, the Output Compare registers can be used as storage locations.

The contents of the Output Compare registers are continually compared with the contents of the free-running counter and, if a match is found, the corresponding output compare flag (OCF1 or OCF2) in the Timer Status register is set; and the corresponding output level (OLVL1 or OLVL2) bit is clocked to an output level register. The Output Compare registers values and the output level bits should be changed after each successful comparison to establish a new elapsed timeout. An interrupt can also accompany a successful output compare provided the corresponding interrupt enable bit (OCIE1 or OCIE2) is set. (The free-running counter is updated every four internal bus clock cycles.)

After a processor write cycle to the Output Compare registers containing the MSB ($16 or $1C), the output compare function is inhibited until the LSB ($17 or $1D) is also written. The user must write both bytes (locations) if the MSB is written first. A write made only to the LSB ($17 or $1D) will not inhibit the compare function. The processor can write to either byte of an Output Compare register without affecting the other byte. The minimum time required to update the Output Compare registers is a function of the program rather than the internal hardware. Because the output compare flags and Output Compare registers are not defined at power on, and not affected by reset, care must be taken when initializing output compare functions with software. The following procedure is recommended:

1) write to Output Compare register 1 and/or 2 High-byte to inhibit further compares;
2) read the Timer Status register to initialize clearing of OCF1 or/and OCF2;
3) write to Output Compare register 1 or/and 2 Low-byte to enable the output compare function.

The output level (OLVL1 or OLVL2) bit is clocked to the output level register (1 or 2) regardless of whether the output compare flag (OCF1 or OCF2) is set or clear.

7.1.3 Input Capture Registers

– Input Capture Register High byte - $14, Low byte - $15

'Input Capture' is a technique whereby an external signal (connected to TCAP pin) is used to trigger a read of the free-running counter. In this way it is possible to relate the timing of an external signal to the internal counter value, and hence to elapsed time.

The two 8-bit registers that make up the 16-bit Input Capture register are read-only, and are used to latch the value of the free-running counter after the corresponding input capture edge detector senses a valid transition. The level transition that triggers the counter transfer is defined by the corresponding input edge bit (IEDG). Reset does not affect the contents of the Input Capture register.

The result obtained from an input capture will be one greater than the value of the free-running counter on the rising edge of the internal bus clock preceding the external transition. This delay is

required for internal synchronization. Resolution is one count of the free-running counter, which is four internal bus clock cycles.

The free-running counter contents are transferred to the Input Capture register on each valid signal transition whether the input capture flag (ICF) is set or clear. The Input Capture register always contains the free-running counter value that corresponds to the most recent input capture.After a read of the Input Capture register MSB ($14), the counter transfer is inhibited until the LSB ($15) is also read. This characteristic causes the time used in the input capture software routine and its interaction with the main program to determine the minimum pulse period. A read of the Input Capture register LSB ($15) does not inhibit the free-running counter transfer since they occur on opposite edges of the internal bus clock.

7.1.4 Timer Control Register (TCR)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on Reset
$12	ICIE	OCIE1	TOIE	OCIE2	0	OLVL2	IEDG	OLVL1	0000 00u0

The TCR is a read/write register containing seven control bits. Four bits control interrupts associated with each of the four flag bits found in the Timer Status register (discussed below). The other three bits control: 1) which edge is significant to the input capture edge detector (i.e., negative or positive), and 2) the next value to be clocked to the output level registers in response to a successful output compare. The Timer Control register and the free-running counter are the only sections of the timer affected by reset. The TCMP1 and TCMP2 pins are forced low during external reset and stays low until a valid compare changes them to high. Definition of each bit is as follows:

ICIE - Input Capture Interrupt Enable

1 (set) – Input Capture interrupt enabled.

0 (clear) – Input Capture interrupt disabled.

OCIE1 - Output Compare Interrupt Enable 1

1 (set) – Output Compare interrupt 1 enabled.

0 (clear) – Output Compare interrupt 1 disabled.

TOIE - Timer Overflow Interrupt Enable

1 (set) – Timer Overflow interrupt enabled.

0 (clear) – Timer Overflow interrupt disabled.

OCIE2 - Output Compare Interrupt Enable 2

1 (set) – Output Compare interrupt 2 enabled.

0 (clear) – Output Compare interrupt 2 disabled.

OLVL2 - Output Level Voltage Latch 2

1 (set) – High output on TCMP2 pin if counter compare 2 is true.

0 (clear) – Low output on TCMP2 pin if counter compare 2 is true.

IEDG - Input Edge

1 (set) – TCAP is positive-going edge sensitive.

0 (clear) – TCAP is negative-going edge sensitive.

When IEDG is set, a positive-going edge on the TCAP pin will trigger a transfer of the free-running counter value to the input capture registers. When clear, a negative-going edge triggers the transfer.

OLVL1 - Output Level Voltage Latch 1

1 (set) – High output on TCMP1 pin if counter compare 1 is true.

0 (clear) – Low output on TCMP1 pin if counter compare 1 is true.

7.1.5 Timer Status Register (TSR)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on Reset
$13	ICF	OCF1	TOF	OCF2	0	0	0	0	uuuu 0000

The Timer Status register ($13) contains the status bits for the above four interrupt conditions.

Accessing the Timer Status register satisfies the first condition required to clear the status bits. The remaining step is to access the register corresponding to the status bit.

ICF - Input Capture Flag

1 (set) – A valid input capture has occurred.

0 (clear) – No input capture has occurred.

This bit is set when the selected polarity of edge is detected by the input capture edge detector; an input capture interrupt will be generated, if ICIE is set, ICF is cleared by reading the TSR and then the Input Capture Low register ($15)

OCF1 - Output Compare Flag 1

1 (set) – A valid output compare has occurred on Output Compare register 1.

0 (clear) – No output compare has occurred on Output Compare register 1.

OCF2 - Output Compare Flag 2

1 (set) – A valid output compare has occurred on Output Compare register 2.

0 (clear) – No output compare has occurred on Output Compare register 2.

OCF1 or/and OCF2 will be set when their corresponding Output Compare register contents match those of the free-running counter; an output compare interrupt will be generated, if the corresponding OCIE is set. OCFs are cleared by reading the TSR and then the corresponding Output Compare Low register ($17 or $1D).

TOF - Timer Overflow Flag

1 (set) – Timer Overflow has occurred.

0 (clear) – No timer overflow has occurred.

This bit is set when the free-running counter overflows from $FFFF to $0000; a timer overflow interrupt will occur, if TOIE (bit 5 in Timer Control register $12) is set. TOF is cleared by reading the TSR and the Counter Low register ($19).

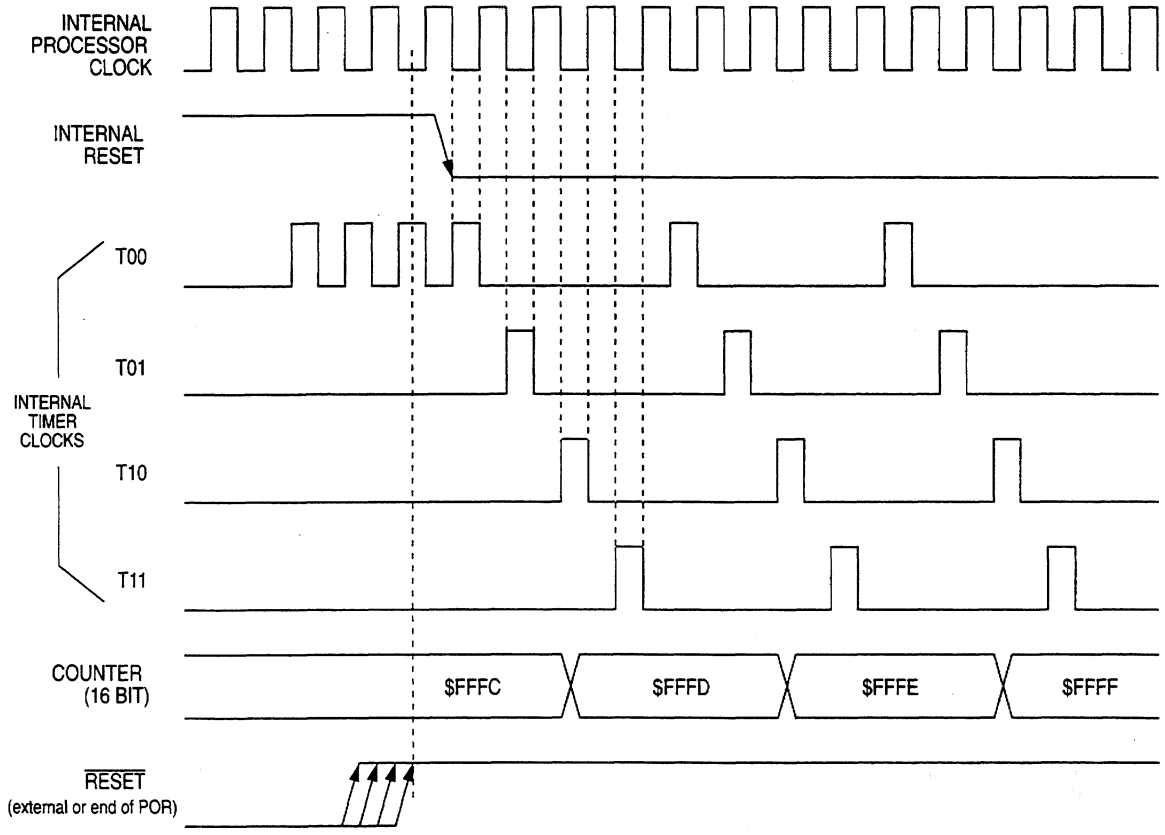
When using the timer overflow function and reading the free-running counter at random times to measure an elapsed time, a problem may occur whereby the timer overflow flag is unintentionally cleared if:

1) the Timer Status register is read or written when the TOF is set, and
2) the LSB of the free-running counter is read, but not for the purpose of servicing the flag.

Reading the Alternate Counter register instead of the Counter register will avoid this potential problem.

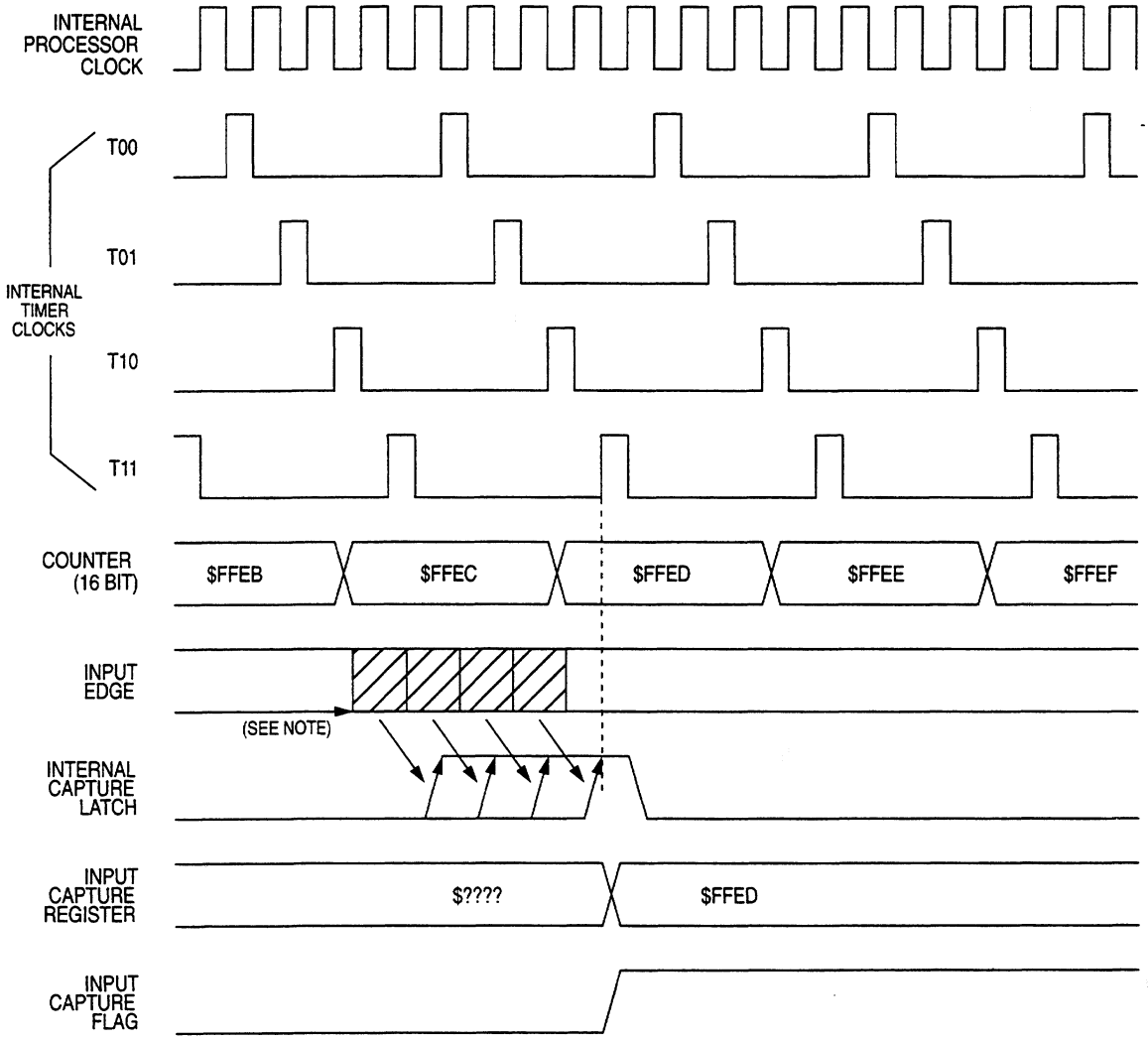
7.1.6 Timer State Diagrams

The relationships between the internal clock signals, the counter contents and the status of the flag bits are shown in the following diagrams. It should be noted that the signals labelled 'internal' (processor clock, timer clocks and Reset) are not available to the user.



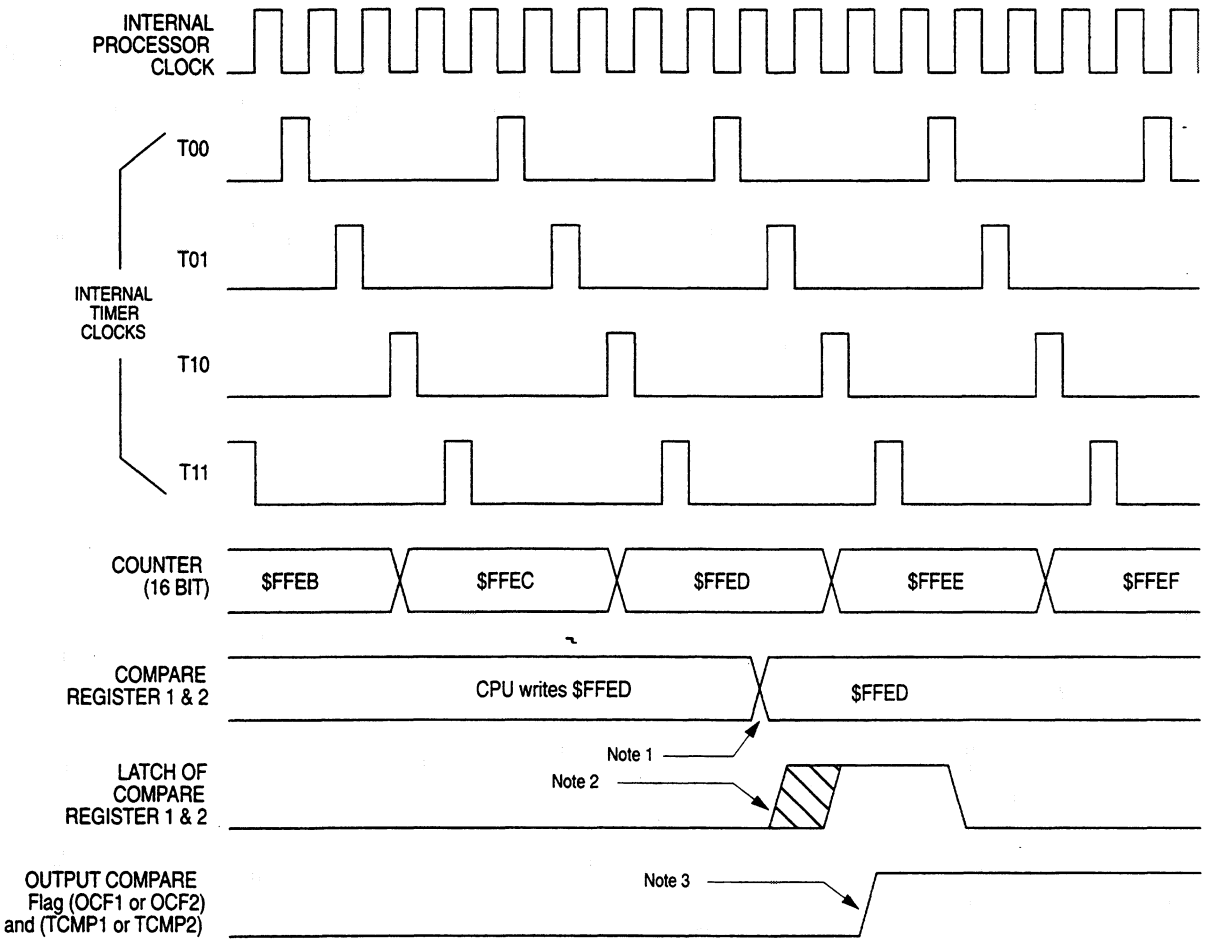
Note: RESET affects only the Counter register and Timer Control register.

Figure 7-2 Timer State Timing Diagram for RESET



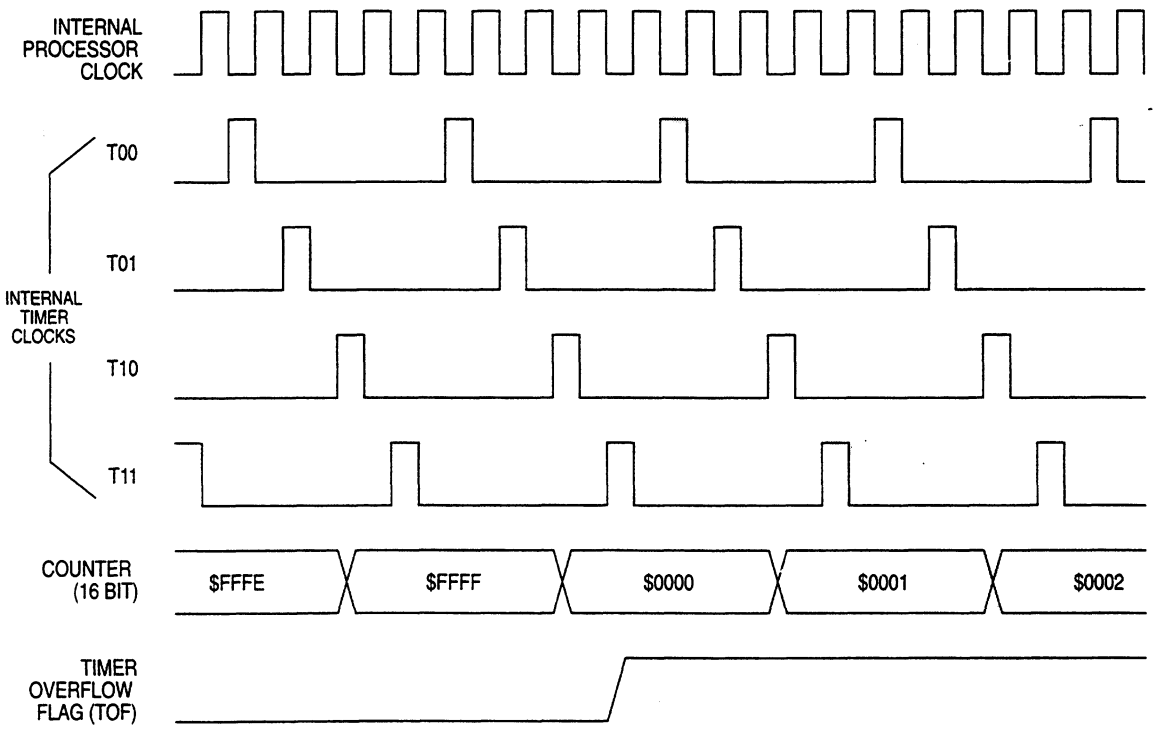
Note: If the input edge occurs in the shaded area from one timer state T10 to the other timer state T10 the input capture flag is set during the next state T11.

Figure 7-3 Timer State Timing Diagram for Input Capture



Note:
1. The CPU write to the compare registers may take place at any time, but a compare only occurs at the timer state T01. Thus, a 4-cycle difference may exist between the write to either one of the compare registers and the actual compare.
2. Internal compare takes place during timer state T01.
3. OCF is set at timer state T11 which follows the comparison match ($FFED in this example).

Figure 7-4 Timer State Timing Diagram for Output Compare



Note: The TOF bit is set at timer state T11 (transition of counter from $FFFF to $0000). It is cleared by a read of the Timer Status register during the internal processor clock high time followed by a read of the Counter Low register.

Figure 7-5 Timer State Diagram for Timer Overflow

7.2 PROGRAMMABLE TONE GENERATORS

The MC68HC05L11 offers users with two Programmable Tone Generators which give pure tone either in musical notes or row/column frequencies for DTMF dialling in telephone applications. These generators are called the Programmable Tone Generator A and the Programmable Tone Generator B.

Both generators are capable of producing 3 octaves of musical tone. TONEA range (from 130.6Hz to 984.6Hz) is one octave lower than TONEB range (from 261.2Hz to 1969.2Hz). It is recommended that these generators should not be used if the CLKS bit in the General Control register (bit 0 of location $25) is clear.

7.2.1 Programmable Tone Generator A

The Programmable Tone Generator A is controlled by addressing the Programmable Tone A register at location $26.

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on Reset
$26	TENA	–	OCT1	OCT0	KEY3	KEY2	KEY1	KEY0	

TENA - TONEA Enable

1 (set) – TONEA output pin is enabled

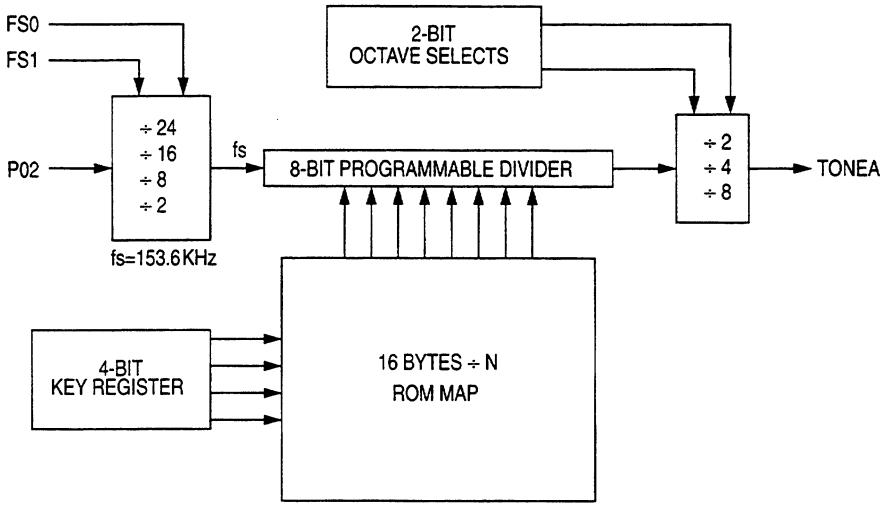
0 (clear) – TONEA output pin is disabled; and may be used as I/O port PF1.

OCT1 & OCT0 - TONEA Octave register bits

OCT1	OCT0	
0	0	Tone output is stuck low.
0	1	Select the Lowest Octave if KEY register < $C else select the Highest octave.
1	0	Select Medium Octave if KEY register < $C else select the Highest Octave.
1	1	Select the Highest Octave.

KEY3, KEY2, KEY1, & KEY0 - KEY register bits

See Figure 7-6 for the highest octave frequencies.



KEY	4-BIT KEY REGISTER	÷N FOR A	TONEA (Hz) FOR HIGHEST OCTAVE	STANDARD (Hz)	% DEVIATION
C	$0	147	522.45	523.25	-0.15
C#	$1	139	552.52	554.35	-0.33
D	$2	131	586.26	587.35	-0.19
D#	$3	123	624.40	662.35	0.33
E	$4	117	656.41	659.30	-0.44
F	$5	110	698.18	698.50	-0.05
F#	$6	104	738.46	740.00	-0.21
G	$7	98	783.67	784.00	-0.04
G#	$8	92	834.78	830.60	0.50
A	$9	87	882.75	880.00	0.31
A#	$A	82	936.59	932.30	0.46
B	$B	78	984.60	987.80	-0.32
fR1	$C	110	698.18	697.00	-0.17
fR2	$D	100	768.00	770.00	0.26
fR3	$E	90	853.33	852.00	-0.16
fR4	$F	82	936.59	941.00	0.47

Figure 7-6 Programmable Tone Generator A

7.2.2 Programmable Tone Generator B

The Programmable Tone Generator B is controlled by addressing the Programmable Tone B register at location $27.

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on Reset
$27	TENB	–	OCT1	OCT0	KEY3	KEY2	KEY1	KEY0	

TENB - TONEB Enable

1 (set) – TONEB output pin is enabled

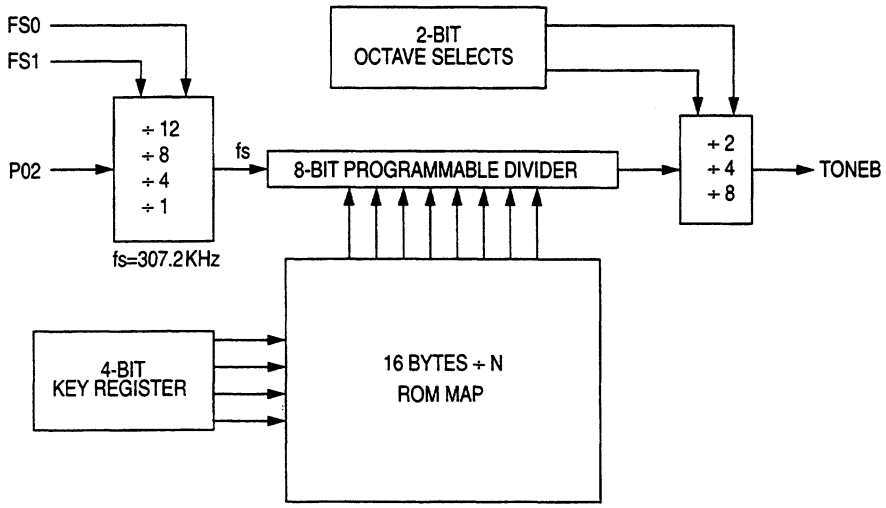
0 (clear) – TONEB output pin is disabled; and may be used as I/O port PF2.

OCT1 & OCT0 - TONEB Octave register bits

OCT1	OCT0	
0	0	Tone output is stuck low.
0	1	Select the Lowest Octave if KEY register < $C else select the Highest octave.
1	0	Select Medium Octave if KEY register < $C else select the Highest Octave.
1	1	Select the Highest Octave.

KEY3, KEY2, KEY1, & KEY0 - KEY register bits

See Figure 7-7 for the highest octave frequencies.



KEY	4-BIT KEY REGISTER	÷N FOR B	TONEB (Hz) FOR HIGHEST OCTAVE	STANDARD (Hz)	% DEVIATION
C	$0	147	1044.90	1046.50	-0.15
C#	$1	139	1105.00	1108.70	-0.33
D	$2	131	1172.50	1174.70	-0.19
D#	$3	123	1248.80	1244.50	0.33
E	$4	117	1312.80	1318.50	-0.44
F	$5	110	1396.40	1396.90	-0.05
F#	$6	104	1476.90	1480.00	-0.21
G	$7	98	1567.30	1568.00	-0.04
G#	$8	92	1669.60	1661.20	0.50
A	$9	87	1765.50	1760.00	0.31
A#	$A	82	1873.20	1864.70	0.46
B	$B	78	1969.20	1975.50	-0.32
fC1	$C	127	1209.40	1209.00	0.03
fC2	$D	115	1335.70	1336.00	-0.02
fC3	$E	104	1476.90	1477.00	-0.01
fC4	$F	94	1634.00	1633.00	0.06

Figure 7-7 Programmable Tone Generator B

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8
SERIAL COMMUNICATIONS INTERFACE (SCI)

A full-duplex asynchronous SCI is provided with a standard NRZ (Non-return-to-zero) format and a selection of baud rates. The SCI transmitter and receiver are functionally independent, but use the same data format and baud rate. The terms baud and bit rate are used synonymously in the following descriptions.

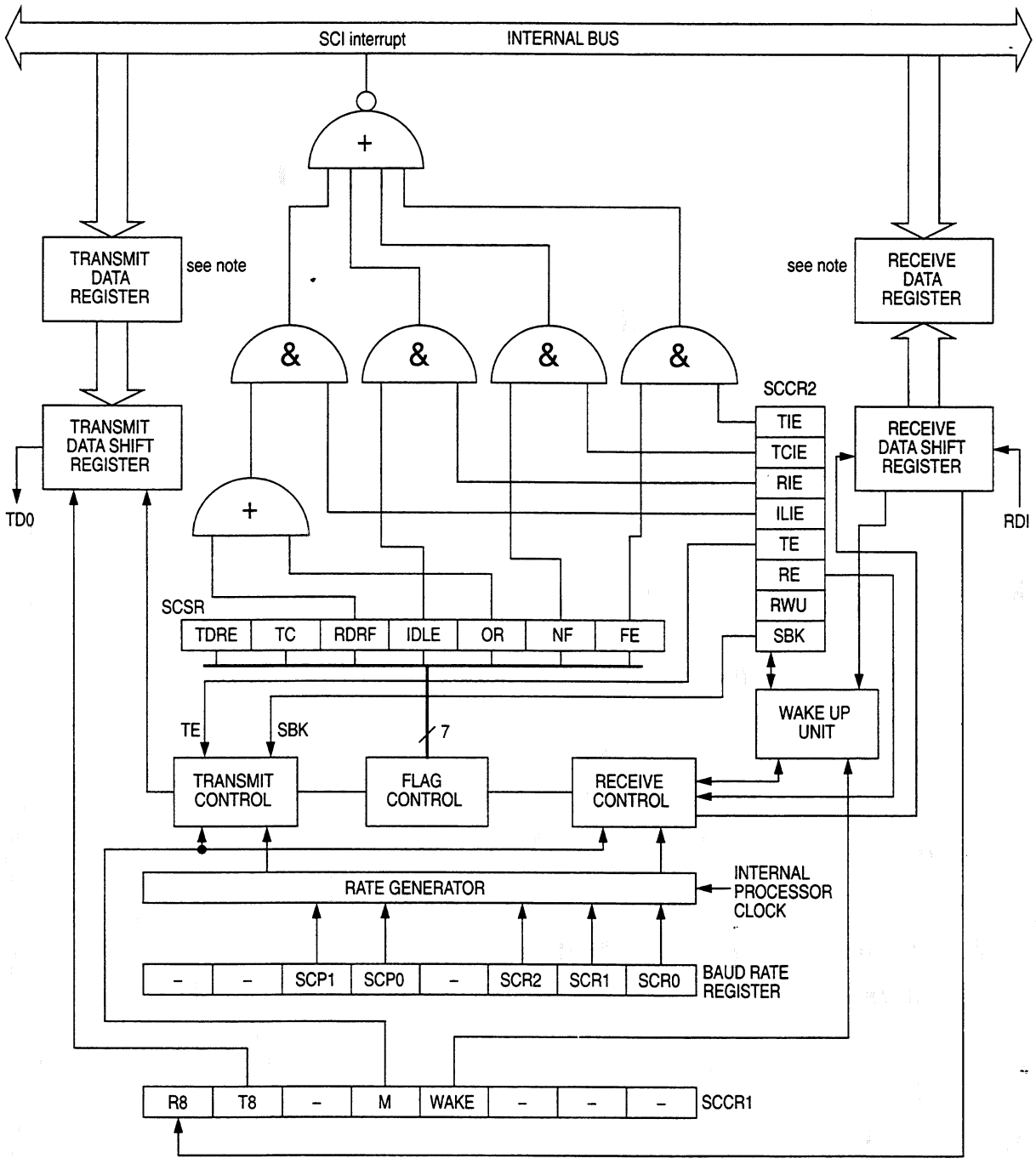
Figure 8-1 shows a block diagram of the Serial Communications Interface.

8.1 SCI Two-Wire System Features

- Standard NRZ (mark/space) format
- Advanced error detection method includes noise detection for noise duration of up to 1/16 bit time
- Full-duplex operation (simultaneous transmit and receive)
- Software programmable for different baud rates
- Software-selectable word length (eight or nine bit words)
- Separate transmitter and receiver enable bits
- SCI may be interrupt driven
- Four separate interrupt conditions

8.2 SCI Receiver Features

- Receiver wake-up function (idle or address bit)
- Idle line detect
- Framing error detect



NOTE: The serial data communications data register (SCDAT) is controlled by the R/$\overline{W}$ signal. It is the Transmit Data register when written and Receive Data register when read.

Figure 8-1 Serial Communications Interface Block Diagram

- Noise detect
- Overrun detect
- Receiver data register full flag

8.3 SCI Transmitter Features

- Transmit data register empty flag
- Transmit complete flag
- Break send

Any SCI two-wire system requires receive data in (RDI) and transmit data out (TDO).

8.4 Data Format

Receive data in (RDI) or transmit data out (TDO) is the serial data presented between the internal data bus and the output pin (TDO) and between the input pin (RDI) and the internal data bus. Data format is as shown for the NRZ in Figure 8-2 and must meet the following criteria:

- A high level indicates a logic one and a low level indicates a logic zero.
- The idle line is in a high (logic one) state prior to transmission/reception of a message.
- A start bit (logic zero) is transmitted/received indicating the start of a message.
- The data is transmitted and received least-significant-bit first.
- A stop bit (high in the tenth or eleventh bit position) indicates the byte is complete.
- A break is defined as the transmission or reception of a low (logic zero) for some multiple of the data format.

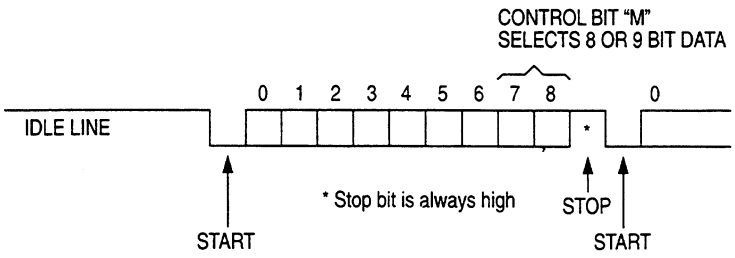


Figure 8-2 Data Format

8.5 Wake-Up Feature

In a typical multiprocessor configuration, the software protocol will usually identify the addressee(s) at the beginning of the message. To allow uninterested MPUs to ignore the remainder of the message, a wake-up feature is included, whereby all further SCI receiver flag (and interrupt) processing can be inhibited until its data line returns to the idle state. An SCI receiver is re-enabled by an idle string of at least ten (or eleven) consecutive ones. Software for the transmitter must provide for the required idle string between consecutive messages and prevent it from occurring within messages.

A second wake-up method is available in which sleeping SCI receivers can be awakened by a logic one in the high-order bit of a received character.

8.6 Receive Data In (RDI)

Receive data in (RDI) is the serial data which is presented from the input pin RDI via the SCI to the Receive Data register (RDR). While waiting for a start bit, the receiver samples the input at a rate 16 times higher than the set baud rate. This increased rate is referred to as the RT rate. The receive clock generator is controlled by the Baud Rate register (see Section 8.9.5); however, the SCI is synchronized by the start bit, independent of the transmitter.

Once a valid start bit is detected, the start bit, each data bit, and the stop bit are each sampled three times at RT intervals 8RT, 9RT and 10RT (1RT is the position where the bit is expected to start), as shown in Figure 8-3. The value of the bit is determined by voting logic, which takes the value of a majority of samples. A noise flag is set when all three samples on a valid start bit, data bit, or stop bit do not agree.

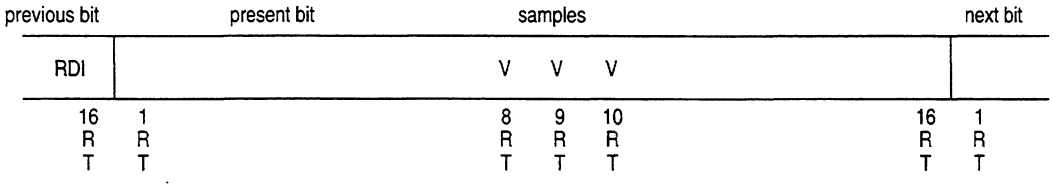


Figure 8-3 Sampling Technique used on All bits

8.7 Start Bit Detection

When the RDI input is detected low, it is tested for three more sample times (referred to as the start edge verification samples in Figure 8-4). If at least two of these three verification samples detect a logic zero, a valid start bit has been detected, otherwise the line is assumed to be idle. A noise flag is set if all three verification samples do not detect a logic zero.

If there has been a framing error (FE) without detection of a break (10 zeros for 8-bit format or 11 zeros for a 9-bit format), the circuit continues to operate as if there actually was a stop bit, and the start edge will be placed artificially. The last bit received in the data shift register is inverted to a logic one, and the three logic one start qualifiers (shown in Figure 8-4) are forced into the sample shift register during the interval when detection of a start bit is anticipated (see Figure 8-5); therefore, the start bit will be accepted no sooner than it is anticipated.

If the receiver detects that a break (RDRF=1, FE=1, Receiver Data register=$00) produced the framing error, the start bit will not be artificially induced, and the receiver must actually detect a logic one before the start bit can be recognized. See Figure 8-6.

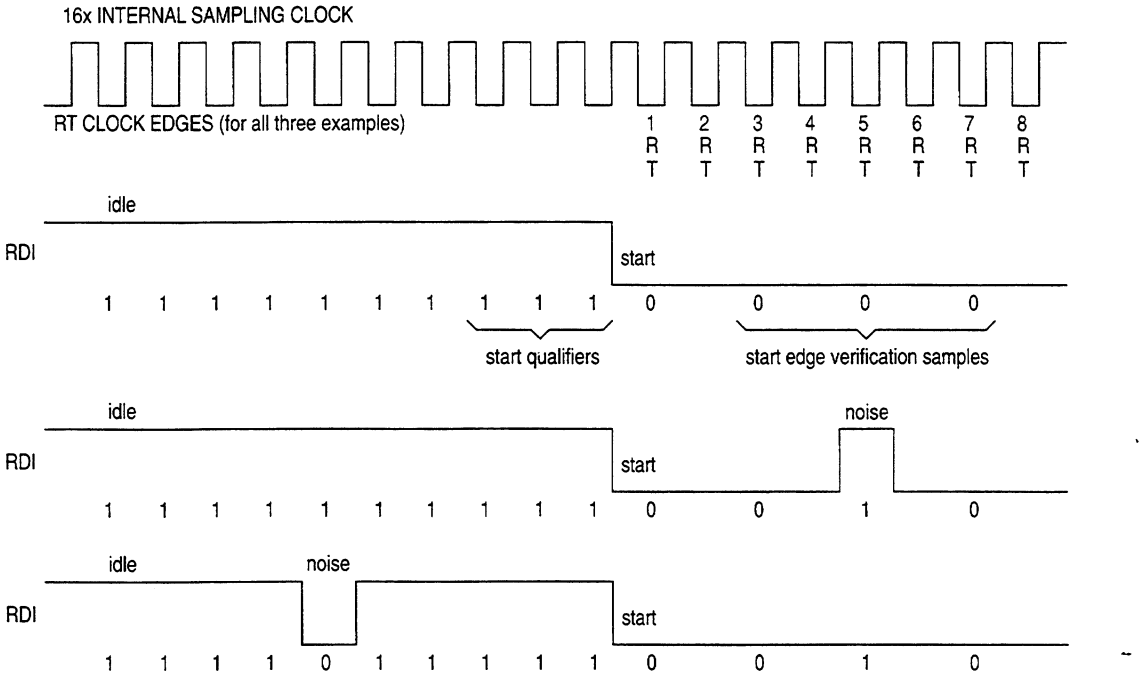
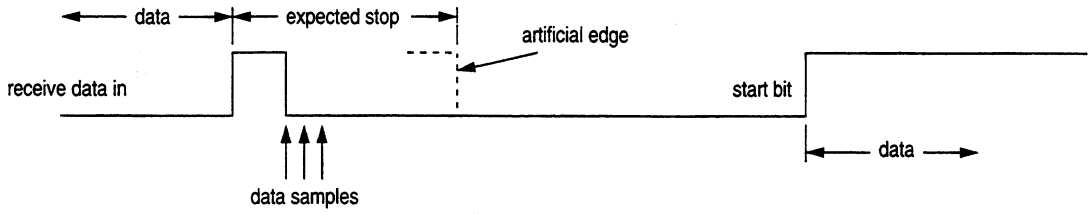
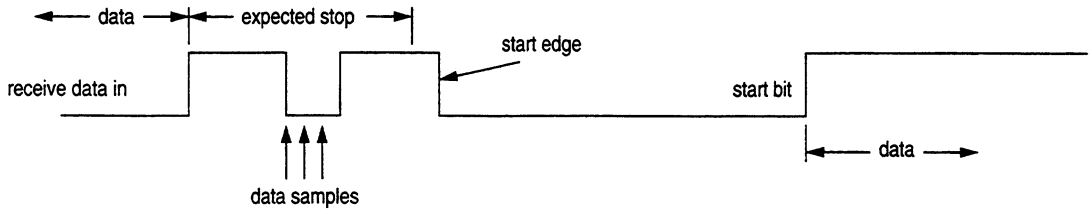


Figure 8-4 Example of Start-Bit Sampling Technique



(a) Case 1: Receive line low during artificial edge



(b) Case 2: Receive line high during start edge

Figure 8-5 SCI Artificial Start following a Framing Error

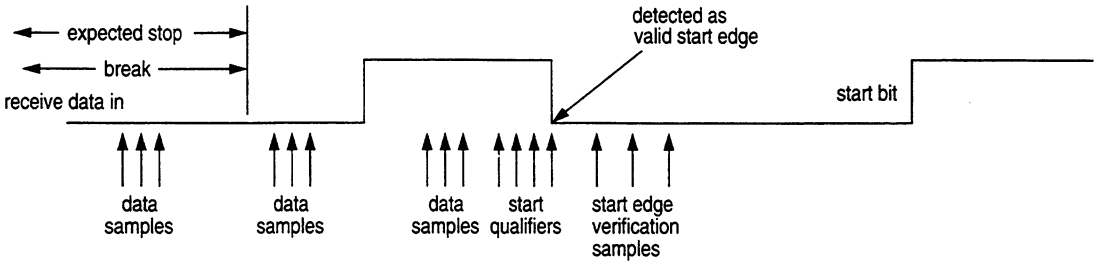


Figure 8-6 SCI Start following a Break

8.8 Transmit Data Out (TDO)

Transmit data out is the serial data which is presented from the internal data bus via the SCI and then to the output pin TDO. Transmit data format is as discussed above and shown in Figure 8-2. The transmitter generates a bit time by using a derivative of the RT clock, thus producing a transmission rate equal to 1/16 that of the receiver sample clock.

8.9 SCI Registers

There are five registers used in the SCI; the configuration of these registers are discussed in the following paragraphs.

8.9.1 Serial Communications Data Register (SCDAT)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on Reset
$11									0000 0000

The Serial Communications Data register performs two functions in the serial communications interface; i.e. it acts as the Receive Data register when it is read and as the Transmit Data register when it is written. Internally, there are two separate registers, namely: the Receive Data register (RDR) and the Transmit Data register (TDR). As shown in Figure 8-1, the TDR provides the parallel interface from the internal data bus to the transmit shift register and the RDR provides the interface from the receive shift register to the internal data bus.

When SCDAT is read, it becomes the Receive Data register and contains the last byte of data received. The Receive Data register, in Figure 8-1, is a read-only register containing the last byte of data received from the shift register for the internal data bus. The RDRF bit in the serial communications status register (bit 5 of location $10) is set to indicate that a byte has been transferred from the input serial shift register to the SCDAT. The transfer is synchronized with the receiver bit rate clock (from the receive control) as shown in Figure 8-1. All data is received least-significant-bit first.

When SCDAT is written, it becomes the Transmit Data register and contains the next byte of data to be transmitted. The Transmit Data register, in Figure 8-1, is a write-only register containing the next byte of data to be applied to the transmit shift register from the internal data bus. As long as the transmitter is enabled, data stored in the SCDAT is transferred to the transmit shift register (after the current byte in the shift register has been transmitted). The transfer from the SCDAT to the transmit shift register is synchronized with the bit rate clock (from the transmit control) as shown in Figure 8-1. All data is transmitted least-significant-bit first.

8.9.2 Serial Communications Control Register 1 (SCCR1)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on Reset
$0E	R8	T8	-	M	WAKE	-	-	-	uu-u u---

The Serial Communications Control register 1 (SCCR1) provides the control bits which:

1) determine the word length (either 8 or 9 bits);

2) selects the method used for the wake-up feature; and

3) bits 6 and 7 provide a location for storing the ninth bit for longer bytes.

R8 - Receive data bit 8

If the "M" bit is set, this bit provides a storage location for the ninth bit in the receive data byte.

T8 - Transmit data bit 8

If the "M" bit is set, this bit provides a storage location for the ninth bit in the transmit data byte.

M - Mode (select character format)

This read/write bit controls the length of the data bits for both the transmitter and receiver.

1 (set) – 1 start bit, 8 data bits, 1 stop bit.

0 (clear) – 1 start bit, 8 data, 9th data bit, 1 stop bit.

WAKE - Wake-up mode select

This bit allows the user to select the method for receive "wake-up". If the WAKE bit is a logic zero, an idle line condition will "wake up" the receiver. If the WAKE bit is set to a logic one, the system acknowledges an address bit (most significant bit). The address bit is dependent on both the WAKE bit and the M bit level (table shown below). (Additionally, the receiver does not use the wake-up feature unless the RWU control bit in Serial Communications Control register 2 is set; discussed below.)

WAKE	M	METHOD OF RECEIVER 'WAKEUP'
0	X	Detection of an idle line allows the next data byte received to cause the Receive Data register to fill and produce an RDRF.
1	0	Detection of a received one in the eight data bit allows an RDRF flag and associated error flags.
1	1	Detection of a received one in the ninth data bit allows an RDRF flag and associated error flag.

8.9.3 Serial Communications Control Register 2 (SCCR2)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on Reset
$0F	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK	0000 0000

The Serial Communications Control register 2 (SCCR2) provides the control bits which:

1) individually enable/disable the transmitter or receiver,
2) enable the system interrupts, and
3) provide the wake-up enable bit and a "send break code" bit.

TIE - Transmit Interrupt Enable

1 (set) – TDRE interrupts enabled

0 (clear) – TDRE interrupts disabled

TCIE - Transmit Complete Interrupt Enable

1 (set) – TC interrupts enabled

0 (clear) – TC interrupts disabled

RIE - Receiver Interrupt Enable

1 (set) – RDRF interrupts enabled

0 (clear) – RDRF interrupts disabled

ILIE - Idle Line Interrupt Enable

1 (set) – IDLE interrupts enabled

0 (clear) – IDLE interrupts disabled

TE - Transmitter Enabled

1 (set) – Port D pin 1 is configured as the SCI transmit output pin TDO.

0 (clear) – Port D pin 1 is configured as a standard I/O pin.

When the transmit enable bit is set, the transmit shift register output is applied to the TDO line. Depending on the state of control bit M in Serial Communications Control register 1, a preamble of 10 (M=0) or 11 (M=1) consecutive ones is transmitted when software sets the TE bit from a cleared state. If a transmission is in progress, and TE is written to a zero, then the transmitter will wait until after the present byte has been transmitted before placing the TDO pin in the idle high-impedance state. If the TE bit has been written to a zero and then set to a one before the current byte is transmitted, the transmitter will wait until that byte is transmitted and will then initiate transmission of a new preamble. After the preamble is transmitted, and provided the TDRE bit is set (no new data to transmit), the line remains idle (driven high while TE = 1); otherwise, normal transmission occurs. This function allows the user to "neatly" terminate a transmission sequence. After loading the last byte in the Serial Communications Data register and receiving the interrupt from TDRE, indicating the data has been transferred into the shift register, the user should clear TE. The last byte will then be transmitted and the line will go idle (high impedance). Reset clears the TE bit.

RE - Receiver Enable

1 (set) – Port D pin 0 is configured as the SCI receive input pin RDI.

0 (clear) – Port D pin 0 is configured as a standard I/O pin.

RWU - Receiver Wake-Up

When the receiver wake-up bit is set, it enables the "wake-up" function. The type of "wake up" mode for the receiver is determined by the WAKE bit discussed above (in the SCCR1). When the RWU bit is set, no status flags will be set. Flags which were set previously will not be cleared with RWU is set. If the WAKE bit is cleared, RWU is cleared after receiving 10 (M=0) or 11 (M=1) consecutive ones. Under these conditions, RWU cannot be set if the line is idle. If the WAKE bit is set, RWU is cleared after receiving an address bit. The RDRF flag will then be set and the address byte will be stored in the Receiver Data register. Reset clears the RWU bit.

SBK - Send Break

When the send break bit is set the transmitter sends zeros in some number equal to a multiple of the data format bits. If the SBK bit is toggled set and clear, the transmitter sends 10 (M=0) or (M=1) zeros and then reverts to idle or sending data. The actual number of zeros sent when SBK is toggled depends on the data format set by the M bit in the Serial Communications Control register 1; therefore, the break code will be synchronous with respect to the data stream. At the completion of the break code, the transmitter sends at least one high bit to guarantee recognition of a valid start bit. Reset clears the SBK bit.

8.9.4 Serial Communications Status Register (SCSR)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on Reset
$10	TDRE	TC	RDRF	IDLE	OR	NF	FE	-	1100 000-

The Serial Communications Status register (SCSR) provides inputs to the interrupt logic circuits for generation of the SCI system interrupt. In addition, a noise flag bit and a framing error bit are contained in the SCSR.

TDRE - Transmit Data Register Empty

The Transmit Data register empty bit is set to indicate that the contents of the Serial Communications Data register have been transferred to the transmit serial shift register. If the TDRE bit is clear, it indicates that the transfer has not yet complete and a write to the Serial Communications Data register will overwrite the previous value. The TDRE bit is cleared by accessing the Serial Communications Status register (with TDRE set), followed by writing to the Serial Communications Data register. New data will not be transmitted unless the Serial Communications Status register is accessed before writing to the Serial Communications Data register to clear the TDRE flag bit.

TC - Transmit Complete Flag

The transmit complete flag is set at the end of a data frame, preamble, or break condition if:

1) TE = 1, TDRE = 1, and no pending data, preamble, or break is to be transmitted; or
2) TE = 0, and the data, preamble, or break (in the transmit shift register) has been transmitted.

The TC bit is a status flag which indicates that one of the above conditions has occurred. The TC bit is cleared by accessing the Serial Communications Status register (with TC set), followed by writing to the Serial Communications Data register. It does not inhibit the transmitter function in any way.

RDRF - Receive Data Register Full Flag

When this flag is set, it indicates that data in the Receiver Serial Shift register has transferred to the Serial Communications Data register. If multiple errors are detected in any one received word, the NF, FE, and RDRF bits will be affected as appropriate during the same clock cycle. The RDRF bit is cleared when the Serial Communications Status register is accessed (with RDRF set) followed by a read of the Serial Communications Data register.

IDLE - Idle Line Detect Flag

When the idle line detect bit is set, it indicates that a receiver idle line is detected (receipt of a minimum number of ones to constitute the number of bits in the byte format). The minimum number of ones needed will be 10 (M=0) or 11 (M=1). This allows a receiver that is not in the wake-up mode to detect the end of a message, detect the preamble of a new message, or to resynchronize with the transmitter. The IDLE bit is cleared by accessing the Serial Communications Status register (with IDLE set) followed by a read of the Serial Communications Data register. The IDLE bit will not be set again until after an RDRF has been set; i.e., a new idle line occurs. The IDLE is not set by an idle line when the receiver "wakes-up" from the wake-up mode.

OR - Overrun Error Flag

When the overrun error bit is set, it indicates that the next byte is ready to be transferred from the receive shift register to the Serial Communications Data register when it is already full (RDRF it is set). Data transfer is then inhibited until the RDRF bit is cleared. Data in the Serial Communications Data register is valid in this case, but additional data received during an overrun condition (including the byte causing overrun) will be lost. The OR bit is cleared when the Serial Communications Status register is accessed (with OR set), followed by a read of the Serial Communications Data register.

NF - Noise Error Flag

The noise flag bit is set if there is noise on a "valid" start bit or if there is noise on any of the data bits, or if there is noise on the stop bit. It is not set by noise on the idle line nor by invalid

(false) start bits. If there is noise, the NF bit is not set until the RDRF flag is set. Each data bit is sampled three times as described above in RECEIVE DATA IN and shown in Figure 8-3. The NF bit represents the status of the byte in the Serial Communications Data register. For the byte being received (shifted in) there will also be a "working" noise flag the value of which will be transferred to the NF bit when the serial data is loaded into the Serial Communications Data register. The NF bit does not generate an interrupt because the RDRF bit gets set with NF and can be used to generate the interrupt. The NF bit is cleared when the Serial Communications Status register is accessed (with NF set), followed by a read of the Serial Communications Data register.

FE - Framing Error Flag

The framing error bit is set when the byte boundaries in the bit stream are not synchronized with the receiver bit counter (generated by a "lost" stop bit). The byte is transferred to the Serial Communications Data register and the RDRF bit is set. The FE bit does not generate an interrupt because the RDRF bit is set at the same time as FE and can be used to generate the interrupt. Note that if the byte received causes a framing error and it will also cause an overrun if transferred to the Serial Communications Data register, then the overrun bit will be set, but not the framing error bit, and the byte will not be transferred to the Serial Communications Data register. The FE bit is cleared when the Serial Communications Status register is accessed (with FE set) followed by a read of the Serial Communications Data register.

8.9.5 Baud Rate Register

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on Reset
$0D	-	-	SCP1	SCP0	-	SCR2	SCR1	SCR0	--00 -uuu

The Baud Rate register provides the means for selecting different baud rates which may be used as the rate control for the transmitter and receiver. The SCP0 & SCP1 bits function as a prescaler for the SCR0, SCR1, & SCR2 bits. Together, these five bits provide multiple, baud rate combinations for a given internal processor clock frequency.

SCP1, SCP0 - Serial Prescaler Select Bits

These two bits in the Baud Rate register are used as a prescaler to increase the range of standard baud rates controlled by the SCR0-SCR2 bits. A table of the prescaler internal processor clock division versus bit levels is provided below.

SCP1	SCP0	INTERNAL PROCESSOR CLOCK DIVIDE BY
0	0	1
0	1	3
1	0	4
1	1	13

SCR2, SCR1, SCR0 - SCI Rate Select Bits

These three bits in the Baud Rate register are used to select the baud rates for both the transmitter and receiver. A table of baud rates versus bit levels is shown below. Reset does not affect the SCR2-SCR0 bits.

SCR2	SCR1	SCR0	PRESCALER OUTPUT DIVIDE BY
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

Note: Figure 8-7 and Tables 8-1 and 8-2 illustrate the divided chain used to obtain the baud rate clock (transmit clock). Note that there is a fixed rate divide-by-16 between the receive clock (RT) and the transmit clock (TX). The actual divider chain is controlled by the combined SCP0 & SCP1 and SCR0-SCR2 bits in the Baud Rate register as illustrated. All divided frequencies shown in the first table represent the final transmit clock (the actual baud rate) resulting from the internal processor clock division shown in the "divide-by" column only (prescaler division only). Table 8-2 illustrates how the prescaler output can be further divided by action of the SCI select bits SCR0-SCR2. For example, assume that a 9600 Hz baud rate is required with a 2.4576 MHz PLL output clock. In this case the prescaler bits (SCP0 & SCP1) could be configured as a divide-by-one or a divide-by-four. If a divide-by-four prescaler is used, then the SCR0-SCR2 bits must be configured as a divide-by-two. This results in a divide-by-128 of the internal processor clock to produce a 9600Hz baud rate clock. Using the same PLL output clock, the 9600 baud rate can be obtained with a prescaler divide-by-one and the SCR0-SCR2 bits configured for a divide-by-eight.

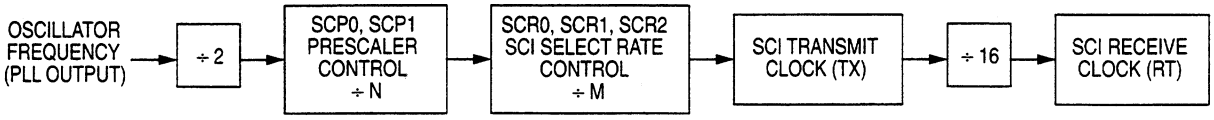


Figure 8-7 Rate Generator Division

Table 8-1 Prescaler Highest Baud Rate Frequency Output

SCP1	SCP0	CLOCK* DIVIDED BY	PLL OUTPUT CLOCK FREQUENCY (MHz)			
			7.3728	4.9125	2.4576	0.6144
0	0	1	230.40KHz	153.50KHz	76.80KHz	19.20KHz
0	1	3	76.80KHz	51.17KHz	25.60KHz	6.40KHz
1	0	4	57.60KHz	38.38KHz	19.20KHz	4.80KHz
1	1	13	17.72KHz	11.81KHz	5.907KHz	1.477KHz

* This clock is the internal processor clock

Note: The divided frequencies shown in Table 8-1 represent baud rates which are the highest transmit baud rate (TX) that can be obtained by a specific clock frequency and only using the prescaler division. Lower baud rate may be obtained by providing a further division using the SCI rate select bits as shown below for some representative prescaler outputs.

Table 8-2 Transmit Baud Rate Output for a given Prescaler Output

SCR2	SCR1	SCR0	DIVIDED BY	REPRESENTATIVE HIGHEST PRESCALER BAUD RATE OUPUT			
				153.50KHz	76.80KHz	19.20KHz	9.600KHz
0	0	0	1	153.50KHz	76.80KHz	19.20KHz	9600Hz
0	0	1	2	76.80KHz	38.40KHz	9600Hz	4800Hz
0	1	0	4	38.40KHz	19.20KHz	4800Hz	2400Hz
0	1	1	8	19.20KHz	9600Hz	2400Hz	1200Hz
1	0	0	16	9600Hz	4800Hz	1200Hz	600Hz
1	0	1	32	4800Hz	2400Hz	600Hz	300Hz
1	1	0	64	2400Hz	1200Hz	300Hz	150Hz
1	1	1	128	1200Hz	600Hz	150Hz	75Hz

Note: Table 8-2 illustrates how the SCI select bits can be used to provide lower transmitter baud rates by further dividing the prescaler output frequency. The four examples are only representative samples. In all cases, the baud rates shown are transmit baud rates (transmit clock) and the receiver clock is 16 times higher in frequency than the actual baud rate.

9
SERIAL PERIPHERAL INTERFACE (SPI)

The serial peripheral interface (SPI) is an interface built into the MC68HC05L11 microcontroller which allows several SPI microcontrollers, or SPI-type peripherals to be interconnected within a single "black box" or on the same printed circuit board. In a serial peripheral interface, separate wires (signals) are required for data and clock. In the SPI format, the clock is not included in the data stream and must be furnished as a separate signal. An SPI system may be configured as one containing one master MCU and several slave MCUs, or as a system in which an MCU is capable of being either a master or slave.

Figure 9-1 illustrates two different system configurations. Figure 9-1(a) represents a system of five different microcontrollers in which there is one master and four slaves (0,1,2,3). In this system four basic lines (signals) are required for MOSI (master out slave in), MISO (master in slave out), SCK (serial clock), and $\overline{SS}$ (slave select) lines. Figure 9-1(b) represents a system of five microcontrollers in which three can be either master of slave and two are slave only.

9.1 SPI Features

- Full Duplex, Three-Wire Synchronous Transfers
- Master or Slave Operation
- 1.8432 MHz (Max.) Master Bit Frequency
- 3.6864 MHz (Max.) Slave Bit Frequency
- Four programmable Master Bit Rates
- Programmable Clock Polarity and Phase
- End of Transmission Interrupt Flag
- Data Collision Flag Protection
- Master-Master Mode Fault Protection Capability

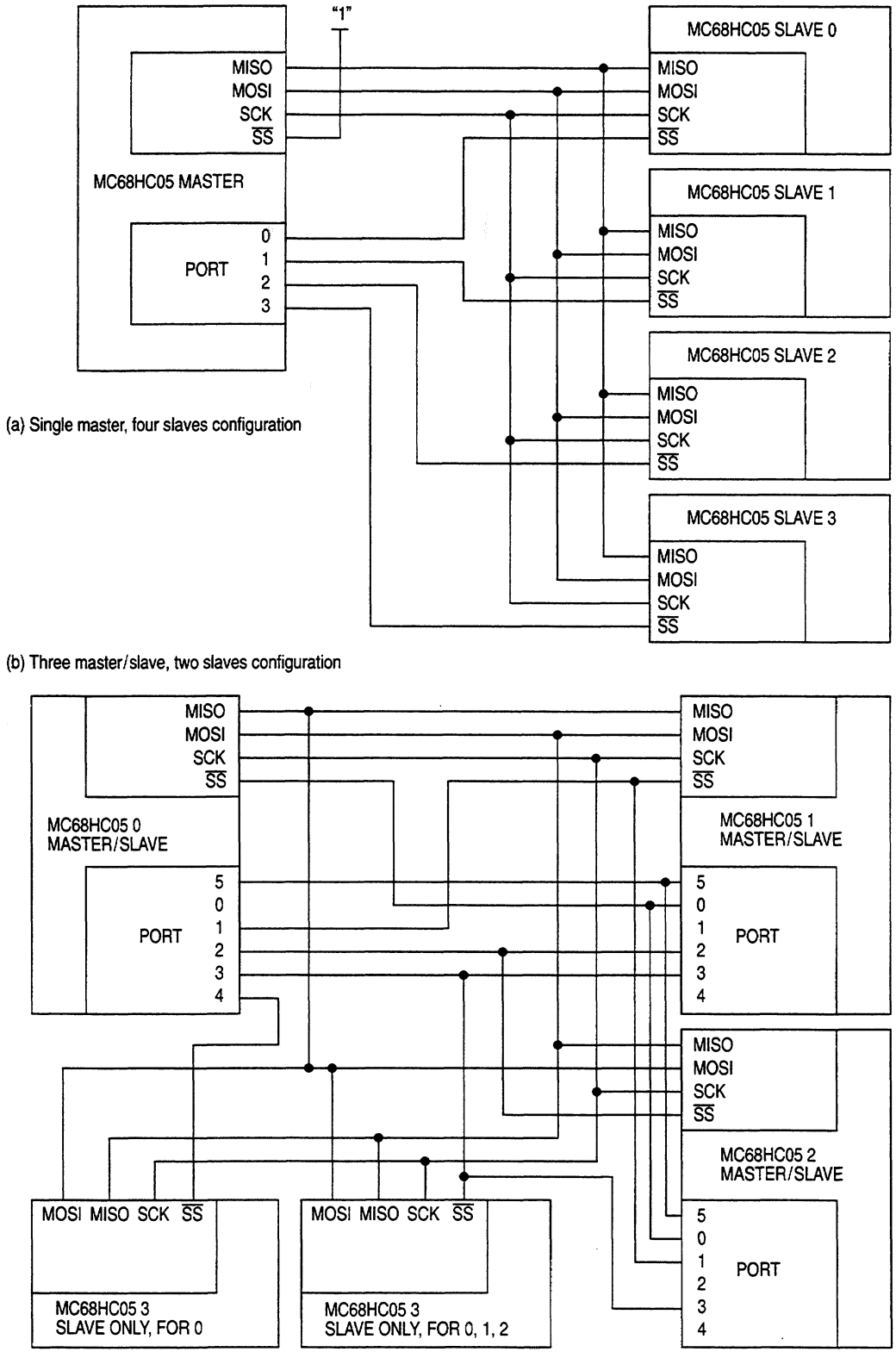


Figure 9-1 SPI Master-Slave System Configurations

9.2 SPI Signals Description

The four SPI signals (MOSI, MISO, SCK, and $\overline{SS}$) are described in the following paragraphs. Each signal is described for both the master and slave mode.

9.2.1 Master Out Slave In (MOSI)

The MOSI pin is configured as an output in a master (mode) device and as an input in a slave (mode) device. Data is transferred serially from a master to a slave on this line, most significant bit first. The timing diagram of Figure 9-2 shows the relationship between data and serial clock (SCK). As shown in Figure 9-2, four possible timing relationships may be chosen by using control bits CPOL & CPHA in the Serial Peripheral Control register (location $22). The master device always allows data to be applied on the MOSI line a half-cycle before the serial clock edge (SCK) in order for the slave device to latch the data.

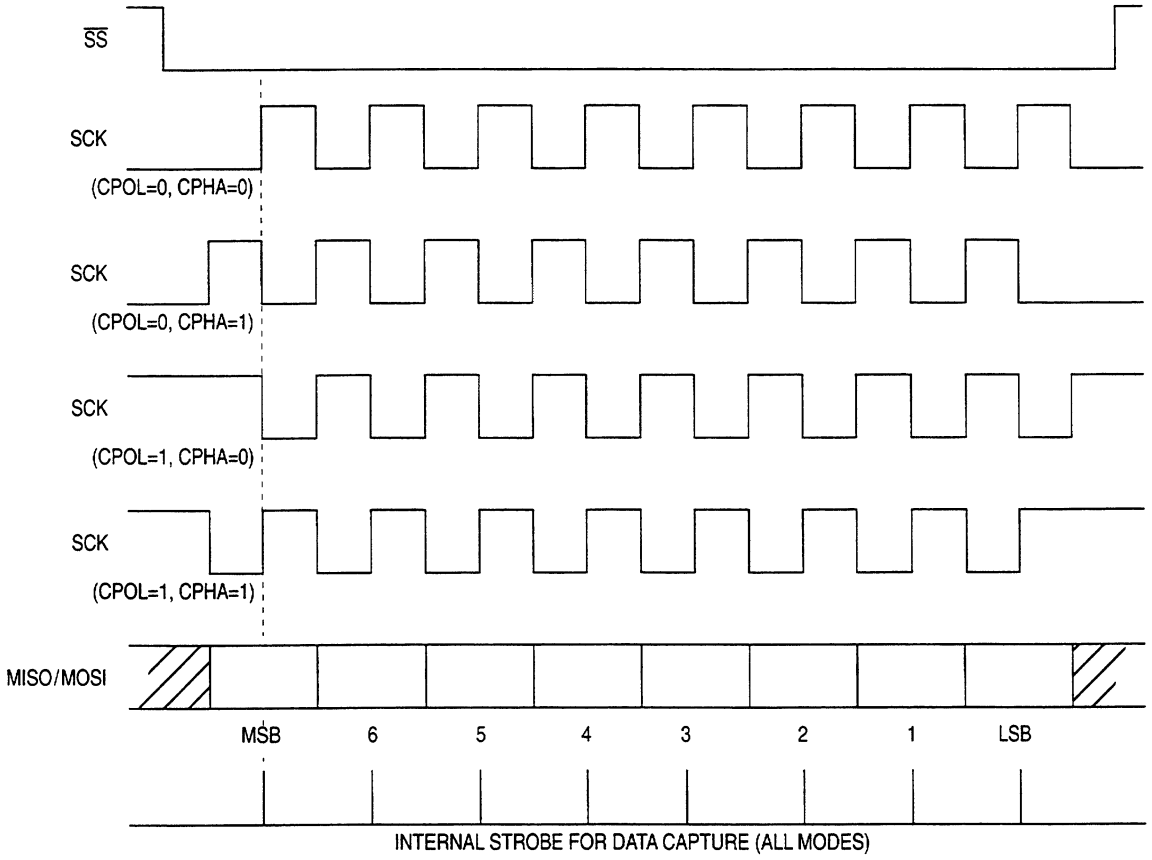


Figure 9-2 SPI Data/Clock Timing Diagram

Note: Both the master device and slave device(s) must be programmed to similar timing modes for proper data transfer.

When the master device transmits data to a slave via the MOSI line, the slave device responds by sending data to the master device via the MISO line. This implies full duplex transmission with both data out and data in synchronized with the same clock signal (one which is provided by the master device). Thus the byte transmitted is replaced by the byte received and eliminates the need for separate transmit-empty and receiver-full status bits. A single status bit (SPIF) in the Serial Peripheral Status register (location $23) is used to signify that the I/O operation is complete.

Configuration of the MOSI pin is a function of the MSTR bit in the Serial Peripheral Control register (SPCR, location $22). When a device is operating as a master, the MOSI pin is an output because the program in firmware set the MSTR bit as a logic one.

9.2.2 Master In Slave Out (MISO)

The MISO pin is configured as an input in a master (mode) device and as an output pin in a slave (mode) device. Data is transferred serially from a slave to a master on this line, most significant bit first. The MISO pin of a slave is placed in a high-impedance state if it is not selected by a master; i.e., its $\overline{SS}$ pin is a logic one. The timing diagram in Figure 9-2 shows the relationship between data and serial clock (SCK). As shown in Figure 9-2, four possible timing relationships may be chosen by using control bits CPOL and CPHA. The master device always allows data to be applied on the MISO line a half-cycle before the serial clock edge (SCK) in order for the slave device to latch the data.

Note: Both the slave device(s) and a master device must be programmed to similar timing modes for proper data transfer.

When a master device transmits data to a slave device via the MOSI line, the slave device responds by sending data to the master device via the MISO line. This implies full duplex transmission with both data out and data in synchronized with the same clock signal (one which is provided by the master device). Thus, the byte transmitted is replaced by the byte received and eliminates the need for separate transmit-empty and receiver-full status bits. A single status bit (SPIF) in the Serial Peripheral Status register (SPSR, location $23) is used to signify that the I/O operation is complete.

In the master device, the MSTR control bit in the Serial Peripheral Control register (SPCR, location $22) is set to a logic one (by the program) to allow the master device to receive data on its MISO pin. In the slave device, its MISO pin is enabled by the logic level of the $\overline{SS}$ pin; i.e., if $\overline{SS}$=1 then the MISO pin is placed in a high impedance state, whereas, if $\overline{SS}$=0 the MISO pin is an output for the slave device.

9.2.3 Slave Select ($\overline{SS}$)

The slave select ($\overline{SS}$) pin is a fixed input which receives an active low signal that is generated by the master device to enable slave device(s) to accept data. To ensure that data will be accepted by a slave device, the $\overline{SS}$ signal line must be a logic low prior to the occurrence of serial SCK and must remain low until after the last (eighth) SCK cycle. Figure 9-2 illustrates the relationship between SCK and the data for two different level combinations of CPHA, when $\overline{SS}$ is pulled low. These are: 1) with CPHA = 1 or 0, the first bit or data is applied to the MISO line for transfer, and 2) when CPHA = 0 the slave device is prevented from writing to its data register. Refer to the WCOL status flag in the Serial Peripheral Status register (bit 6, location $23) description for further information on the effects that the $\overline{SS}$ input and CPHA control bit have on the I/O register. A high level $\overline{SS}$ signal forces the MISO line to the impedance state. Also, SCK and the MOSI line are ignored by a slave device when its $\overline{SS}$ signal is high.

When the device is a master, it constantly monitors its $\overline{SS}$ signal input for a logic low. The master device will become a slave device when its $\overline{SS}$ signal is detected low. This ensures that there is only one master controlling the $\overline{SS}$ line for a particular system. When the $\overline{SS}$ line is detected low, it clears the MSTR control bit in the SPSR (bit 4, location $22). Also, control bit SPE in the SPCR (bit 6, location $22) is cleared and causes the serial peripheral interface to be disabled. The MODF flag bit in the Serial Peripheral Status register (location $23) is also set to indicate to the master device that another device is attempting to become a master. Two devices attempting to be outputs are normally the result of a software error; however, a system could be configured which would contain a default master which would automatically “take-over” and restart the system.

9.2.4 Serial Clock (SCK)

The serial clock is used to synchronize the movement of data both in and out the device through its MOSI and MISO pins. The master and slave devices are capable of exchanging a data byte of information during a sequence of eight clock pulses. Since SCK is generated by the master device, the SCK line becomes an input in all slave devices and synchronizes slave data transfer. The type of clock and its relationship to data are controlled by the CPOL and CPHA bits in the SPCR (location $22). Refer to Figure 9-2 for timing.

The master device generates the SCK through a circuit driven by the internal processor clock. Two bits (SPR0 and SPR1) in the SPCR (location $22) of the master device select the clock rate. The master device uses the SCK to latch incoming slave device data on the MISO line and shifts out data to the slave device on the MOSI line. Both master and slave devices must be operated in the same timing mode as controlled by the CPOL and CPHA bit in the SPCR. In the slave device, SPR0 & SPR1 have no effect on the operation of the serial peripheral interface. Timing is shown in Figure 9-2.

9.3 Functional Description

A block diagram of the serial peripheral interface is shown in Figure 9-3. In a master configuration, the master start logic receives an input from the CPU (in form of a write to the SPI rate generator) and generates the serial clock (SCK) based on the internal processor clock. This clock is also used internally to control the state controller as well as the 8-bit shift register. As a master device, data is parallel loaded into the 8-bit shift register (from internal bus) during a write cycle and then shifted out serially to the MOSI pin for application to the slave device(s). During a read cycle, data is applied serially from a slave device via the MISO pin to the 8-bit shift register. After the 8-bit shift register is loaded, its data is parallel transferred to the read buffer and then is made available to the internal data bus during a CPU read cycle.

In a slave configuration, the slave start logic receives a logic low (from a master device) at the $\overline{SS}$ pin and serial clock input (from the same master device) at the SCK pin. Thus, the slave is synchronized with the master. Data from the master is received serially at the slave MOSI pin and loads the 8-bit shift register. After the 8-bit shift register is loaded, its data is parallel transferred to the read buffer and then is made available to the internal data bus during a CPU cycle. During a write cycle, data is parallel loaded into the 8-bit shift register from the internal data bus and then shifted out serially to the MISO pin for application to the master device.

Figure 9-4 illustrates the MOSI, MISO, and SCK master-slave interconnections. Note that in Figure 9-4 the master $\overline{SS}$ pin is tied to a logic high and the slave $\overline{SS}$ pin is a logic low. Figure 9-1 shows a larger system interconnection for these pins. Note that in Figure 9-1, all $\overline{SS}$ pins are connected to a port pin of a master/slave device. In this case any of the devices can be a slave.

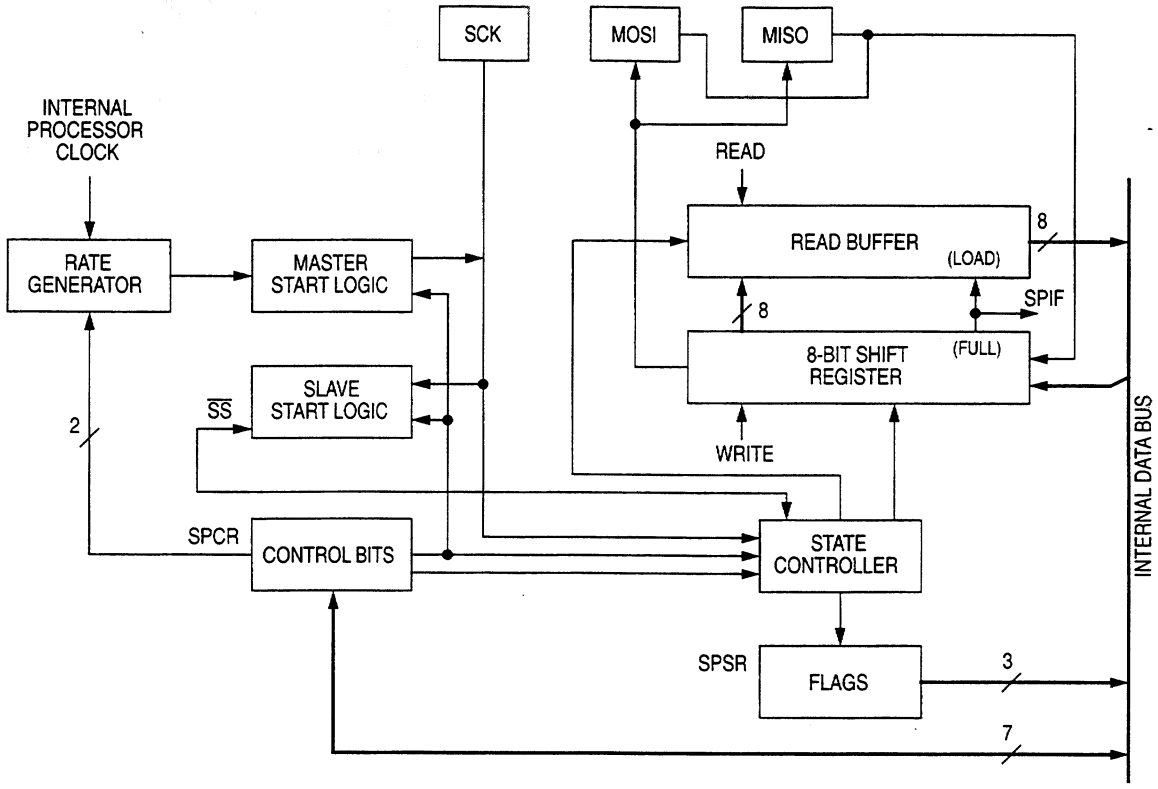
9.4 SPI Registers

There are three registers in the serial parallel interface which provide control, status, and data storage functions. These registers are the Serial Peripheral Control register (SPCR, location $22), Serial Peripheral Status register (SPSR, location $23), and Serial Peripheral Data I/O register (SPDR, location $24). Description of each register is described below.

9.4.1 Serial Peripheral Control Register (SPCR)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on Reset
$22	SPIE	SPE	-	MSTR	CPOL	CPHA	SPR1	SPR0	00-0 uuuu

The Serial Peripheral Control register bits are defines as follows:



Note: $\overline{SS}$, SCK, MOSI, and MISO are external pins; where

$\overline{SS}$ - provides a logic low to select a slave device for a transfer with a master device.

SCK - provides system clock when device is configured as a master unit. Receives system clock when device is configured as a slave unit.

MOSI - provides serial output to slave unit(s) when device is configured as a master. Receives serial input from master when device is configured as a slave unit.

MISO - receives serial input from slave unit(s) when device is configured as a master. Provides serial output to master when device is configured as a slave unit.

Figure 9-3 Serial Peripheral Interface Block Diagram

SPIE - Serial Peripheral Interrupt Enable

1 (set) – Serial Peripheral Interrupt Enabled

0 (clear) – Serial Peripheral Interrupt Disabled

SPE - Serial Peripheral Output Enable

1 (set) – Port D pins 2, 3, 4, 5 configured as SPI pins

0 (clear) – Port D pins 2, 3, 4, 5 configured as standard I/O pins

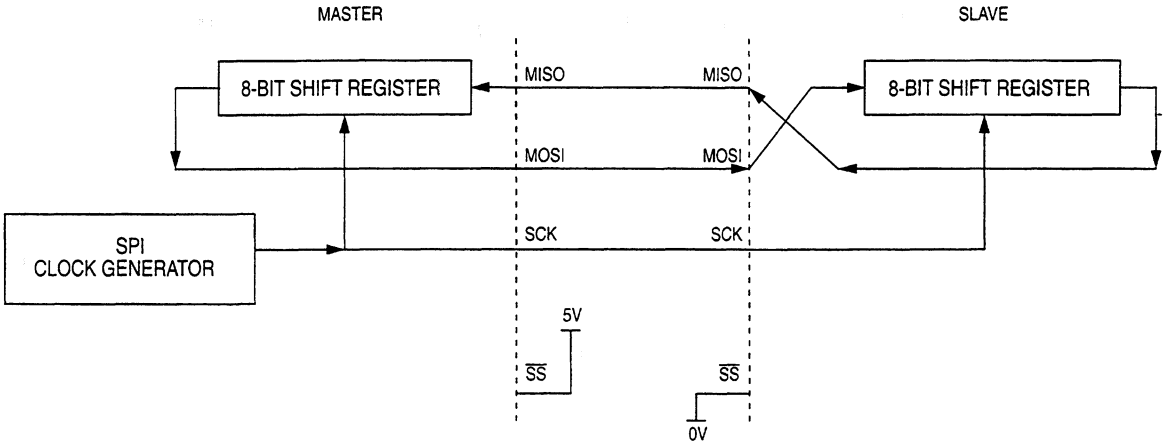


Figure 9-4 SPI Master-Slave Interconnection

When the serial peripheral output enable control bit is set, all output drive is applied to the external pins and the system is enabled. When the SPE bit is set, it enables the SPI system by connecting it to the external pins thus allowing it to interface with the external SPI bus. The pins that are defined as output depend on which mode (master or slave) the device is in. Because the SPE bit is cleared by reset, the SPI system is not connected to the external pins upon reset.

MSTR - Master

1 (set) – SPI configured as master

0 (clear) – SPI configured as slave

The master bit determines whether the device is a master or a slave. If the MSTR bit is a logic zero it indicates a slave device and a logic one denotes a master device. If the master mode is selected, the function of the SCK pin changes from an input to an output and the function of the MSIO and MOSI pins are reversed. This allows the user to wire device pins MISO to MISO, and MOSI to MOSI, and SCK to SCK without incident. The MSTR bit is cleared by reset; therefore, the device is always placed in the slave mode during reset.

CPOL - Clock Polarity

1 (set) – SCK pin high during master idle

0 (clear) – SCK pin low during master idle

The clock polarity bit controls the normal or steady state logic of the clock when data is not being transferred. The CPOL bit affects both the master and slave modes. It must be used in conjunction with the clock phase control bit (CPHA) to produce the desired clock-data relationship between a master and a slave device. When the CPOL bit is a logic zero, it

produces a steady state low value at the SCK pin of the master device. If the CPOL bit is a logic one, a high value is produced at the SCK pin of the master device when no data is being transferred. The CPOL bit is not affected by reset. Refer to Figure 9-2.

CPHA - Clock Phase

1 (set) – 2nd clock edge transition

0 (clear) – 1st clock edge transition

The clock phase bit controls the relationship between the data on the MISO and MOSI pins and the clock produced or received at the SCK pin. This control has effect in both the master and slave modes. It must be used in conjunction with the clock polarity control bit (CPOL) to produce the wanted clock-data relation. The CPHA bit in general selects the clock edge which captures data and allows it to change states. It has its greatest impact on the first bit transmitted (MSB) in that it does or does not allow a clock transition before the first data capture edge. The CPHA bit is not affected by reset. Refer to Figure 9-2.

SPR1, SPR0 - Serial Peripheral Rate

These two serial peripheral rate bits select one of four baud rates to be used as SCK if the device is a master; however, they have no effect in slave mode. The slave device is capable of shifting data in and out at a maximum rate which is equal to the CPU clock. A rate table is given below for the generation of the SCK from the master. The SPR1 and SPR0 bits are not affected by reset.

SPR1	SPR0	INTERNAL PROCESSOR CLOCK DIVIDE BY
0	0	2
0	1	4
1	0	16
1	1	32

9

9.4.2 Serial Peripheral Status Register (SPSR)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on Reset
$23	SPIF	WCOL	-	MODF	-	-	-	-	00-0 ----

This is a read-only register. The status flags which generate a serial peripheral interface (SPI) interrupt may be masked by the SPIE control bit in the Serial Peripheral Control register. The WCOL bit does not cause an interrupt. The Serial Peripheral Status register bits are defined as follows:

SPIF - Serial Peripheral Data Transfer Complete Flag

The serial peripheral data transfer flag bit notifies the user that a data transfer between the device and an external device has been completed. With the completion of the data transfer, SPIF is set, and if SPIE is set, a serial peripheral interrupt is generated. During the clock cycle that SPIF is being set, a copy of the received data byte in the shift register is moved to a buffer. When the data register is read, it is the buffer that is read. During an overrun condition, when the master device has sent several bytes of data and the slave device has not responded to the first SPIF, only the first byte sent is contained in the receiver buffer and all other bytes are lost.

The transfer of data is initiated by the master device writing to its Serial Peripheral Data register.

Clearing the SPIF bit is accomplished by a software sequence of accessing the Serial Peripheral Status register while SPIF is set and followed by a write to or a read of the Serial Peripheral Data register. While SPIF is set, all writes to the Serial Peripheral Data register are inhibited until the Serial Peripheral Status register is read. This occurs in the master device. In the slave device, SPIF can be cleared (using a similar sequence) during a second transmission; however, it must be cleared before the second SPIF in order to prevent an overrun condition. The SPIF bit is cleared by reset.

WCOL - Write Collision Status

The function of the write collision status bit is to notify the user that an attempt was made to write to the Serial Peripheral Data register while a data transfer was taking place with an external device. The transfer continues uninterrupted; therefore, a write will be unsuccessful. A "read collision" will never occur since the received data byte is placed in a buffer in which access is always synchronous with the MCU operation. If a "write collision" occurs, WCOL is set but no SPI interrupt is generated. The WCOL is a status flag only.

Clearing the WCOL bit is accomplished by a software sequence of accessing the Serial Peripheral Status register while WCOL is set, followed by 1), a read if the Serial Peripheral Data register prior to the SPIF bit being set, or 2) a read or write of the Serial Peripheral Data register after the SPIF bit is set. A write to the Serial Peripheral Data register (SPDR) prior to the SPIF bit being set, will result in the generation of another WCOL status flag. Both the SPIF and WCOL bits will be cleared in the same sequence. If a second transfer has started while trying to clear (the previously set) SPIF and WCOL bits with a clearing sequence containing a write to the Serial Peripheral Data register, only the SPIF bit will be cleared.

A collision of a write to the Serial Peripheral Data register while an external data transfer is taking place can occur in both the master mode and the slave mode, although with proper programming the master device should have sufficient information to prevent this collision.

Collision in the master device is defined as a write of the Serial Peripheral Data register while the internal rate clock (SCK) is in the process of transfer. The signal of the $\overline{SS}$ pin is always high on the master device.

A collision in a slave device is defined in two separate modes. One problem arises in a slave device when the CPHA control bit is a logic zero. When CPHA is a logic zero, data is latched with the occurrence of the first clock transition. The slave device does not have any way of knowing when that transition will occur; therefore, the slave device collision occurs when it attempts to write the Serial Peripheral Data register after its $\overline{SS}$ pin has been pulled low. The $\overline{SS}$ pin of the slave device freezes the data in its Serial Peripheral Data register and does not allow it to be altered if the CPHA bit is logic zero. The master device must raise the $\overline{SS}$ pin of the slave device high between each byte transferred to the slave device.

The second collision mode is defined for the state of the CPHA control bit being a logic one. With the CPHA bit set, the slave device will be receiving a clock (SCK) edge prior to the latch of the first data transfer. This first clock edge will freeze the data in the slave device I/O register and allow the most significant bit onto the external MISO pin of the slave device. The $\overline{SS}$ pin low state enables the slave device but the drive onto the MOSI pin does not take place until the first data transfer clock edge. The WCOL bit will only be set if the I/O register is accessed while a transfer is taking place. By definition of the second collision mode, a master device might hold a slave device $\overline{SS}$ pin low during a transfer of several bytes of data without a problem.

A special case of write collision occurs in the slave device. This happens when the master device starts a transfer sequence (an edge of SCK for CPHA=1; or an active $\overline{SS}$ transition for CPHA=0) at the same time the slave device CPU is writing to its serial peripheral interface data register. In this case it is assumed that the data byte written (in the slave device serial peripheral interface) is lost and the contents of the slave device read buffer becomes the byte that is transferred. Because the master device receives back the last byte transmitted, the master device can detect that a fatal write collision occurred.

Since the slave device is operating asynchronously with the master device, the WCOL bit may be used as an indicator of a collision occurrence. This helps to alleviate the user from a strict real-time programming effort. The WCOL bit is cleared by reset.

9

MODF - Mode Fault

The function of the mode fault flag bit is defined for the master mode (device). If the device is a slave device the MODF bit will be prevented from toggling from a logic zero to a logic one; however, this does not prevent the device from being in the slave mode with MODF bit set. The MODF bit is normally a logic zero and is set only when the master device has its $\overline{SS}$ pin pulled low. Toggling the MODF bit to a logic one affects the internal serial peripheral interface (SPI) system in the following ways:

1) MODF is set and SPI interrupt is generated if SPIE=1;
2) The SPE bit is forced to a logic zero. This blocks all output drive from the device, disables the SPI system;
3) The MSTR bit is forced to a logic zero, thus forcing the device into the slave mode.

Clearing the MODF is accomplished by a software sequence of accessing the Serial Peripheral Status register while MODF is set followed by a write to the Serial Peripheral Control register. Control bits SPE and MSTR may restored to their original set states during this clearing sequence or after the MODF bit has been cleared. Hardware does not allow the user to set the SPE and MSTR bit while MODF is a logic one unless it is during the proper clearing sequence. The MODF flag bit indicates that there might have been a multi-master conflict for system control and allows a proper exit from system operation to a reset or default system state. The MODF is cleared by reset.

9.4.3 Serial Peripheral Data I/O Register (SPDR)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on Reset
$24									

The Serial Peripheral Data I/O register is used to transmit and receive data on the serial bus. A write to this register will initiate transmission/reception of another byte and this will only occur in the master device. A slave device writing to this data I/O register will not initiate a transmission. At the completion of transmitting a byte of data, the SPIF is set in both the master and slave devices. A write or read of the Serial Peripheral Data I/O register, after accessing the Serial Peripheral Status register with SPIF set, will clear SPIF.

During the clock cycle that the SPIF bit is being set, a copy of the received data byte in the shift register is moved to a buffer. When the user reads the Serial Peripheral Data I/O register, the buffer is actually being read. During an overrun condition, when the master device has sent several bytes of data and the slave device has not internally responded to clear the first SPIF, only the first byte is contained in the receive buffer of the slave device; all others are lost. The user may read the buffer at any time. The first SPIF must be cleared by the time a second transfer of data from the shift register to the read buffer is initiated, otherwise an overrun condition will exist.

A write to the Serial Peripheral Data I/O register is not buffered and places data directly into the shift register for transmission.

The ability to access the Serial Peripheral Data I/O register is limited when a transmission is taking place. It is important to read the discussion defining the WCOL and SPIF status bits to understand the limits on using the Serial Peripheral Data I/O register.

9.5 SPI during Wait Mode

When the MCU enters the Wait mode, the CPU clock is halted. All CPU action is suspended; however, the SPI system remain active. In fact an interrupt from the SPI (in addition to a logic low on the IRQ1, IRQ2 or interrupt from keyboard or RTC or a logic low on the RESET pin or a power on reset) causes the processor to exit the Wait mode. See also Section 6.2.4.

9.6 SPI during Stop Mode

When the processor executes the STOP instruction, the internal oscillator is turned off. This halts all internal CPU processing, including the operation of the serial peripheral interface. The only way for the MCU to "wake-up" from the Stop mode is by receipt of an external interrupt (logic low on $\overline{IRQ1}$, $\overline{IRQ2}$), interrupt from keyboard, RTC, or the detection of a reset (logic low on $\overline{RESET}$ pin or a power-on reset).

When the MCU enters the Stop mode, the baud rate generator which drives the SPI shuts down. This essentially stops all master mode SPI operation; the master SPI is unable to transmit or receive any data. If the STOP instruction is executed during an SPI transfer, that transfer is halted until the MCU exits the Stop mode (provided it is an exit resulting from a logic low on the $\overline{IRQ1}$, $\overline{IRQ2}$ pin, interrupt from keyboard or RTC or by the detection of a reset of logic low on $\overline{RESET}$ pin or a power on reset). If the Stop mode is exited by a reset, then the appropriate control/status bits are cleared and the SPI is disabled. If the device is in the slave mode when the STOP instruction is executed, the slave SPI will still operate. It can still accept data and clock information in addition to transmitting its own data back to a master device.

Since the MC68HC05 is the bus master, it internally controls the function of its MOSI and MISO lines; thus writing data to the slave devices on the MOSI and reading data from the slave devices on the MISO lines. The master device selects the individual slave devices by using four pins of a parallel port to control the four $\overline{SS}$ pins of the slave devices. A slave device is selected when the master device pulls its $\overline{SS}$ pin low. The $\overline{SS}$ pins are pulled high during reset since the master device ports will be forced to be inputs at that time, thus disabling the slave devices. Note that the master can enable all slaves when writing to them, but can only read from one slave at a time. This is to prevent bus contention on the MISO line.

Example: in a one master, three slaves system, the master writes to the three slaves' display driver to clear a display with a single I/O operation. To ensure that proper data transmission between the master device and a slave device, the master device may have the slave device responding with a data byte previously sent by the master (this data byte could be inverted or at least be a byte that is different from the last one sent by the master device). The master device will always receive the byte back from the slave device if all MISO and MOSI lines are connected and the slave has not written to its data I/O register. Other transmission protocols may be defined using ports for handshake lines or data bytes with command fields.

A multi-master system may also be configured by the user. A system of this type is shown in Figure 9-1(b). An exchange of master control could be implemented using a handshake method through the I/O ports or by an exchange of code messages through the serial peripheral interface system. There are two bits which are important to this configuration, the MSTR bit in the Serial Peripheral Control register and the MODF bit in the Serial Peripheral Status register.

See also Section 6.1.4.

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10
LIQUID CRYSTAL DISPLAY

This section describes the liquid crystal display control unit.

10.1 Features

- Full graphics manipulation using serial access
- Hardware assisted smoothing for vertical and horizontal scrolling
- Hardware assisted screen partitioning and attribution
- Selectable font pitch sizes
- Selectable multiplexing ratio from 32 to 256 for different panel sizes

10.2 General System

The LCD control unit in the MC68HC05L11 is designed for optimum performance when used in conjunction with Motorola's Segment and Backplane Drivers. Typically, the MC141514 and MC141518 segment drivers, and the MC141512 and MC141516 backplane drivers, are suitable for this MCU.

Figure 10-1 is a block diagram showing a typical LCD system connected to the MC68HC05L11. In the MCU, the Row Data Serial Interface is responsible for transferring a row of display data between the MCU and LCD drivers. The address of the row is supplied by the data bus with the help of the Segment Control Interface. The LCD Timing Generator is responsible for generating two periodic signals (FRM - frame timing synchronization, and BPCLK - backplane clock) to synchronize LCD drivers activities. Figure 10-2 shows a more detailed description of the LCD drivers. (See Appendix A for Segment Drivers and Appendix B for Backplane Drivers).

As the LCD display is not memory mapped to the MCU's main memory, the principle of operation is by shifting data bits serially in and out between the MCU and cascaded segment drivers (see Figure 10-2). Segment drivers and Backplane drivers can be cascaded to fit different LCD panel sizes. Most LCD operations involve writing or reading the segment drivers. Driver waveforms for the backplane drivers are periodic and fixed. (See Appendix A & B)

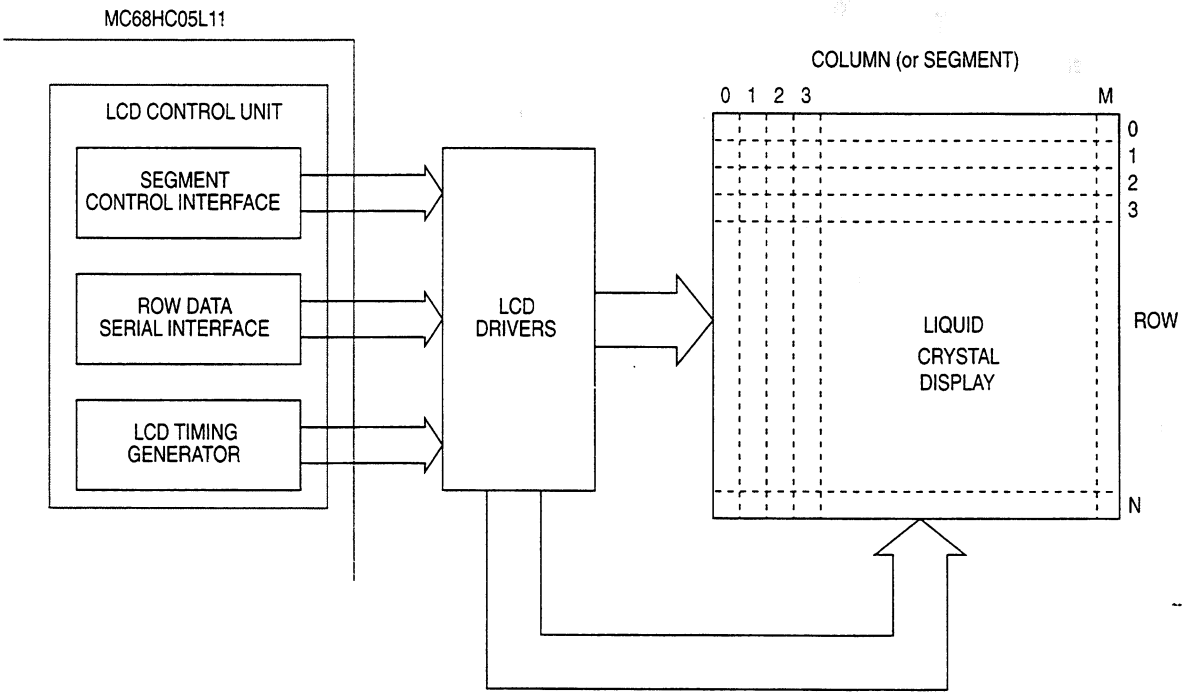


Figure 10-1 Typical LCD system

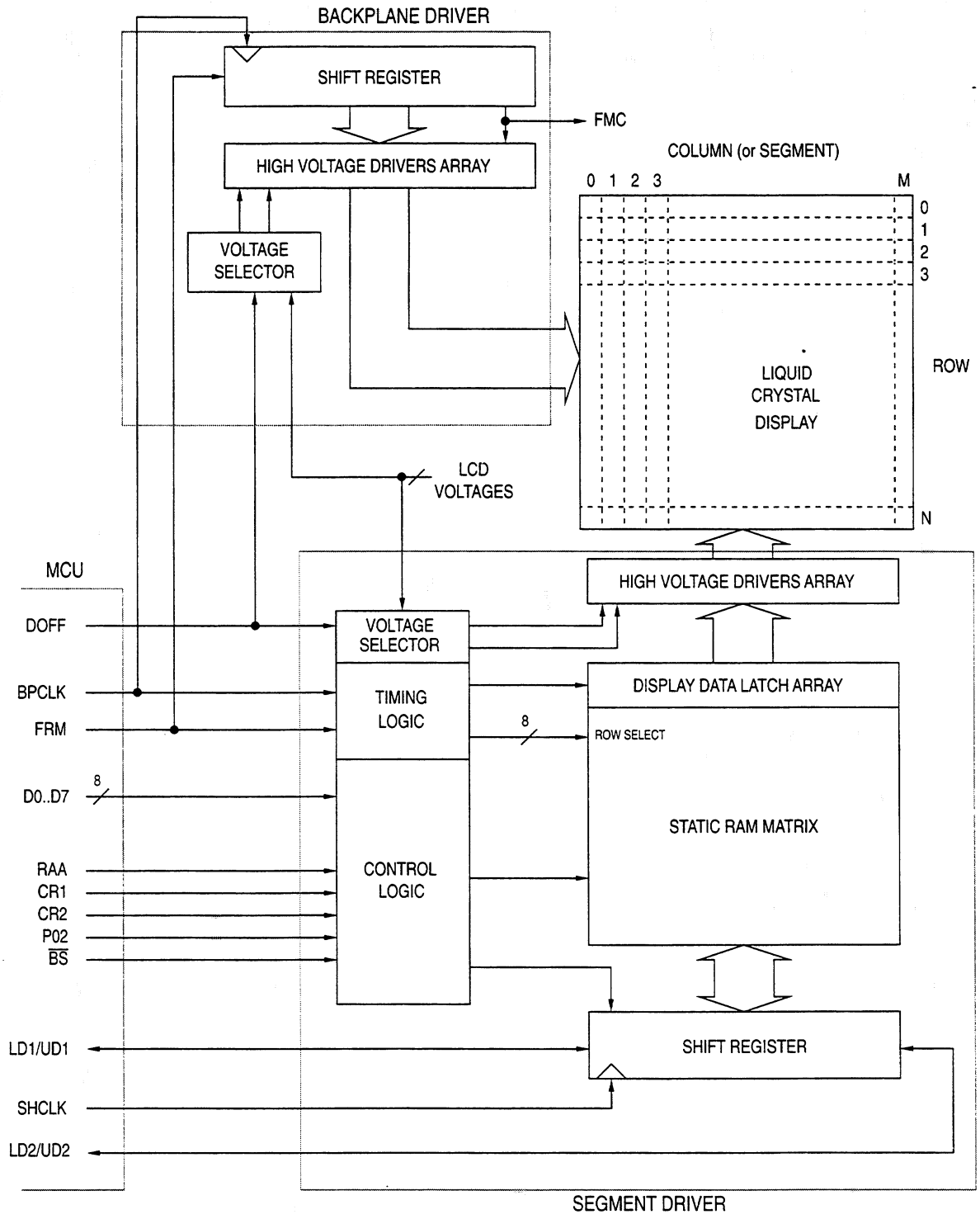


Figure 10-2 Typical LCD System - detailed

10.3 Row Data Serial Interface

This serial interface supports high speed bit rate transfer among LCD drivers and the MC68HC05L11 MCU using a communication protocol similar to SPI (see Section 9 for detailed SPI operation). The MCU and the cascaded segment drivers are connected to form a data ring (see Figure 10-4) and the data in the ring can be configured to flow in either direction. Figure 10-3 is a block diagram of the Row Data Serial Interface. Although the LCD panel can be split into a Lower panel and an Upper panel, the serial data stream may only flow in one data ring at any one time. The only exception is when the upper and lower rings form a new serial loop as described in section 10.5.2., where DPAN, BS1, and BS0 are set to "1"s.

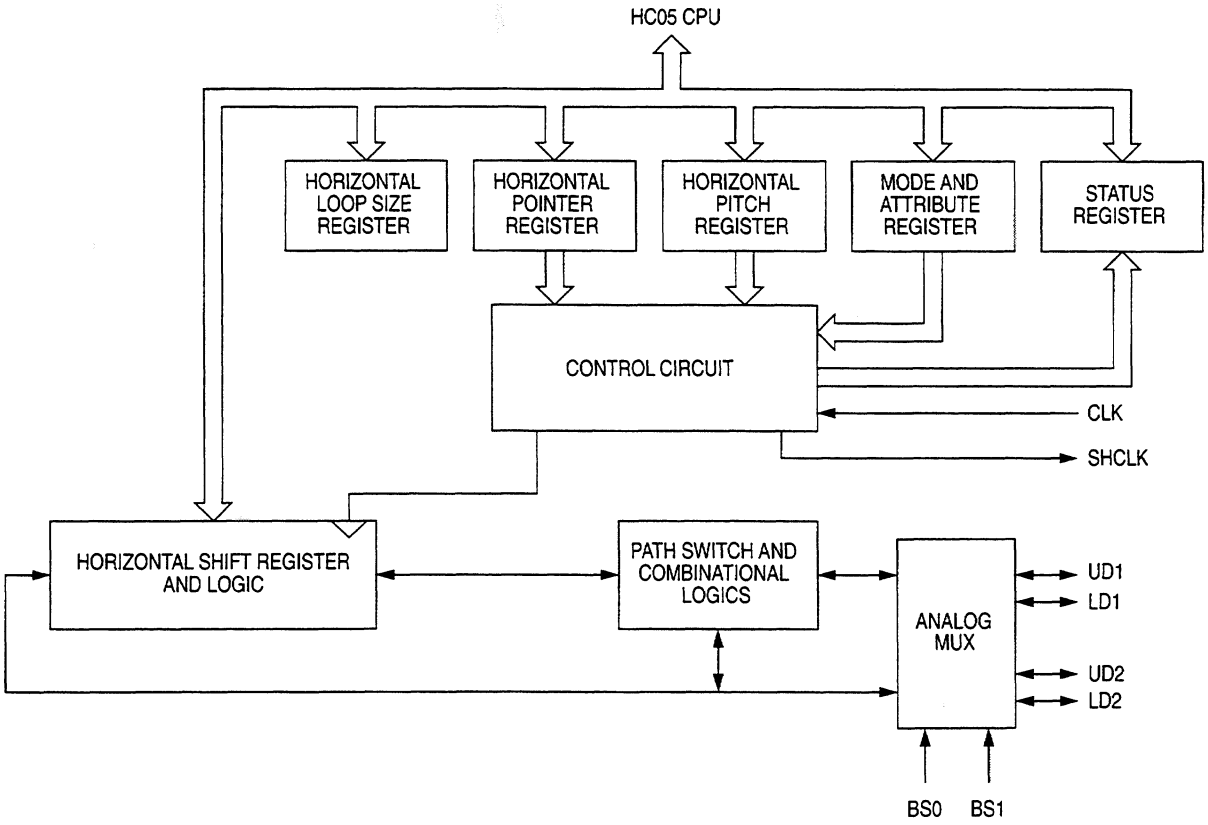


Figure 10-3 Row Data Serial Interface Block Diagram

10

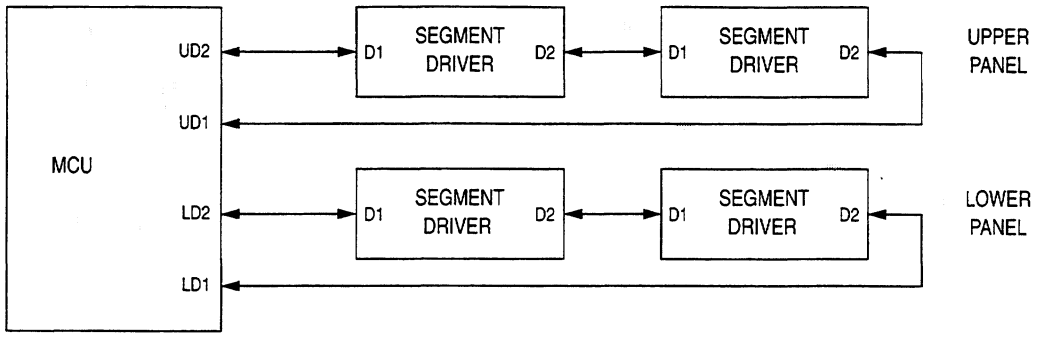


Figure 10-4 Data Ring formed by MCU and Segment Drivers

10.3.1 Horizontal Loop Size Register

This is a 10-bit register which shares the same address location as the Horizontal Shift register, and is selected when the RSW bit of the Mode and Attribute register is set (bit 7 of address $28).

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on Reset
$2E	b7	b6	b5	b4	b3	b2	b1	b0	
$2D							b9	b8	

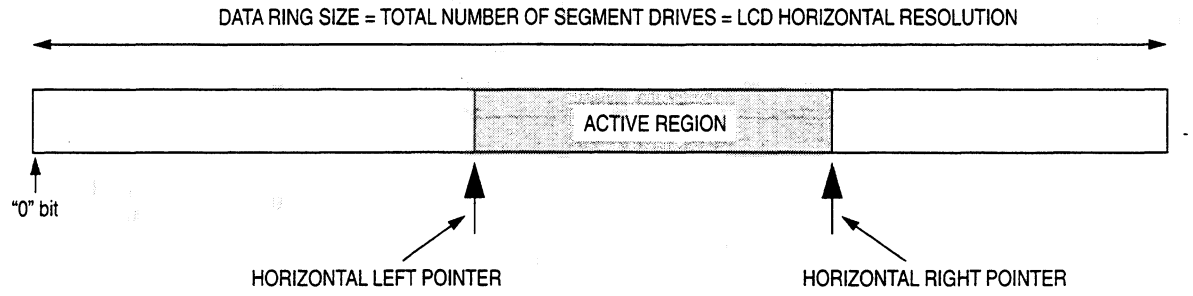
The Horizontal Loop Size register is set once at initialization by the user. Its value should be equal to the number of segment drives (LCD horizontal pixel resolution) minus one. For example, If the LCD horizontal resolution is 320 dots, then the Horizontal Loop Size register should be set to 320-1=319=$13F. A 10-bit counter utilizes this horizontal loop size value to keep track of the position of shifted data in the ring.

10.3.2 Horizontal Pointer Registers

The Horizontal Pointer registers are two 10-bit registers. These registers are used for defining the active data region within a data ring. Data transfers and certain operations, as specified by the Mode & Attribute register, will only be carried out within this active region. These pointer registers should be set to appropriate values at initialization. Below is the definition of the active region where both pointers must be less than or equal to the Horizontal Loop Size register.

$$\text{LEFT POINTER} \leq \text{ACTIVE REGION} \leq \text{RIGHT POINTER}.$$

A graphical representation of the active region is shown in Figure 10-5.



All positions are referenced to the "0" bit, therefore if the LCD horizontal resolution is 320 dots, the Horizontal Loop Size register = 319, and the Left & Right Pointers cannot be greater than 319

Figure 10-5 Definition of Active Region

Horizontal Left Pointer Register

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on Reset
$2A	b7	b6	b5	b4	b3	b2	b1	b0	
$29							b9	b8	

Horizontal Right Pointer Register

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on Reset
$2C	b7	b6	b5	b4	b3	b2	b1	b0	
$2B							b9	b8	

10.3.3 Horizontal Shift Register

This is a 16-bit register which shares the same address location as the Horizontal Loop Size register, and is selected when the RSW bit of the Mode and Attribute register is cleared (bit 7 of address $28).

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on Reset
$2D	High Byte								
$2E	Low Byte								

Ring data in the active region is shifted in and out of this Horizontal Shift register. The CPU can then manipulate the data in this register. The number of bits shifted is set by the Horizontal Pitch register at location $2F. This allows the system to display fonts of different widths from 1 to 16 dots. When not all of the Horizontal Shift register is used, the higher order bits are redundant.

10.3.4 Horizontal Pitch Register

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on Reset
$2F	Current Pitch Count				Horizontal Pitch				

This is an 8-bit register which is divided into two nibbles. The lower nibble contains the number of bits to be shifted between the active region and the Horizontal Shift register. The actual number of bits to be shifted is equal to value of the lower nibble + 1. Therefore, if the value in the Horizontal Pitch register's lower nibble is 6, then the number of shifted bits will be 7.

The Horizontal Pitch nibble is associated with a 4-bit Horizontal Pitch Counter. This counter is loaded with the Horizontal Pitch value and is decremented each time when data bits in the ring are shifted in/out of the active region. As the counter underflows, the CPU will take appropriate action as specified by the Mode & Attribute register. The upper nibble is for read only. It contains the current value of the Horizontal Pitch Counter. With this, users can determine how many bits in the Horizontal Shift register have been transferred to/from the data ring per operation.

10.3.5 Mode & Attribute Register

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on Reset
$28	RSW	MOD	INVB	INVA	S1	S0	OSH	SEQ	

The Mode & Attribute register is used to configure the operation of the Row Data Serial Interface.

MOD - Mode of Operation
OSH - One Shot Operation
SEQ - Sequential Operation

MOD	OSH	SEQ	Operation	Reference
X	0	0	No operation	–
0	0	1	Sequential write operation	Section 10.4.1.1
1	0	1	Sequential read operation	Section 10.4.1.2
0	1	0	One-shot insert operation	Section 10.4.2.1
1	1	0	One-shot replace operation	Section 10.4.2.2

An operation is started once a "1" is written to either OSH or SEQ.

S1, S0 - Special Logical Operations

S1	S0	Operation
0	0	Normal operation as described above
0	1	Content of Horizontal Shift register logically 'OR' with the current ring data
1	0	Content of Horizontal Shift register logically 'AND' with the current ring data
1	1	Content of Horizontal Shift register logically 'XOR' with the current ring data

Notice that the functions described by S1, S0 are designed for using with sequential write and one-shot replace operations; though the usages of these functions with sequential read and one-shot insert operation are not restricted.

INVA - Invert data outside active region

When this bit is set, the ring data outside the active region is inverted.

INVB - Invert data outside active region

When this bit is set, the ring data within the active region is inverted.

10.3.6 LCD Status Register

The LCD Status register occupies the lower nibble of address $30. The higher nibble occupies the Prescaler register (See Section 10.6.1).

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on Reset
$30	PS3	PS2	PS1	PS0	RGST	HPUF	ACT	RDY	

The LCD Status register reports status of the Row Data Serial Interface.

RDY - Ready

1 (set) – Data in data ring has stopped shifting and waiting for command.

0 (clear) – Data in data ring is shifting.

ACT - Active Region

1 (set) – Current bit is within the active region.
i.e. left pointer≤Horizontal Loop Size Counter≤right pointer

0 (clear) – Current bit is outside the active region.

HPUF - Horizontal Pitch Counter Underflow Flag

1 (set) – Underflow has occurred in the Horizontal Pitch Counter.

0 (clear) – Underflow has not occurred in the Horizontal Pitch Counter.

RGST - Ring Start

1 (set) – Row Data Serial Interface is active (LCD R/W operation is active).

0 (clear) – Row Data Serial Interface is idle (LCD R/W operation has completed or inactive).

10.4 Serial Operations

All registers mentioned in the above sections are for Serial Transfer Control. With these, the MCU can initiate four serial operations: two sequential and two one-shot.

10.4.1 Sequential R/W Operations

Figure 10-6 is a flowchart for both the sequential read and write operations. A sequential operation is defined as a shift-and-halt process that the Row Data Serial Interface will carry out within the active region (see Section 10.3.2 for definition of the active region). To make programming easier, the MCU can specify a read sensitive operation (i.e. the sequential read operation) which the Row Data Serial Interface will halt for a MCU's read from the Horizontal Shift register, or a write sensitive operation (i.e. the sequential write operation) which the Interface will halt for a MCU's write to the Horizontal Shift register. Once the Row Data Serial Interface has sensed the completion of the specified MCU's read/write on the Horizontal Shift register, the shifting process resumes. The low byte of the Horizontal Shift register must be accessed in order to complete the register access.

The number of bits shifted in a single shift operation is set by the Horizontal Pitch register. At the start of a shift operation the Horizontal Pitch Counter is loaded with the value set by the Horizontal Pitch register. The Horizontal Pitch Counter is decremented each time when data bits are shifted once in the designated direction. The shifting will halt when the Horizontal Pitch Counter underflows. As a result, the number of bits shifted is equal to the value set in the Horizontal Pitch register. However, there is a case in which the number of bits that have been shifted is not the same as specified in the Horizontal Pitch register. It occurs at the last shifting operation before the active region is exited; i.e. the active region comes to an end before the Horizontal Pitch Counter underflows. Users will find HPUF clear after the operations have completed (RGST is cleared; see Section 10.3.6).

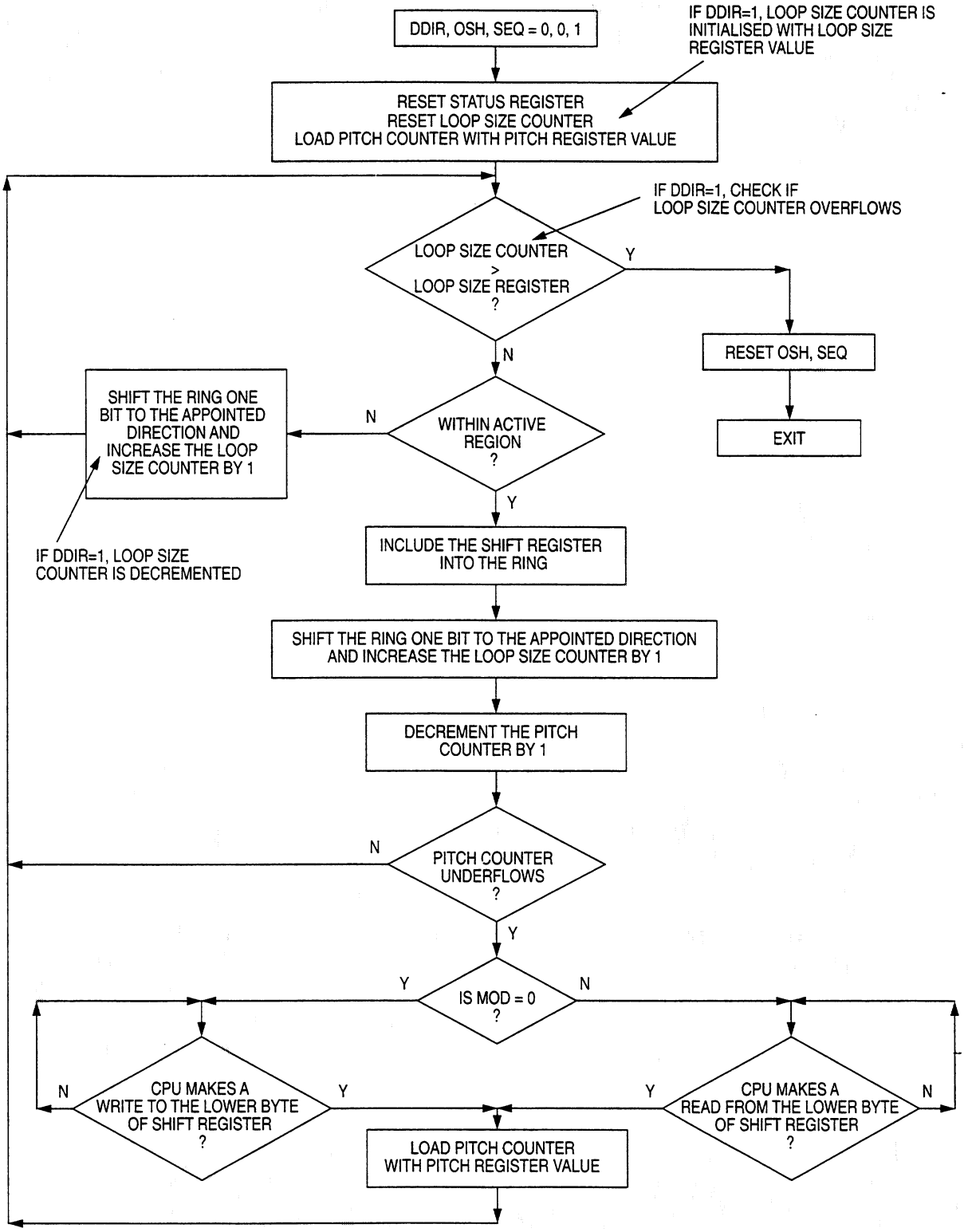


Figure 10-6 Sequential Read/Write Flowchart

10.4.1.1 Write Operation

In a sequential write operation, the data in the Horizontal Shift register is exchanged with the data in the active region.

With the Horizontal Shift register excluded from the data ring, shifting in the ring starts and continues until the first pointer (Left or Right Pointer depending on shifting direction) is encountered (ACT and RDY in the LCD Status register is set). The Horizontal Shift register is then included in the data ring and the first set of data is shifted into the data ring. The data from the active region is shifted into the Horizontal Shift register. The next set of data is then written, and the shift process starts again. This shift and halt process continues until the end of the active region is reached (when the second pointer is encountered). Then, with the Horizontal Shift register excluded from the data ring, shifting continues until the start of the ring is encountered; i.e. an entire display row is realigned. This is detected when the Horizontal Loop Size Counter is greater than the value set in the Horizontal Loop Size register.

If the operated data in the Horizontal Shift register is less than 16-bits; at one end, data enters and exits at the least significant bit of the low byte Horizontal Shift register. At the other end, controlled by the Horizontal Pitch register, data enters and exits the Horizontal Shift register via the 16 to 1 bidirectional multiplexer. In effect, the size of this Horizontal Shift register is programmable. Note that all this is transparent to the user. See Figure 10-7.

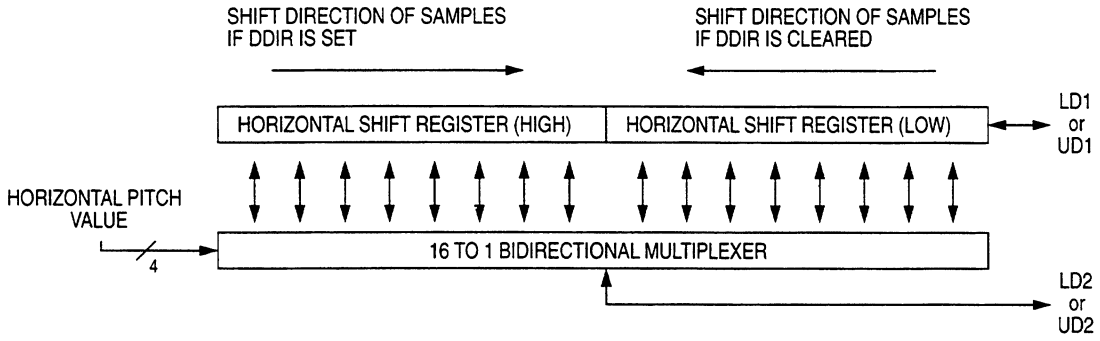


Figure 10-7 Exchange Process in the Horizontal Shift Register

10.4.1.2 Read Operation

In a sequential read operation, the ring data will be sampled and shifted into the Horizontal Shift register, as shown in Figure 10-8. For instance, if the Horizontal Pitch register is $A, only the 3 least significant bits of the Horizontal Shift High register and the whole byte of the Horizontal Shift Low register are involved in the sample-and-shift process.

Note that since the 68HC05 performs a dummy read before write (it is actually a dead cycle to the CPU, therefore, it can only perform an 'unharmful' read). As a result a write made by this processor can initiate shifting though a sequential read operation is selected.

The MCU can use a sequential read to copy a part of screen marked by the Pointers into its system memory. The operation is like a sequential write except the Horizontal Shift register will sample the ring data as soon as the first Pointer is hit by the Loop Size Counter. In this case, the Horizontal Shift register is not part of the data ring. If the operation finishes with HPUF cleared, it means not enough bits have been sampled by the Horizontal Shift register and the second pointer has been reached. The number of sampled bits can be revealed by reading the Horizontal Pitch Counter.

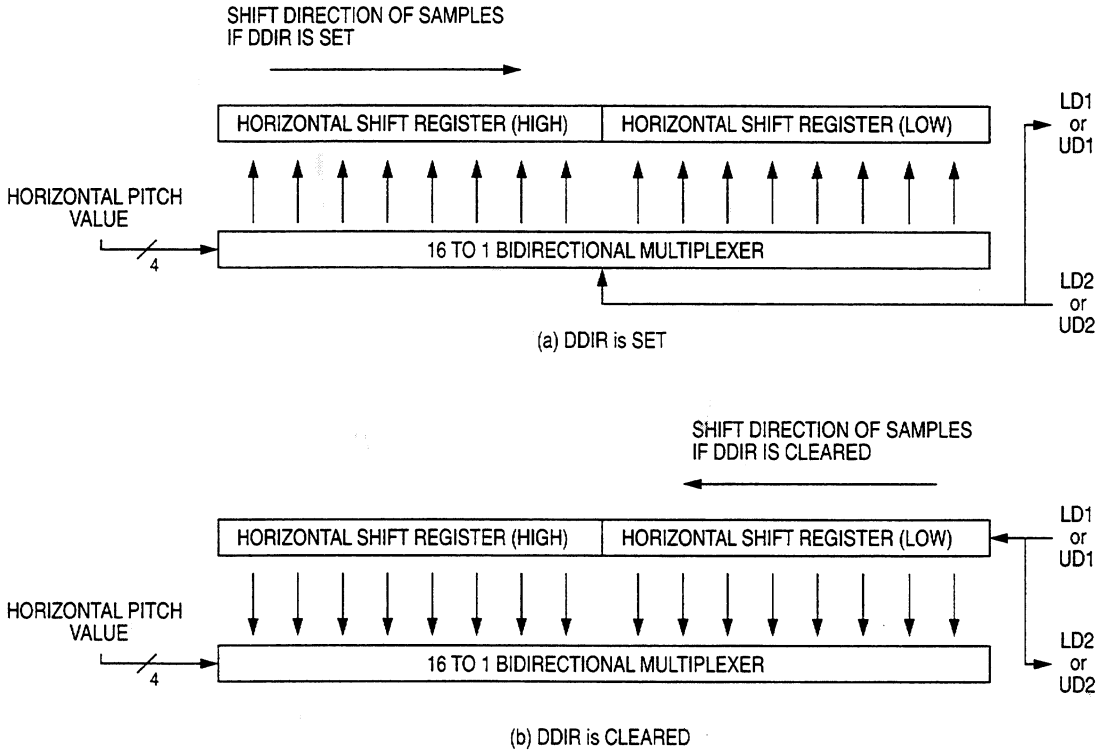


Figure 10-8 Sample and Shift Process in the Horizontal Shift Register

10.4.2 One-Shot Insert And Replace

One-shot operations are similar to the sequential read/write process except the Horizontal Shift register's content is shifted once into the data ring. Figure 10-9 shows the flowchart for both the one-shot replace and insert operations.

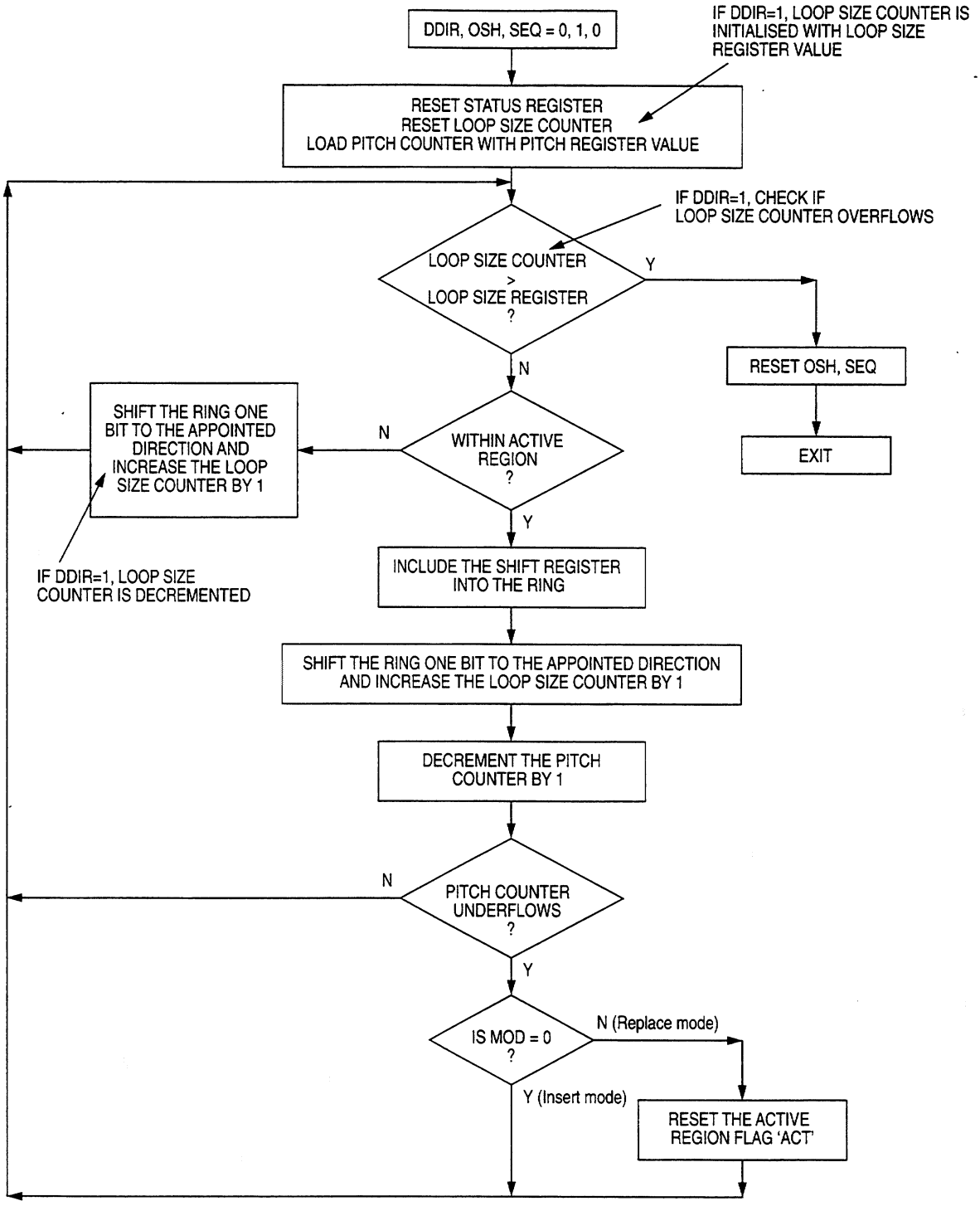


Figure 10-9 One-Shot Insert and Replace Flowchart

10.4.2.1 One-Shot Replace

The one-shot replace is an operation which the Horizontal Shift register is included in the data ring as soon as the first Pointer is hit, and excluded out of the ring as soon as the number of bits specified by the Horizontal Pitch register have been shifted into the data ring. The result is the number of bits as specified by the Horizontal Pitch register in the Horizontal Shift register is exchanged with the same number of bits of data immediately following the first pointer.

Data bits to be inserted or replaced have to be set up before these operations are initiated, i.e. before OSH is set.

10.4.2.2 One-Shot Insert

The one-shot insert is similar to the one-shot replace. The Horizontal Shift register is included in the data as the first pointer is hit, and excluded out of the data ring when the second Pointer is hit by the Loop Size Counter. The effect is that the number of bits as specified by the Horizontal Pitch register in the Horizontal Shift register is inserted at the first Pointer and the same number of bits in front of the second Pointer including the bit pointed by the second Pointer is removed from the data ring and kept in the Horizontal Shift register.

Data bits to be inserted or replaced have to be set up before these operations are initiated, i.e. before OSH is set.

10.4.3 Other Options Of Operation

During a sequential operation and when the Row Data Serial Interface halts for a CPU access, it is allowed to change the Horizontal Pitch register, the Mode and Attribute register and the second pointer.

If, during a sequential operation, the Mode and Attribute register is changed to initiate an one-shot replace process, the Horizontal Shift register is excluded from the data ring immediately and the non-stop shifting is performed until the RGST bit of the Loop Size Counter is clear.

If the SEQ bit is cleared by the MCU during a sequential operation, the operation is aborted at the current position. It is a way to do horizontal scrolling.

10.5 Segment Control Interface

The Segment Control Interface is responsible for controlling various functions of the segment drivers.

10.5.1 Segment Control Register

This is an 8-bit register which shares the same address location as the MUX register, and is selected when the MSW bit of the Control Miscellaneous register is cleared (bit 7 of address $32). It is a multi-function register which either supplies a row address for serial data or controlling the environment of the segment drivers depending on the CR1 and CR2 bits of the Control Miscellaneous register (bits 2 & 1 of address $32). (See Appendix A for Segment Drivers and description of this register).

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on Reset
$31									

10.5.2 Control Miscellaneous Register

This is an 8-bit read/write register which controls various LCD interface functions.

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on Reset
$32	MSW	DPAN	BS1	BS0	DDIR	CR2	CR1	DON	

DON - Display On

1 (set) – LCD on, DOFF pin is low state.

0 (clear) – LCD off, DOFF pin is high state.

This bit also turns off the LCD timing generator, and is affected by the auto-display off feature described in Section 10.7.

CR1, CR2

See Appendix A for definitions.

DDIR - Data Direction

1 (set) – Data enters the MCU from UD2 or LD2 and exits at UD1 or LD1, depending on BS1 & BS0 settings.If both banks are selected, data enters the MCU from UD2, through the internal shift register, and exits at LD1.

0 (clear) – Data enters the MCU from UD1 or LD1 and exits at UD2 or LD2, depending on BS1 & BS0 settings. If both banks are selected, data enters the MCU from LD1, through the internal shift register, and exits at UD2.

DPAN, BS1, BS0

DPAN	BS1	BS0	Segment Banks Selected
0	X	0	No segment bank is selected
0	X	1	Lower panel segment bank is selected
1	0	0	No segment bank is selected
1	0	1	Lower panel segment bank is selected
1	1	0	Upper panel segment bank is selected
1	1	1	Both segment banks are selected and they automatically form a new serial ring by connecting UD1 of the upper segment bank to LD2 of the lower segment bank. Usually this situation is found when display data of the upper panel has to be transferred to/from the lower panel. However, if CPU gives commands as Table 1 in Appendix A listed with all these bits set, both Lower and Upper segment banks will carry out the same action simultaneously.

The levels of output pins $\overline{BS1}$ and $\overline{BS0}$ are the negations of these bits BS1 and BS0 respectively.

10.6 LCD Timing Generator

Figure 10-10 shows a block diagram for the LCD timing generator.

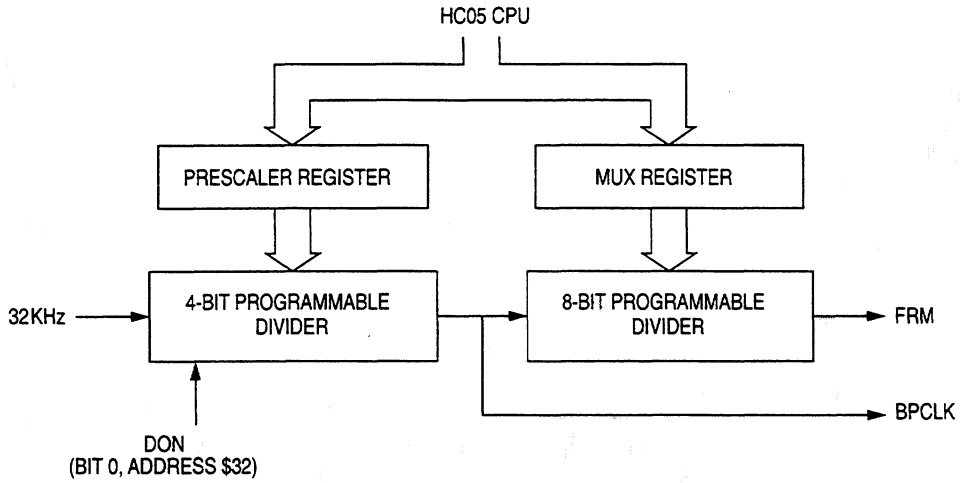


Figure 10-10 Block Diagram of the LCD Timing Generator

The clocks for FRM and BPCLK pins are set by the Prescaler register and the MUX register. They are described in the following sections.

10.6.1 Prescaler Register

The Prescaler register occupies the higher nibble of address $30. The lower nibble is the LCD Status register (See Section 10.3.6). This register is for setting the BPCLK frequency.

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on Reset
$30	PS3	PS2	PS1	PS0	RGST	HPUF	ACT	RDY	

10.6.2 MUX Register

This is an 8-bit register which shares the same address location as the Segment Control register, and is selected when the MSW bit of the Control Miscellaneous register is set (bit 7 of address $32). This register is for setting the LCD multiplex ratio.

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on Reset
$31									

The Prescaler register and MUX register are related to the 32KHz clock by the formula:

$$32768 = FRM \times MUX \times 2 \times PRESCALER$$

Figure 10-11 shows the timing signals for FRM and BPCLK.

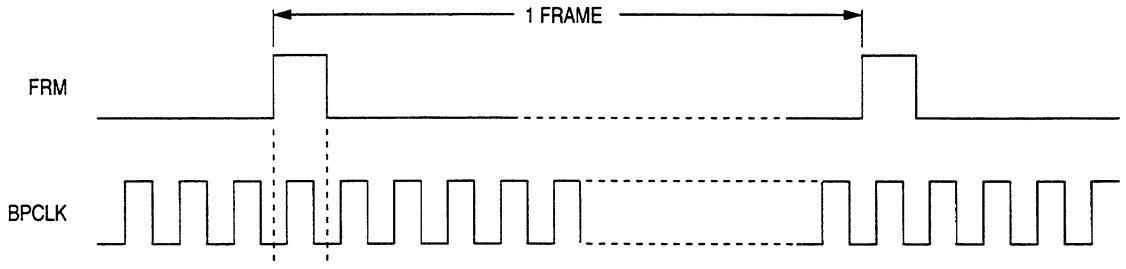


Figure 10-11 Timing of Signals FRM and BPCLK

10.7 Auto-Display Off

General Control Register

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on Reset
$25	TIMI	KEYE	IR1O	IR2O	PORTI	AUTO	OSEN	CLKS	0000 0000

The AUTO bit in the General Control register (bit 2 at address $25) enables the auto display off feature of the LCD control unit. When set, the LCD is turned off after a STOP instruction has been executed and the Count Down register has reached zero. Auto display off will clear the DON bit in the Control Miscellaneous register (bit 0 at address $32).

Below is an example on how it is used.

```
BSET  2,$25 Select auto display off feature.
BSET  0,$32 Turn on LCD.
STOP        Enter stop mode to conserve power.
(LCD will turn off when the count down register reaches zero)
*MCU waked up by interrupt or reset.
BSET  0,$32 LCD is turned off by the auto display off feature, so turns
            it back on.
```

The 4-bit Count Down register at address $20 represents the amount of time (in minute) that has to elapse before the LCD is turned off. This register has a default value of 3 during power-on reset or $\overline{\text{RESET}}$.

Count Down Register

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on Reset
$20	-	-	-	-					---- 0011

11
MEMORY MANAGEMENT UNIT (MMU)

The features introduced below are designed for facilitating external memory access. With the MMU, the MC68HC05L11 can interface with a memory system up to 8M-bytes. Any memory system which is larger than 1M-byte is defined to be a large system and any system below 1M-byte is a small system. The size of the memory system used is configured at power-on reset or $\overline{\text{RESET}}$ by sampling the SL pin. After initialization the SL pin is used as $\overline{\text{CS2}}$ if a small system is configured, or A22 if a large system is defined. Figure 11-1 is a circuitry for SL pin.

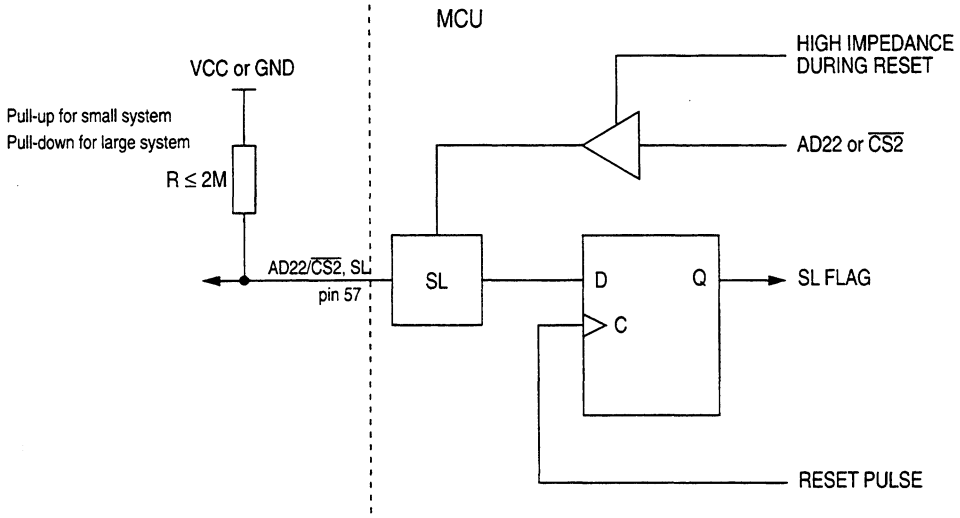


Figure 11-1 Circuitry for SL Pin

For a small system, the MCU provides programmable chip-selects $\overline{\text{CS0}}$, $\overline{\text{CS1}}$ & $\overline{\text{CS2}}$ for address decoding, while in a large system users have to build their own decoding logic as there are too many strategies in memory decoding. Details of the two memory systems are described below.

11.1 Large Memory Systems

Users can choose to use a large system by pulling the SL pin down to ground with a resistor (approx. 2MΩ). In this case, the MMU can be used to expand the 64K-byte CPU logical address space up to 8M-bytes addressable memory. This 8M-bytes of memory can be separated into 2 areas, the common area and the paging area. The common area is default to be the bottom 32K of the memory. The paging area is divided into 1020 8K-banks. The CPU can access the 32K common area and four 8K-banks without altering the contents of the four MMU registers (see Figure 11-2 and the following section). This builds up an one time accessible memory of 64K. The starting address of the first 8K bank is found at $008000, the second bank is 8K above, at $00A000, and so forth. The common area can be expanded in 8K blocks, with the sacrifice of successive paging windows. During power-on reset or $\overline{\text{RESET}}$, these MMU registers will be reset to point at the address of the upper 32K of the memory, i.e. from $8000 to $FFFF.

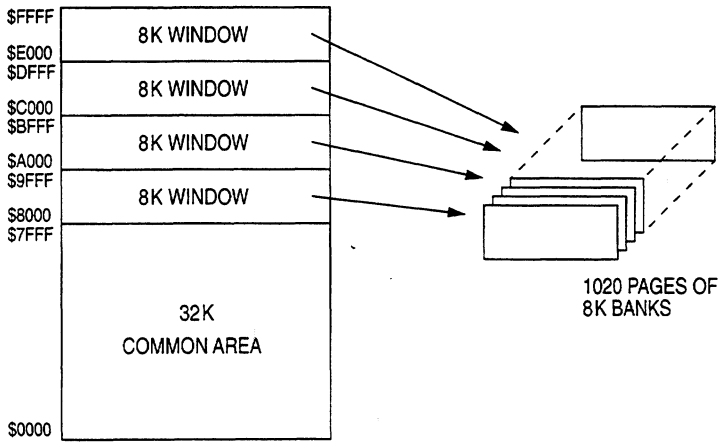


Figure 11-2 Memory Map for a Large Memory System

11

11.1.1 MMU Registers for Large Systems

The four MMU registers are sets of 10-bit registers which serve as page pointers for mapping the different banks of 8k memory. As shown in Figure 11-3, there are 4 MMU registers, named as MMU register A, B, C and D. The contents in these 10-bit registers (register address RA22..RA13) are the contents of MCU's physical address applied to the address output pins AD22..AD13. The register address applied depends on which register is enabled by the decoding logic for the CPU addresses CA15..CA13 (refer to the truth table in Figure 11-3). If the common area is accessed, all MMU registers are disabled and address lines AD22..AD15 are forced to zero; CA14 & CA13 are used as AD14 & AD13; this happens when CA15=0. Beware of the fact that these MMU registers can point to the common area with their content of the upper 8 bits all clear.

OE - OUTPUT ENABLE
F0 - OUTPUT FORCED TO ZERO

CA15	CA14	CA13	OUTPUT ENABLE
0	X	X	DISABLE
1	0	0	A
1	0	1	B
1	1	0	C
1	1	1	D

TRUTH TABLE OF DECODER

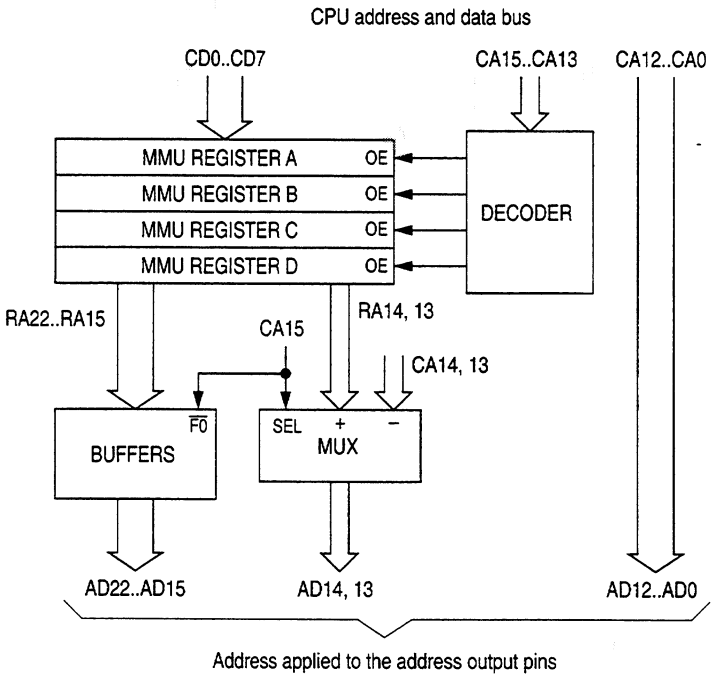


Figure 11-3 Block Diagram of 8M-bytes MMU

The address lines AD20 and AD21 are forced to zeros during Stop or Wait. The address line AD22 is high impedance and it relies on the pull-down resistor to assert a low level on the AD22 pin.

MMU REGISTER A

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
$34	RA20	RA19	RA18	RA17	RA16	RA15	RA14	RA13
$38							RA22	RA21

MMU REGISTER B

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
$35	RA20	RA19	RA18	RA17	RA16	RA15	RA14	RA13
$38					RA22	RA21		

MMU REGISTER C

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
$36	RA20	RA19	RA18	RA17	RA16	RA15	RA14	RA13
$38			RA22	RA21				

MMU REGISTER D

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
$37	RA20	RA19	RA18	RA17	RA16	RA15	RA14	RA13
$38	RA22	RA21						

11.2 External Memory Chip-Select ($\overline{RCS}$)

Whether a large or a small system is configured, there is one programmable chip-select pin which is dedicated for accessing external memory e.g. static RAM. Figure 11-4 shows the block diagram for this chip select. $\overline{RCS}$ is selected only if content of address AD19-AD12 falls in the range bounded by the $\overline{RCS}$'s higher & lower boundary register, and AD20, AD21 & AD22 are zeros. These boundaries allow an external device between 1M-bytes and 4K-bytes to be addressed. During power-on reset or $\overline{RESET}$, the Lower Boundary register is set to one and the Higher Boundary register is cleared to zero. As a result $\overline{RCS}$ is inactive upon reset. $\overline{RCS}$ is also inactive during MCU's Stop & Wait modes, or when accessing internal addresses.

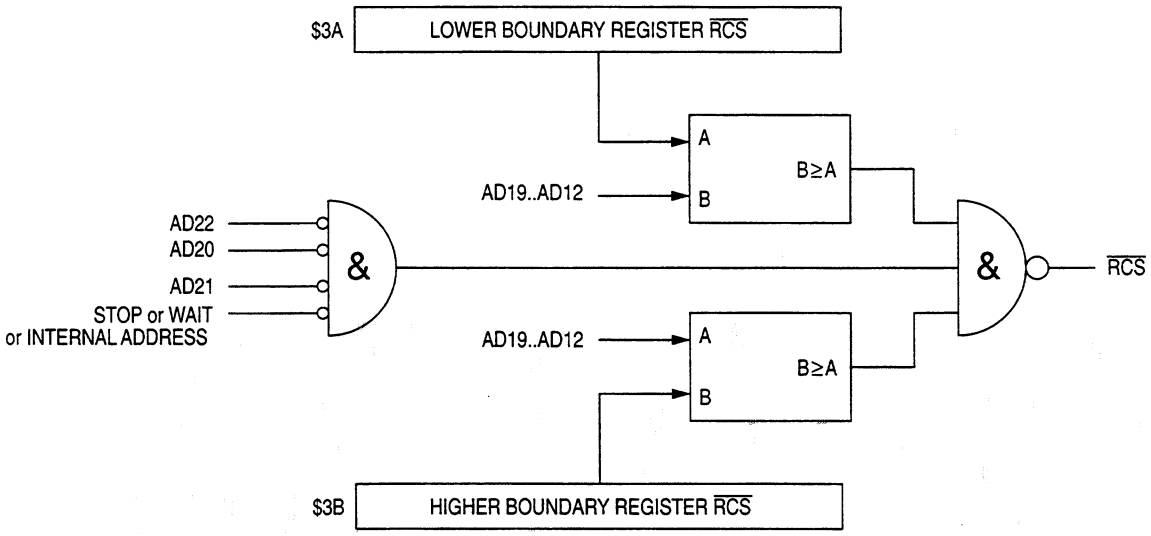


Figure 11-4 Block Diagram of the Decoding Logic for $\overline{RCS}$

11.3 Small Memory Systems

A small memory system is configured with the SL pin pulled to V_{CC} with a resistor (approx. 2MΩ). In this configuration the MMU is used to expand the 64K-byte CPU logical address space up to

1 M-bytes.Similar to the large memory system configuration, the small system's memory is divided into a 32K common area and a paging area. In this case, the paging area consists of 120 pages of 8K banks, with the page pointers set at the MMU registers A, B, C, & D. For a small memory system, the top three MMU register bits are used; since AD22, AD21, & AD20 are used for chip-selects $\overline{CS2}$, $\overline{CS1}$, & $\overline{CS0}$ respectively. AD22, AD21, & AD20 are internally forced to zeros. Address $38 is used as a Chip-Select Control register. See following section.

11.3.1 Chip Selects for Small Systems

If a small system is configured, AD22, AD21, & AD20 are used as chip select lines $\overline{CS2}$, $\overline{CS1}$, & $\overline{CS0}$ respectively; while the address lines AD19 to AD0 are carried straight out from the MMU. This allows a maximum memory access of 1M-bytes. $\overline{CS0}$ is reserved for the common area; it is enabled after a power-on reset or $\overline{RESET}$. Figure 11-5 shows a block diagram for $\overline{CS0}$ decoding logic.

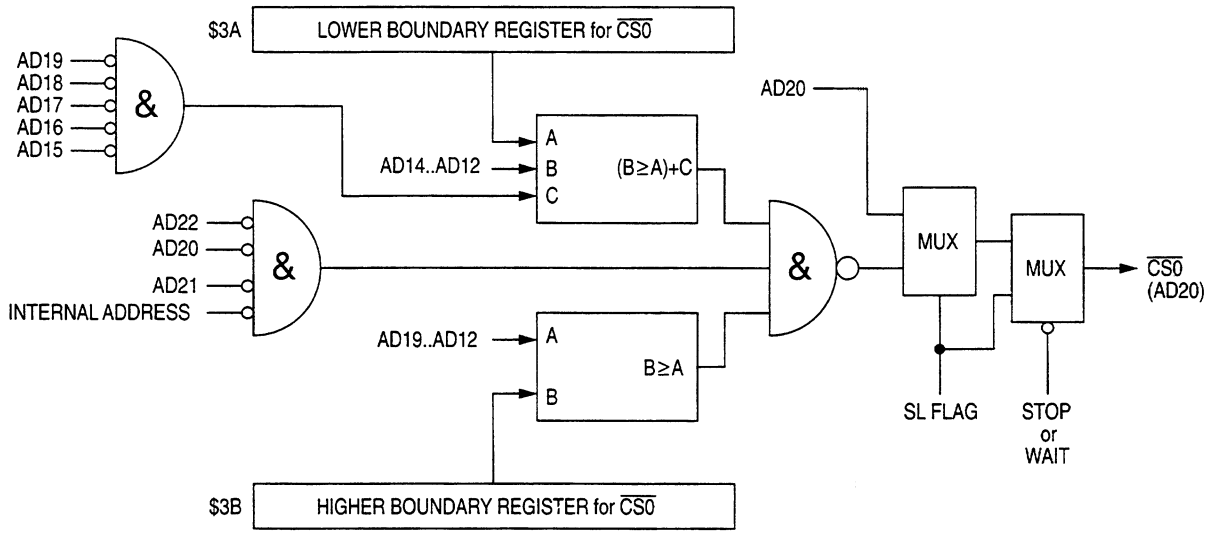


Figure 11-5 Decoding Logic for $\overline{CS0}$

Decoding logic for $\overline{CS1}$ (Figure 11-6) is similar to $\overline{CS0}$; the first output multiplexer responds to the SL Flag from the SL pin and determines whether that output should be a chip-select or an address line. The second output multiplexer determines the state for that output pin during the Stop or Wait.

For $\overline{CS2}$, the second multiplexer is a tri-state driver (Figure 11-7). It turns $\overline{CS2}$ (AD22) to high impedance during the Stop or Wait.

Like $\overline{RCS}$, there are pairs of boundary registers for $\overline{CS0}$, $\overline{CS1}$ and $\overline{CS2}$. These registers are multiplexed to share the same address location $39. The CPU can access these registers

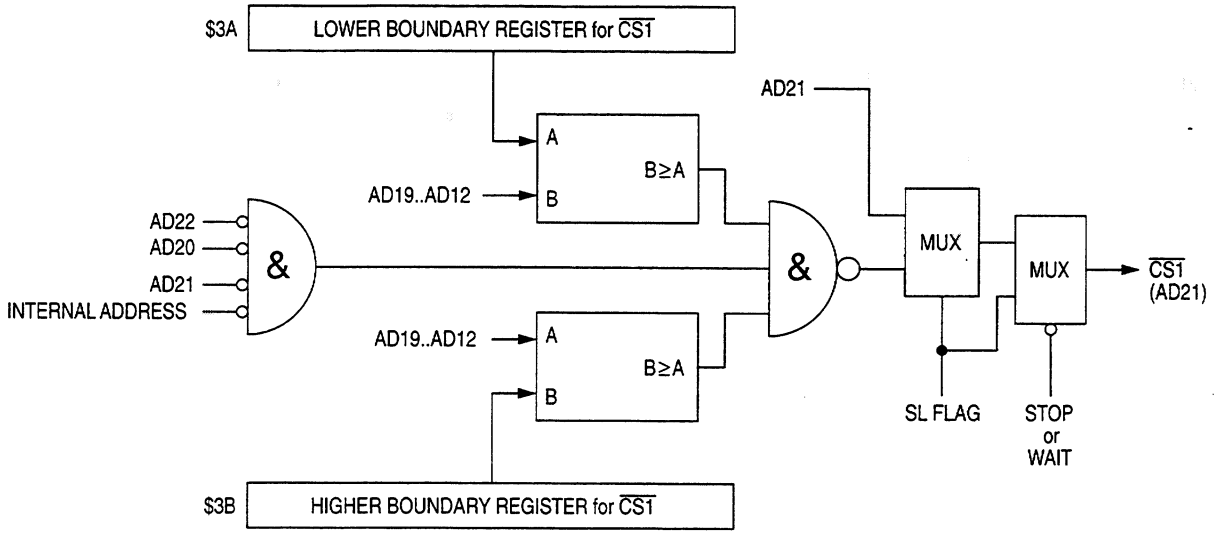


Figure 11-6 Decoding Logic for $\overline{CS1}$

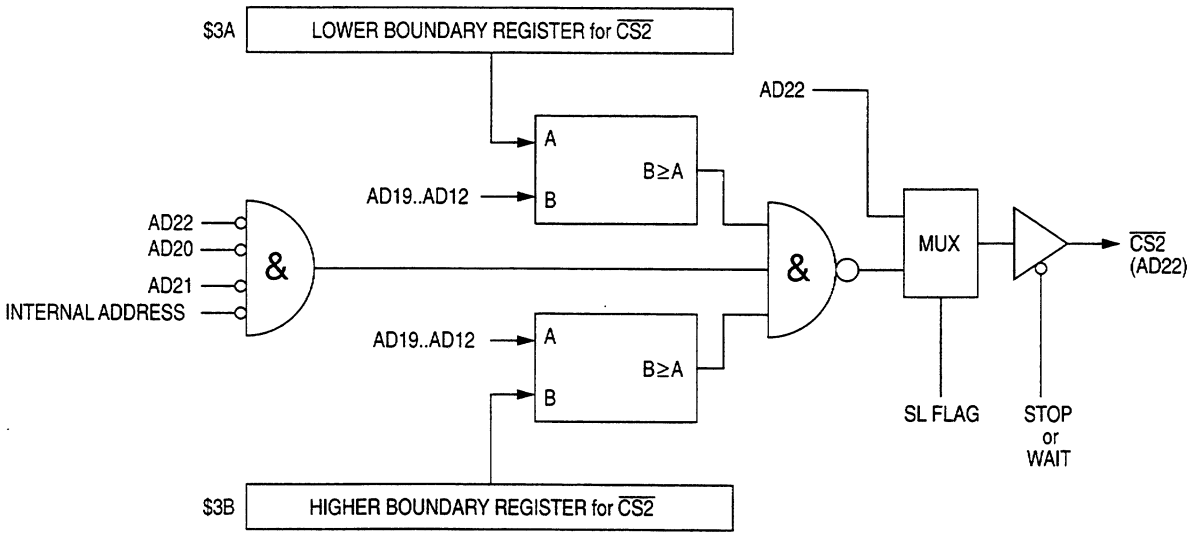


Figure 11-7 Decoding Logic for $\overline{CS2}$

individually through the Chip Select Control register at address $38. See Table 11-1 for Boundary register selection.

Since $\overline{CS0}$ is connected to the default start-up memory device, its Lower Boundary register has to be in the bottom 32K of memory. Therefore only the lower 3 bits from the Data Bus is regarded as valid data when the CPU writes to this register. During any power-on reset or $\overline{RESET}$, the Lower

Table 11-1 Multiplexing Relationship Among Boundary Registers

CONTROL REGISTER $38			CHIP SELECTS BOUNDARY REGISTER $39 BECOMES
bit2	bit1	bit0	
0	0	0	LOWER BOUNDARY REGISTER for $\overline{CS0}$
0	0	1	HIGHER BOUNDARY REGISTER for $\overline{CS0}$
0	1	0	LOWER BOUNDARY REGISTER for $\overline{CS1}$
0	1	1	HIGHER BOUNDARY REGISTER for $\overline{CS1}$
1	0	0	LOWER BOUNDARY REGISTER for $\overline{CS2}$
1	0	1	HIGHER BOUNDARY REGISTER for $\overline{CS2}$

Boundary register for $\overline{CS0}$ and the Higher Boundary register for others are reset to zeros; the Higher Boundary register for $\overline{CS0}$ is set to $7 and the Lower Boundary for others are set to $FF. Therefore, only $\overline{CS0}$ is active upon power-on reset or $\overline{RESET}$. After power-on or $\overline{RESET}$, the Higher Boundary for $\overline{CS0}$ can be programmed to address locations as high as 1 M-byte. However, its Lower Boundary is restricted to land on the common area. $\overline{CS0}$ and $\overline{CS1}$ are forced high during any MCU's Stop or Wait, and during accessing internal addresses. $\overline{CS2}$ is forced high impedance as soon as the MCU goes into Stop or Wait. $\overline{CS2}$ relies on the external pull-up resistor for the high level logic.

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12
CPU CORE AND INSTRUCTION SET

This section provides a description of the CPU core registers, the instruction set and the addressing modes of the MC68HC05L11.

12.1 Registers

The MCU contains five registers, as shown in the programming model of Figure 12-1. The interrupt stacking order is shown in Figure 4-2.

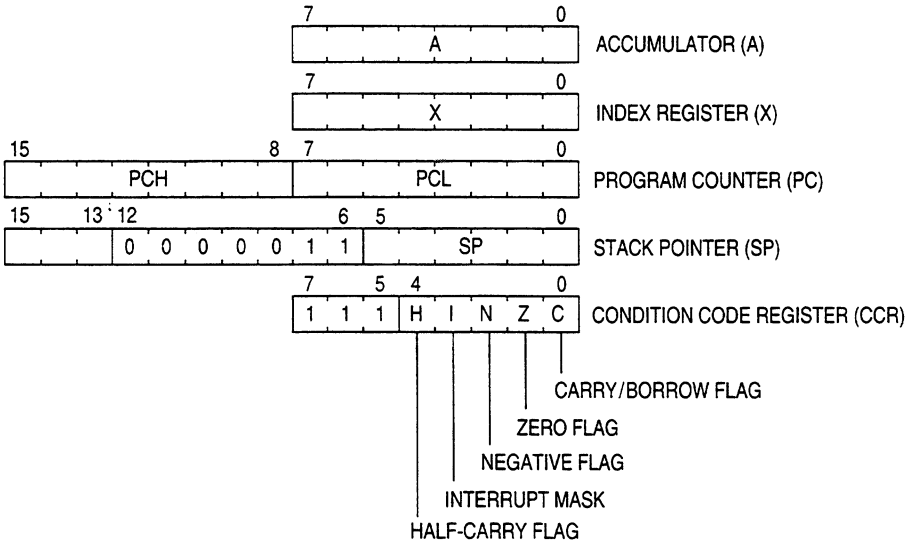


Figure 12-1 Programming Model

12.1.1 Accumulator (A)

The accumulator is a general purpose 8-bit register used to hold operands and results of arithmetic calculations or data manipulations.

12.1.2 Index register (X)

The index register is an 8-bit register, which can contain the indexed addressing value used to create an effective address. The index register may also be used as a temporary storage area.

12.1.3 Program counter (PC)

The program counter is a 16-bit register, which contains the address of the next byte to be fetched.

12.1.4 Stack pointer (SP)

The stack pointer is a 16-bit register, which contains the address of the next free location on the stack. During an MCU reset or the reset stack pointer (RSP) instruction, the stack pointer is set to location $00FF. The stack pointer is then decremented as data is pushed onto the stack and incremented as data is pulled from the stack.

When accessing memory, the ten most significant bits are permanently set to 0000000011. These ten bits are appended to the six least significant register bits to produce an address within the range of $00C0 to $00FF. Subroutines and interrupts may use up to 64 (decimal) locations. If 64 locations are exceeded, the stack pointer wraps around and overwrites the previously stored information. A subroutine call occupies two locations on the stack; an interrupt uses five locations.

12.1.5 Condition code register (CCR)

The CCR is a 5-bit register in which four bits are used to indicate the results of the instruction just executed, and the fifth bit indicates whether interrupts are masked. These bits can be individually tested by a program, and specific actions can be taken as a result of their state. Each bit is explained in the following paragraphs.

Half carry (H)

This bit is set during ADD and ADC operations to indicate that a carry occurred between bits 3 and 4.

Interrupt (I)

When this bit is set, all maskable interrupts are masked. If an interrupt occurs while this bit is set, the interrupt is latched and remains pending until the interrupt bit is cleared.

Negative (N)

When set, this bit indicates that the result of the last arithmetic, logical, or data manipulation was negative.

Zero (Z)

When set, this bit indicates that the result of the last arithmetic, logical, or data manipulation was zero.

Carry/borrow (C)

When set, this bit indicates that a carry or borrow out of the arithmetic logical unit (ALU) occurred during the last arithmetic operation. This bit is also affected during bit test and branch instructions and during shifts and rotates.

12.2 Instruction set

The MCU has a set of 62 basic instructions. They can be grouped into five different types as follows:

- Register/memory
- Read/modify/write
- Branch
- Bit manipulation
- Control

The following paragraphs briefly explain each type. All the instructions within a given type are presented in individual tables.

This MCU uses all the instructions available in the M146805 CMOS family plus one more: the unsigned multiply (MUL) instruction. This instruction allows unsigned multiplication of the contents of the accumulator (A) and the index register (X). The high-order product is then stored in the index register and the low-order product is stored in the accumulator. A detailed definition of the MUL instruction is shown in Table 12-1.

12.2.1 Register/memory Instructions

Most of these instructions use two operands. The first operand is either the accumulator or the index register. The second operand is obtained from memory using one of the addressing modes. The jump unconditional (JMP) and jump to subroutine (JSR) instructions have no register operand. Refer to Table 12-2 for a complete list of register/memory instructions.

12.2.2 Branch instructions

These instructions cause the program to branch if a particular condition is met; otherwise, no operation is performed. Branch instructions are two-byte instructions. Refer to Table 12-3.

12.2.3 Bit manipulation instructions

The MCU can set or clear any writable bit that resides in the first 256 bytes of the memory space (page 0). All port data and data direction registers, timer and serial interface registers, control/status registers and a portion of the on-chip RAM reside in page 0. An additional feature allows the software to test and branch on the state of any bit within these locations. The bit set, bit clear, bit test and branch functions are all implemented with single instructions. For the test and branch instructions, the value of the bit tested is also placed in the carry bit of the condition code register. Refer to Table 12-4.

12.2.4 Read/modify/write instructions

These instructions read a memory location or a register, modify or test its contents, and write the modified value back to memory or to the register. The test for negative or zero (TST) instruction is an exception to this sequence of reading, modifying and writing, since it does not modify the value. Refer to Table 12-5 for a complete list of read/modify/write instructions.

12.2.5 Control instructions

These instructions are register reference instructions and are used to control processor operation during program execution. Refer to Table 12-6 for a complete list of control instructions.

12.2.6 Tables

Tables for all the instruction types listed above follow. In addition there is a complete alphabetical listing of all the instructions (see Table 12-7), and an opcode map for the instruction set of the M68HC05 MCU family (see Table 12-8).

Table 12-1 MUL instruction

Operation	X:A ← X*A			
Description	Multiplies the eight bits in the index register by the eight bits in the accumulator and places the 16-bit result in the concatenated accumulator and index register.			
Condition codes	H : Cleared I : Not affected N : Not affected Z : Not affected C : Cleared			
Source	MUL			
Form	Addressing mode Inherent	Cycles 11	Bytes 1	Opcode $42

Table 12-2 Register/memory instructions

		Addressing modes																	
		Immediate			Direct			Extended			Indexed (no offset)			Indexed (8-bit offset)			Indexed (16-bit offset)		
Function	**Mnemonic**	**Opcode**	**# Bytes**	**# Cycles**	**Opcode**	**# Bytes**	**# Cycles**	**Opcode**	**# Bytes**	**# Cycles**	**Opcode**	**# Bytes**	**# Cycles**	**Opcode**	**# Bytes**	**# Cycles**	**Opcode**	**# Bytes**	**# Cycles**
Load A from memory	LDA	A6	2	2	B6	2	3	C6	3	4	F6	1	3	E6	2	4	D6	3	5
Load X from memory	LDX	AE	2	2	BE	2	3	CE	3	4	FE	1	3	EE	2	4	DE	3	5
Store A in memory	STA				B7	2	4	C7	3	5	F7	1	4	E7	2	5	D7	3	6
Store X in memory	STX				BF	2	4	CF	3	5	FF	1	4	EF	2	5	DF	3	6
Add memory to A	ADD	AB	2	2	BB	2	3	CB	3	4	FB	1	3	EB	2	4	DB	3	5
Add memory and carry to A	ADC	A9	2	2	B9	2	3	C9	3	4	F9	1	3	E9	2	4	D9	3	5
Subtract memory	SUB	A0	2	2	B0	2	3	C0	3	4	F0	1	3	E0	2	4	D0	3	5
Subtract memory from A with borrow	SBC	A2	2	2	B2	2	3	C2	3	4	F2	1	3	E2	2	4	D2	3	5
AND memory with A	AND	A4	2	2	B4	2	3	C4	3	4	F4	1	3	E4	2	4	D4	3	5
OR memory with A	ORA	AA	2	2	BA	2	3	CA	3	4	FA	1	3	EA	2	4	DA	3	5
Exclusive OR memory with A	EOR	A8	2	2	B8	2	3	C8	3	4	F8	1	3	E8	2	4	D8	3	5
Arithmetic compare A with memory	CMP	A1	2	2	B1	2	3	C1	3	4	F1	1	3	E1	2	4	D1	3	5
Arithmetic compare X with memory	CPX	A3	2	2	B3	2	3	C3	3	4	F3	1	3	E3	2	4	D3	3	5
Bit test memory with A (logical compare)	BIT	A5	2	2	B5	2	3	C5	3	4	F5	1	3	E5	2	4	D5	3	5
Jump unconditional	JMP				BC	2	2	CC	3	3	FC	1	2	EC	2	3	DC	3	4
Jump to subroutine	JSR				BD	2	5	CD	3	6	FD	1	5	ED	2	6	DD	3	7

Table 12-3 Branch instructions

		Relative addressing mode		
Function	**Mnemonic**	**Opcode**	**# Bytes**	**# Cycles**
Branch always	BRA	20	2	3
Branch never	BRN	21	2	3
Branch if higher	BHI	22	2	3
Branch if lower or same	BLS	23	2	3
Branch if carry clear	BCC	24	2	3
(Branch if higher or same)	(BHS)	24	2	3
Branch if carry set	BCS	25	2	3
(Branch if lower)	(BLO)	25	2	3
Branch if not equal	BNE	26	2	3
Branch if equal	BEQ	27	2	3
Branch if half carry clear	BHCC	28	2	3
Branch if half carry set	BHCS	29	2	3
Branch if plus	BPL	2A	2	3
Branch if minus	BMI	2B	2	3
Branch if interrupt mask bit is clear	BMC	2C	2	3
Branch if interrupt mask bit is set	BMS	2D	2	3
Branch if interrupt line is low	BIL	2E	2	3
Branch if interrupt line is high	BIH	2F	2	3
Branch to subroutine	BSR	AD	2	6

Table 12-4 Bit manipulation instructions

		Addressing modes					
		Bit set/clear			Bit test and branch		
Function	**Mnemonic**	**Opcode**	**# Bytes**	**# Cycles**	**Opcode**	**# Bytes**	**# Cycles**
Branch if bit n is set	BRSET n (n=0–7)				2•n	3	5
Branch if bit n is clear	BRCLR n (n=0–7)				01+2•n	3	5
Set bit n	BSET n (n=0–7)	10+2•n	2	5			
Clear bit n	BCLR n (n=0–7)	11+2•n	2	5			

12

Table 12-5 Read/modify/write instructions

		Addressing modes														
		Inherent (A)			Inherent (X)			Direct			Indexed (no offset)			Indexed (8-bit offset)		
Function	Mnemonic	Opcode	# Bytes	# Cycles	Opcode	# Bytes	# Cycles	Opcode	# Bytes	# Cycles	Opcode	# Bytes	# Cycles	Opcode	# Bytes	# Cycles
Increment	INC	4C	1	3	5C	1	3	3C	2	5	7C	1	5	6C	2	6
Decrement	DEC	4A	1	3	5A	1	3	3A	2	5	7A	1	5	6A	2	6
Clear	CLR	4F	1	3	5F	1	3	3F	2	5	7F	1	5	6F	2	6
Complement	COM	43	1	3	53	1	3	33	2	5	73	1	5	63	2	6
Negate (two's complement)	NEG	40	1	3	50	1	3	30	2	5	70	1	5	60	2	6
Rotate left through carry	ROL	49	1	3	59	1	3	39	2	5	79	1	5	69	2	6
Rotate right through carry	ROR	46	1	3	56	1	3	36	2	5	76	1	5	66	2	6
Logical shift left	LSL	48	1	3	58	1	3	38	2	5	78	1	5	68	2	6
Logical shift right	LSR	44	1	3	54	1	3	34	2	5	74	1	5	64	2	6
Arithmetic shift right	ASR	47	1	3	57	1	3	37	2	5	77	1	5	67	2	6
Test for negative or zero	TST	4D	1	3	5D	1	3	3D	2	4	7D	1	4	6D	2	5
Multiply	MUL	42	1	11												

Table 12-6 Control instructions

		Inherent addressing mode		
Function	Mnemonic	Opcode	# Bytes	# Cycles
Transfer A to X	TAX	97	1	2
Transfer X to A	TXA	9F	1	2
Set carry bit	SEC	99	1	2
Clear carry bit	CLC	98	1	2
Set interrupt mask bit	SEI	9B	1	2
Clear interrupt mask bit	CLI	9A	1	2
Software interrupt	SWI	83	1	10
Return from subroutine	RTS	81	1	6
Return from interrupt	RTI	80	1	9
Reset stack pointer	RSP	9C	1	2
No-operation	NOP	9D	1	2
Stop	STOP	8E	1	2
Wait	WAIT	8F	1	2

Table 12-7 Instruction set

Mnemonic	Addressing modes										Condition codes				
	INH	IMM	DIR	EXT	REL	IX	IX1	IX2	BSC	BTB	H	I	N	Z	C
ADC											◊	•	◊	◊	◊
ADD											◊	•	◊	◊	◊
AND											•	•	◊	◊	•
ASL											•	•	◊	◊	◊
ASR											•	•	◊	◊	◊
BCC											•	•	•	•	•
BCLR											•	•	•	•	•
BCS											•	•	•	•	•
BEQ											•	•	•	•	•
BHCC											•	•	•	•	•
BHCS											•	•	•	•	•
BHI											•	•	•	•	•
BHS											•	•	•	•	•
BIH											•	•	•	•	•
BIL											•	•	•	•	•
BIT											•	•	◊	◊	•
BLO											•	•	•	•	•
BLS											•	•	•	•	•
BMC											•	•	•	•	•
BMI											•	•	•	•	•
BMS											•	•	•	•	•
BNE											•	•	•	•	•
BPL											•	•	•	•	•
BRA											•	•	•	•	•
BRN											•	•	•	•	•
BRCLR											•	•	•	•	◊
BRSET											•	•	•	•	◊
BSET											•	•	•	•	•
BSR											•	•	•	•	•
CLC											•	•	•	•	0
CLI											•	0	•	•	•
CLR											•	•	0	1	•
CMP											•	•	◊	◊	◊

Address mode abbreviations

BSC	Bit set/clear	IMM	Immediate
BTB	Bit test & branch	IX	Indexed (no offset)
DIR	Direct	IX1	Indexed, 1 byte offset
EXT	Extended	IX2	Indexed, 2 byte offset
INH	Inherent	REL	Relative

Not implemented

Condition code symbols

H	Half carry (from bit 3)	◊	Tested and set if true, cleared otherwise
I	Interrupt mask	•	Not affected
N	Negate (sign bit)	?	Load CCR from stack
Z	Zero	0	Cleared
C	Carry/borrow	1	Set

Table 12-7 Instruction set (Continued)

Mnemonic	Addressing modes										Condition codes				
	INH	IMM	DIR	EXT	REL	IX	IX1	IX2	BSC	BTB	H	I	N	Z	C
COM											•	•	◊	◊	1
CPX											•	•	◊	◊	◊
DEC											•	•	◊	◊	•
EOR											•	•	◊	◊	•
INC											•	•	◊	◊	•
JMP											•	•	•	•	•
JSR											•	•	•	•	•
LDA											•	•	◊	◊	•
LDX											•	•	◊	◊	•
LSL											•	•	◊	◊	◊
LSR											•	•	0	◊	◊
MUL											0	•	•	•	0
NEG											•	•	◊	◊	◊
NOP											•	•	•	•	•
ORA											•	•	◊	◊	•
ROL											•	•	◊	◊	◊
ROR											•	•	◊	◊	◊
RSP											•	•	•	•	•
RTI											?	?	?	?	?
RTS											•	•	•	•	•
SBC											•	•	◊	◊	◊
SEC											•	•	•	•	1
SEI											•	1	•	•	•
STA											•	•	◊	◊	•
STOP											•	0	•	•	•
STX											•	•	◊	◊	•
SUB											•	•	◊	◊	◊
SWI											•	1	•	•	•
TAX											•	•	•	•	•
TST											•	•	◊	◊	•
TXA											•	•	•	•	•
WAIT											•	0	•	•	•

Address mode abbreviations

BSC	Bit set/clear	IMM	Immediate
BTB	Bit test & branch	IX	Indexed (no offset)
DIR	Direct	IX1	Indexed, 1 byte offset
EXT	Extended	IX2	Indexed, 2 byte offset
INH	Inherent	REL	Relative

Not implemented

Condition code symbols

H	Half carry (from bit 3)	◊	Tested and set if true, cleared otherwise
I	Interrupt mask	•	Not affected
N	Negate (sign bit)	?	Load CCR from stack
Z	Zero	0	Cleared
C	Carry/borrow	1	Set

Table 12-8 M68HC05 opcode map

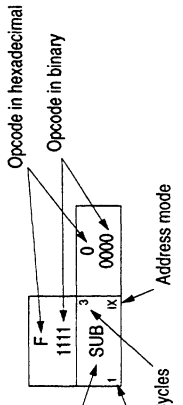
	Bit manipulation		Branch	Read/modify/write					Control		Register/memory						
	BTB	BSC	REL	DIR	INH	INH	IX1	IX	INH	INH	IMM	DIR	EXT	IX2	IX1	IX	High / Low
	0 0000	1 0001	2 0010	3 0011	4 0100	5 0101	6 0110	7 0111	8 1000	9 1001	A 1010	B 1011	C 1100	D 1101	E 1110	F 1111	
0 0000	BRSET0 3 BTB 2	BSET0 5 BSC 2	BRA 3 REL 2	NEG 5 DIR 1	NEGA 3 INH 1	NEGX 3 INH 1	NEG 6 IX1 1	NEG 5 IX 1	RTI 9 INH 1		SUB 2 IMM 2	SUB 3 DIR 3	SUB 4 EXT 3	SUB 5 IX2 2	SUB 4 IX1 1	SUB 3 IX 1	0 0000
1 0001	BRCLR0 3 BTB 2	BCLR0 5 BSC 2	BRN 3 REL 2						RTS 6 INH 1		CMP 2 IMM 2	CMP 3 DIR 3	CMP 4 EXT 3	CMP 5 IX2 2	CMP 4 IX1 1	CMP 3 IX 1	1 0001
2 0010	BRSET1 3 BTB 2	BSET1 5 BSC 2	BHI 3 REL 2		MUL 11 INH 1						SBC 2 IMM 2	SBC 3 DIR 3	SBC 4 EXT 3	SBC 5 IX2 2	SBC 4 IX1 1	SBC 3 IX 1	2 0010
3 0011	BRCLR1 3 BTB 2	BCLR1 5 BSC 2	BLS 3 REL 2	COM 5 DIR 1	COMA 3 INH 1	COMX 3 INH 1	COM 6 IX1 1	COM 5 IX 1	SWI 10 INH 1		CPX 2 IMM 2	CPX 3 DIR 3	CPX 4 EXT 3	CPX 5 IX2 2	CPX 4 IX1 1	CPX 3 IX 1	3 0011
4 0100	BRSET2 3 BTB 2	BSET2 5 BSC 2	BCC 3 REL 2	LSR 5 DIR 1	LSRA 3 INH 1	LSRX 3 INH 1	LSR 6 IX1 1	LSR 5 IX 1			AND 2 IMM 2	AND 3 DIR 3	AND 4 EXT 3	AND 5 IX2 2	AND 4 IX1 1	AND 3 IX 1	4 0100
5 0101	BRCLR2 3 BTB 2	BCLR2 5 BSC 2	BCS 3 REL 2								BIT 2 IMM 2	BIT 3 DIR 3	BIT 4 EXT 3	BIT 5 IX2 2	BIT 4 IX1 1	BIT 3 IX 1	5 0101
6 0110	BRSET3 3 BTB 2	BSET3 5 BSC 2	BNE 3 REL 2	ROR 5 DIR 1	RORA 3 INH 1	RORX 3 INH 1	ROR 6 IX1 1	ROR 5 IX 1			LDA 2 IMM 2	LDA 3 DIR 3	LDA 4 EXT 3	LDA 5 IX2 2	LDA 4 IX1 1	LDA 3 IX 1	6 0110
7 0111	BRCLR3 3 BTB 2	BCLR3 5 BSC 2	BEQ 3 REL 2	ASR 5 DIR 1	ASRA 3 INH 1	ASRX 3 INH 1	ASR 6 IX1 1	ASR 5 IX 1		TAX 2 INH 1		STA 3 DIR 3	STA 4 EXT 3	STA 5 IX2 2	STA 5 IX1 1	STA 4 IX 1	7 0111
8 1000	BRSET4 3 BTB 2	BSET4 5 BSC 2	BHCC 3 REL 2	LSL 5 DIR 1	LSLA 3 INH 1	LSLX 3 INH 1	LSL 6 IX1 1	LSL 5 IX 1		CLC 2 INH 1	EOR 2 IMM 2	EOR 3 DIR 3	EOR 4 EXT 3	EOR 5 IX2 2	EOR 4 IX1 1	EOR 3 IX 1	8 1000
9 1001	BRCLR4 3 BTB 2	BCLR4 5 BSC 2	BHCS 3 REL 2	ROL 5 DIR 1	ROLA 3 INH 1	ROLX 3 INH 1	ROL 6 IX1 1	ROL 5 IX 1		SEC 2 INH 1	ADC 2 IMM 2	ADC 3 DIR 3	ADC 4 EXT 3	ADC 5 IX2 2	ADC 4 IX1 1	ADC 3 IX 1	9 1001
A 1010	BRSET5 3 BTB 2	BSET5 5 BSC 2	BPL 3 REL 2	DEC 5 DIR 1	DECA 3 INH 1	DECX 3 INH 1	DEC 6 IX1 1	DEC 5 IX 1		CLI 2 INH 1	ORA 2 IMM 2	ORA 3 DIR 3	ORA 4 EXT 3	ORA 5 IX2 2	ORA 4 IX1 1	ORA 3 IX 1	A 1010
B 1011	BRCLR5 3 BTB 2	BCLR5 5 BSC 2	BMI 3 REL 2							SEI 2 INH 1	ADD 2 IMM 2	ADD 3 DIR 3	ADD 4 EXT 3	ADD 5 IX2 2	ADD 4 IX1 1	ADD 3 IX 1	B 1011
C 1100	BRSET6 3 BTB 2	BSET6 5 BSC 2	BMC 3 REL 2	INC 5 DIR 1	INCA 3 INH 1	INCX 3 INH 1	INC 6 IX1 1	INC 5 IX 1		RSP 2 INH 1		JMP 2 DIR 3	JMP 3 EXT 3	JMP 4 IX2 2	JMP 3 IX1 1	JMP 2 IX 1	C 1100
D 1101	BRCLR6 3 BTB 2	BCLR6 5 BSC 2	BMS 3 REL 2	TST 4 DIR 1	TSTA 3 INH 1	TSTX 3 INH 1	TST 5 IX1 1	TST 4 IX 1		NOP 2 INH 1	BSR 6 REL 2	JSR 5 DIR 3	JSR 6 EXT 3	JSR 7 IX2 2	JSR 6 IX1 1	JSR 5 IX 1	D 1101
E 1110	BRSET7 3 BTB 2	BSET7 5 BSC 2	BIL 3 REL 2						STOP 2 INH 1		LDX 2 IMM 2	LDX 3 DIR 3	LDX 4 EXT 3	LDX 5 IX2 2	LDX 4 IX1 1	LDX 3 IX 1	E 1110
F 1111	BRCLR7 3 BTB 2	BCLR7 5 BSC 2	BIH 3 REL 2	CLR 5 DIR 1	CLRA 3 INH 1	CLRX 3 INH 1	CLR 6 IX1 1	CLR 5 IX 1	WAIT 2 INH 1	TXA 2 INH 1		STX 4 DIR 3	STX 5 EXT 3	STX 6 IX2 2	STX 5 IX1 1	STX 4 IX 1	F 1111

Abbreviations for address modes and registers

BSC	Bit set/clear	IX	Indexed (no offset)
BTB	Bit test and branch	IX1	Indexed, 1 byte (8-bit) offset
DIR	Direct	IX2	Indexed, 2 byte (16-bit) offset
EXT	Extended	REL	Relative
INH	Inherent	A	Accumulator
IMM	Immediate	X	Index register

Not implemented

Legend



12

12.3 Addressing modes

Ten different addressing modes provide programmers with the flexibility to optimize their code for all situations. The various indexed addressing modes make it possible to locate data tables, code conversion tables and scaling tables anywhere in the memory space. Short indexed accesses are single byte instructions; the longest instructions (three bytes) enable access to tables throughout memory. Short absolute (direct) and long absolute (extended) addressing are also included. One or two byte direct addressing instructions access all data bytes in most applications. Extended addressing permits jump instructions to reach all memory locations.

The term 'effective address' (EA) is used in describing the various addressing modes. The effective address is defined as the address from which the argument for an instruction is fetched or stored. The ten addressing modes of the processor are described below. Parentheses are used to indicate 'contents of' the location or register referred to. For example, (PC) indicates the contents of the location pointed to by the PC (program counter). An arrow indicates 'is replaced by' and a colon indicates concatenation of two bytes. For additional details and graphical illustrations, refer to the ***M6805 HMOS/M146805 CMOS Family Microcomputer/ Microprocessor User's Manual*** or to the ***M68HC05 Applications Guide.***

12.3.1 Inherent

In the inherent addressing mode, all the information necessary to execute the instruction is contained in the opcode. Operations specifying only the index register or accumulator, as well as the control instruction, with no other arguments are included in this mode. These instructions are one byte long.

12.3.2 Immediate

In the immediate addressing mode, the operand is contained in the byte immediately following the opcode. The immediate addressing mode is used to access constants that do not change during program execution (e.g. a constant used to initialize a loop counter).

$$EA = PC+1;\ PC \leftarrow PC+2$$

12.3.3 Direct

In the direct addressing mode, the effective address of the argument is contained in a single byte following the opcode byte. Direct addressing allows the user to directly address the lowest 256 bytes in memory with a single two-byte instruction.

$$EA = (PC+1);\ PC \leftarrow PC+2$$
$$\text{Address bus high} \leftarrow 0;\ \text{Address bus low} \leftarrow (PC+1)$$

12.3.4 Extended

In the extended addressing mode, the effective address of the argument is contained in the two bytes following the opcode byte. Instructions with extended addressing mode are capable of referencing arguments anywhere in memory with a single three-byte instruction. When using the Motorola assembler, the user need not specify whether an instruction uses direct or extended addressing. The assembler automatically selects the short form of the instruction.

EA = (PC+1):(PC+2); PC ← PC+3
Address bus high ← (PC+1); Address bus low ← (PC+2)

12.3.5 Indexed, no offset

In the indexed, no offset addressing mode, the effective address of the argument is contained in the 8-bit index register. This addressing mode can access the first 256 memory locations. These instructions are only one byte long. This mode is often used to move a pointer through a table or to hold the address of a frequently referenced RAM or I/O location.

EA = X; PC ← PC+1
Address bus high ← 0; Address bus low ← X

12.3.6 Indexed, 8-bit offset

In the indexed, 8-bit offset addressing mode, the effective address is the sum of the contents of the unsigned 8-bit index register and the unsigned byte following the opcode. Therefore the operand can be located anywhere within the lowest 511 memory locations. This addressing mode is useful for selecting the mth element in an n element table.

EA = X+(PC+1); PC ← PC+2
Address bus high ← K; Address bus low ← X+(PC+1)
where K = the carry from the addition of X and (PC+1)

12.3.7 Indexed, 16-bit offset

In the indexed, 16-bit offset addressing mode, the effective address is the sum of the contents of the unsigned 8-bit index register and the two unsigned bytes following the opcode. This address mode can be used in a manner similar to indexed, 8-bit offset except that this three-byte instruction allows tables to be anywhere in memory. As with direct and extended addressing, the Motorola assembler determines the shortest form of indexed addressing.

EA = X+[(PC+1):(PC+2)]; PC ← PC+3
Address bus high ← (PC+1)+K; Address bus low ← X+(PC+2)
where K = the carry from the addition of X and (PC+2)

12.3.8 Relative

The relative addressing mode is only used in branch instructions. In relative addressing, the contents of the 8-bit signed byte (the offset) following the opcode are added to the PC if, and only if, the branch conditions are true. Otherwise, control proceeds to the next instruction. The span of relative addressing is from –126 to +129 from the opcode address. The programmer need not calculate the offset when using the Motorola assembler, since it calculates the proper offset and checks to see that it is within the span of the branch.

EA = PC+2+(PC+1); PC ← EA if branch taken;
otherwise EA = PC ← PC+2

12.3.9 Bit set/clear

In the bit set/clear addressing mode, the bit to be set or cleared is part of the opcode. The byte following the opcode specifies the address of the byte in which the specified bit is to be set or cleared. Any read/write bit in the first 256 locations of memory, including I/O, can be selectively set or cleared with a single two-byte instruction.

EA = (PC+1); PC ← PC+2
Address bus high ← 0; Address bus low ← (PC+1)

12.3.10 Bit test and branch

The bit test and branch addressing mode is a combination of direct addressing and relative addressing. The bit to be tested and its condition (set or clear) is included in the opcode. The address of the byte to be tested is in the single byte immediately following the opcode byte (EA1). The signed relative 8-bit offset in the third byte (EA2) is added to the PC if the specified bit is set or cleared in the specified memory location. This single three-byte instruction allows the program to branch based on the condition of any readable bit in the first 256 locations of memory. The span of branch is from –125 to +130 from the opcode address. The state of the tested bit is also transferred to the carry bit of the condition code register.

EA1 = (PC+1); PC ← PC+2
Address bus high ← 0; Address bus low ← (PC+1)
EA2 = PC+3+(PC+2); PC ← EA2 if branch taken;
otherwise PC ← PC+3

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13
OPERATING MODES

The MC68HC05L11 MCU has two modes of operation, the User Mode and the Self-Check Mode. Figure 13-1 shows the flowchart of entry to these two modes, and Table 13-1 shows operating mode selection.

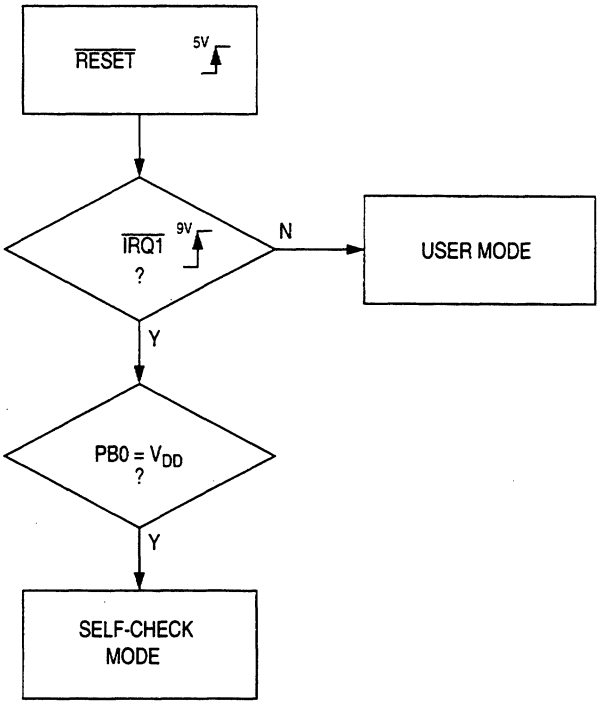

Figure 13-1 Flowchart of Mode Entering

Table 13-1 Mode Selection

$\overline{\text{RESET}}$	$\overline{\text{IRQ1}}$	PB0	MODE
5V ↑	V_{SS} to V_{DD}	V_{SS} to V_{DD}	USER
5V ↑	9V ↑ +9V Rising Edge*	V_{DD}	SELF-CHECK
* Minimum hold time should be 2 clock cycles, after that it can be used as a normal $\overline{\text{IRQ}}$ function pin.			

13.1 User Mode (Normal Operation)

The normal operational mode of the MC68HC05L11 is the user mode. The user mode will be entered if the $\overline{\text{RESET}}$ line is brought low, and the $\overline{\text{IRQ}}$ pin is within its normal operational range (V_{SS}-V_{DD}). The rising edge of the $\overline{\text{RESET}}$ will cause the MCU to enter the user mode.

13.2 Self-Check Mode

The MC68HC05L11 self-check mode is for the user to check device functions with an on-chip self-check program masked at location $7E10 to $7FEF under minimum hardware support. The hardware is shown in Figure 13-3. Since the self-check program is also part of the on-chip ROM, the RDIS flag is forced to zero (ROM enable) whenever entering this mode. Figure 13-2 is the criteria to enter self-check mode, where PB0's condition is latched within first two clock cycles after the rising edge of the reset. PB0 can then be used for other purposes. After entering the self-check mode, CPU branches to the self-check program and carries out the self-check. Self-check is a repetitive test, i.e. if all parts are checked to be good, the CPU will repeat the self-check again. Therefore, the LEDs attached to Port C will be flashing if the device is good; else the combination of LEDs' on/off patterns can show what part of the device is suspected to be bad. Table 13-2 lists the LEDs' on/off patterns and their corresponding indications.

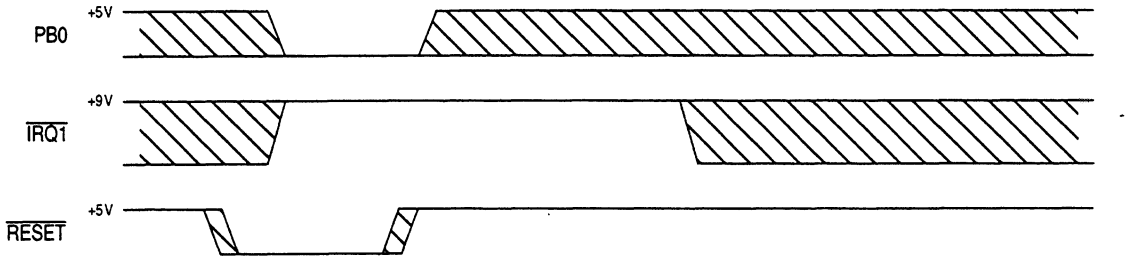

Figure 13-2 Self-Check Mode Timing

Table 13-2 Self-Check Report

PC3	PC2	PC1	PC0	REMARKS
1	0	0	1	Bad I/O
1	0	1	0	Bad RAM
1	0	1	1	Bad Timer
1	1	0	0	Bad SCI
1	1	0	1	Bad ROM
1	1	1	0	Bad SPI
1	1	1	1	Bad Interrupts or IRQ Request
Flashing				Good Device
All Others				Bad Device, Bad Port A, etc.

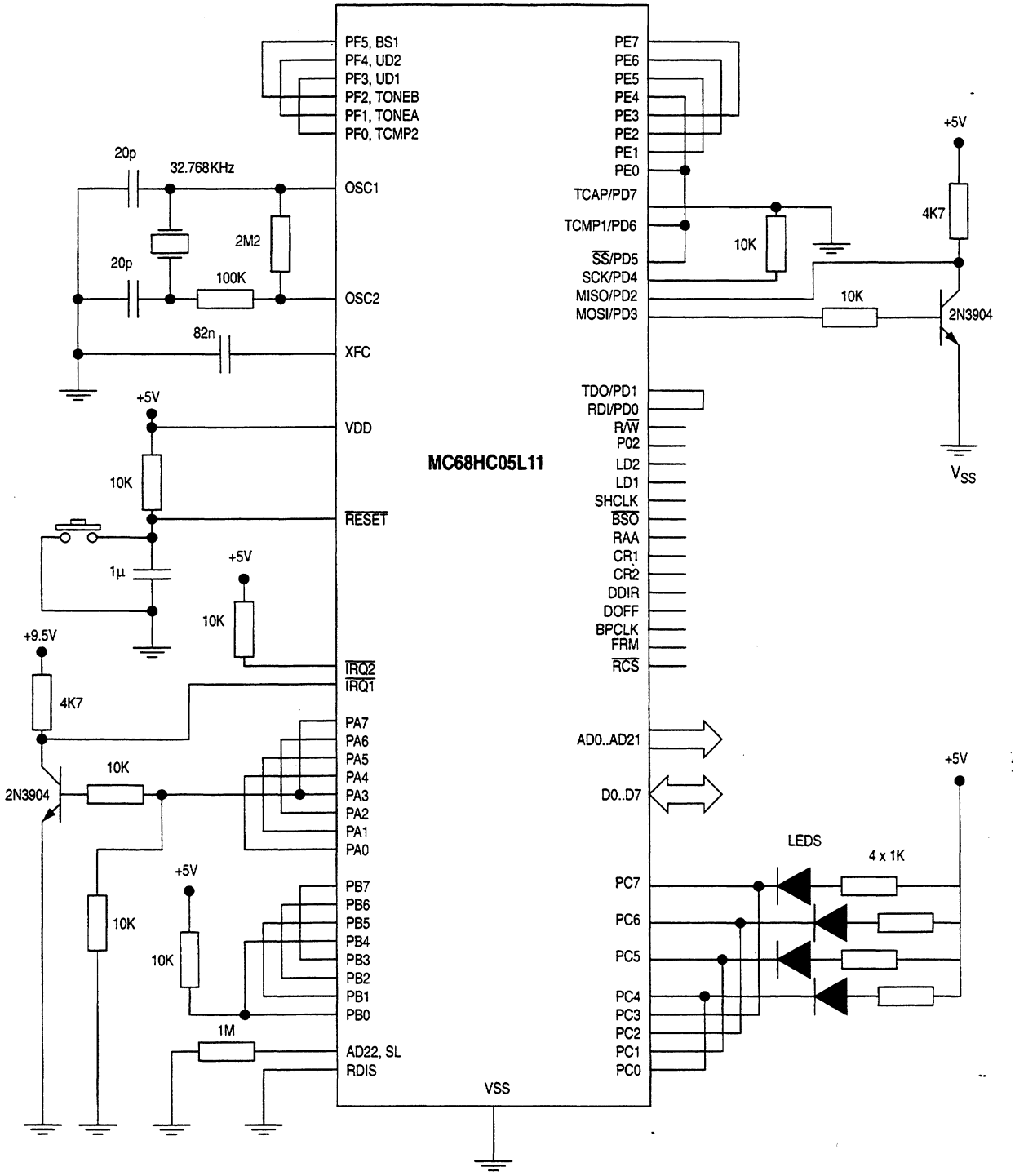

Figure 13-3 Self-Test Circuit

13

14
ELECTRICAL SPECIFICATIONS

This section contains the electrical specifications of MC68HC05L11.

14.1 Maximum Ratings

Voltages referenced to V_{SS}

RATINGS	SYMBOL	VALUE	UNIT
Supply Voltage	V_{DD}	–0.3 to +7.0	V
Input Voltage	V_{in}	V_{SS}–0.3 to V_{DD}+0.3	V
$\overline{IRQ1}$	V_{in}	V_{SS}–0.3 to 2xV_{DD}+0.3	V
Current Drain per pin excluding V_{DD} and V_{SS}	I_D	25	mA
Operating Temperature	T_A	0 to 70	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this high impedance circuit. For proper operation it is recommended that Vin and Vout be constrained to the range $V_{SS} \le (V_{in} \text{ or } V_{out}) \le V_{DD}$. Reliability of operation is enhanced if unused inputs are connected to an appropriate logic voltage level (e.g. either V_{SS} or V_{DD}).

14.2 DC Electrical Characteristics (V_{DD}=5V)

V_{DD}=5.0Vdc ±10%, V_{SS}=0Vdc, temperature range=0 to 70°C

CHARACTERISTICS	SYMBOL	MINIMUM	TYPICAL	MAXIMUM	UNIT
Output voltage $I_{LOAD} \leq -10\mu A$ $I_{LOAD} \leq +10\mu A$	 V_{OH} V_{OL}	 V_{DD}-0.1 –	 – –	 – 0.1	 V V
Output high voltage (I_{LOAD}=1.6mA) PA0-PA7, PB0-PB7, PC0-PC7, PD1, PD3-PD5, PD7, PE0-PE7, PF0-PF4, TONE, PO2, R/$\overline{W}$, D0-D7,$\overline{RCS}$, AD0-AD22, FRM, BPCLK, M, SHCLK, $\overline{BS0}$, RAA, C/R, DOFF, LDL, LDR, $\overline{LIR}$	V_{OH}	V_{DD}-0.8	–	–	V
Output low voltage (I_{LOAD}=1.6mA) PA0-PA7, PB0-PB7, PC0-PC7, PD1, PD3-PD5, PD7, PE0-PE7, PF0-PF4, TONE, PO2, R/$\overline{W}$, D0-D7,$\overline{RCS}$, AD0-AD22, FRM, BPCLK, M, SHCLK, $\overline{BS0}$, RAA, C/R, DOFF, LDL, LDR, $\overline{LIR}$	V_{OL}	–	–	0.4	V
Input high voltage PA0-PA7, PB0-PB7, PC0-PC7, PD0-PD7, PD3-PD5, PE0-PE7, PF0-PF4, $\overline{IRQ1}$, $\overline{IRQ2}$, $\overline{RESET}$, OSC1, D0-D7, LDL, LDR	V_{IH}	0.7xV_{DD}	–	V_{DD}	V
Input low voltage PA0-PA7, PB0-PB7, PC0-PC7, PD0-PD7, PD3-PD5, PE0-PE7, PF0-PF4, $\overline{IRQ1}$, $\overline{IRQ2}$, $\overline{RESET}$, OSC1, D0-D7, LDL, LDR	V_{IL}	V_{SS}	–	0.2xV_{DD}	V
Data Retention Mode	V_{RM}	2.0	–	–	V
Supply current Run (3.68MHz) (2.45MHz) (1.22MHz) (307KHz) Wait (3.68MHz) (2.45MHz) (1.22MHz) (307KHz) Stop (oscillator off) (oscillator on)	 I_{DD} 	 – 	 12 11 4.6 1.3 1.5 1.2 0.8 0.5 3 25	 19 16 7 2 2.5 2.0 1.4 0.8 12 40	 mA mA mA mA mA mA mA mA µA µA
I/O ports high-Z leakage current PA0-PA7, PB0-PB7, PC0-PC7, PD0-PD7, PE0-PE7, PF0-PF4	I_{IL}	–	–	±10	µA
Input current TCAP, $\overline{IRQ1}$, $\overline{IRQ2}$, $\overline{RESET}$, PD0, OSC1	I_{IN}	–	–	±1	µA
Capacitance ports (as input or output) D0-D7, AD0-AD22, PO2, TONE, R/$\overline{W}$, $\overline{LIR}$, $\overline{RESET}$, $\overline{IRQ1}$, $\overline{IRQ2}$, OSC1, PD0-PD7	 C_{OUT} C_{IN}	 – –	 – –	 12 8	 pF pF

14.3 DC Electrical Characteristics (V_{DD}=3.3V)

V_{DD}=3.3Vdc ±10%, V_{SS}=0Vdc, temperature range=0 to 70°C

CHARACTERISTICS	SYMBOL	MINIMUM	TYPICAL	MAXIMUM	UNIT
Output voltage $I_{LOAD} \leq -10\mu A$ $I_{LOAD} \leq +10\mu A$	 V_{OH} V_{OL}	 V_{DD}-0.1 –	 – –	 – 0.1	 V V
Output high voltage (I_{LOAD}=0.8mA) PA0-PA7, PB0-PB7, PC0-PC7, PD1, PD3-PD5, PD7, PE0-PE7, PF0-PF4, TONE, PO2, R/$\overline{W}$, D0-D7,$\overline{RCS}$, AD0-AD22, FRM, BPCLK, M, SHCLK, $\overline{BS0}$, RAA, C/R, DOFF, LDL, LDR, $\overline{LIR}$	V_{OH}	V_{DD}-0.3	–	–	V
Output low voltage (I_{LOAD}=0.8mA) PA0-PA7, PB0-PB7, PC0-PC7, PD1, PD3-PD5, PD7, PE0-PE7, PF0-PF4, TONE, PO2, R/$\overline{W}$, D0-D7,$\overline{RCS}$, AD0-AD22, FRM, BPCLK, M, SHCLK, $\overline{BS0}$, RAA, C/R, DOFF, LDL, LDR, $\overline{LIR}$	V_{OL}	–	–	0.3	V
Input high voltage PA0-PA7, PB0-PB7, PC0-PC7, PD0-PD7, PD3-PD5, PE0-PE7, PF0-PF4, $\overline{IRQ1}$, $\overline{IRQ2}$, $\overline{RESET}$, OSC1, D0-D7, LDL, LDR	V_{IH}	0.7xV_{DD}	–	V_{DD}	V
Input low voltage PA0-PA7, PB0-PB7, PC0-PC7, PD0-PD7, PD3-PD5, PE0-PE7, PF0-PF4, $\overline{IRQ1}$, $\overline{IRQ2}$, $\overline{RESET}$, OSC1, D0-D7, LDL, LDR	V_{IL}	V_{SS}	–	0.2xV_{DD}	V
Data Retention Mode	V_{RM}	2.0	–	–	V
Supply current Run (1.22MHz) (307KHz) Wait (1.22MHz) (307KHz) Stop (oscillator off) (oscillator on)	I_{DD}	–	 2.7 0.7 0.4 0.2 2 15	 5 2 0.8 0.4 8 30	 mA mA mA mA µA µA
I/O ports high-Z leakage current PA0-PA7, PB0-PB7, PC0-PC7, PD0-PD7, PE0-PE7, PF0-PF4	I_{IL}	–	–	±10	µA
Input current TCAP, $\overline{IRQ1}$, $\overline{IRQ2}$, $\overline{RESET}$, PD0, OSC1	I_{IN}	–	–	±1	µA
Capacitance ports (as input or output) D0-D7, AD0-AD22, PO2, TONE, R/$\overline{W}$, $\overline{LIR}$, $\overline{RESET}$, $\overline{IRQ1}$, $\overline{IRQ2}$, OSC1, PD0-PD7	C_{OUT} C_{IN}	– –	– –	12 8	pF pF

14.4 Bus Timing

V_{DD}=5.0Vdc ±10%, V_{SS}=0Vdc,T_A=0 to 70°C

REF	CHARACTERISTICS	SYMBOL	300KHz		3.69MHz		UNIT
			MIN	MAX	MIN	MAX	
1	Cycle time	tcyc	3334	–	271	–	ns
2	Pulse width, PO2 low	PO2l					ns
3	Pulse width, PO2 high	PO2h					ns
4	PO2 rise time	tr	–	25	–	25	ns
5	PO2 fall time	tf	–	25	–	25	ns
6	Address delay time fromPO2 fall	tad	–	40	–	40	ns
7	Address hold time from PO2 rise	tah	10	–	10	–	ns
8	R/$\overline{W}$ delay time from PO2 fall	trwd	–	40	–	40	ns
9	R/$\overline{W}$ hold time from PO2 rise	trwh	10	–	10	–	ns
10	Write data delay time	tddw	–	40	–	4-	ns
11	Write data hold time	tdhw	10	–	10	–	ns
12	Read data setup time	tdsr	30	–	30	–	ns
13	Read data hold time	tdhr	10	–	10	–	ns
14	$\overline{CS0}$, $\overline{CS1}$, $\overline{CS2}$, $\overline{RCS}$ output delay	tcsd	–	40	–	40	ns

All timing is shown with respect to 20% V_{DD} and 70% V_{DD}

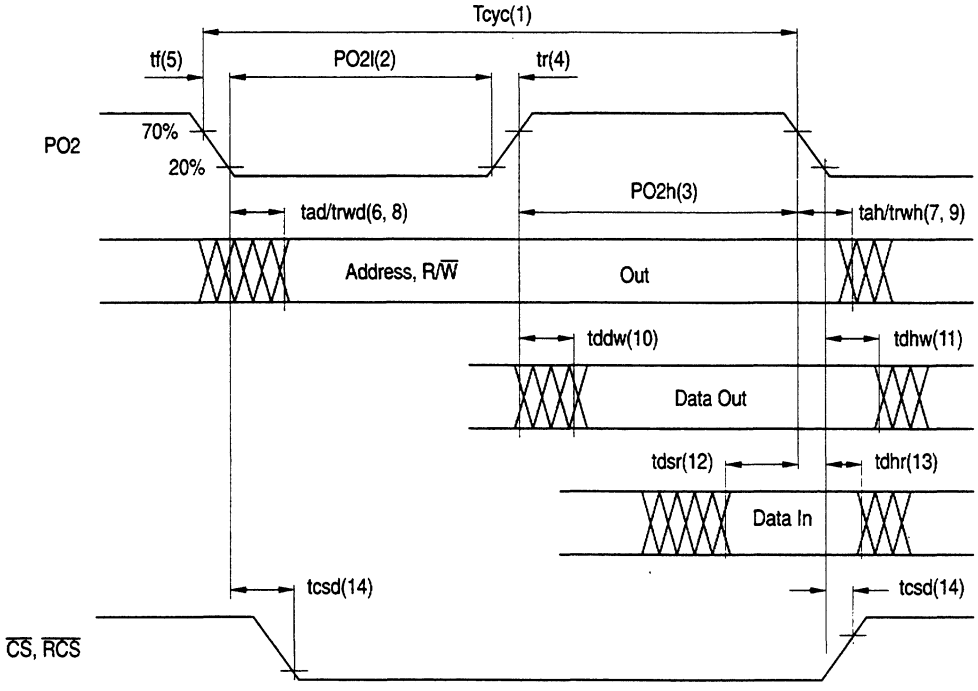

Figure 14-1 Bus Timing

14.5 Ports Timing

V_{DD}=5.0Vdc ±10%, V_{SS}=0Vdc,T_A=0 to 70°C

REF	CHARACTERISTICS	SYMBOL	300KHz		3.69MHz		UNIT
			MIN	MAX	MIN	MAX	
1	Cycle time	tcyc	3334	–	271	–	ns
2	Port data in setup time	tpdsu	100	–	100	–	ns
3	Port data in hold time	tpdh	350	–	50	–	ns
4	Port data write delay time	tpwd	–	40	–	40	ns

All timing is shown with respect to 20% V_{DD} and 70% V_{DD}

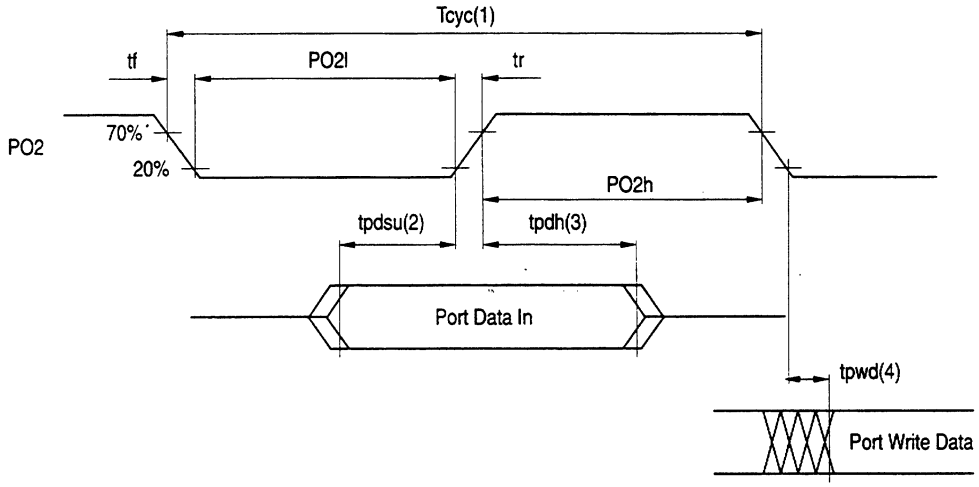

Figure 14-2 Ports Timing

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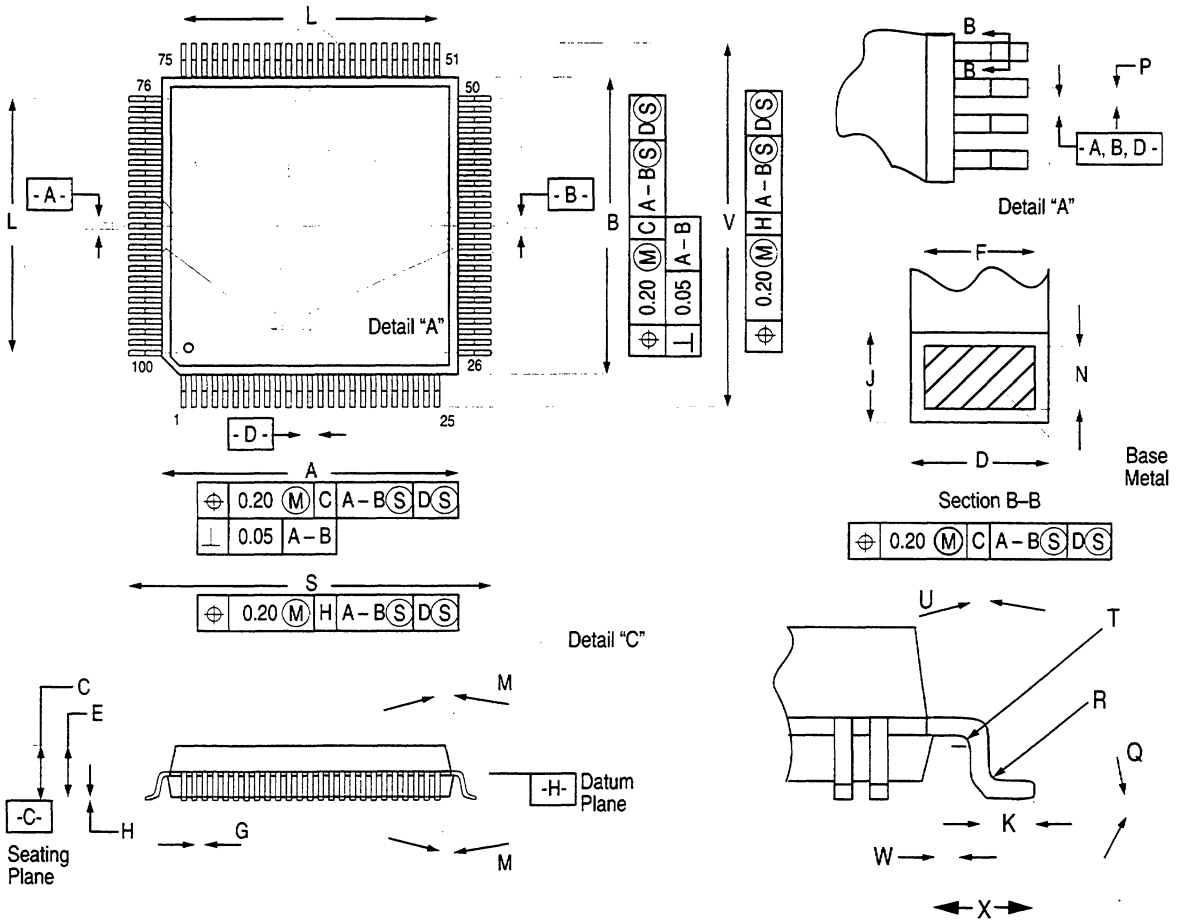
15
MECHANICAL SPECIFICATIONS

This section provides the mechanical dimensions for the 100-pin QFP package and the die bond coordinates.

15.1 Package Dimensions



Dim.	Min.	Max.
A	13.90	14.10
B	13.90	14.10
C	2.15	2.47
D	0.30	0.45
E	2.05	—
F	0.20	—
G	0.50 BSC	
H	—	0.25
J	0.15	—
K	0.80	—
L	12.00 REF	

Notes

1. Datum Plane –H– is located at bottom of lead and is coincident with the lead where the lead exits the plastic body at the bottom of the parting line.
2. Datums A–B and –D to be determined at Datum Plane –H–.
3. Dimensions S and V to be determined at seating plane –C–.
4. Dimensions A and B do not include mould protrusion. Allowable mould protrusion is 0.25 mm per side. Dimensions A and B do include mould mismatch and are determined at Datum Plane –H–.
5. Dimension D does not include dambar protrusion. Allowable dambar protrusion shall be 0.08 total in excess of the D dimension at maximum material condition. Dambar cannot be located on the lower radius or the foot.
6. Dimensions and tolerancing per ANSI Y 14.5M, 1982.
7. All dimensions in mm.

Dim.	Min.	Max.
M	5°	10°
N	0.13	0.17
P	0.40 BSC	
Q	0°	7°
R	0.13	0.30
S	16.95	17.45
T	0.13	—
U	0°	—
V	16.95	17.45
W	0.40	—
X	1.6 REF	

Figure 15-1 100-pin QFP Mechanical Dimension

15.2 Bonding Diagram

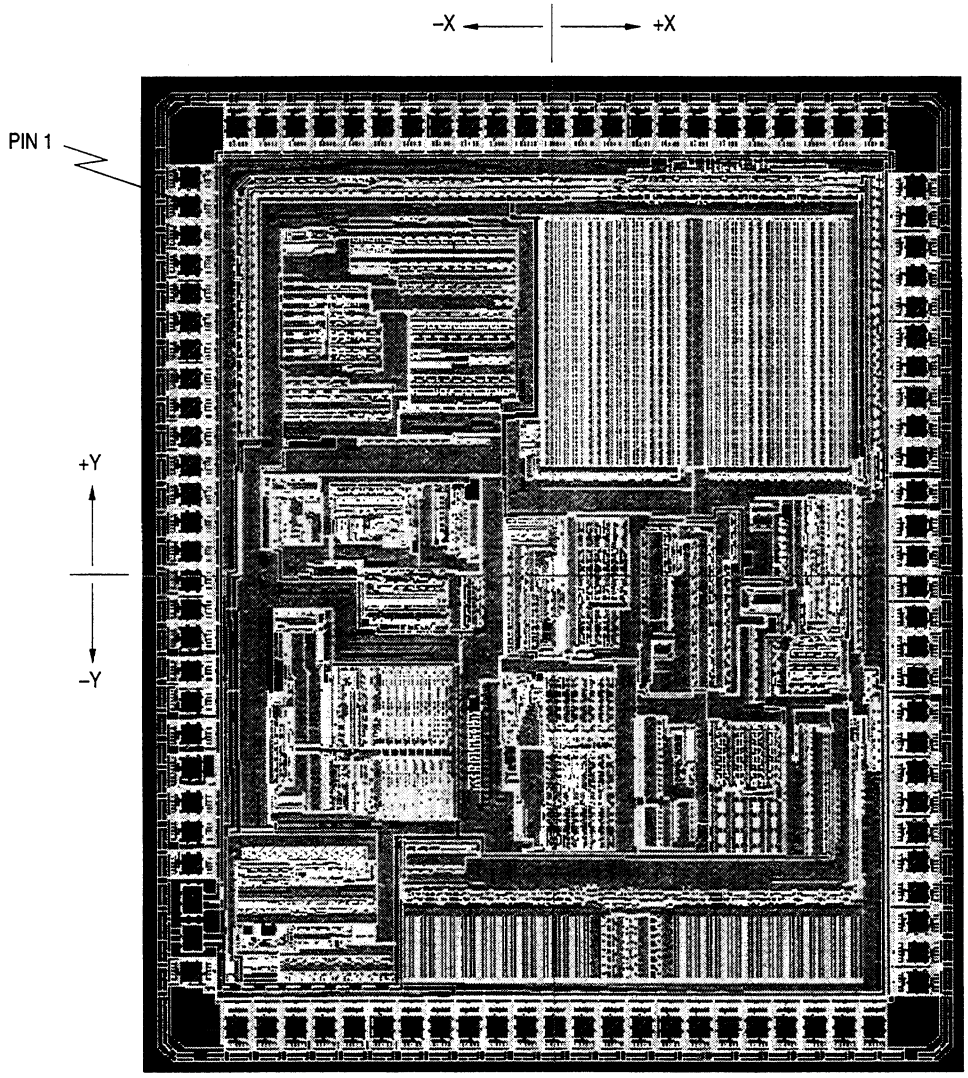


Figure 15-2 Die Bond Diagram

Table 15-1 Bond Pad Coordinates

PIN No.	PIN NAME	COORDINATES	
		X	Y
1	PC1	-2595.0	2655.5
2	PC2	-2595.0	2449.5
3	PC3	-2595.0	2241.0
4	PC4	-2595.0	2037.5
5	PC5	-2595.0	1831.5
6	PC6	-2595.0	1625.5
7	PC7	-2595.0	1419.5
8	PE7	-2595.0	1213.5
9	PE6	-2595.0	1007.5
10	PE5	-2595.0	801.5
11	PE4	-2595.0	595.5
12	PE3	-2595.0	389.5
13	PE2	-2595.0	183.5
14	PE1	-2595.0	-22.5
15	PE0	-2595.0	-228.5
16	OSC1	-2595.0	-434.0
17	OSC2	-2595.0	-673.0
18	$\overline{\text{RESET}}$	-2595.0	-892.0
19	$\overline{\text{IRQ2}}$	-2595.0	-1131.0
20	$\overline{\text{IRQ1}}$	-2595.0	-1367.5
21	R/$\overline{\text{W}}$	-2595.0	-1619.5
22	RDIS	-2595.0	-1822.5
23	PO2	-2595.0	-2061.0
24	VDD	-2595.0	-2314.0
25	VSS	-2595.0	-2587.5

PIN No.	PIN NAME	COORDINATES	
		X	Y
26	XFC	-2595.0	-2827.0
27	D0	-2276.0	-3228.0
28	D1	-2069.0	-3228.0
29	D2	-1862.0	-3228.0
30	D3	-1655.0	-3228.0
31	D4	-1448.0	-3228.0
32	D5	-1241.0	-3228.0
33	D6	-1034.0	-3228.0
34	D7	-827.0	-3228.0
35	AD0	-620.0	-3228.0
36	AD1	-413.0	-3228.0
37	AD2	-206.0	-3228.0
38	AD3	1.0	-3228.0
39	AD4	208.0	-3228.0
40	AD5	415.0	-3228.0
41	AD6	622.0	-3228.0
42	AD7	829.0	-3228.0
43	AD8	1036.0	-3228.0
44	AD9	1243.0	-3228.0
45	AD10	1450.0	-3228.0
46	AD11	1657.0	-3228.0
47	AD12	1864.0	-3228.0
48	AD13	2071.0	-3228.0
49	AD14	2278.0	-3228.0
50	AD15	2595.5	-2909.5

Dimensions in µm

Table 15-1 Bond Pad Coordinates

PIN No.	PIN NAME	COORDINATES	
		X	Y
51	AD16	2595.5	-2694.0
52	AD17	2595.5	-2478.5
53	AD18	2595.5	-2263.0
54	AD19	2595.5	-2047.5
55	AD20/$\overline{CS0}$	2595.5	-1832.0
56	AD21/$\overline{CS1}$	2595.5	-1616.5
57	AD22/$\overline{CS2}$, SL	2595.5	-1401.0
58	$\overline{RCS}$	2595.5	-1185.5
59	PD0/RDI	2595.5	-970.0
60	PD1/TDO	2595.5	-719.0
61	PD2/MISO	2595.5	-503.5
62	PD3/MOSI	2595.5	-288.0
63	PD4/SCK	2595.5	-72.0
64	PD5/$\overline{SS}$	2595.5	146.5
65	PD6/TCMP1	2595.5	362.0
66	PD7/TCAP	2595.5	609.5
67	PB0	2595.5	860.5
68	PB1	2595.5	1076.0
69	PB2	2595.5	1291.5
70	PB3	2595.5	1507.0
71	PB4	2595.5	1722.5
72	PB5	2595.5	1938.0
73	PB6	2595.5	2153.5
74	PB7	2595.5	2369.0
75	PA0	2595.5	2584.5

PIN No.	PIN NAME	COORDINATES	
		X	Y
76	PA1	2595.5	2800.0
77	PA2	2289.0	3228.5
78	PA3	2082.0	3228.5
79	PA4	1875.0	3228.5
80	PA5	1668.0	3228.5
81	PA6	1461.0	3228.5
82	PA7	1254.0	3228.5
83	PF0/TCMP2	1047.0	3228.5
84	PF1/TONEA	840.0	3228.5
85	PF2/TONEB	633.0	3228.5
86	PF3/UD1	426.0	3228.5
87	PF4/UD2	219.0	3228.5
88	PF5/$\overline{BS1}$	12.0	3228.5
89	LD1	-195.0	3228.5
90	LD2	-402.0	3228.5
91	$\overline{BS0}$	-605.5	3228.5
92	SHCLK	-812.5	3228.5
93	RAA	-1019.5	3228.5
94	CR2	-1226.5	3228.5
95	CR1	-1433.5	3228.5
96	DOFF	-1640.5	3228.5
97	BPCLK	-1847.5	3228.5
98	FRM	-2054.5	3228.5
99	DDIR	-2261.5	3228.5
100	PC0	-2595.0	2861.5

Dimensions in µm

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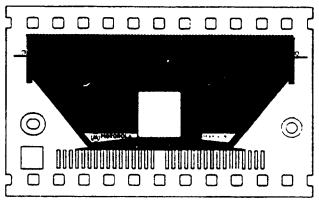
APPENDIX A
SEGMENT DRIVERS

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

REV 2.4 APR 94

MC141514



MC141514T1 TAB
MC141514T2 TAB

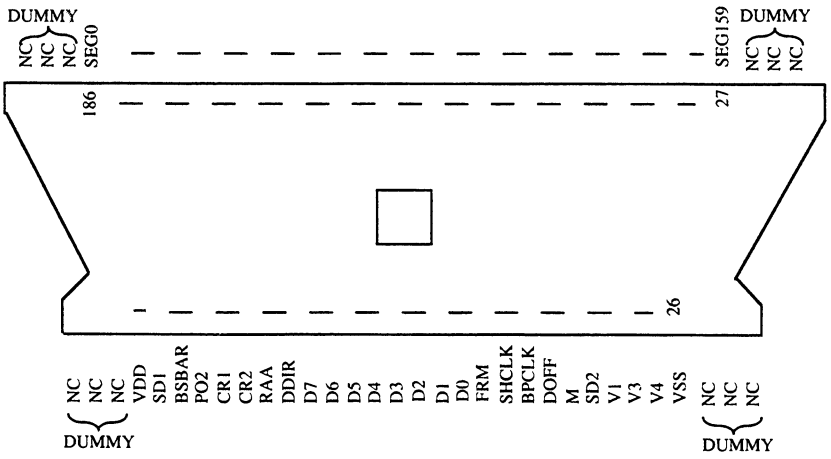
Product Preview

LCD Segment Driver

The Segment Driver is a CMOS chip which consists of 160 x 146 Static RAM for display storage and having 160 high voltage LCD driving signals. It is a companion chip of MC141512T and MC141515T Backplane Drivers for large LCD panel. All these chips are controlled by the MC68HC05L11 microcomputer.

FEATURES

- : 160 LCD segments driving signals
- : 160 x 146 LCD Static RAM Matrix (display RAM)
- : Expansion to higher driver count by cascade
- : Serial data interface with MC68HC05L11
- : 1:5 to 1:13 bias
- : Selectable multiplex ratio from 16 to 146
- : 186-pin TAB

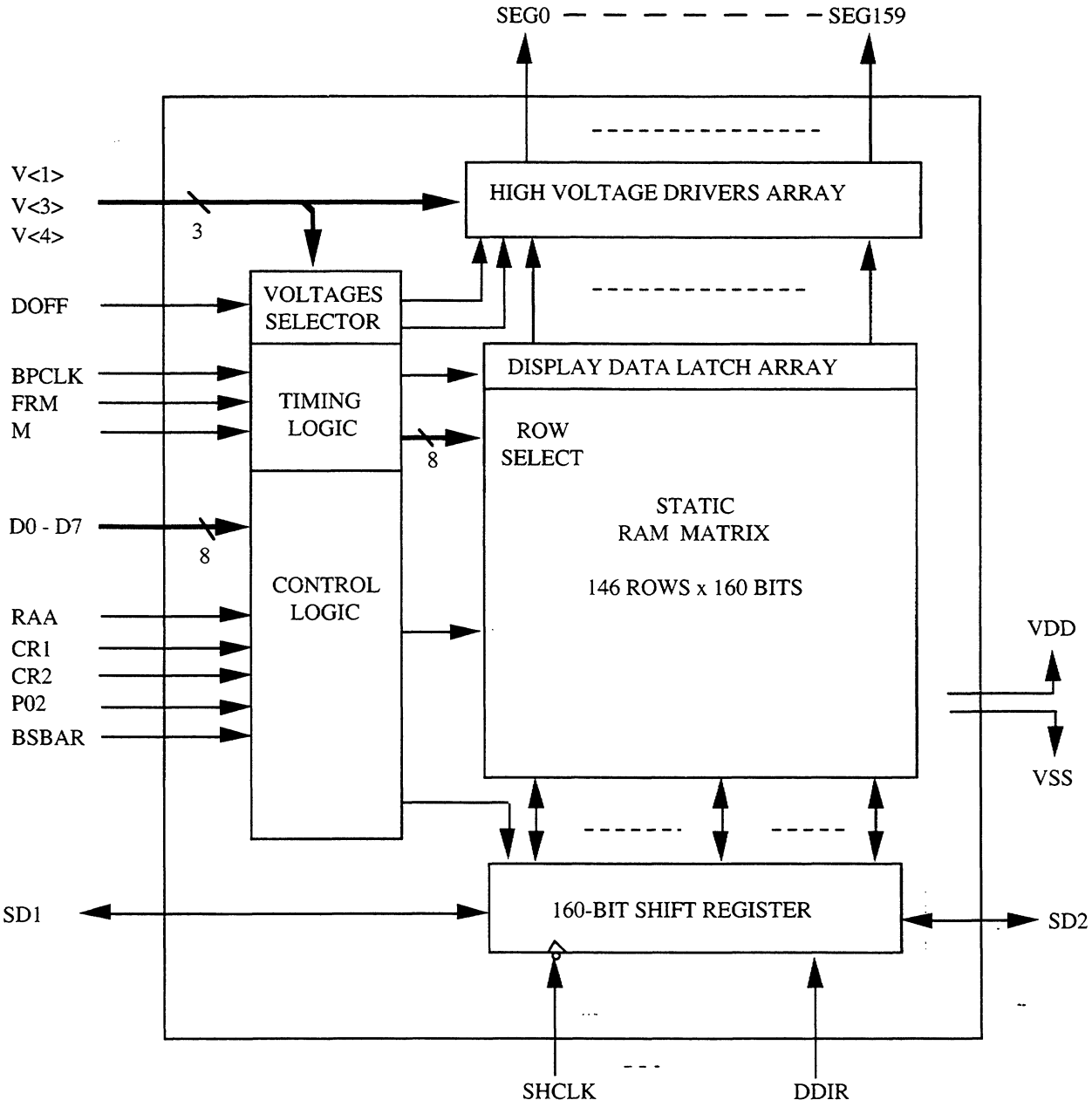


MC141514T1
MC141514T2
Pin Assignment (copper view)

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MOTOROLA

BLOCK DIAGRAM



MAXIMUM RATINGS* (Voltages Referenced to V_{SS}, T_A = 25°C)

Ratings	Symbol	Value	Unit
Supply Voltage	VDD	-0.3 to + 7.0	V
	V<1>	VSS-0.3 to VSS+27.5	V
Input Voltage	Vin	VSS-0.3 to VDD +0.3	V
Current Drain Per Pin Excluding VDD and VSS	I	25	mA
Operating Temperature Range	TA	0 to 70	°C
Storage Temperature Range	Tstg	-65 to + 150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions to be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that Vin and Vout be constrained to the range VSS < or = (Vin or Vout) < or = VDD. Reliability of operation is enhanced if unused input are connected to an appropriate logic voltage level (e.g., either VSS or VDD). Unused outputs must be left open.

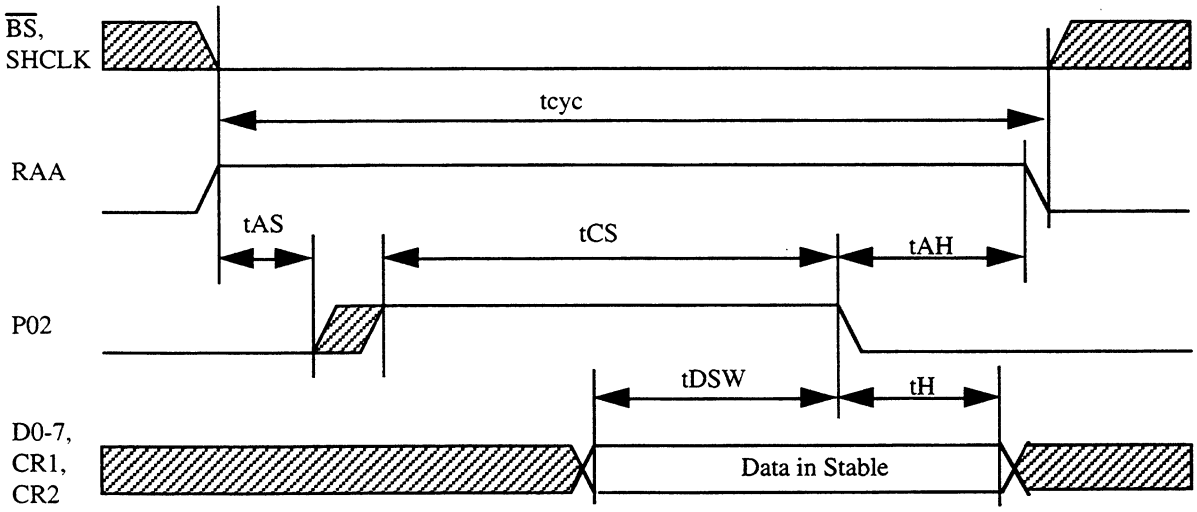
ELECTRICAL CHARACTERISTICS (Voltages Referenced to VSS, TA = 25°C, VDD = 5.0V)

Characteristis	Symbol	Min	Typ	Max	Unit
Input High Voltage BPCLK, FRM, P02, RAA, CR1, CR2, $\overline{BS}$, D7-D0, SD1,SD2, SHCLK, DOFF, M, DDIR	VIH	0.7xVDD	-	VDD	V
Input Low Voltage BPCLK, FRM, P02, RAA, CR1, CR2, $\overline{BS}$, D7-D0, SD1,SD2, SHCLK, DOFF, M, DDIR	VIL	VSS	-	0.3xVDD	V
Data Retention	VR	2.0	-	-	V
Input Current BPCLK, FRM, P02, RAA, CR1, CR2, $\overline{BS}$, D7-D0, SD1,SD2, SHCLK, DOFF, M, DDIR	Iin	-	-	±1	uA
Capacitance BPCLK, FRM, P02, RAA, CR1, CR2, $\overline{BS}$, D7-D0, SD1,SD2, SHCLK, DOFF, M, DDIR	Cin	-	-	8	pF
Internal Pull Down Resistance DOFF	Rdown	-	1	-	M Ohm
Output High Voltage SD1,SD2	VOH	0.8xVDD	-	VDD	V
Output Low Voltage SD1,SD2	VOL	VSS	-	0.2xVDD	V
Operating Voltages Supply Voltage (referenced to VSS)	VDD	4.5	-	5.5	V
LCD Voltage (referenced to VSS)	V<1>	8.0	-	26.0	V
Operating supply current (VDD) (VDD = 5 V,referenced to VSS) Access Mode	IACC	0	200	-	uA
Display Mode	IDP	0	30	-	uA
Standby Mode	ISB	0	2	-	uA
Operating supply current (V<1>) (V<1> = 25 V,referenced to VSS) Display Mode	ILDP	0	12	-	uA
Standby Mode	ILSB	0	1	-	uA

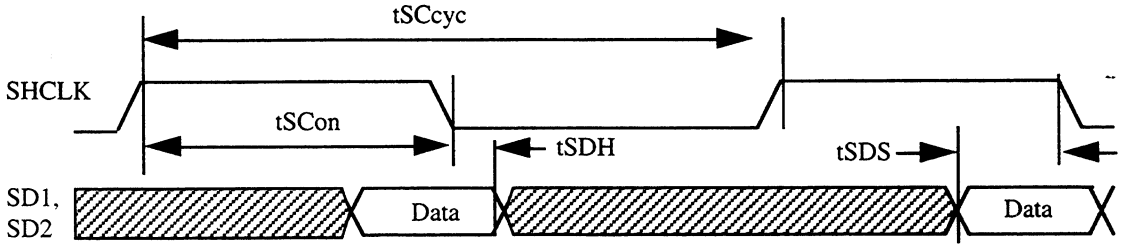
AC OPERATION CONDITIONS AND CHARACTERISTICS

(VCC = 5.0 V +/- 5%, VSS = 0, TA = 25°C)

Characteristics	Symbol	Min	Max	Unit
Access Cycle Time	tcyc	235	-	ns
Access Set Up Time	tAS	100	-	ns
RAA Hold Time	tAH	0	-	ns
Chip Select Pulse Width	tCS	135	-	ns
Data SetUp Time	tDSW	100	-	ns
Input Hold Time	tH	10	-	ns
Shift Clock Cycle Time	tSCcyc	200	-	ns
Shift Clock On Time	tSCon	100	-	ns
Serial Data Setup Time	tSDS	50	-	ns
Serial Data Hold Time	tSDH	10	-	ns



Parallel Access Timing



Serial Access Timing (with $\overline{BS}$ = 0)

PIN DESCRIPTION

VDD AND VSS

Power is supplied to the driver using these two pins. VDD is power and VSS is ground.

V<1>, V<3>, V<4>

These are the levels of voltage generated from an external voltages divider (Fig. 2). These voltage provide different voltage levels for shaping up the display output waveforms Seg0 - Seg159.

DOFF

This is an output from MC68HC05L11 to signal the backplane driver to turn off LCD.If this pin is clear, the segment driver supplies LCD with drivering signal. If this pin is set, the segment driver outputs is high-impedanced and LCD display is disabled.

FRM

A periodic active high input to the segment driver for frame timing synchronization. This pin is connected to the signal FRM of MC68HC05L11. The frequency depends on the bias ratio and BPCLK signal.

BPCLK

A periodic clock output from MC68HC05L11 to the segment driver for timing synchronization. The signal controls the refresh timing of LCD display.

M

A periodic output from backplane driver. This pin is used for synchronization among display drivers.

D0 - D7

An eight-bit input-only data bus which is connected to the D0 - D7 of MC68HC05L11. These pins are used for address input and data input. Pls refer to Fig.1 for definition.

P02

A bus clock input that is using for data bus timing synchronization. This pin is connected to P02 of MC68HC05L11.

BSBAR

This is an active low input for chip select.

RAA

It is a strobe signal from MC68HC05L11 indicating that a valid segment control data is on D0 - D7 for a period of P02.

CR1, CR2

These two control signals from MC68HC05L11 to Segment driver describing the nature of the content in D0 - D7. The effect of CRs are shown on Fig 1.

SD1, SD2

These two pins are two bi-directional data lines connecting to the UD2 or LD2 and UD1 or LD1 respectively. These allow the display data from MC68HC05L11 entering the segment driver in both directions.

SHCLK

This is the shift clock from MC68HC05L11 to segment driver for clocking the serial data on SD1 and SD2. See Timing Diagram on Page 5 for illustration.

DDIR

It is an input pin carrying the signal from MC68HC05L11 to segment driver to control the direction of the serial data. If DDIR is set, the serial data enters the segment driver through SD1 and leaves the segment driver through SD2. If DDIR is clear, SD1 and SD2 are redefined as an output and input respectively.

SEG0 - SEG159

These 160 output lines provide the segment driving signal to the LCD panel. They are all in high-impedance state while the display is turned off (i.e. DOFF is set).

OPERATION OF LIQUID CRYSTAL DISPLAY DRIVER

INTRODUCTION

The LCD segment driver can support multiplex ratio of a LCD system up to 256 (146 at the present version) and cascading of more than one driver for expansion is possible. It can be set from 1:5 bias (for 16 mux) to 1:13 bias (for 146 mux), by the voltage divider ratio of Fig.2. The ratio of bias or the contrast ratio (a) is defined as

$$1 : \frac{4 \times R1 + R2}{R1} = 1 : a$$

As the multiplex ratio changes, the ratio of bias has to be changed accordingly. The ratio of bias relates to the multiplex ratio as

$$a = \sqrt{mux} + 1$$

To set up a multiplex ratio, please refer to MC68HC05L11 specification Section 6.2.5.

CONTROL LOGIC produces the control signals necessary for display RAM read / write and serial data latching. This Control Logic is directly supervised by the MCU through the Data Bus, i.e. D0 - D7, CR1 and CR2. MCU writing a byte of instruction to the Segment Control Register will cause Segment Driver(s) to fetch this instruction from the Data Bus and the command executed at the next P02 cycle. Fig .2 shows the functions of which the Control Logic will carry out in respond to MCU access through the Segment Control Register.

ROW ADDRESS(WRITE IN) instruction causes Segment driver(s) to load the content of the SHIFT REGISTER into a row of RAM which address is specified by D7 to D0.

ROW ADDRESS(READ FROM) instruction causes Segment driver(s) to copy a row of RAM which address is specified by D7 to D0 into the 160 BIT SHIFT REGISTER.

SCROLL UP ADVANCE instruction causes Segment driver(s) to do a vertical scroll up or down. The content of D7 to D0 only represents the vertical offset of the new screen to the current screen. This vertical offset presenting in the Data Bus then is added up with an old offset which is stored in a register called the VERTICAL SCROLL VECTOR REGISTER to generate a new offset. This new offset will then be stored in the VERTICAL SCROLL VECTOR REGISTER. Periodically the content of this register will be fetched and loaded into a presettable counter in the TIMING LOGIC to generate the row addresses for screen refreshing.

RESET BIT0 Writing an "1" to this bit will set the VERTICAL SCROLL VECTOR REGISTER to zero.

UL BIT1 If this bit is set, the segment driver serves the upper panel in case of splitted panel. This will cause a swap in signals flow between SD1 and SD2.

CLRSH BIT2 Writing an "1" to this bit will clear the content of the 160-BIT SHIFT REGISTER.

TIMING LOGIC, according to M, BPCLK and FRM, fills the DISPLAY DATA LATCH ARRAY with rows of RAM matrix's content periodically starting from the row address specified by the VERTICAL SCROLL VECTOR REGISTER.

VOLTAGES SELECTOR consists of switching circuit to select appropriate voltage levels from the external voltage divider. (See Fig. 2).

DISPLAY DATA LATCH ARRAY is used to buffer up a row of display data from RAM.

STATIC RAM MATRIX consists of 160x146 bits of SRAM cell. The content of these RAM cells can be altered by read/write from/to the shift register with the Segment Control Interface (refer to MC68HC05L11 specification Section 6.2.4).

HIGH VOLTAGE DRIVERS ARRAY is a row of high voltage drivers connecting to segment lines of any LCD panel. The output waveform of the high voltage driver is shown as Seg(x) in Fig 3.

SHIFT REGISTER is a 160-bit bi-directional register which acts as an input either from SD1 or SD2. The direction of data flow depends on the content of DDIR. And, it can be swapped by setting the UL bit to high. Data enter this shift register in serial . Shift register latches data at the falling edge of the signal SHCLK. See Timing Diagram on Page 5 for illustration.

CR2	CR1	D7	D6	D5	D4	D3	D2	D1	D0
0	0	ROW ADDRESS (WRITE IN)							
0	1	ROW ADDRESS (READ FROM)							
1	0	SCROLL UP ADVANCE							
1	1	0	X	X	X	X	CLR SH	UL	RESET

FIGURE 1 - A Summary of the Control Functions of Segment Driver

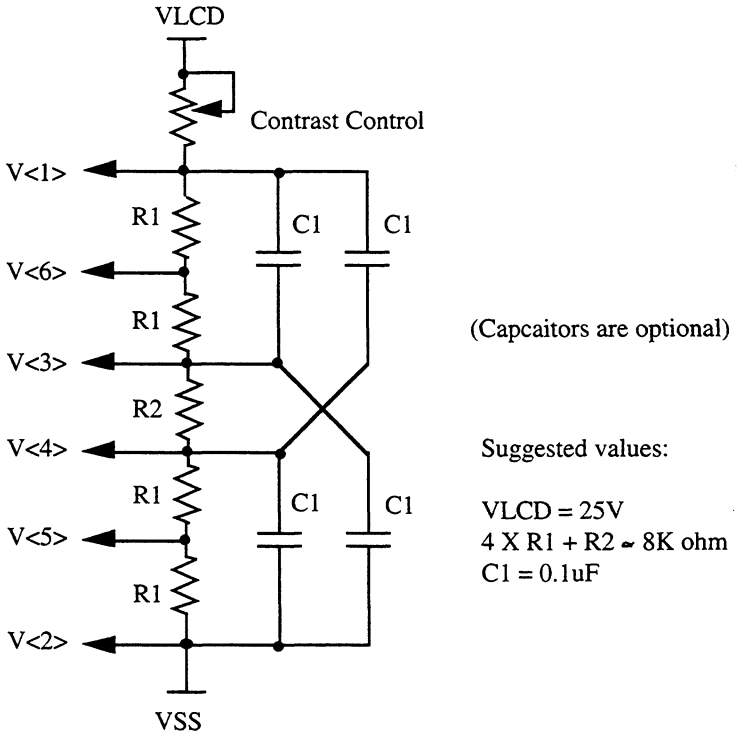


FIGURE 2 - External Voltage Divider

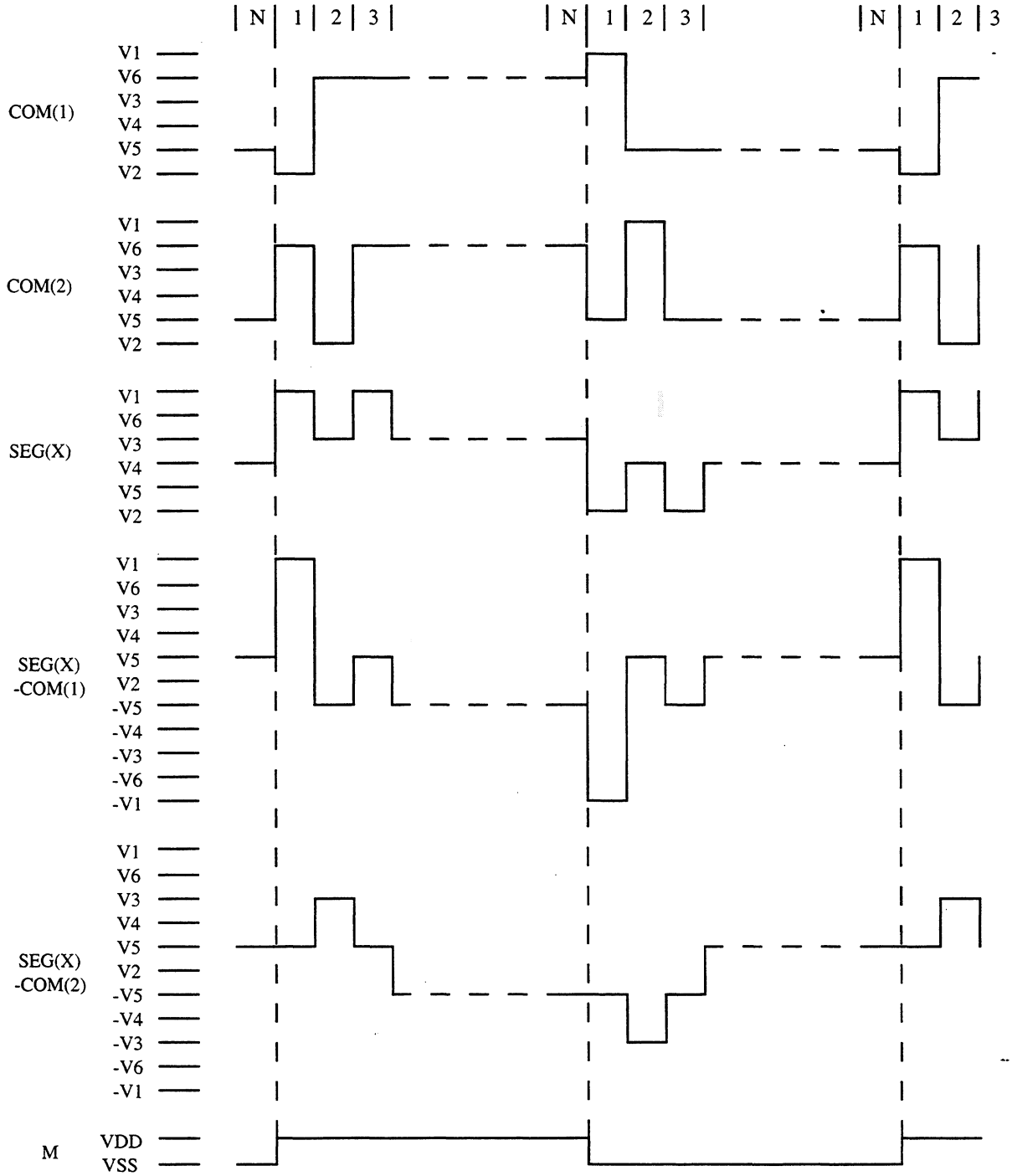
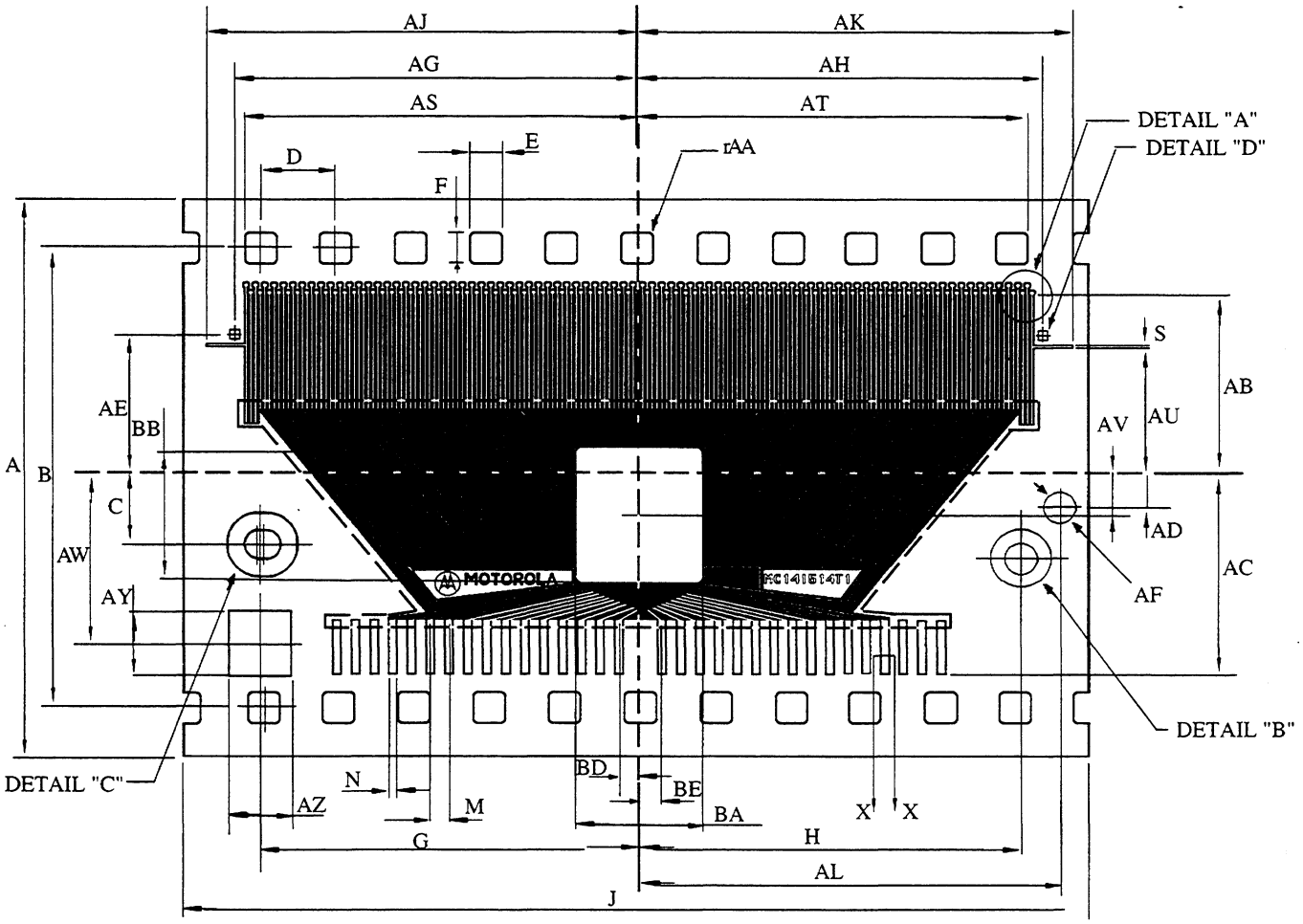
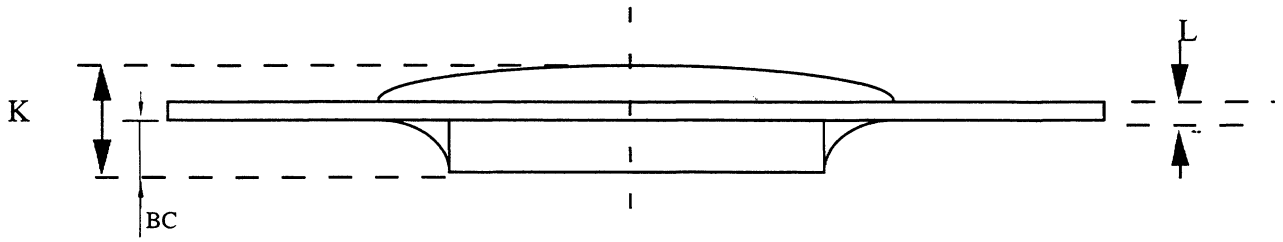


FIGURE 3 - Driving waveforms of 1:N multiplex
(M is used for timing synchronization)

MC141514T1 TAB PACKAGE DIMENSION (1 of 3)

DRAWING IS NOT IN SCALE

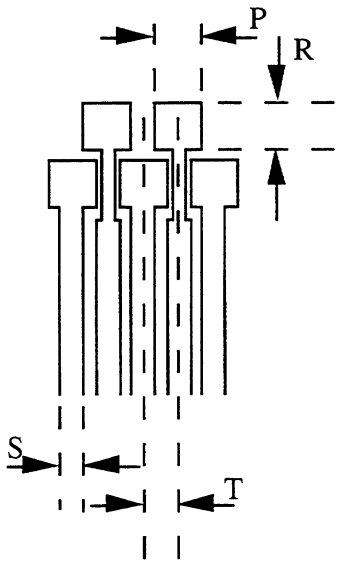




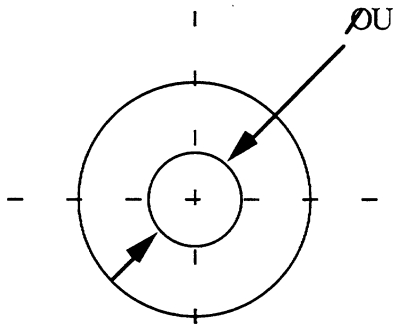
MAGNIFIED VIEW

MC141514T1 TAB PACKAGE DIMENSION (2 of 3)

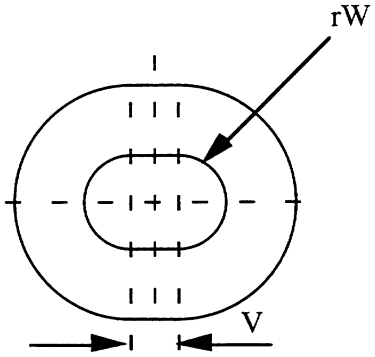
DRAWING IS NOT IN SCALE



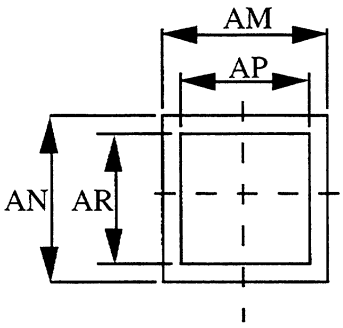
DETAIL 'A'



DETAIL 'B'



DETAIL 'C'



MC141514T1 TAB PACKAGE DIMENSION (3 of 3)

Notes:

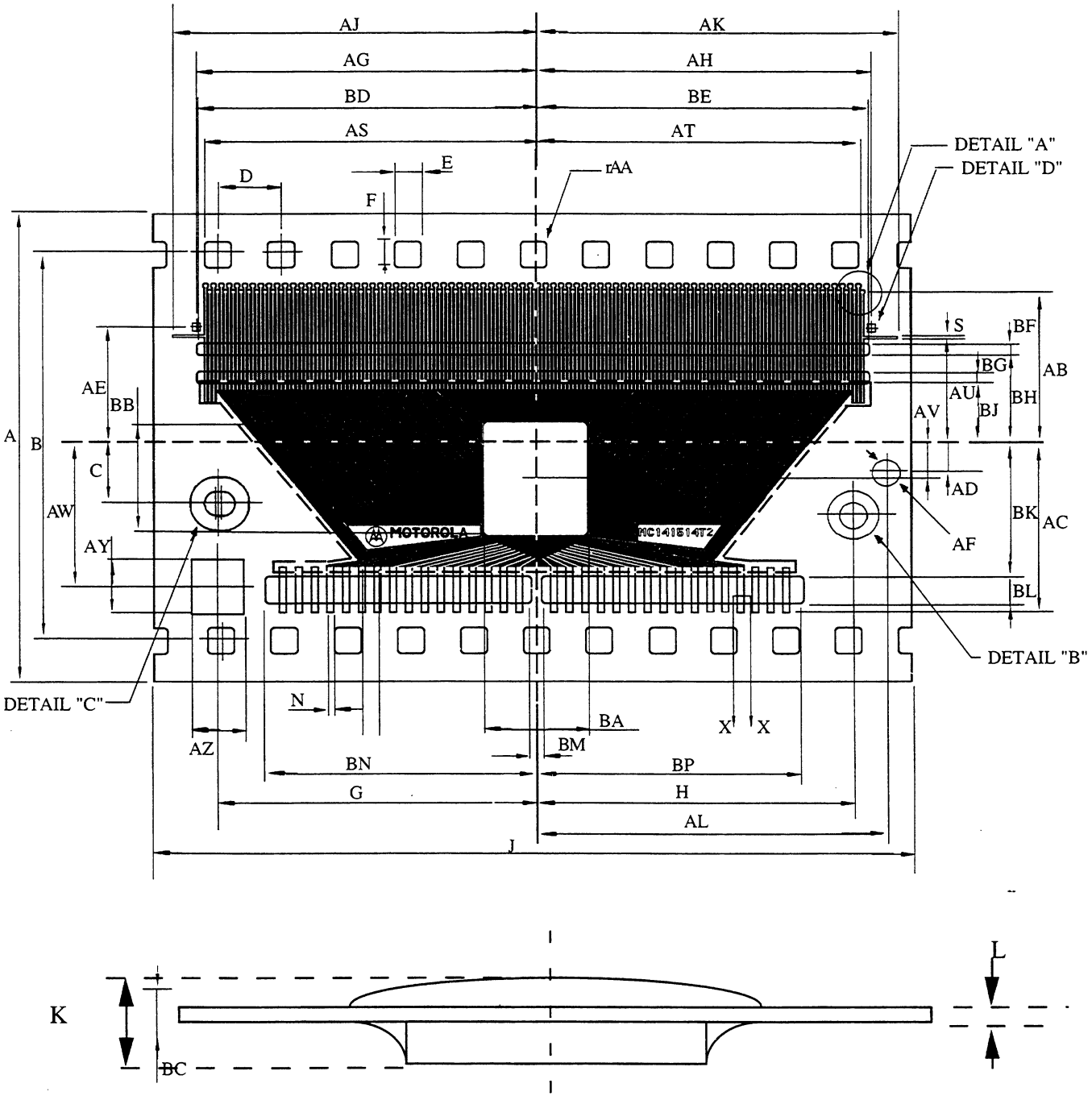
1. Dimensioning and tolerancing per ANSI Y14.5M, 1982.
2. Controlling dimension: millimeter.
3. Copper Thickness : 1 oz
4. Tin Plating Thickness : 0.4um
3. Recommended excise area J x (AB + AC)

	Dim (in mm)		Dim (in inches)	
	min	max	min	max
A	34.775	35.175	1.3691	1.3848
B	28.907	29.017	1.1381	1.1424
C	4.950	5.050	0.1949	0.1988
D	4.720	4.780	0.1858	0.1882
E	1.951	2.011	0.0768	0.0792
F	1.951	2.011	0.0768	0.0792
G	24.200	24.300	0.9528	0.9567
H	24.200	24.300	0.9528	0.9567
J	56.900	57.100	2.2402	2.2480
K	0.686	0.838	0.0270	0.0399
L	0.0675	0.0825	0.0027	0.0033
M	1.190	1.210	0.0469	0.0476
N	0.480	0.520	0.0189	0.0205
P	0.350	0.450	0.0138	0.0177
R	0.350	0.450	0.0138	0.0177
S	0.150	0.190	0.0059	0.0075
T	0.290	0.310	0.0114	0.0122
U	1.750	1.850	0.0689	0.0728
V	0.450	0.550	0.0177	0.0217
W	0.850	0.950	0.0335	0.0374

	Dim (in mm)		Dim (in inches)	
	min	max	min	max
AA	---	0.200	---	0.0079
AB	10.900	11.900	0.4291	0.4685
AC	11.900	12.900	0.4685	0.5079
AD	1.500	2.500	0.0591	0.0984
AE	8.690	8.790	0.3421	0.3461
AF	1.950	2.050	0.0768	0.0807
AG	25.350	25.450	0.9980	1.0020
AH	25.510	25.610	1.0043	1.0083
AJ	27.130	27.230	1.0681	1.0720
AK	27.430	27.530	1.0799	1.0839
AL	26.500	27.500	1.0433	1.0827
AM	0.750	0.850	0.0295	0.0335
AN	0.750	0.850	0.0295	0.0335
AP	0.600	0.700	0.0236	0.0276
AR	0.600	0.700	0.0236	0.0276
AS	24.551	24.649	0.9666	0.9704
AT	24.850	24.950	0.9784	0.9823
AU	7.670	7.770	0.3020	0.3059
AV	2.450	2.550	0.0965	0.1004
AW	10.000	11.000	0.3937	0.4331
AY	3.500	4.500	0.1378	0.1772
AZ	3.500	4.500	0.1378	0.1772
BA	---	10.062	---	0.3961
BB	---	9.747	---	0.3837
BC	0.5794	0.6294	0.0228	0.0248
BD	1.150	1.250	0.0453	0.0492
BE	1.150	1.250	0.0453	0.0492

MC141514T2 TAB PACKAGE DIMENSION (1 of 3)

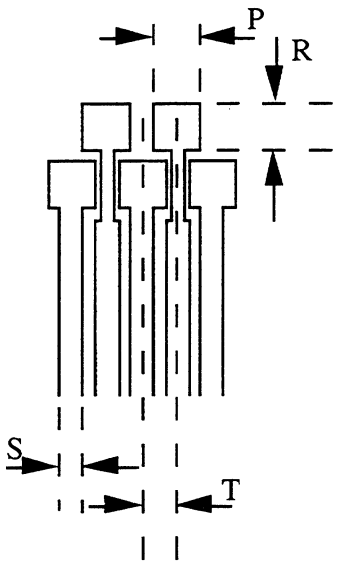
DRAWING IS NOT IN SCALE



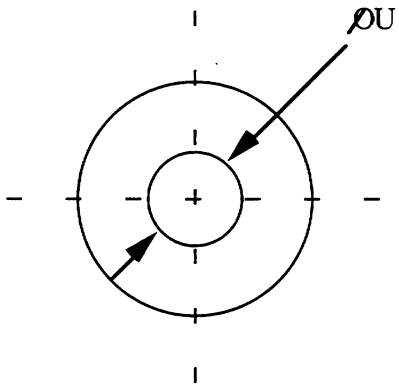
MAGNIFIED VIEW

MC141514T2 TAB PACKAGE DIMENSION (2 of 3)

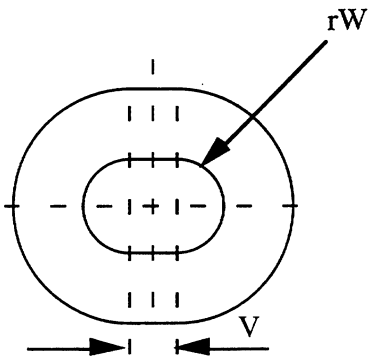
DRAWING IS NOT IN SCALE



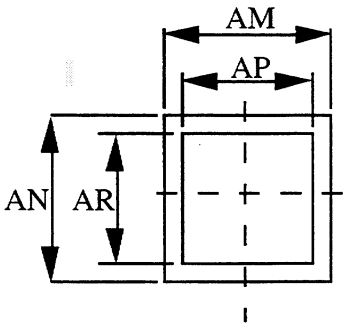
DETAIL 'A'

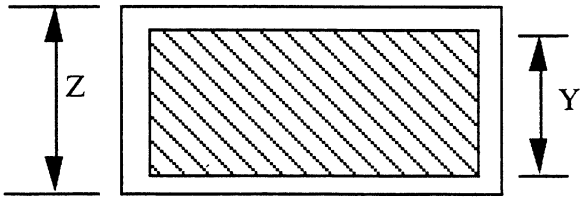


DETAIL 'B'



DETAIL 'C'





SECTION X-X

MC141514T2 TAB PACKAGE DIMENSION (3 of 3)

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M, 1982.

2. Controlling dimension: millimeter.

3. Copper Thickness : 1 oz

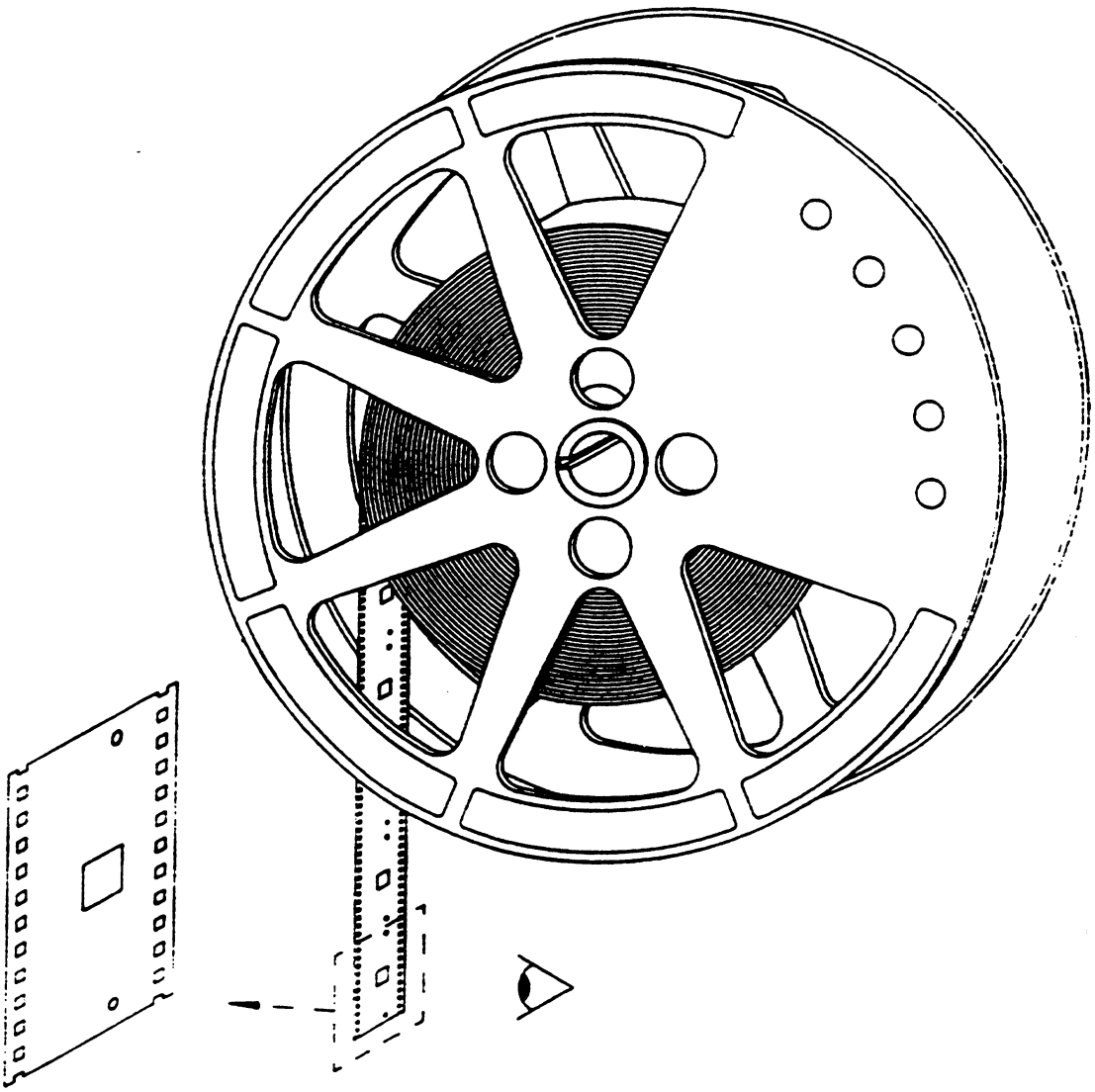
4. Tin Plating Thickness : 0.4um

3. Recommended excise area J x (AB + AC)

	Dim (in mm)		Dim (in inches)	
	min	max	min	max
A	34.775	35.175	1.3691	1.3848
B	28.927	29.027	1.1389	1.1428
C	4.950	5.050	0.1949	0.1988
D	4.720	4.780	0.1858	0.1882
E	1.951	2.011	0.0768	0.0792
F	1.951	2.011	0.0768	0.0792
G	24.200	24.300	0.9528	0.9567
H	24.200	24.300	0.9528	0.9567
J	56.500	57.500	2.2244	2.2638
K	0.686	0.838	0.0270	0.0330
L	0.0675	0.0825	0.0027	0.0032
M	1.190	1.210	0.0469	0.0476
N	0.480	0.520	0.0189	0.0205
P	0.350	0.450	0.0138	0.0177
R	0.350	0.450	0.0138	0.0177
S	0.150	0.190	0.0059	0.0075
T	0.290	0.310	0.0114	0.0122
U	1.750	1.850	0.0689	0.0728
V	0.450	0.550	0.0177	0.0217
W	0.850	0.950	0.0335	0.0374
Y	0.032	0.038	0.0013	0.0015
Z	0.032	0.038	0.0013	0.0015
AA	---	0.20	---	0.0079
AB	10.900	11.900	0.4291	0.4685
AC	11.900	12.900	0.4685	0.5079
AD	1.500	2.500	0.0591	0.0984
AE	8.690	8.790	0.3421	0.3461
AF	1.950	2.050	0.0768	0.0807
AG	25.350	25.450	0.9980	1.0020
AH	25.510	25.610	1.0043	1.0083
AJ	27.130	27.230	1.0681	1.0720
AK	27.430	27.530	1.0799	1.0839
AL	26.500	27.500	1.0433	1.0827

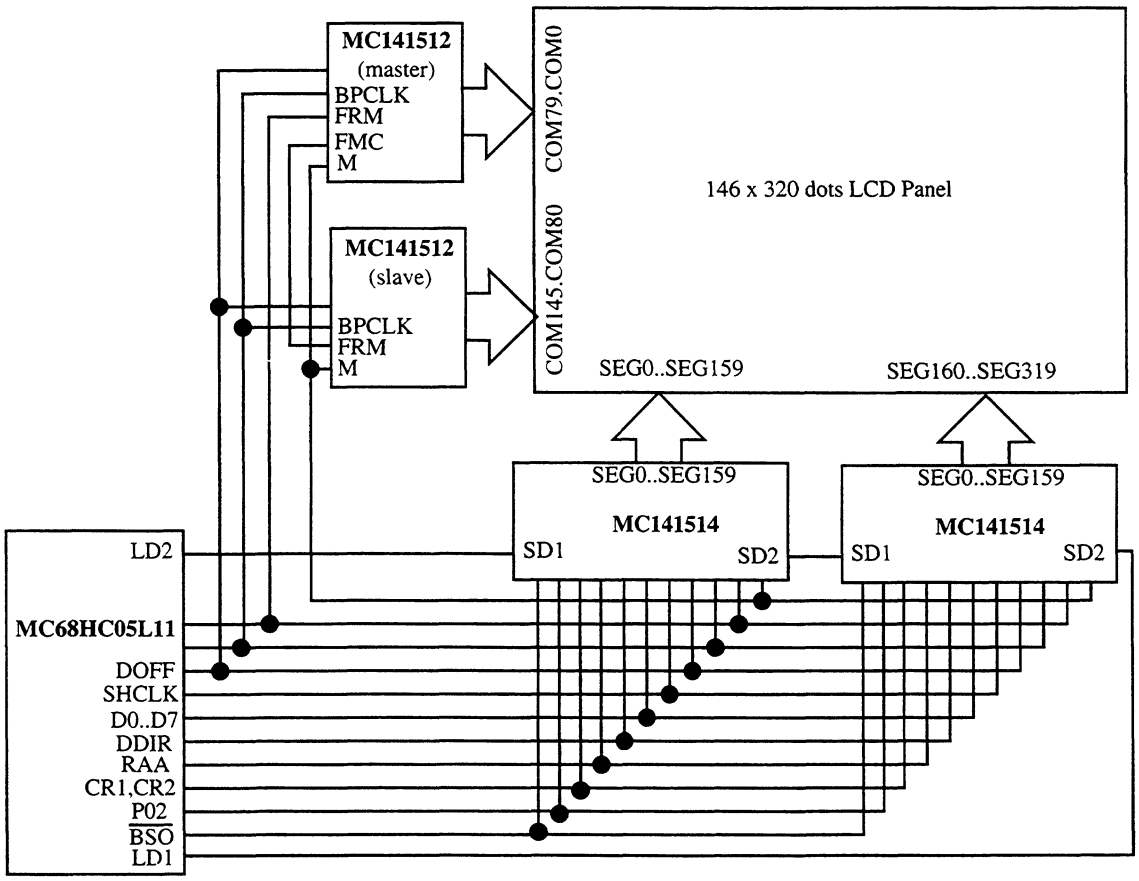
	Dim (in mm)		Dim (in inches)	
	min	max	min	max
AM	0.750	0.850	0.0295	0.0335
AN	0.750	0.850	0.0295	0.0335
AP	0.600	0.700	0.0236	0.0276
AR	0.600	0.700	0.0236	0.0276
AS	24.5508	24.6492	0.9666	0.9704
AT	24.8502	24.9498	0.9784	0.9823
AU	7.937	8.037	0.3125	0.3164
AV	2.450	2.550	0.0965	0.1004
AW	10	11	0.3937	0.4331
AY	3.500	4.500	0.1378	0.1772
AZ	3.500	4.500	0.1372	0.1772
BA	---	10.062	---	0.3961
BB	---	9.747	---	0.3837
BC	0.5794	0.6294	0.0228	0.0248
BD	25.200	25.300	0.9921	0.9961
BE	25.500	25.600	1.0039	1.0079
BF	0.850	0.950	0.0335	0.0374
BG	0.850	0.950	0.0335	0.0374
BH	6.850	6.950	0.2697	0.2736
BJ	4.750	4.850	0.1870	0.1909
BK	9.750	9.850	0.3839	0.3878
BL	1.950	2.050	0.0768	0.0807
BM	0.750	0.850	0.0295	0.0335
BN	20.450	20.550	0.8051	0.8091
BP	20.450	20.550	0.8051	0.8091
BR	1.15	1.25	0.0453	0.0492
BS	1.15	1.25	0.0453	0.0492

TAB TAPE REEL ORIENTATION

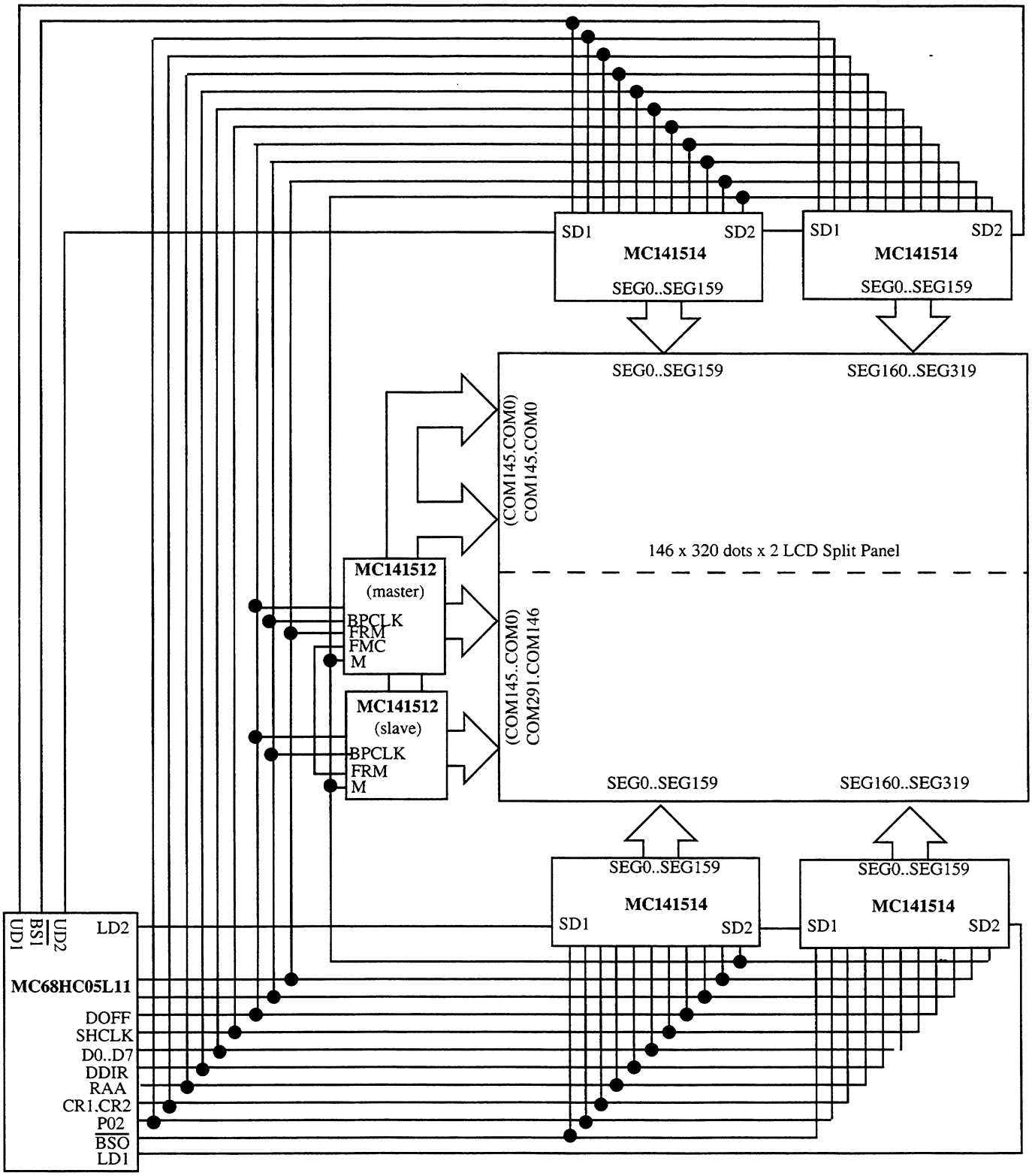


TYPICAL APPLICATIONS

146 x 320 SINGLE PANEL LCD SYSTEM WITH MC68HC05L11



146 x 320 x 2 SPLIT PANEL LCD SYSTEM WITH MC68HC05L11



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

APR 94 REV 2.2

Product Preview

LCD Segment Driver

MC141518

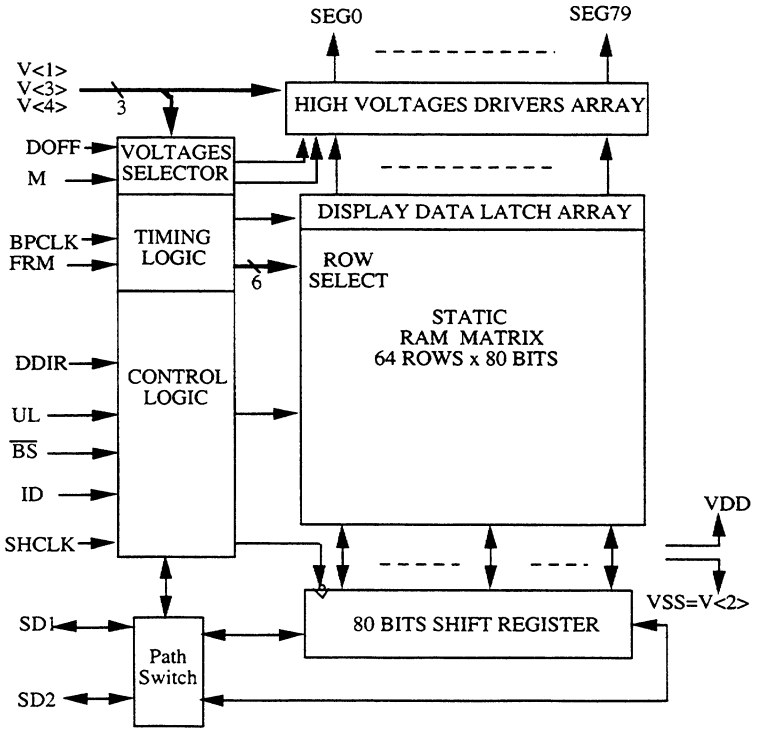
PACKAGE	PART NO.
QFP	XC141518FJ
DIE	XCC141518

The Segment Driver is a CMOS device which consists of 64 rows by 80 bits of static RAM for display. It is a companion chip of MC141516FJ Backplane Driver for 64 MUX or lower LCD panel. It can be directly connected to the display controller inside the Motorola's microcomputer MC68HC05L11.

FEATURES

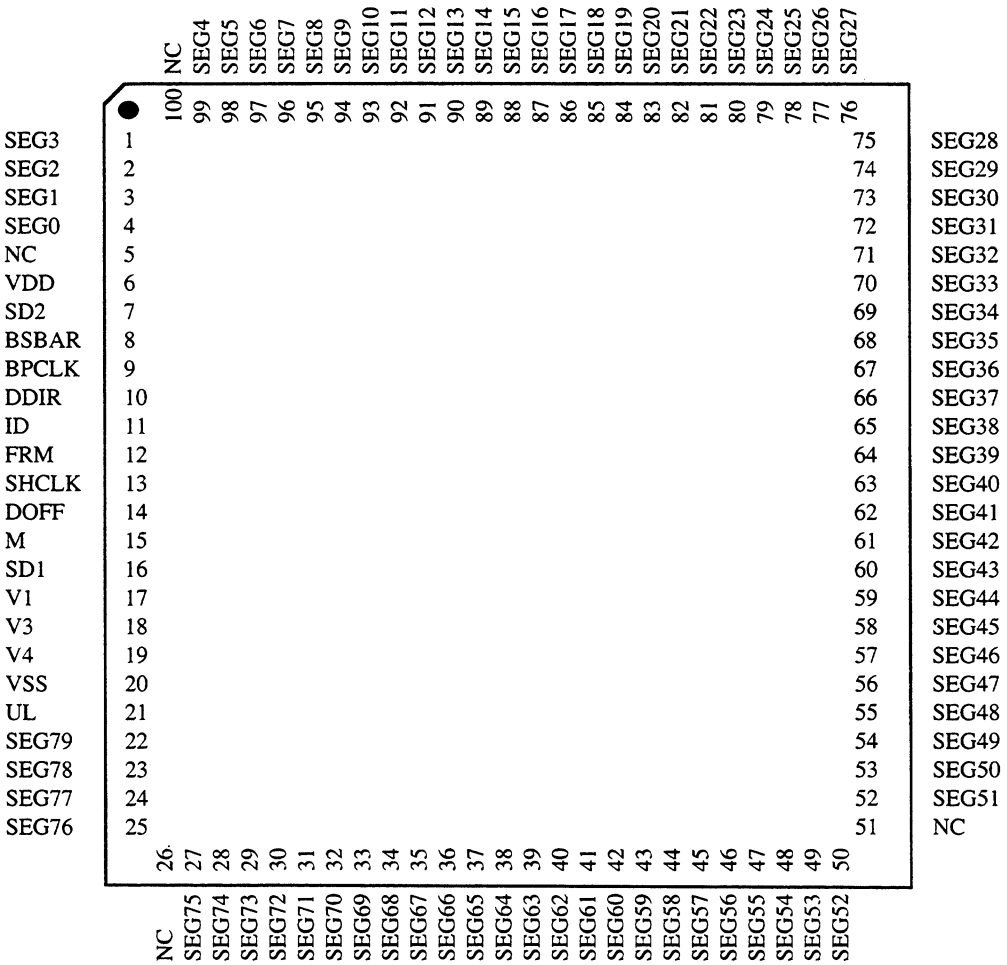
- 80 LCD segment driving signals
- Casadable for more LCD segment driving outputs
- Serial interface (SPI like) for both display data and control instruction transfers
- Selectable bias ratio up to 1:9
- Selectable multiplex ratio up to 64
- 100-pin QFP

BLOCK DIAGRAM



This document contains infomation on a new product. Specifications and information herein are subject to change without notice.

MOTOROLA



MC141518FJ Pin Assignment

MAXIMUM RATINGS* (Voltages Referenced to V_{SS}, T_A = 25°C)

Ratings	Symbol	Value	Unit
Supply Voltage	VDD	-0.3 to + 7.0	V
	V<1>	VSS-0.3 to VSS+15	V
Input Voltage	Vin	VSS-0.3 to VDD +0.3	V
Current Drain Per Pin Excluding VDD and VSS	I	25	mA
Operating Temperature Range	TA	0 to 70	°C
Storage Temperature Range	Tstg	-65 to + 150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions to be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that Vin and Vout be constrained to the range VSS < or = (Vin or Vout) < or = VDD. Reliability of operation is enhanced if unused input are connected to an appropriate logic voltage level (e.g., either VSS or VDD). Unused outputs must be left open.

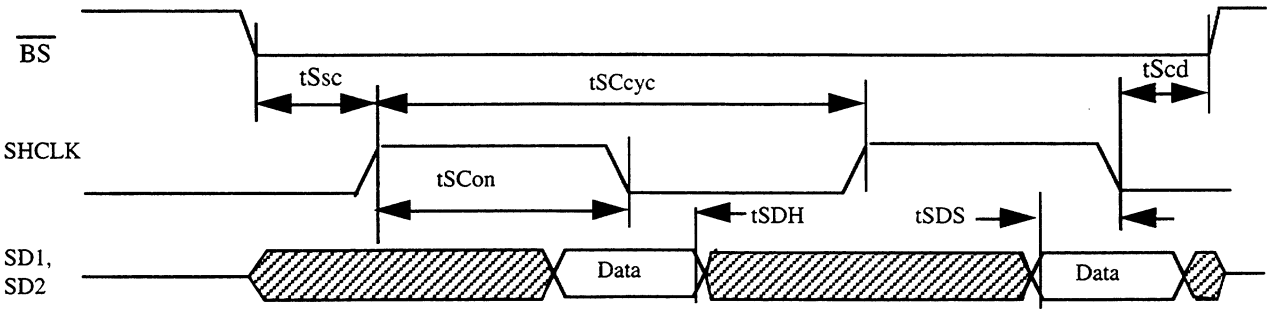
ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS}, T_A = 25°C, VDD = 5.0V)

Characteristis	Symbol	Min	Typ	Max	Unit
Input High Voltage BPCLK, FRM, M, ID, DDIR, $\overline{BS}$, SD1,SD2, SHCLK, DOFF	VIH	0.7xVDD	-	VDD	V
Input Low Voltage BPCLK, FRM, M, ID,DDIR, $\overline{BS}$, SD1,SD2, SHCLK, DOFF	VIL	VSS	-	0.3xVDD	V
Data Retention	VR	2.0	-	-	V
Input Current BPCLK, FRM, M, ID,DDIR, $\overline{BS}$, SD1,SD2, SHCLK, DOFF	Iin	-	-	±1	uA
Capacitance BPCLK, FRM, M, ID,DDIR, $\overline{BS}$, SD1,SD2, SHCLK, DOFF	Cin	- -	- -	8	pF
Output High Voltage SD1,SD2	VOH	0.8xVDD	-	VDD	V
Output Low Voltage SD1,SD2	VOL	VSS	-	0.2xVDD	V
Operating Voltages Supply Voltage (referenced to VSS)	VDD	4.5	-	5.5	V
LCD Voltage (referenced to VSS)	V<1>	0.0	-	+13.0	V
Operating supply current VDD (VDD = 5 V)					
Dynamic Mode (Display on, R/W access)	IACC	-	200	-	uA
(Display on, R/W disable)	IDP	-	20	-	uA
Standby Mode (Display off, R/W disable)	ISB	-	5	-	uA
Operating supply current V<1> (V<1> = 13V)					
Display Mode	ILDP	-	30	-	uA
Standby Mode	ILSB	-	2	-	uA

AC OPERATION CONDITIONS AND CHARACTERISTICS

(VCC = 5.0 V +/- 5%, VSS = 0)

Characteristics	Symbol	Min	Max	Unit
Shift Clock Cycle Time	tSCcyc	200	-	ns
Shift Clock On Time	tSCon	100	-	ns
Serial Data Setup Time	tSDS	50	-	ns
Serial Data Hold Time	tSDH	10	-	ns
Select to clock on	tSsc	100	-	ns
Clock on to device disable	tSsc	10	-	ns



Serial Access Timing (with $\overline{BS}$ = 0)

PIN DESCRIPTION

VDD and VSS

Power is supplied to the driver using these two pins. VDD is power and VSS is ground.

V<1>,V<3>,V<4>

These are the levels of voltage from the voltages generator (Fig. 2).

DOFF

This is an output pin from the microcomputer to signal the segment driver to turn off LCD.

FRM

A periodic active high output from the microcomputer to segment driver for frame timing synchronisation. This pin is connected either to FRM of the microcomputer MC68HC05L11 or to FRM of the Backplane MC141516.

BPCLK

A periodic output from the microcomputer to segment driver for timing synchronisation. This pin is connected either to BPCLK of the microcomputer MC68HC05L11 or to BPCLK of the Backplane MC141516.

SEG0-SEG79

These 80 output lines provide the segment driving signal to the LCD panel. They are all high impedance while the display is turned off (i.e. DOFF is selected).

$\overline{BS}$

This is the Bank Select pin. It is an active low input for chip enable.

UL

This pin is used to configure the segment driver to support the Upper or Lower panel for a split LCD panel system. Since any segment driver to the upper panel will be 180 deg rotated with respect to the lower panel's segment drivers, to maintain easier routing and consistent in data format, the serial data direction has to be reversed. Therefore whenever UL is tied high, the serial data direction inside the segment drivers will be reversed with respect to the serial data direction as UL is ground. Details about the serial data direction can be found in the SD1, SD2 description.

SD1, SD2

These pins are two bidirectional serial data lines connected to either one of the two serial ports of the microcomputer MC68HC05L11 (UD1, UD2 LD1 and LD2) depending on the UL pin. If the segment driver is configured to serve the upper panel with its UL tied high, serial data direction between SD1 and SD2 is reversed. In such case, SD1 is connected either to UD1 or to LD1 of MC68HC05L11. SD2 is then connected to UD2 or LD2 of MC68HC05L11. However, if the UL pin is ground, SD1 and SD2 are then connected to UD2 or LD2 and to UD1 or LD1 of MC68HC05L11 respectively. SD1 and SD2 allow the display data or instruction from the microcomputer entering the segment driver in both directions. During $\overline{BS}$ high, these two pins are high impedance In case of an instruction from the microcomputer with ID pin set. SD1 and SD2 are disconnected from the 80-bit shift register and form a transparent loop. Instruction bits entering the segment through a serial port (say SD1) are exported to its cascading device immediately through another serial port (i.e. SD2). In such a way, this instruction from the microcomputer can be boardcasted to a bank of cascading segments. See Typical Application Section for typical system connections.

ID

This is the Instruction/Data pin. If this pin is set, an instruction byte is shifting in from the bidirectional data lines as soon as $\overline{BS}$ goes low. Otherwise, data in the bidirectional lines is the display data. (See SD1 and SD2 definitions). Instructions are described in Table 2.

Though each instruction has eight bits, the segment needs 12 SHCLK cycles to complete it. Eight cycles to fill in the internal instruction register and the last four cycles are for instructions processing. Once the instruction is completed, additional SHCLK is ignored until $\overline{BS}$ signal toggles from high to low again. See Figure 1 for details. Notice that internal sampling for the instruction register should be as the order of MSB to LSB if DDIR is 0 and LSB to MSB if DDIR is 1, doesn't matter what UL is.

SHCLK

This is the shift clock from the microcomputer MC68HC05L11 to the segment for clocking the serial data on SD1 and SD2.

DDIR

It is an input from the MCU to the segment dirver specifying the direction of the serial data. DDIR definition is also affected by UL pin as specified in Table 2. If UL pin is found low and DDIR is set, the serial data enters the segment driver through SD1 and leaves the segment driver through SD2. If both UL and DDIR are zeroes, SD1 and SD2 are redefined as output and input respectively. If UL pin is high and DDIR is set, the serial data then enters the segment driver through SD2 and leaves the segment driver through SD1. If UL is high but DDIR is clear, SD2 and SD1 are output and input respectively.

UL	DDIR	Internal Serial Data Direction
0	0	—SD2—bidirectional shifter register—SD1→
0	1	←SD2—bidirectional shifter register—SD1–
1	0	←SD2—bidirectional shifter register—SD1–
1	1	—SD2—bidirectional shifter register—SD1→

Table 1. Summary Of Data Direction Flow Responding To DDIR and UL bit.

OPERATION OF LCD DRIVER

INTRODUCTION

LCD segment driver can be hardware-configured from 1:6 bias (for 32 mux) to 1:9 bias (for 64 mux), depending on the voltage divider ratio of Fig.2. The ratio of bias or the contrast ratio (a) is defined as

$$1 : \frac{4 \times R1 + R2}{R1} = 1 : a$$

As the multiplex ratio changes, the ratio of bias has to be changed accordingly. The ratio of bias relates to the multiplex ratio as

$$a = \sqrt{mux} + 1.$$

To set up a multiplex ratio, please refer to either **Section 6.2.5.**, the Product Preview of MC68HC05L11 or the Product Preview of the Backplane MC141516.

CONTROL LOGIC produces the control signals necessary for display RAM read/write and serial data latching. This Control Logic can be controlled by the MCU through the serial interface with ID set. MCU writing a byte of instruction (ID7 to ID0) to the Segment Control Register through the serial interface will cause Segment driver(s) to carry functions as shown as Table 2.

ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
0	0	ROW ADDRESS (WRITE IN)					
0	1	ROW ADDRESS (READ FROM)					
1	0	SCROLL UP ADVANCE					
1	1	X	X	X	CLR SH	UL	RESET

TABLE 2. A Summary of the Control Functions of Segment Driver

ROW ADDRESS(WRITE IN) instruction causes Segment driver(s) to load the content of the 80 BITS SHIFT REGISTER into a row of RAM which address is specified by ID5 to ID0.

ROW ADDRESS(READ FROM) instruction causes Segment driver(s) to copy a row of RAM which address is specified by ID5 to ID0 into the 80 BITS SHIFT REGISTER.

SCROLL UP ADVANCE instruction causes Segment driver(s) to do a vertical scroll up or down. The content of ID5 to ID0 only represents the vertical offset of the new screen to the current screen. This vertical offset presenting in the Data Bus then is added up with an old offset which is stored in a register called the VERTICAL SCROLL VECTOR REGISTER. The sum of these is the new offset and will be stored in the VERTICAL SCROLL VECTOR REGISTER. Periodically content of this register will be fetched and loaded into a presettable counter in the TIMING LOGIC to generate the row addresses for screen refreshing. The VERTICAL SCROLL VECTOR REGISTER is default zero during power-on.

RESET BIT0 Writing an "1" to this bit will clear the VERTICAL SCROLL VECTOR REGISTER and the UL bit.

CLRSH BIT2 Writing an "1" to this bit will clear the content of the 80 BITS SHIFT REGISTER.

An instruction (ID7 to ID0) is transferred to the segment driver through the serial interface as Figure 1 demonstrated. Figure 1-a shows a case that the DDIR bit is clear. The most significant bit ID7 of the instruction will come in as the first bit. After 8 SHCLK cycles, a byte of instruction data is kept in an instruction register. However, the instruction needs another 3 cycles to complete, as long as $\overline{BS}$ holds low, segment driver will Figure 1. The order of Instruction byte shifted wait for these 3 cycles to complete the instruction. After the instruction, the segment driver will ignore any coming SHCLK cycle until the signal $\overline{BS}$ toggles from high to low again. Figure 1-b shows in case of DDIR bit set. The UL bit will not affect the order of instruction shifting. For most case, user does not need to worry about the order of shifting if the segment is connected to the display controller in the microcomputer MC68HC05L11.

TIMING LOGIC, according to BPCLK and FRM, fills the DISPLAY DATA LATCH ARRAY with rows of RAM matrix's content periodically starting from the row address specified in the VERTICAL SCROLL VECTOR REGISTER.

VOLTAGES SELECTOR consists of switching circuit to select appropriate voltage levels from external voltage divider. (See Fig. 2).

DISPLAY DATA LATCH ARRAY is used to buffer up a row of display data from RAM.

STATIC RAM MATRIX consists of 64 rows x 80 bits of SRAM cell. The content of these RAM cells can be altered by read/write from/to the shift register by accessing the command register through the serial interface.

HIGH VOLTAGE DRIVERS ARRAY is a row of high voltage drivers connecting to segment lines of any LCD panel. The output waveform of the high voltage driver is shown as Seg(x) in Fig. 3.

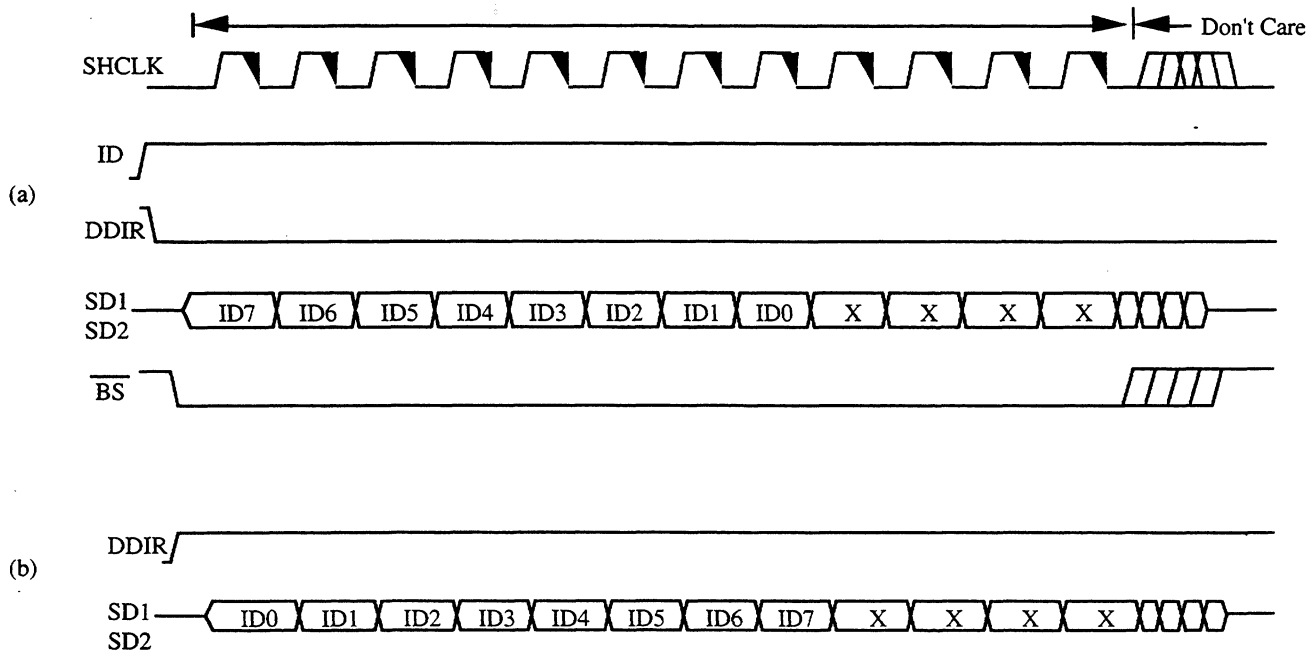


Figure 1. The order of Instruction byte shifted

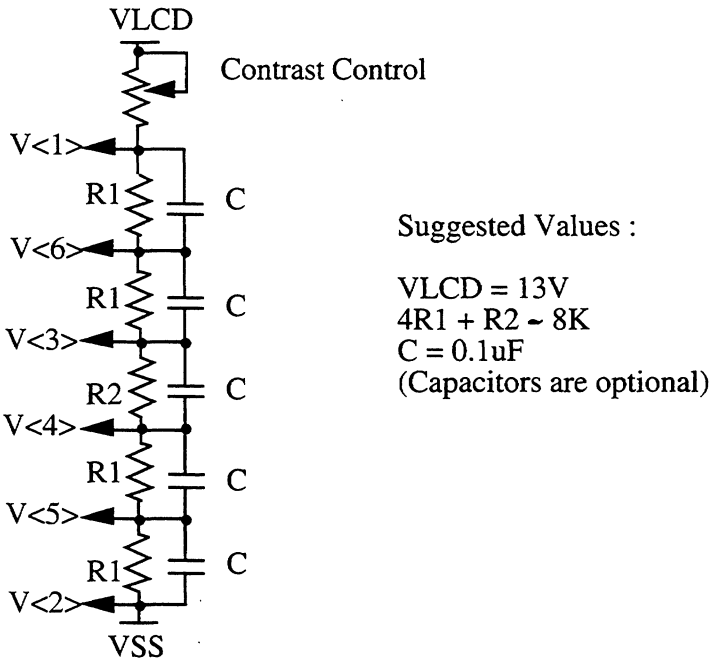


FIG.2 External Voltage Divider

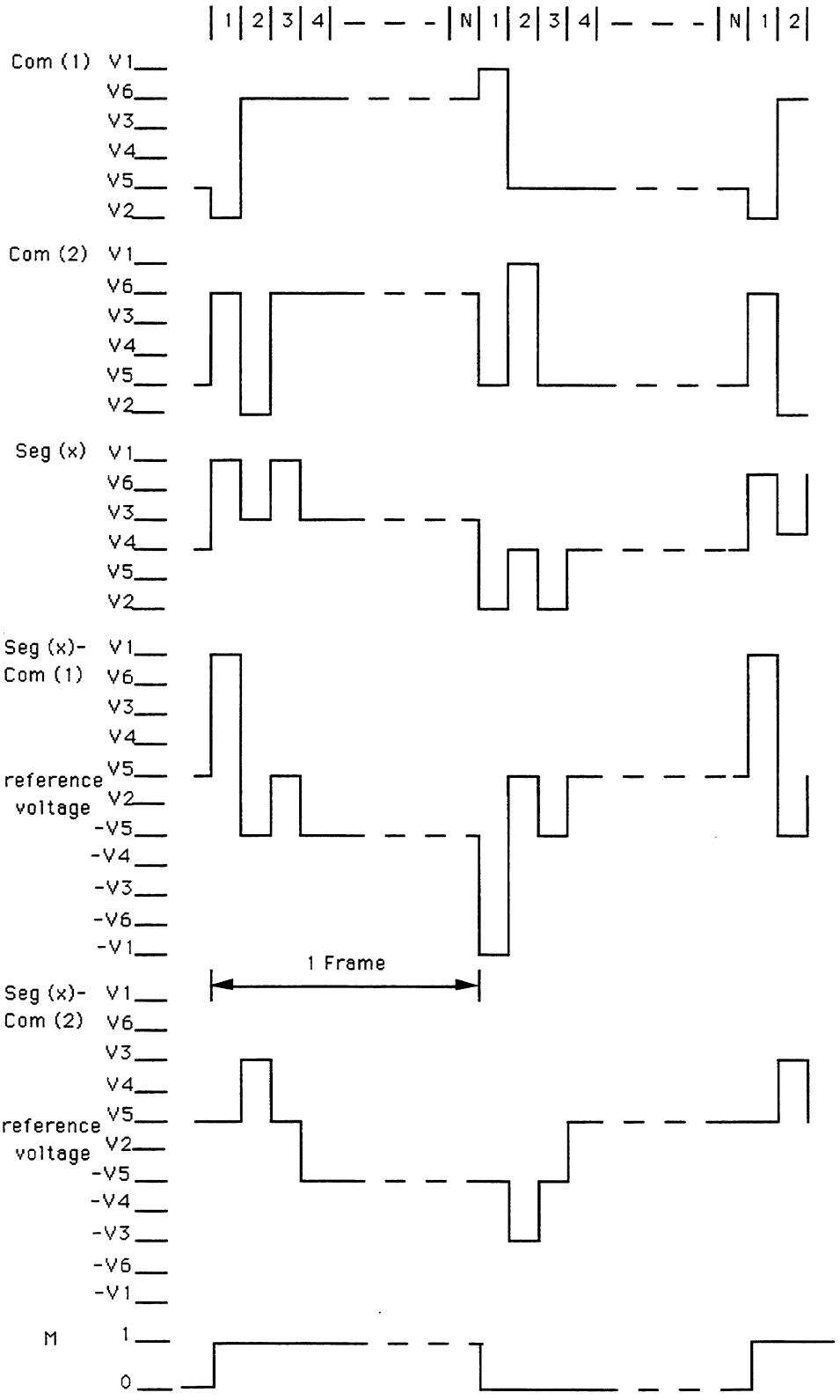
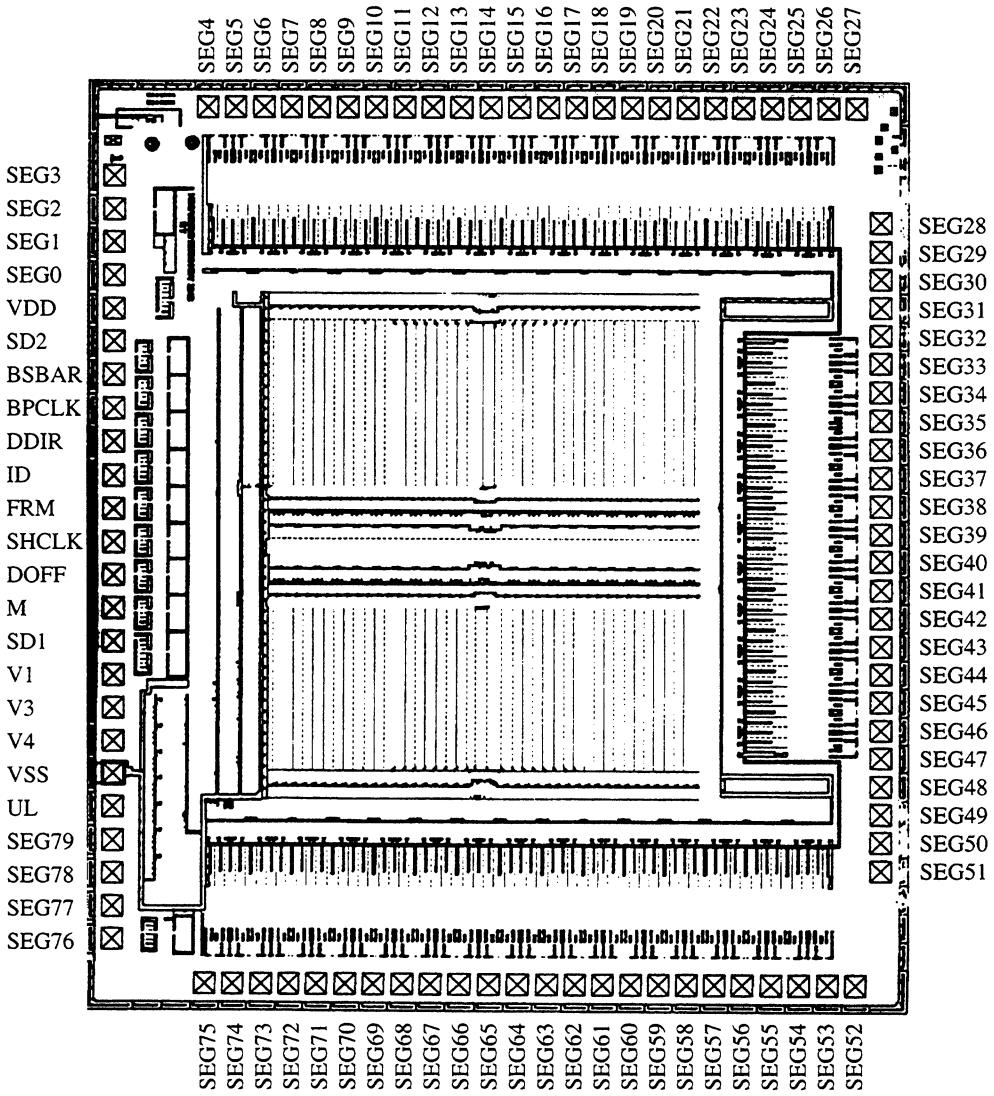


FIG. 3 Driving waveforms of 1:N multiplex

MCC141518 PIN ASSIGNMENT



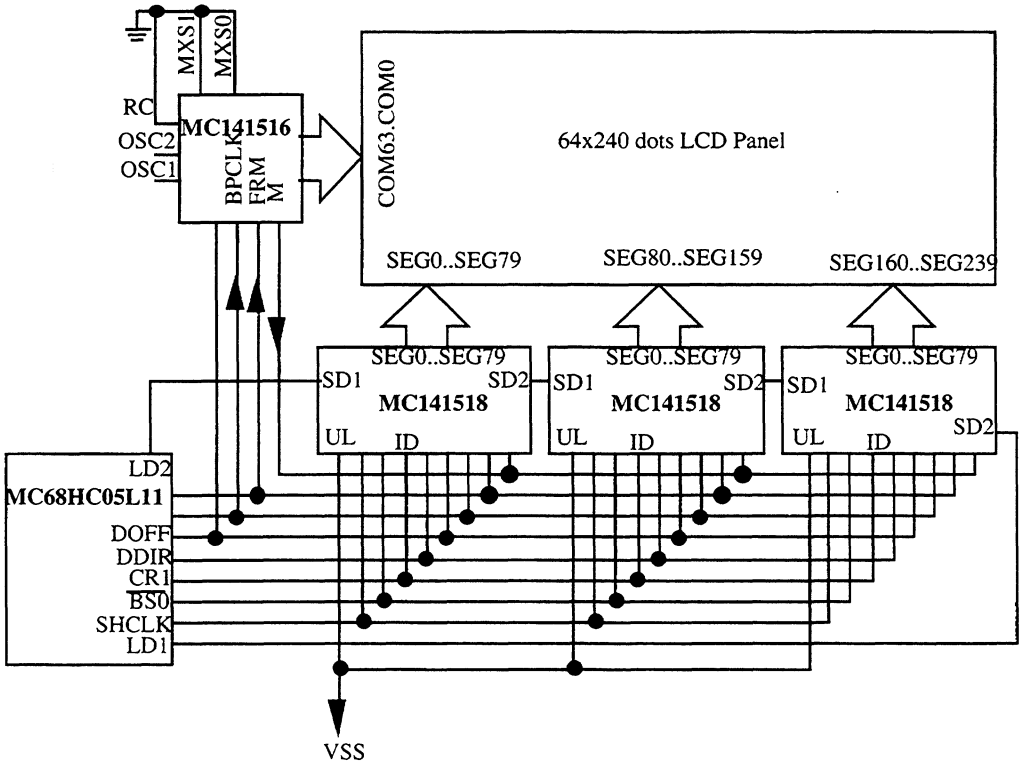
MCC141518 PAD COORDINATES : (UNIT : UM)

PIN NAME	X	Y	PIN NAME	X	Y
SEG3	-2294.9	-2373.1	SEG28	-2012.4	2373.1
SEG2	-2088.6	-2373.1	SEG29	-1837.4	2373.1
SEG1	-1882.4	-2373.1	SEG30	-1662.4	2373.1
SEG0	-1676.1	-2373.1	SEG31	-1487.4	2373.1
VDD	-1469.9	-2373.1	SEG32	-1312.4	2373.1
SD2	-1263.6	-2373.1	SEG33	-1137.4	2373.1
BSBAR	-1057.4	-2373.1	SEG34	-962.4	2373.1
BPCLK	-851.1	-2373.1	SEG35	-787.4	2373.1
DDIR	-644.9	-2373.1	SEG36	-612.4	2373.1
ID	-438.6	-2373.1	SEG37	-437.4	2373.1
FRM	-232.4	-2373.1	SEG38	-262.4	2373.1
SHCLK	-26.1	-2373.1	SEG39	-87.4	2373.1
DOFF	180.1	-2373.1	SEG40	87.6	2373.1
M	386.4	-2373.1	SEG41	262.6	2373.1
SD1	592.6	-2373.1	SEG42	437.6	2373.1
V1	798.9	-2373.1	SEG43	612.6	2373.1
V3	1005.1	-2373.1	SEG44	787.6	2373.1
V4	1211.4	-2373.1	SEG45	962.6	2373.1
VSS	1417.6	-2373.1	SEG46	1137.6	2373.1
UL	1623.9	-2373.1	SEG47	1312.6	2373.1
SEG79	1830.1	-2373.1	SEG48	1487.6	2373.1
SEG78	2036.4	-2373.1	SEG49	1662.6	2373.1
SEG77	2242.6	-2373.1	SEG50	1837.6	2373.1
SEG76	2448.9	-2373.1	SEG51	2012.6	2373.1

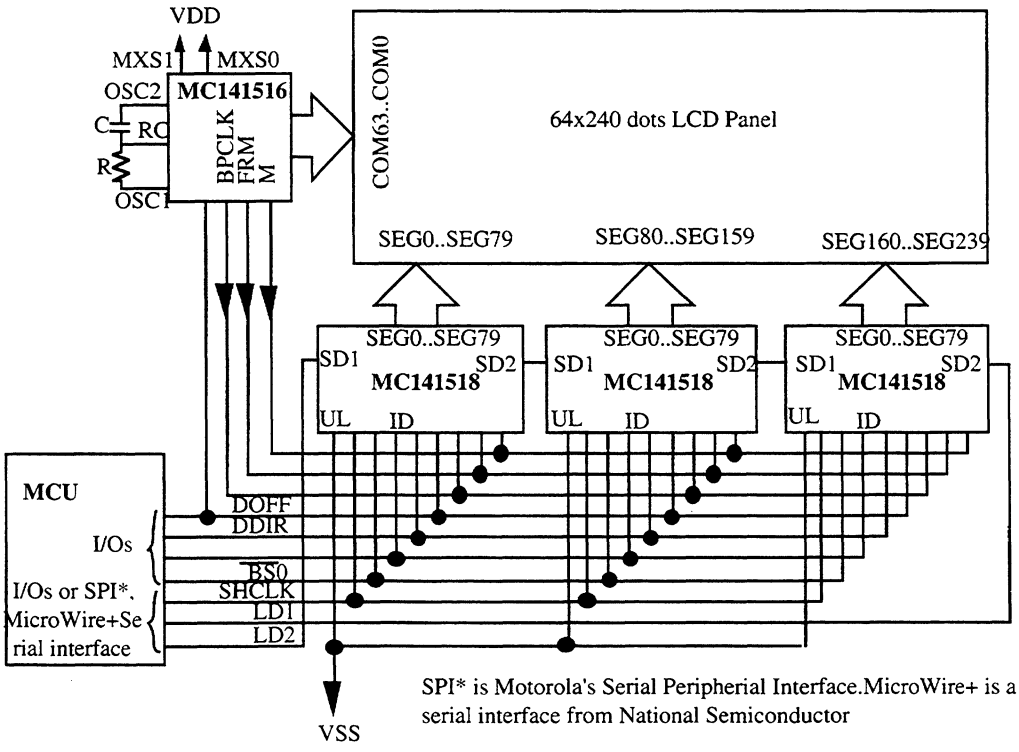
PIN NAME	X	Y	PIN NAME	X	Y
SEG4	-2724.9	-1803.1	SEG75	2725.1	-1803.1
SEG5	-2724.9	-1628.1	SEG74	2725.1	-1628.1
SEG6	-2724.9	-1453.1	SEG73	2725.1	-1453.1
SEG7	-2724.9	-1278.1	SEG72	2725.1	-1278.1
SEG8	-2724.9	-1103.1	SEG71	2725.1	-1103.1
SEG9	-2724.9	-928.1	SEG70	2725.1	-928.1
SEG10	-2724.9	-753.1	SEG69	2725.1	-753.1
SEG11	-2724.9	-578.1	SEG68	2725.1	-578.1
SEG12	-2724.9	-403.1	SEG67	2725.1	-403.1
SEG13	-2724.9	-228.1	SEG66	2725.1	-228.1
SEG14	-2724.9	-53.1	SEG65	2725.1	-53.1
SEG15	-2724.9	121.9	SEG64	2725.1	121.9
SEG16	-2724.9	296.9	SEG63	2725.1	296.9
SEG17	-2724.9	471.9	SEG62	2725.1	471.9
SEG18	-2724.9	646.9	SEG61	2725.1	646.9
SEG19	-2724.9	821.9	SEG60	2725.1	821.9
SEG20	-2724.9	996.9	SEG59	2725.1	996.9
SEG21	-2724.9	1171.9	SEG58	2725.1	1171.9
SEG22	-2724.9	1346.9	SEG57	2725.1	1346.9
SEG23	-2724.9	1521.9	SEG56	2725.1	1521.9
SEG24	-2724.9	1696.9	SEG55	2725.1	1696.9
SEG25	-2724.9	1871.9	SEG54	2725.1	1871.9
SEG26	-2724.9	2046.9	SEG53	2725.1	2046.9
SEG27	-2724.9	2221.9	SEG52	2725.1	2221.9

TYPICAL APPLICATIONS

64X240 SINGLE PANEL LCD SYSTEM WITH MC68HC05L11

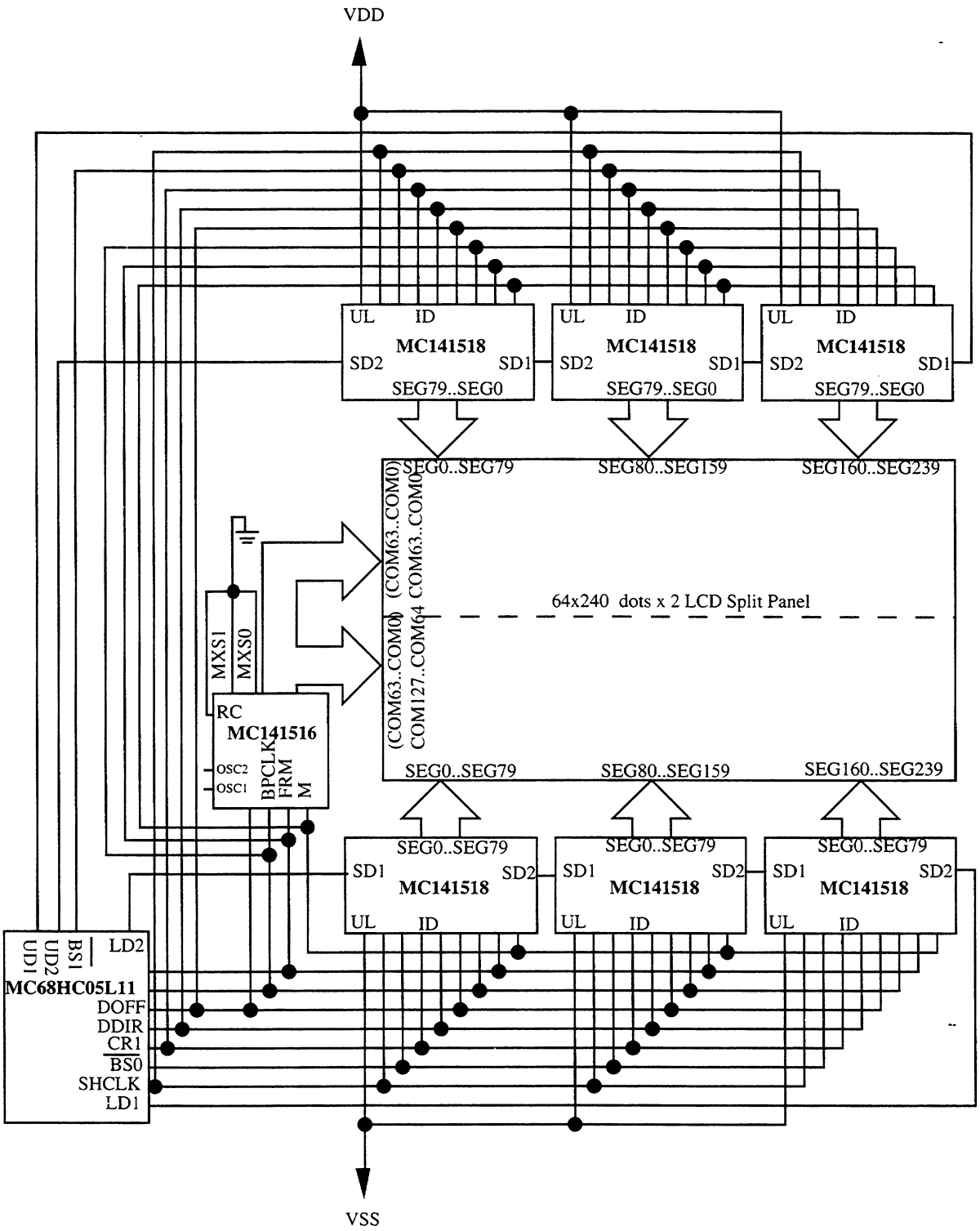


64x240 SINGLE PANEL LCD SYSTEM WITH OTHER MCU



SPI* is Motorola's Serial Peripherial Interface.MicroWire+ is a serial interface from National Semiconductor

64x240x2 SPLIT PANEL LCD SYSTEM



APPENDIX B
BACKPLANE DRIVERS

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

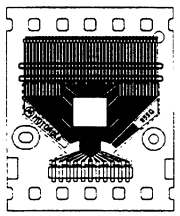
REV2.4 APR 94

MC141512
MC141515

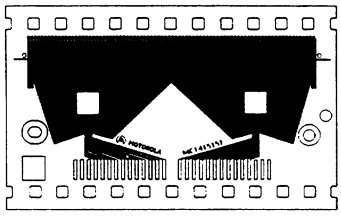
Product Preview

LCD Backplane Driver

The MC141512 and the MC141515 are CMOS chips . They are companion chips to MC141514 segment driver for large LCD panels. ALL these drivers are controlled by the MC68HC05L11 microcomputer. The MC141512 provides 80 high voltage LCD driving signals whereas the MC141515 provides 160 high voltage LCD driving signals.
The MC141515 is the twin die version of the MC141512.



MC141512T1



MC141515T

FEATURES

- : 80(512) / 160(515) LCD blackplane driving signals
- : Expansion to higher driver count by cascade
- : Serial data interface with MC68HC05L11
- : 1:5 to 1:13 bias
- : Selectable multiplex ratio from 16 to 146
- : 91(512) / 182(515) -pin TAB

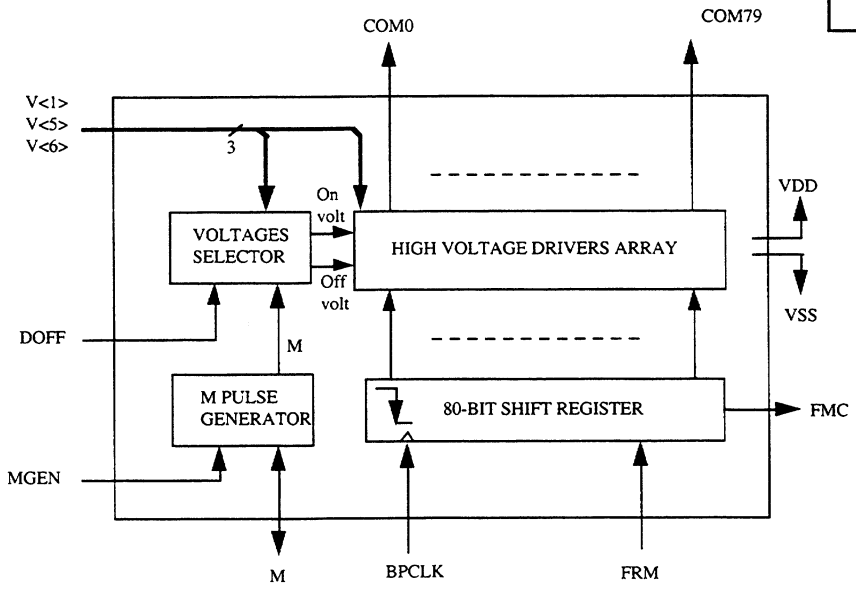
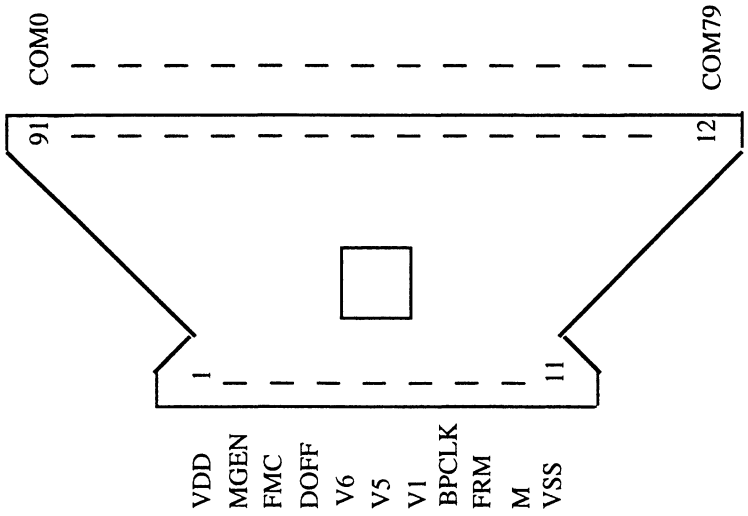


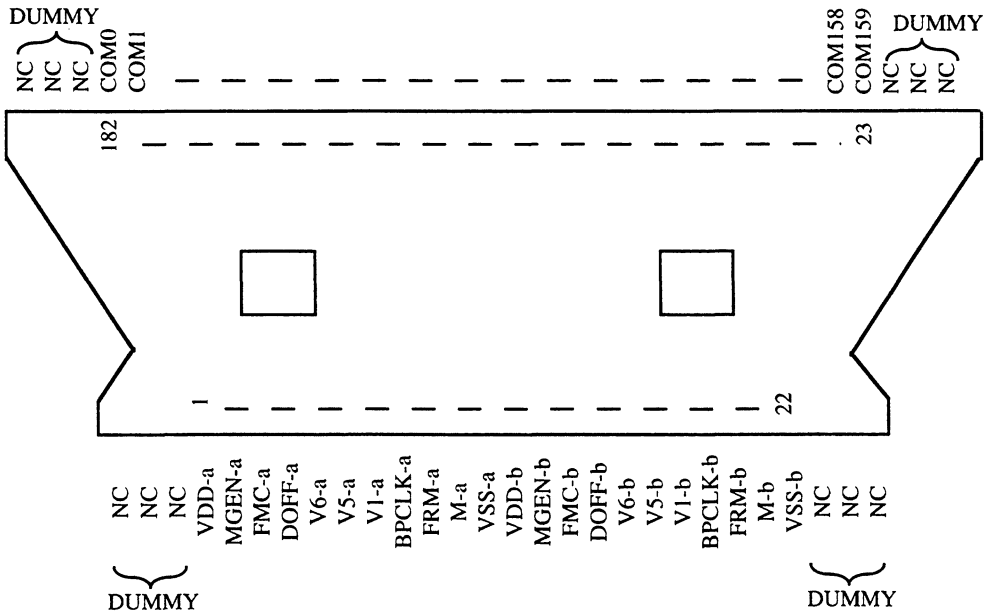
FIG.1 LCD Backplane Driver Functional Block Diagram

This document contains infomation on a new product. Specifications and information herein are subject to change without notice.

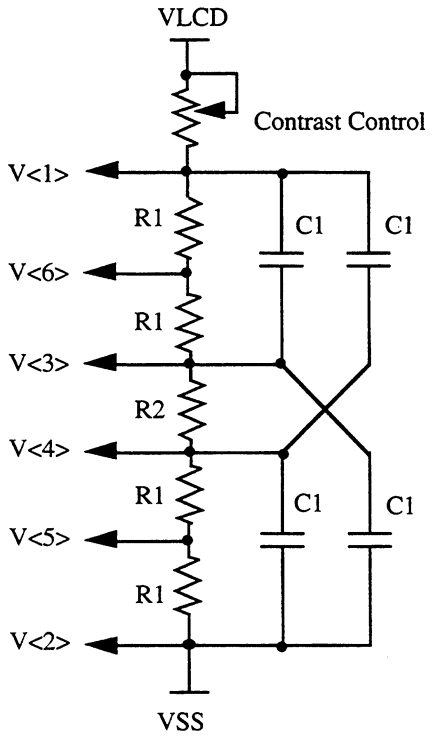
MOTOROLA



MC141512T1 Pin Assignment (copper view)



MC141515T Pin Assignment (copper view)



Suggested value : VLCD = 25V
4 X R1 + R2 ≃ 8K ohm
C1 = 0.1uF

FIG.2 External Voltage Divider

MAXIMUM RATINGS* (Voltages Referenced to V_{SS}, T_A = 25°C)

Ratings	Symbol	Value	Unit
Supply Voltage	VDD	-0.3 to + 7.0	V
	V<1>	VSS-0.3 to VSS+27.5	V
Input Voltage	Vin	VSS-0.3 to VDD +0.3	V
Current Drain Per Pin Excluding VDD and VSS	I	25	mA
Operating Temperature Range	TA	0 to 70	°C
Storage Temperature Range	Tstg	-65 to + 150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be retricted to the limits in the Electrical Charateristics tables or Pin Description section.

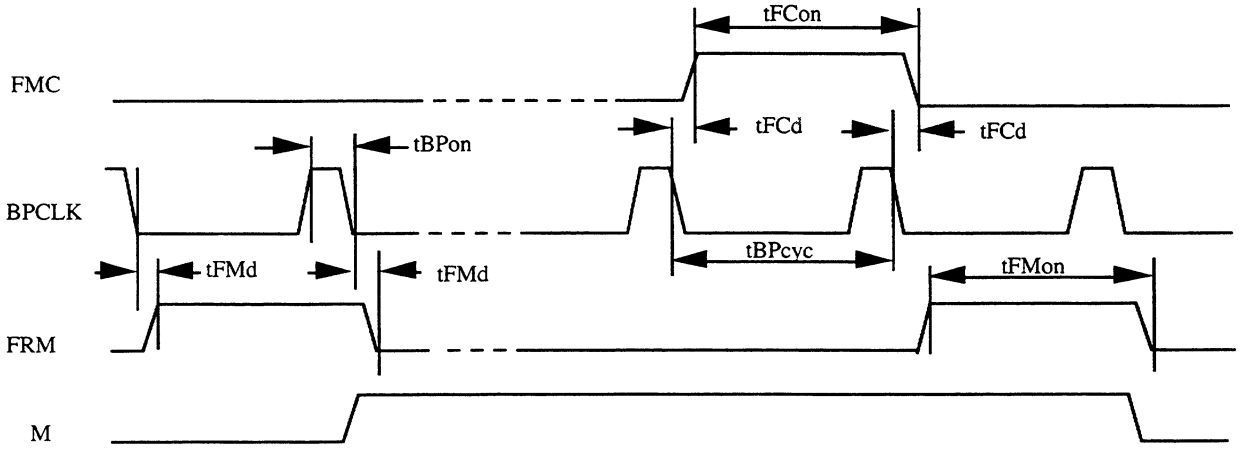
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions to be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that Vin and Vout be constrained to the range VSS < or = (Vin or Vout) < or = VDD. Reliability of operation is enhanced if unused input pins are connected to an appropriate logic voltage level (e.g., either VSS or VDD).

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS}, T_A = 25°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Voltage BPCLK, FRM, M,DOFF,FMC,MGEN	VIH	0.7xVDD	-	VDD	V
Input Low Voltage BPCLK, FRM, M,DOFF,FMC,MGEN	VIL	VSS	-	0.3xVDD	V
Capacitance BPCLK,FRM,M,DOFF,FMC	Cin	-	-	8	pF
Operating Voltages Supply Voltage (referenced to VSS)	VDD	3.0	-	5.5	V
LCD Voltage (referenced to VSS)	V<1>	10.0	-	+25.0	V
Input Current BPCLK, FRM, M,DOFF,FMC,MGEN	Iin	-	-	±1	uA
Output Low Voltage M,FMC	VOL	VSS	-	0.2xVDD	V
Output High Voltage M,FMC	VOH	0.8xVDD	-	VDD	V
Output Low Currect M,FMC (VOL = 0.5 V)	IOL	-	-	- 100	uA
Output High Current M,FMC (VOH = 4.5 V)	IOH	100	-	-	uA
Operating supply current VDD (VDD = 5 V) Display Mode	IDY	-	10	-	uA
Standby Mode	ISB	-	1	-	uA
Operating supply current V<1> (V<1> = 25 V) Display Mode	ILDY	-	10	-	uA
Standy Mode	ILSB	-	1	-	uA

AC OPERATION CONDITIONS AND CHARACTERISTICS

Characteristics	Symbol	Min	Max	Unit
Carry Out Frame On time	tFCon	122	—	us
Carry Out Frame Delay Time	tFCd	10	100	ns
BPCLK Pulse On Time	tBPon	61	—	us
BPCLK Cycle Period	tBPcyc	61	—	us
Frame Delay Time	tFMd	10	100	ns
Frame Pulse On Time	tFMon	122	—	us



TIMING DIAGRAM
MC141512
MC141515

PIN DESCRIPTION

VDD AND VSS
Power is supplied to the driver using these two pins. VDD is power and VSS is ground.

V<1>, V<5>, V<6>
These are the levels of voltage generated from an external voltages divider (Fig. 2).

DOFF
This is an output from MC68HC05L11 to signal the backplane driver to turn off LCD. If this signal is clear, the backplane driver will supplies LCD with driving signal. If this signal is set, the backplane driver outputs will be high-impedanced and LCD display is disabled.

FRM
A periodic active high input to the backplane driver for frame timing synchronization which is connected to FRM of MC68HC05L11.

BPCLK
A periodic output from MC68HC05L11 to backplane driver for timing synchronization. The signal will affect the refreshing time of LCD display.

FMC
This is an output pin of backplane driver which is connected to the FRM of the next backplane driver in case of cascading.

M
This pin is using for synchronization between the display driver. When MGEN is set, it will generate an M signal for synchronization. When MGEN is clear, it becomes an input pin and expecting a M signal from other device.

MGEN
An input which is used for program the M pin as an input or output.If MGEN is logic high, M acts as an output. If MGEN is logic low, M becomes an input.

COM 0 - 79
These are the high voltage outputs of the backplane driver which are connected to set of common lines of any LCD panel.

OPERATION OF LIQUID CRYSTAL DISPLAY DRIVER

The LCD backplane driver can support multiplex ratio of a LCD system up to 146 and cascading of more than one driver for expansion is possible. It can beset from 1:5 bias (for 16 mux) to 1:13 bias (for 146mux), by the voltage divider ratio of Fig.2. The ratio of bias or the contrast ratio (a) is defined as

$$1 : \frac{4 \times R1 + R2}{R1} = 1 : a$$

As the multiplex ratio changes, the ratio of bias has to be changed accordingly. The ratio of bias relates to the multiplex ratio as

$$a = \sqrt{mux} + 1$$

To set up a multiplex ratio, please refer to MC68HC05L11 specification Section 6.2.5.

VOLTAGES SELECTOR consists of switching circuit to select appropriate voltage levels from external voltage divider. (See Fig. 2).

80-BIT SHIFT REGISTER samples the FRM at the falling edge of BPCLK and shifts the sample to the left 80 times before exports to the next backplane driver through FMC.

HIGH VOLTAGE DRIVERS ARRAY is a row of high voltage drivers connecting to segment lines of any LCD panel. The output waveform of the high voltage driver is shown as Com(1) and Com(2)are shown in Figure 3.

POWER UP SYNCHRONIZATION is activating upon the receipt the first M pulse. The M pin of the Backplane Driver will act as an input when MGEN is connected to Low. When MGEN is Set, this backplane driver will be the master of the synchronization system. M pin will then supply a periodic signal for all LCD drivers.

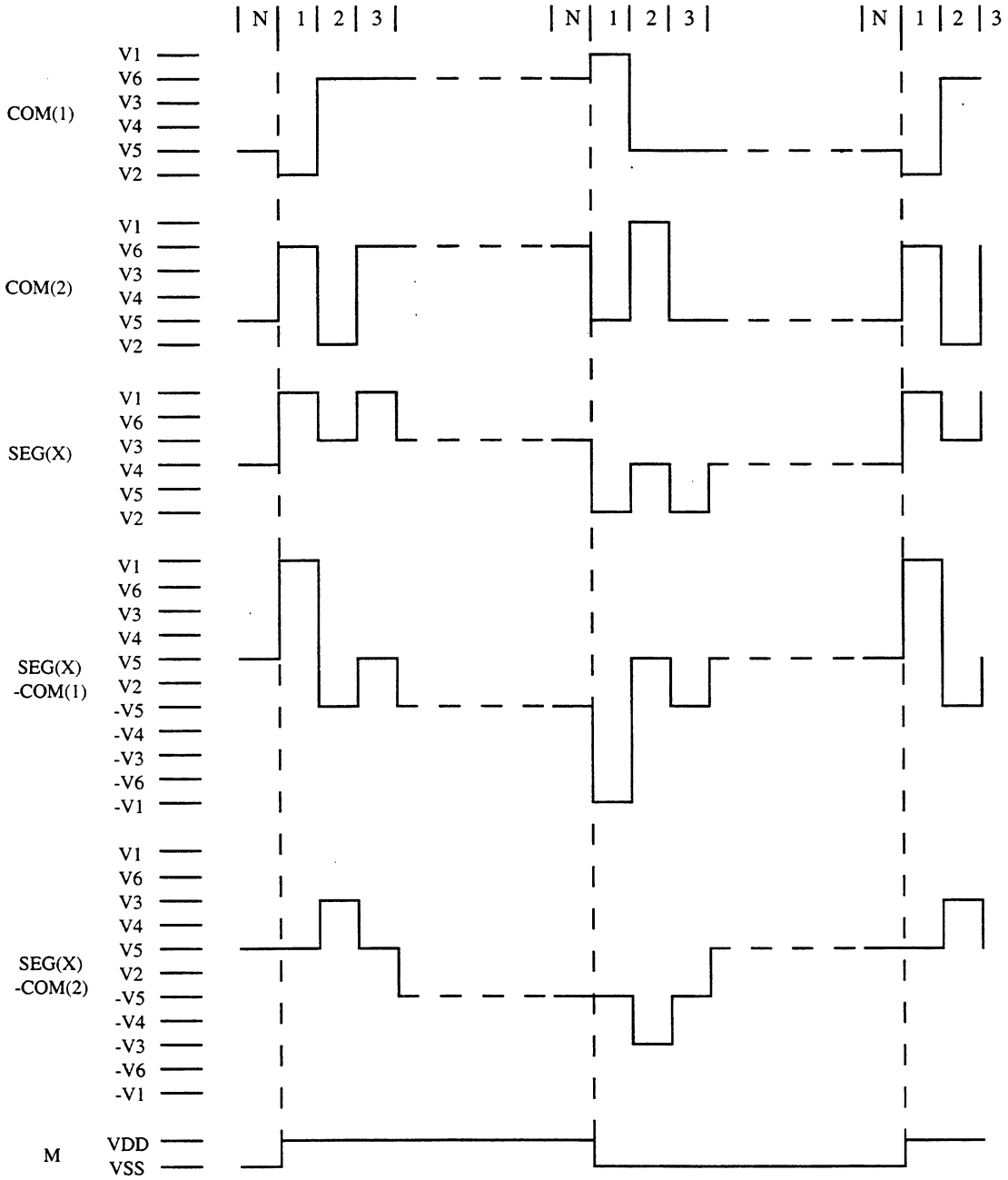
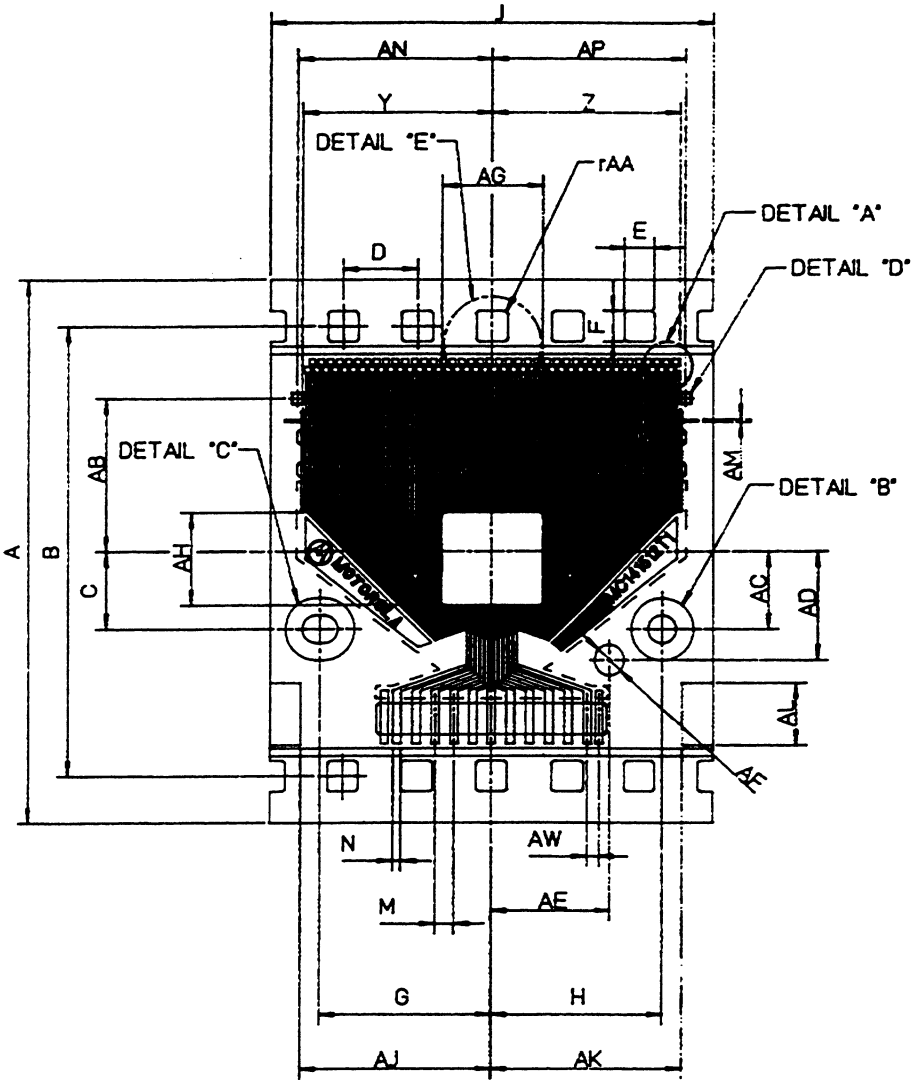
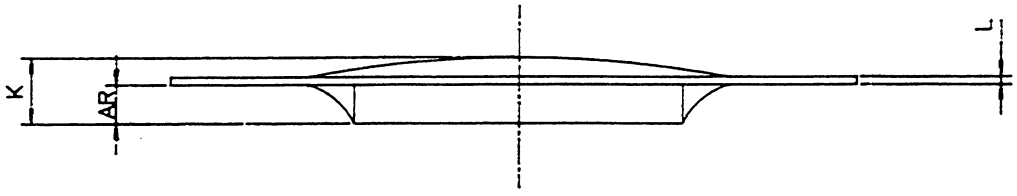


FIG. 3 Driving waveforms of 1:N multiplex
(M is the signal of drivers' timing synchronization)

MC141512T1 PACKAGE DIMENSION

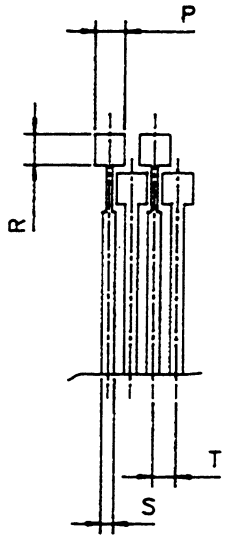
DRAWING IS NOT IN SCALE



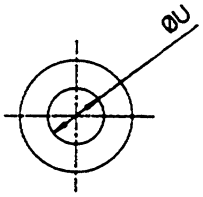


MAGNIFIED VIEW

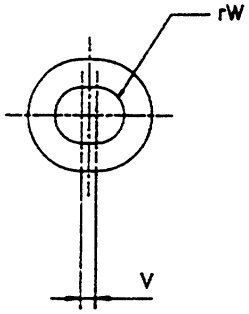
MC141512T1 PACKAGE DIMENSION
DRAWING IS NOT IN SCALE



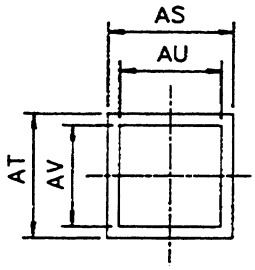
DETAIL "A"



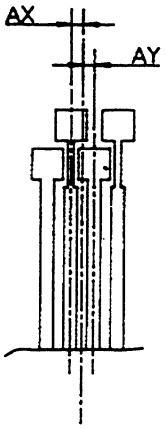
DETAIL "B"



DETAIL "C"



DETAIL "D"



DETAIL "E"

MC141512T1 PACKAGE DIMENSION
DRAWING IS NOT IN SCALE

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. Cu THICKNESS: 1 oz
4. TIN PLATING THICKNESS: 0.4μm

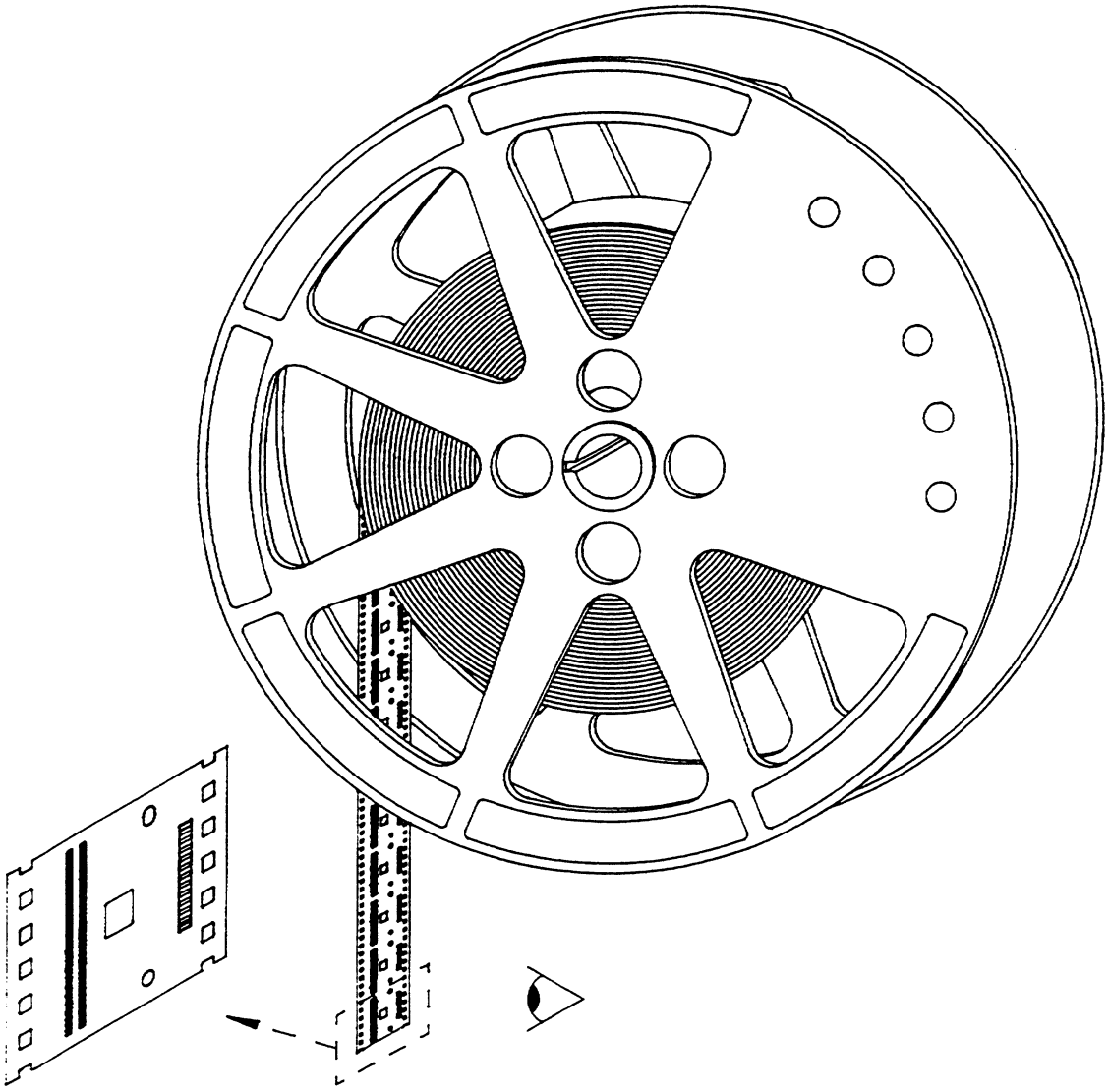
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX	DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	34.775	35.175	1.369	1.385	W	0.880	0.920	0.035	0.036
B	28.907	29.017	1.138	1.142	Y	12.100	12.200	0.4764	0.4803
C	4.950	5.050	0.195	0.199	Z	12.100	12.200	0.4764	0.4803
D	4.700	4.800	0.185	0.189	AA	---	0.200	---	0.008
E	1.951	2.011	0.077	0.079	AB	9.778	9.878	0.3850	0.3889
F	1.951	2.011	0.077	0.079	AC	4.950	5.050	0.1949	0.1988
G	10.950	11.050	0.431	0.435	AD	6.500	7.500	0.2559	0.2953
H	10.950	11.050	0.431	0.435	AE	7.000	8.000	0.2756	0.3150
J	28.000	29.000	1.102	1.142	AF	1.950	2.050	0.0768	0.0807
K	0.686	0.838	0.027	0.033	AG	---	6.410	---	0.2524
L	0.0675	0.0825	0.0027	0.0032	AH	---	5.968	---	0.2350
M	1.190	1.210	0.047	0.048	AJ	11.750	12.750	0.4626	0.5020
N	0.480	0.520	0.019	0.020	AK	11.750	12.750	0.4626	0.5020
P	0.380	0.420	0.015	0.016	AL	3.950	4.050	0.1555	0.1594
R	0.380	0.420	0.015	0.016	AM	0.150	0.190	0.0059	0.0075
S	0.150	0.190	0.006	0.007	AN	12.430	12.530	0.4894	0.4933
T	0.290	0.310	0.011	0.012	AP	12.430	12.530	0.4894	0.4933
U	1.750	1.850	0.069	0.073	AR	0.5794	0.6294	0.0228	0.0248
V	0.480	0.520	0.019	0.020	AS	0.750	0.850	0.0295	0.0335

MC141512T1 PACKAGE DIMENSION

DRAWING IS NOT IN SCALE

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX	DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
AT	0.750	0.850	0.0295	0.0335					
AU	0.600	0.700	0.0236	0.0276					
AV	0.600	0.700	0.0236	0.0276					
AW	0.790	0.810	0.0311	0.0319					
AX	0.140	0.160	0.0055	0.0063					
AY	0.140	0.160	0.0055	0.0063					

MC141512T1 TAB TAPE REEL ORIENTATION

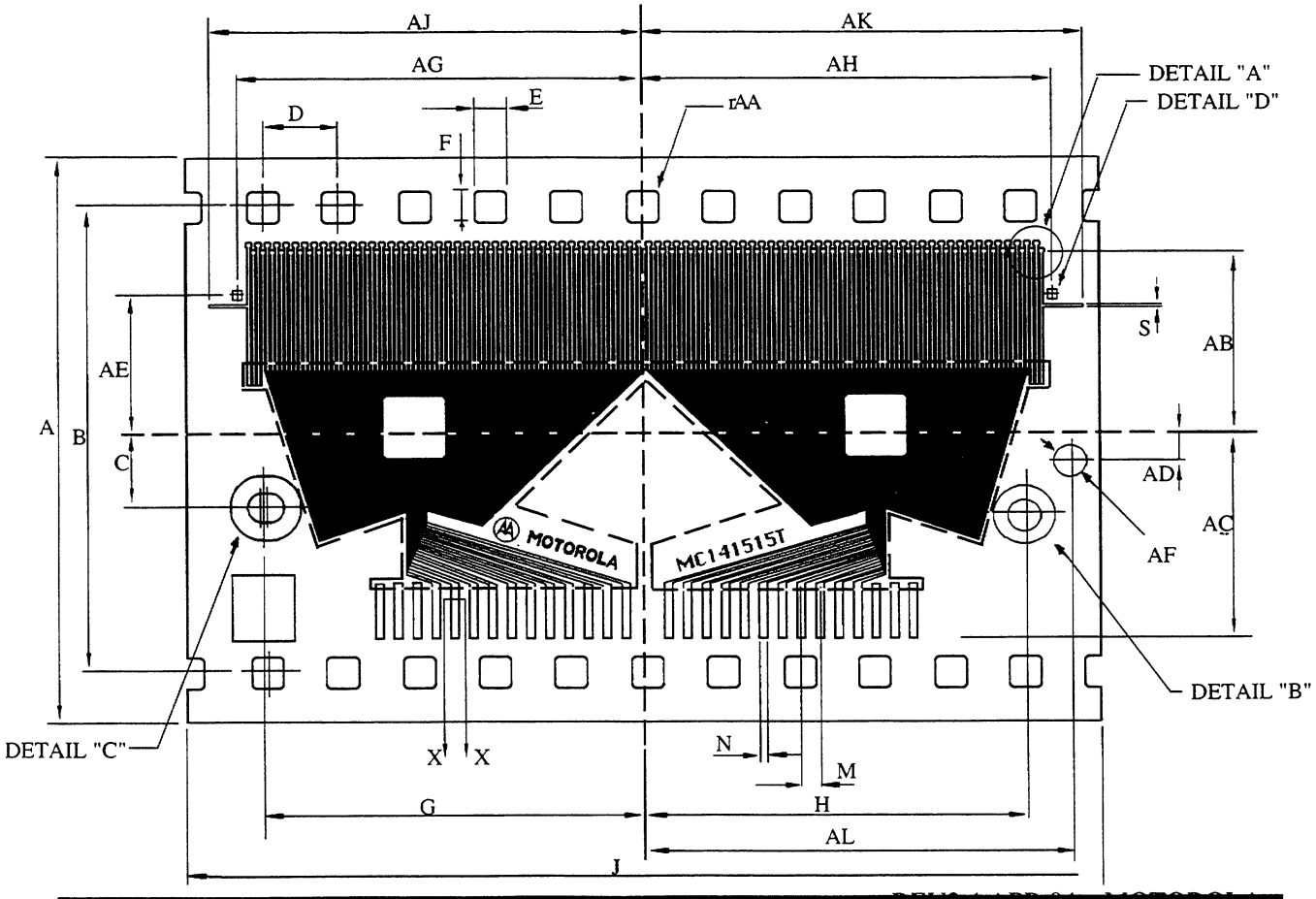


MC141515T PACKAGE DIMENSION

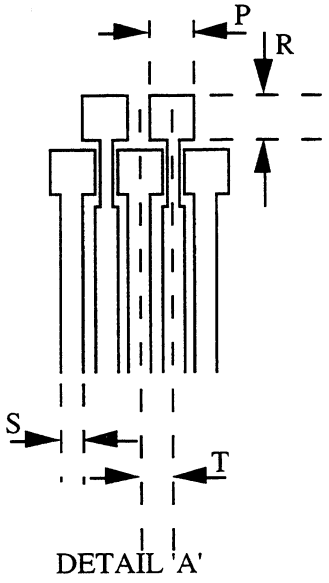
DRAWING IS NOT IN SCALE

	Dim (in mm)		Dim (in inches)	
	min	max	min	max
A	34.775	35.175	1.3691	1.3848
B	28.907	29.017	1.1381	1.1424
C	4.950	5.050	0.1949	0.1988
D	4.700	4.800	0.1850	0.1890
E	1.951	2.011	0.0768	0.0792
F	1.951	2.011	0.0768	0.0792
G	20.450	20.550	0.8051	0.8091
H	20.450	20.550	0.8051	0.8091
J	52.150	52.350	2.0531	2.0610
K	0.686	0.838	0.0270	0.0399
L	0.0675	0.0825	0.0027	0.0033
M	1.190	1.210	0.0469	0.0476
N	0.480	0.520	0.0189	0.0205
P	0.380	0.420	0.0150	0.0165
R	0.380	0.420	0.0150	0.0165
S	0.150	0.190	0.0059	0.0075
T	0.290	0.310	0.0114	0.0122
U	1.780	1.820	0.0701	0.0717
V	0.480	0.520	0.0189	0.0205

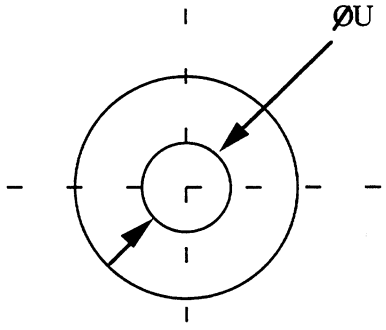
	Dim (in mm)		Dim (in inches)	
	min	max	min	max
W	0.880	0.920	0.0347	0.0362
Y	0.032	0.038	0.0013	0.0015
Z	0.0325	0.0385	0.0013	0.0015
AA	---	0.20	---	0.008
AB	11.300	11.500	0.4449	0.4527
AC	12.300	12.500	0.4843	0.4921
AD	1.950	2.050	0.0768	0.0807
AE	8.694	9.794	0.3423	0.3856
AF	1.950	2.050	0.0768	0.0807
AG	25.350	25.450	0.9980	1.0020
AH	25.210	25.310	0.9925	0.9965
AJ	25.060	26.060	0.9866	1.0260
AK	27.435	27.585	1.0801	1.0860
AL	26.950	27.050	1.0610	1.0650
AM	0.750	0.850	0.0295	0.0335
AN	0.750	0.850	0.0295	0.0335
AP	0.600	0.700	0.0236	0.0276
AR	0.600	0.700	0.0236	0.0276



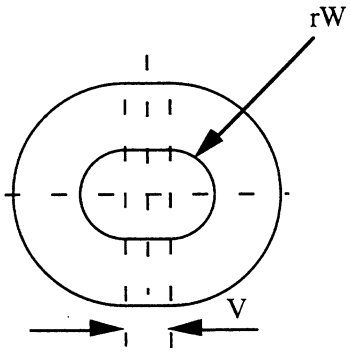
MC141515T PACKAGE DIMENSION
DRAWING IS NOT IN SCALE



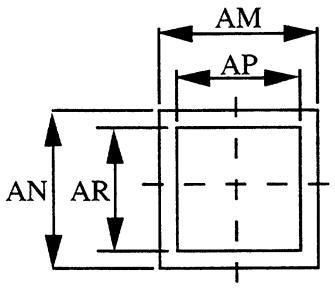
DETAIL 'A'



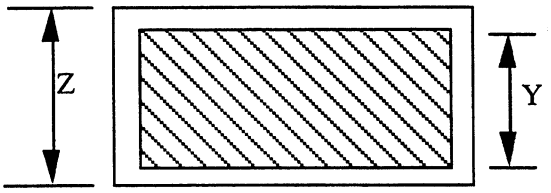
DETAIL 'B'



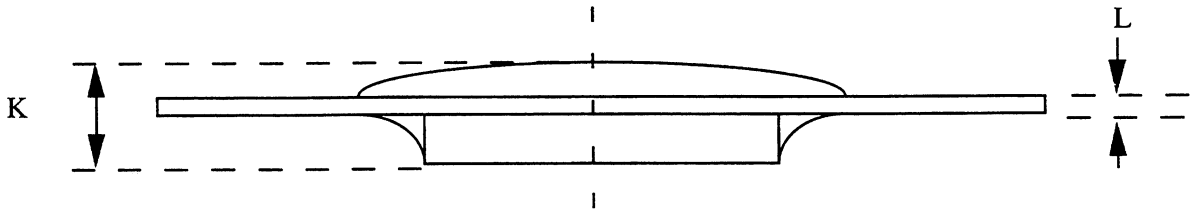
DETAIL 'C'



DETAIL 'D'



SECTION X-X



MAGNIFIED VIEW

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

APR 94 REV 2.2

Product Preview

LCD Backplane Driver

MC141516

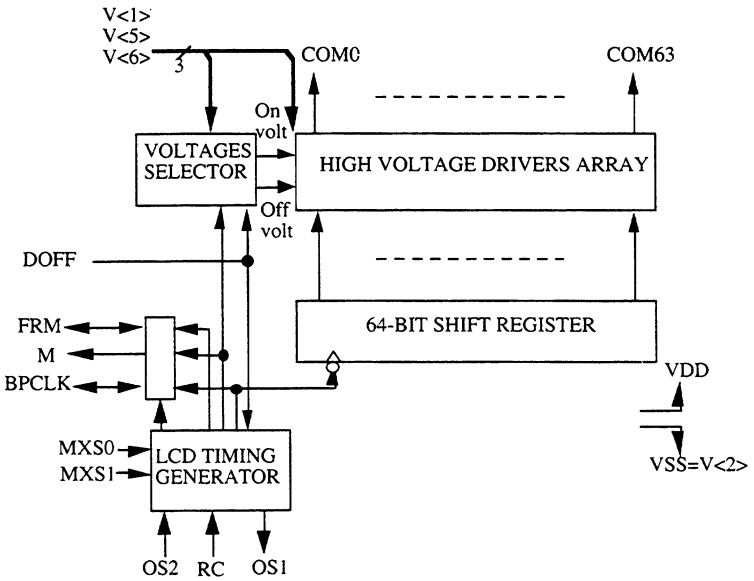
PACKAGE	PART NO.
QFP	XC141516FJ
DIE	XCC141516

The BackPlane Driver is a CMOS device which consists of 64 high voltage LCD driving signals. It is a companion device of MC141518FJ, the segment driver for 64 mux or lower LCD panel. It has a LCD timing generator which serves the same purpose as the LCD timing generator in a Motorola's microcomputer MC68HC05L11. If these drivers are used with MC68HC05L11, its internal LCD timing generator can be inhibited. Necessary timing signals are imported from MC68HC05L11. Otherwise, the driver's internal LCD timing generator can be activated to provide timing signals for system synchronisation.

FEATURES

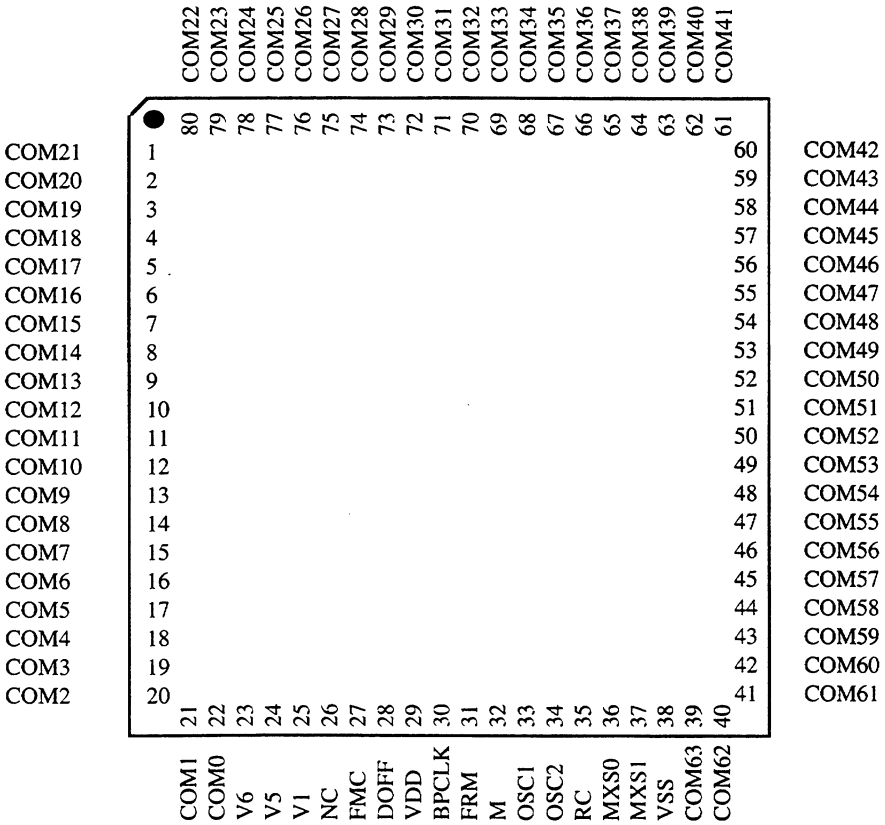
- : 64 LCD blackplane driving signals
- : Selectable bias ratio up to 1:9
- : Selectable 32,48 or 64 multiplex ratio if the on-chip RC oscillator is used
- : Selectable multiplex ratio from 32 to 64 if work with MC68HC05L11
- : 80 pins QFP

Block Diagram



This document contains infomation on a new product. Specifications and information herein are subject to change without notice.

MOTOROLA



MC141516FJ Pin Assignment

MAXIMUM RATINGS * (Voltages Referenced to V_{SS}, T_A = 25°C)

Ratings	Symbol	Value	Unit
Supply Voltage	VDD	-0.3 to + 7.0	V
	V<1>	VSS-0.3 to VSS+15	V
Input Voltage	Vin	VSS-0.3 to VDD +0.3	V
Current Drain Per Pin Excluding VDD and VSS	I	25	mA
Operating Temperature Range	TA	0 to 70	°C
Storage Temperature Range	Tstg	-65 to + 150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.

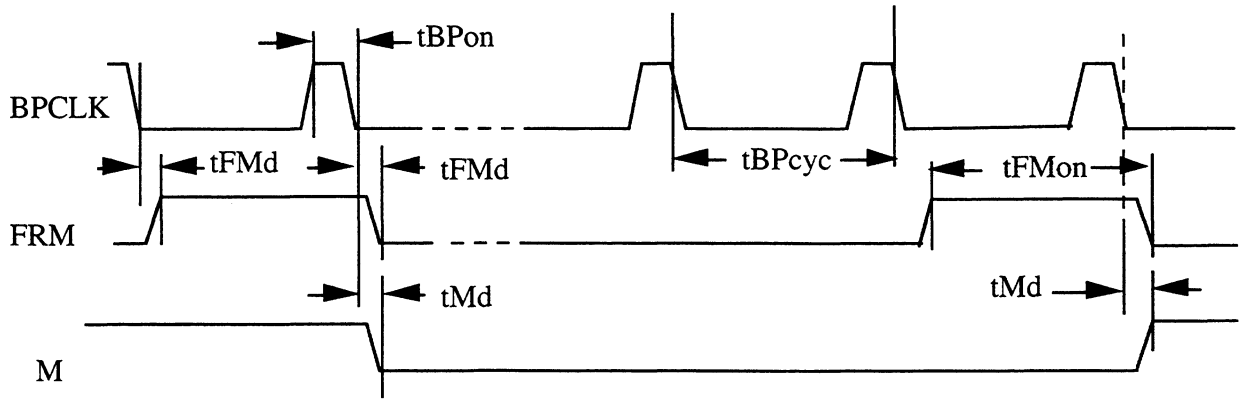
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions to be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that Vin and Vout be constrained to the range VSS < or = (Vin or Vout) < or = VDD. Reliability of operation is enhanced if unused input are connected to an appropriate logic voltage level (e.g., either VSS or VDD).

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS}, T_A = 25°C, VDD = 5.0V)

Characteristis	Symbol	Min	Typ	Max	Unit
Input High Voltage BPCLK, FRM, M,DOFF	VIH	0.7xVDD	-	VDD	V
Input Low Voltage BPCLK, FRM, M,DOFF	VIL	VSS	-	0.3xVDD	V
Capacitance BPCLK,FRM,M,DOFF	Cin	-	-	8	pF
Operating Voltages Supply Voltage (referenced to VSS)	VDD	3.0	-	5.5	V
LCD Voltage (referenced to VSS)	V<1>	0.0	-	+13	V
Input Current (Oscillator OFF) BPCLK, FRM, M,DOFF, MXS0, MXS1	Iin	-	-	±1	uA
Output Low Voltage (Oscillator ON) M,FRM, BPCLK	VOL	VSS	-	0.2xVDD	V
Output High Voltage (Oscillator ON) M,FRM, BCLK	VOH	0.8xVDD	-	VDD	V
Output Low Currect (Oscillator ON) M,FRM,BCLK (VOL = 0.5 V)	IOL	-	-	- 100	.uA
Output High Current (Oscillator ON) M,FRM,BCLK (VOH = 4.5 V)	IOH	100	-	-	uA
Operating supply current VDD (VDD = 5 V)					
Dynamic Mode (Oscillator ON, M=30Hz)	IDP1	-	15	-	uA
(Oscillator OFF)	IDP2	-	5	-	uA
Standby Mode	ISB	-	2	-	uA
Operating supply current V<1> (V<1> = 13V)					
Display Mode	ILDP	-	-	8	uA
Standby Mode	ILSB	-	2	-	uA

AC OPERATION CONDITIONS AND CHARACTERISTICS (VCC = 5.0V +/- 5%, VSS = 0)

Characteristics	Symbol	Min	Max	Unit
BPCLK Pulse On Time	tBPon	61	—	us
BPCLK Cycle Period	tBPcyc	122	—	us
Frame Delay Time	tFMd	5	30	ns
Frame Pulse On Time	tFMon	122	—	us
M Pulse Delay Time	tMd	0	30	ns



TIMING DIAGRAM
MC141516

PIN DESCRIPTION

VDD AND VSS

Power is supplied to the driver using these two pins. VDD is power and VSS is ground.

V<1>, V<5>, V<6>

These input pins provide the voltage levels for the backplane driver and are connected to the V<1>, V<5>, V<6> of the voltages generator as in Figure 2 of the Segment driver Product Specification.

DOFF

It is an active-high input for turning off the LCD. If DOFF is set, all high voltage outputs will be turned to high impedance. DOFF will also suppress the on-chip RC oscillator from oscillation when the LCD timing generator is enabled.

OSC1, OSC2, RC

These pins provide connections for external circuitry to the on-chip RC oscillator for frequency selection. The on-chip RC oscillator is part of the internal LCD timing generator. Output of this oscillator will be fed out as BPCLK and further divided down internally to produce signals FRM and M if the LCD timing generator is enabled.

MXS1, MXS0

These pins can be hardwared to select different mux ratio. Table 1 shows the combinations of these signals and their cooresponding mux ratios. These four combinations provide selections for 32,48 and 64 mux ratio and a disable state. Except for the disable state, all other selections will enable the LCD timing generator. With DOFF clear, the periodic signal from the on-chip RC oscillator is fed to the whole LCD system as the BPCLK. BPCLK will then be further divided down through the LCD timing generator to produce signals FRM and M for the whole LCD system.

MXS1,MXS0	MUX RATIO
0,0	DISABLED
0,1	32
1,0	48
1,1	64

Table 1. The Selections of Mux Ratio using MXS1 and MXS0

BPCLK

It is either an input connecting to signal BPCLK of the microcomputer MC68HC05L11 or an output pin supplying the synchronisation pulse BPCLK to segment drives. If the LCD timer generator is disabled, this pin is assumed to be input.

FRM

It is either an input connecting to signal FRM of the microcomputer MC68HC05L11 or an output pin supplying the synchronisation pulse FRM to segment drives. If the LCD timer generator is disabled, the status of this pin is input.

M

This is an output pin providing the necessary modulation signal to shape up the class B LCD waveform (see Fig.3, Product Specification of MC141518). It is a signal with 50% duty cycle and its frequency is half of FRM.

COM0-COM63

These are the high voltage drivers output of the backplane driver which are connected to the common lines of any LCD panel. These high voltage drivers are high impedance if DOFF is set. See Fig.3 Product Specification of MC141518 for these high voltage outputs waveform.

FMC

This is a test pin. This pin should be left opened in application.

LIQUID CRYSTAL DISPLAY BACKPLANE DRIVER

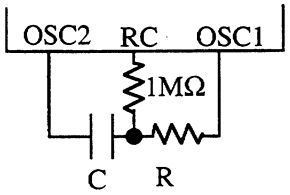
INTRODUCTION

The backplane driver can support multiplex ratio of a LCD system from 32 to 64. Three signals that need to be varied as a result of different mux ratio are BPCLK, FRM and M. The first two can be imported externally (if the microprocessor MC68HC05L11 is used) or the backplane driver generates them internally. In case of internal generation, user has to design the on-chip RC oscillator circuit producing a frequency with respect to desirable mux ratio.

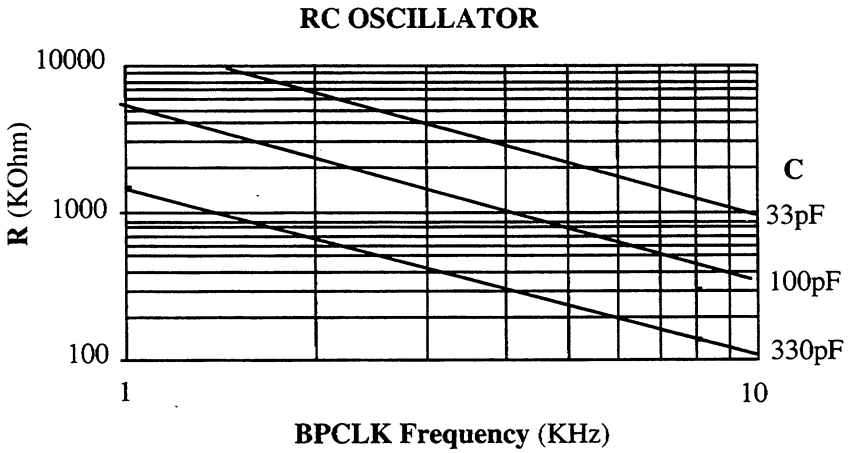
Followings are some rules to do the design.

- Freq. of FRM = Freq. of M x 2.
- Freq. of BPCLK= Freq. of FRM x MUX.
  [max period = (1/60)sec / no. of display lines]

If frequency of BPCLK is known, user can locate the values for R and C of Figure1(a) in Figure 1(b). Usually frequency of M is between 30 Hz to 35 Hz - a range that refresh fricker is invisible.



(a)



(For reference only)

(b)

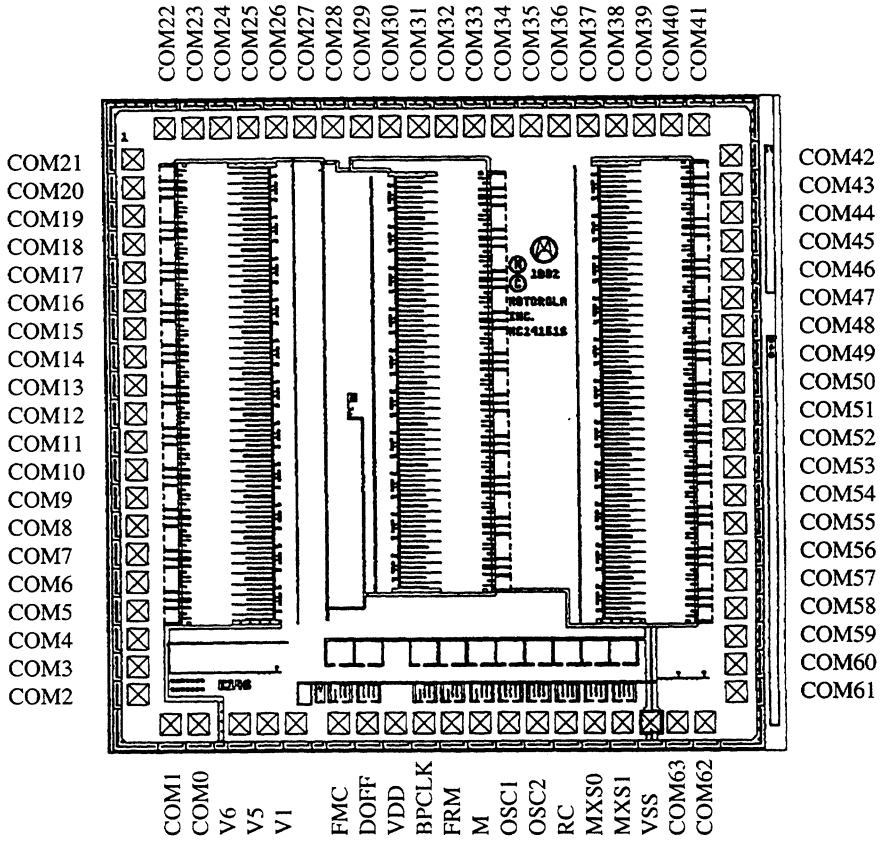
Figure 1. (a) the external circuit to the on-chip RC oscillator and its (b) frequency relationship with the external resistor and capacitor.

VOLTAGES SELECTOR consists of switching circuit to select appropriate voltage levels from external voltage divider. See Fig.2, Product Specification of the segment driver MC141518.

64 BITS SHIFT REGISTER samples FRM and shift at the falling edge of BPCLK.

HIGH VOLTAGE DRIVERS ARRAY is a row of high voltage drivers which outputs are connecting to the backplane (or common) lines of any LCD panel. The waveform of these drivers are shown as Com(1) or Com(2) in Fig. 3, the Product Specification of the segment driver MC141518.

MCC141516 PIN ASSIGNMENT



MCC141516 PAD COORDINATES : (UNIT : UM)

PIN NAME	X	Y	PIN NAME	X	Y
COM1	-1330.0	-1481.5	COM61	1489.5	-1331.5
COM0	-1190.0	-1481.5	COM60	1489.5	-1191.5
V6	-982.0	-1481.5	COM59	1489.5	-1051.5
V5	-842.0	-1481.5	COM58	1489.5	-911.5
V1	-702.0	-1481.5	COM57	1489.5	-771.5
FMC	-490.0	-1481.5	COM56	1489.5	-631.5
DOFF	-350.0	-1481.5	COM55	1489.5	-491.5
VDD	-210.0	-1481.5	COM54	1489.5	-351.5
BPCLK	-70.0	-1481.5	COM53	1489.5	-211.5
FRM	70.0	-1481.5	COM52	1489.5	-71.5
M	210.0	-1481.5	COM51	1489.5	68.5
OSC1	350.0	-1481.5	COM50	1489.5	208.5
OSC2	490.0	-1481.5	COM49	1489.5	348.5
RC	630.0	-1481.5	COM48	1489.5	488.5
MXS0	770.0	-1481.5	COM47	1489.5	628.5
MXS1	910.0	-1481.5	COM46	1489.5	768.5
VSS	1050.0	-1481.5	COM45	1489.5	908.5
COM63	1190.0	-1481.5	COM44	1489.5	1048.5
COM62	1330.0	-1481.5	COM43	1489.5	1188.5
			COM42	1489.5	1328.5

PIN NAME	X	Y	PIN NAME	X	Y
COM2	-1489.5	-1331.5	COM22	-1330.0	1481.0
COM3	-1489.5	-1191.5	COM23	-1190.0	1481.0
COM4	-1489.5	-1051.5	COM24	-1050.0	1481.0
COM5	-1489.5	-911.5	COM25	-910.0	1481.0
COM6	-1489.5	-771.5	COM26	-770.0	1481.0
COM7	-1489.5	-631.5	COM27	-630.0	1481.0
COM8	-1489.5	-491.5	COM28	-490.0	1481.0
COM9	-1489.5	-351.5	COM29	-350.0	1481.0
COM10	-1489.5	-211.5	COM30	-210.0	1481.0
COM11	-1489.5	-71.5	COM31	-70.0	1481.0
COM12	-1489.5	68.5	COM32	70.0	1481.0
COM13	-1489.5	208.5	COM33	210.0	1481.0
COM14	-1489.5	348.5	COM34	350.0	1481.0
COM15	-1489.5	488.5	COM35	490.0	1481.0
COM16	-1489.5	628.5	COM36	630.0	1481.0
COM17	-1489.5	768.5	COM37	770.0	1481.0
COM18	-1489.5	908.5	COM38	910.0	1481.0
COM19	-1489.5	1048.5	COM39	1050.0	1481.0
COM20	-1489.5	1188.5	COM40	1190.0	1481.0
COM21	-1489.5	1328.5	COM41	1330.0	1481.0

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