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MC68L300EC16/D

MC68L300

Technical Supplement

16.78 MHz Electrical Characteristics

Devices in the M68300 Modular Microcontroller Family are built up from a selection of standard functional modules. The MC68331 and MC68332 contain the same central processing unit (CPU32) and system integration module (SIM), and thus have similar electrical characteristics.

M68300 devices that operate at 3.3 volts are now available. This publication contains electrical characteristics that supplement the *MC68331 User's Manual* (MC68331UM/AD) and the *MC68332 User's Manual* (MC68332UM/AD).

MC68L331 and MC68L332 are currently offered for operation in external clock mode only.

Enhanced versions of the MC68331 and MC68332 will offer extended V_{DD} operating range, PLL, 5 volt tolerant I/O, and higher frequency.

TABLE OF CONTENTS

Table 1 Maximum Ratings

Num	Rating	Symbol	Value	Unit
1	Supply Voltage[1,2,3]	V_{DD}	– 0.3 to + 6.5	V
2	Input Voltage [1,2,3,4,5,7]	V_{IN}	– 0.3 to + 6.5	V
3	Instantaneous Maximum Current Single Pin Limit (all pins)[1,3,5,6]	I_D	25	mA
4	Operating Maximum Current Digital Input Disruptive Current[3,5,6,7,8] $V_{NEGCLMAP} \cong -0.3$ V $V_{POSCLAMP} \cong V_{DD} + 0.3$	I_{id}	– 500 to 500	µA
5	Operating Temperature Range C Suffix	T_A	T_L to T_H – 40 to 85	°C
6	Storage Temperature Range	T_{stg}	– 55 to 150	°C

NOTES:

1. Permanent damage can occur if maximum ratings are exceeded. Exposure to voltages or currents in excess of recommended values affects device reliability. Device modules may not operate normally while being exposed to electrical extremes.
2. Although sections of the device contain circuitry to protect against damage from high static voltages or electrical fields, take normal precautions to avoid exposure to voltages higher than maximum-rated voltages.
3. This parameter is periodically sampled rather than 100% tested.
4. All pins except TSC.
5. Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.
6. Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current.
7. All functional non-supply pins are internally clamped to V_{SS}. All functional pins except EXTAL and XFC are internally clamped to V_{DD}.
8. Total input current for all digital input-only and all digital input/output pins must not exceed 10 mA. Exceeding this limit can cause disruption of normal operation.

Table 2 MC68L331 Typical Ratings

Num	Rating	Symbol	Value	Unit
1	Supply Voltage	V_{DD}	3.3	V
2	Operating Temperature	T_A	25	°C
3	V_{DD} Supply Current RUN LPSTOP, External clock, max f_{sys}	I_{DD}	 38 1.0	 mA mA
4	Clock Synthesizer Operating Voltage	V_{DDSYN}	3.3	V
5	V_{DDSYN} Supply Current External Clock, maximum f_{sys}	I_{DDSYN}	1.5	mA
6	RAM Standby Current Normal RAM operation Standby operation	I_{SB}	 3.0 10	 µA µA
7	Power Dissipation	P_D	125.0	mW

Table 3 MC68L332 Typical Ratings

Num	Rating	Symbol	Value	Unit
1	Supply Voltage	V_{DD}	3.3	V
2	Operating Temperature	T_A	25	°C
3	V_{DD} Supply Current	I_{DD}		
	RUN		45	mA
	LPSTOP, External clock, max f_{sys}		1.0	mA
4	Clock Synthesizer Operating Voltage	V_{DDSYN}	3.3	V
5	V_{DDSYN} Supply Current	I_{DDSYN}		
	External Clock, maximum f_{sys}		2.0	mA
6	RAM Standby Current	I_{SB}		
	Normal RAM operation		3.0	µA
	Standby operation		10	µA
7	Power Dissipation	P_D	148.0	mW

Table 4 Thermal Characteristics

Num	Rating	Symbol	Value	Unit
1	Thermal Resistance	Θ_{JA}		°C/W
	Plastic 132-Pin Surface Mount		38	
	Plastic 144-Pin Surface Mount		49	

The average chip-junction temperature (TJ) in C can be obtained from:

$$T_J = T_A + (P_D \times \Theta_{JA}) \quad (1)$$

where:

T_A = Ambient Temperature, °C
Θ_{JA}= Package Thermal Resistance, Junction-to-Ambient, °C/W
$P_D = P_{INT} + P_{I/O}$
P_{INT}= $I_{DD} \times V_{DD}$, Watts — Chip Internal Power
$P_{I/O}$= Power Dissipation on Input and Output Pins — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D + (T_A + 273°C) + \Theta_{JA} \times P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

Table 5 16.78 MHz DC Characteristics

(V_{DD} and V_{DDSYN} = 3.0 to 3.6Vdc, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)

Num	Characteristic	Symbol	Min	Max	Unit
1	Input High Voltage	V_{IH}	0.7 (V_{DD})	V_{DD} + 0.3	V
2	Input Low Voltage	V_{IL}	V_{SS} – 0.3	0.2 (V_{DD})	V
3	Input Hysteresis[1]	V_{HYS}	0.5	—	V
4	Input Leakage Current [2] $V_{in} = V_{DD}$ or V_{SS} Input-only pins	I_{in}	–2.5	2.5	µA
5	High Impedance (Off-State) Leakage Current[2] $V_{in} = V_{DD}$ or V_{SS} All input/output and output pins	I_{OZ}	–2.5	2.5	µA
6	CMOS Output High Voltage[2, 3] I_{OH} = –10.0 µA Group 1, 2, 4 input/output and all output pins	V_{OH}	V_{DD} –0.2	—	V
7	CMOS Output Low Voltage[2] I_{OL} = 10.0 µA Group 1, 2, 4 input/output and all output pins	V_{OL}	—	0.2	V
8	Output High Voltage[2, 3] I_{OH} = –0.4 mA Group 1, 2, 4 input/output and all output pins	V_{OH}	V_{DD} –0.5	—	V
9	Output Low Voltage[2] I_{OL} = 0.8 mA Group 1 I/O pins CLKOUT, FREEZE/QUOT, $\overline{\text{IPIPE}}$/DSO I_{OL} = 2.6 mA Group 2 and group 4 I/O pins, $\overline{\text{CSBOOT}}$, $\overline{\text{BG}}/\overline{\text{CS1}}$ I_{OL} = 6.0 mA Group 3	V_{OL}	— — —	0.4 0.4 0.4	V
10	Three State Control Input High Voltage	V_{IHTSC}	2.4 (V_{DD})	9.1	V
11	Data Bus Mode Select Pull-up Current [4] $V_{in} = V_{IL}$ $V_{in} = V_{IH}$	I_{MSP}	— –8	–95 —	µA
12A	MC68331 V_{DD} Supply Current[5] Run LPSTOP, external clock input = max f_{sys}	I_{DD}	— —	49 2	mA mA
12B	MC68332 V_{DD} Supply Current[5] Run LPSTOP, external clock input = max f_{sys}	I_{DD}	— —	56 2	mA mA
13	Clock Synthesizer Operating Voltage	V_{DDSYN}	3.0	3.6	V
14	V_{DDSYN} Supply Current External Clock, maximum f_{sys}	I_{DDSYN}	—	3	mA
15	MC68332 RAM Standby Voltage Specified V_{DD} applied $V_{DD} = V_{SS}$	V_{SB}	0.0 2.7	V_{DD} 3.6	V
16	MC68332 RAM Standby Current[6, 7] Normal RAM operation $V_{DD} > V_{SB} - 0.5$ V Transient condition $V_{SB} - 0.5\text{ V} \geq V_{DD} \geq V_{SS} + 0.5$ V Standby operation $V_{DD} < V_{SS} + 0.5$ V	I_{SB}	— — —	10 3 50	µA mA µA
17A	MC68331 Power Dissipation[8]	P_D	—	187	mW
17B	MC68332 Power Dissipation	P_D	—	212	mW
18	Input Capacitance[2, 9] All input-only pins All input/output pins	C_{in}	— —	10 20	pF
19	Load Capacitance[2] Group 1 I/O Pins, CLKOUT, FREEZE/QUOT, $\overline{\text{IPIPE}}$ Group 2 I/O Pins and $\overline{\text{CSBOOT}}$, $\overline{\text{BG}}/\overline{\text{CS}}$ Group 3 I/O Pins Group 4 I/O Pins	C_L	— — — —	90 100 100 100	pF

NOTES:

1. Applies to:
   QSM pins
   $\overline{\text{IRQ[7:1]}}$, $\overline{\text{RESET}}$, EXTAL, TSC, $\overline{\text{RMC}}$, $\overline{\text{BKPT}}$/DSCLK, $\overline{\text{IFETCH}}$/DSI
2. Input-Only Pins: TSC, $\overline{\text{BKPT}}$/DSCLK, RXD
   Output-Only Pins: $\overline{\text{CSBOOT}}$, $\overline{\text{BG}}$/$\overline{\text{CS}}$, CLKOUT, FREEZE/QUOT, $\overline{\text{IPIPE}}$/DSO
   Input/Output Pins:
      Group 1: DATA[15:0], $\overline{\text{IFETCH}}$/DSI
      Group 2: ADDR[23:19]/$\overline{\text{CS[10:6]}}$, FC[2:0]/$\overline{\text{CS[5:3]}}$, $\overline{\text{DSACK[1:0]}}$, $\overline{\text{AVEC}}$, $\overline{\text{RMC}}$, $\overline{\text{DS}}$, $\overline{\text{AS}}$, SIZ[1:0]
      $\overline{\text{IRQ[7:1]}}$, MODCLK, ADDR[18:0], R/$\overline{\text{W}}$, $\overline{\text{BERR}}$, $\overline{\text{BR}}$/$\overline{\text{CS0}}$, $\overline{\text{BGACK}}$/$\overline{\text{CS2}}$, PCS[3:1], PCS0/$\overline{\text{SS}}$, TXD
      Group 3: $\overline{\text{HALT}}$, $\overline{\text{RESET}}$
      Group 4: MISO, MOSI, SCK
3. Does not apply to $\overline{\text{HALT}}$ and $\overline{\text{RESET}}$ because they are open drain pins.
   Does not apply to Port QS[7:0] (TXD, PCS[3:1], PCS0/$\overline{\text{SS}}$, SCK, MOSI, MISO) in wired-OR mode.
4. Current measured at maximum system clock frequency.
5. Total operating current is the sum of the appropriate V_{DD} supply and V_{DDSYN} supply current.
6. When V_{SB} is more than 0.3V greater than V_{DD}, current flows between the V_{STBY} and V_{DD} pins, which causes standby current to increase toward the maximum condition specification. System noise on the V_{DD} and V_{STBY} pin can contribute to this condition.
7. The SRAM module will not switch into standby mode as long as V_{SB} does not exceed V_{DD} by more than 0.5 volts. The SRAM array cannot be accessed while the module is in standby mode.
8. Power dissipation measured at specified system clock frequency. Power dissipation can be calculated using the expression:
   $$P_D = 3.6V\ (I_{DDSYN} + I_{DD})$$
9. Input capacitance is periodically sampled rather than 100% tested.

Table 6 16.78 MHz AC Timing

(V_{DD} and V_{DDSYN} = 3.0 to 3.6Vdc, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)[1]

Num	Characteristic	Symbol	Min	Max	Unit
F1	Frequency of Operation	f_{sys}	—	16.78	MHz
1	Clock Period	t_{cyc}	59.6	—	ns
1A	ECLK Period	t_{Ecyc}	476	—	ns
1B	External Clock Input Period[2]	t_{Xcyc}	59.6	—	ns
2, 3	Clock Pulse Width	t_{CW}	24	—	ns
2A, 3A	ECLK Pulse Width	t_{ECW}	236	—	ns
2B, 3B	External Clock Input High/Low Time[2]	t_{XCHL}	29.8	—	ns
4, 5	CLKOUT Rise and Fall Time	t_{Crf}	—	7	ns
4A, 5A	Rise and Fall Time (All outputs except CLKOUT)	t_{rf}	—	8	ns
4B, 5B	External Clock Input Rise and Fall Time	t_{XCrf}	—	4	ns
6	Clock High to ADDR, FC, $\overline{\text{RMC}}$, SIZ Valid	t_{CHAV}	0	29	ns
7	Clock High to ADDR, Data, FC, $\overline{\text{RMC}}$,SIZ High Impedance	t_{CHAZx}	0	59	ns
8	Clock High to ADDR, FC, $\overline{\text{RMC}}$, SIZ Invalid	t_{CHAZn}	0	—	ns
9	Clock Low to $\overline{\text{AS}}$, $\overline{\text{DS}}$, $\overline{\text{CS}}$ Asserted	t_{CLSA}	0	25	ns
9A	$\overline{\text{AS}}$ to $\overline{\text{DS}}$ or $\overline{\text{CS}}$ Asserted (Read)[3]	t_{STSA}	–15	15	ns
9C	Clock Low to $\overline{\text{IFETCH}}$, $\overline{\text{IPIPE}}$ Asserted	t_{CLIA}	2	22	ns
11	ADDR, FC, $\overline{\text{RMC}}$, SIZ Valid to $\overline{\text{AS}}$, $\overline{\text{CS}}$, (and $\overline{\text{DS}}$ Read) Asserted	t_{AVSA}	15	—	ns
12	Clock Low to $\overline{\text{AS}}$, $\overline{\text{DS}}$, $\overline{\text{CS}}$ Negated	t_{CLSN}	2	29	ns
12A	Clock Low to $\overline{\text{IFETCH}}$, $\overline{\text{IPIPE}}$ Negated	t_{CLIN}	2	29	ns
13	$\overline{\text{AS}}$, $\overline{\text{DS}}$, $\overline{\text{CS}}$ Negated to ADDR, FC, SIZ Invalid (Address Hold)	t_{SNAI}	15	—	ns
14	$\overline{\text{AS}}$, $\overline{\text{CS}}$ (and $\overline{\text{DS}}$ Read) Width Asserted	t_{SWA}	100	—	ns
14A	$\overline{\text{DS}}$, $\overline{\text{CS}}$ Width Asserted (Write)	t_{SWAW}	45	—	ns
14B	$\overline{\text{AS}}$, $\overline{\text{CS}}$ (and $\overline{\text{DS}}$ Read) Width Asserted (Fast Cycle)	t_{SWDW}	40	—	ns
15	$\overline{\text{AS}}$, $\overline{\text{DS}}$, $\overline{\text{CS}}$ Width Negated[4]	t_{SN}	40	—	ns
16	Clock High to $\overline{\text{AS}}$, $\overline{\text{DS}}$, R/$\overline{\text{W}}$ High Impedance	t_{CHSZ}	—	59	ns
17	$\overline{\text{AS}}$, $\overline{\text{DS}}$, $\overline{\text{CS}}$ Negated to R/$\overline{\text{W}}$ High	t_{SNRN}	15	—	ns
18	Clock High to R/$\overline{\text{W}}$ High	t_{CHRH}	0	29	ns
20	Clock High to R/$\overline{\text{W}}$ Low	t_{CHRL}	0	29	ns
21	R/$\overline{\text{W}}$ High to $\overline{\text{AS}}$, $\overline{\text{CS}}$ Asserted	t_{RAAA}	15	—	ns
22	R/$\overline{\text{W}}$ Low to $\overline{\text{DS}}$, $\overline{\text{CS}}$ Asserted (Write)	t_{RASA}	70	—	ns
23	Clock High to Data Out Valid	t_{CHDO}	—	29	ns
24	Data Out Valid to Negating Edge of $\overline{\text{AS}}$, $\overline{\text{CS}}$ (Fast Write Cycle)	t_{DVASN}	15	—	ns
25	$\overline{\text{DS}}$, $\overline{\text{CS}}$ Negated to Data Out Invalid (Data Out Hold)	t_{SNDOI}	15	—	ns
26	Data Out Valid to $\overline{\text{DS}}$, $\overline{\text{CS}}$ Asserted (Write)	t_{DVSA}	15	—	ns
27	Data In Valid to Clock Low (Data Setup)	t_{DICL}	5	—	ns
27A	Late $\overline{\text{BERR}}$, $\overline{\text{HALT}}$ Asserted to Clock Low (Setup Time)	t_{BELCL}	20	—	ns
28	$\overline{\text{AS}}$, $\overline{\text{DS}}$ Negated to $\overline{\text{DSACK[1:0]}}$, $\overline{\text{BERR}}$, $\overline{\text{HALT}}$, $\overline{\text{AVEC}}$ Negated	t_{SNDN}	0	80	ns
29	$\overline{\text{DS}}$, $\overline{\text{CS}}$ Negated to Data In Invalid (Data In Hold)[5]	t_{SNDI}	0	—	ns
29A	$\overline{\text{DS}}$, $\overline{\text{CS}}$ Negated to Data In High Impedance[5, 6]	t_{SHDI}	—	55	ns
30	CLKOUT Low to Data In Invalid (Fast Cycle Hold)[5]	t_{CLDI}	10	—	ns
30A	CLKOUT Low to Data In High Impedance[5]	t_{CLDH}	—	90	ns
31	$\overline{\text{DSACK[1:0]}}$ Asserted to Data In Valid[7]	t_{DADI}	—	50	ns
33	Clock Low to $\overline{\text{BG}}$ Asserted/Negated	t_{CLBAN}	—	29	ns
35	$\overline{\text{BR}}$ Asserted to $\overline{\text{BG}}$ Asserted ($\overline{\text{RMC}}$ not Asserted)[8]	t_{BRAGA}	1	—	t_{cyc}
37	$\overline{\text{BGACK}}$ Asserted to $\overline{\text{BG}}$ Negated	t_{GAGN}	1	2	t_{cyc}
39	$\overline{\text{BG}}$ Width Negated	t_{GH}	2	—	t_{cyc}
39A	$\overline{\text{BG}}$ Width Asserted	t_{GA}	1	—	t_{cyc}
46	R/$\overline{\text{W}}$ Width Asserted (Write or Read)	t_{RWA}	150	—	ns

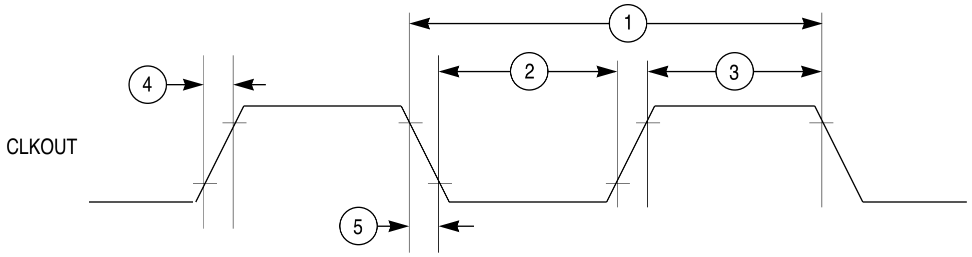
Table 6 16.78 MHz AC Timing (Continued)

(V_{DD} and V_{DDSYN} = 3.0 to 3.6Vdc, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)[1]

Num	Characteristic	Symbol	Min	Max	Unit
46A	R/$\overline{\text{W}}$ Width Asserted (Fast Write or Read Cycle)	t_{RWAS}	90	—	ns
47A	Asynchronous Input Setup Time $\overline{\text{BR}}$, $\overline{\text{BGACK}}$, $\overline{\text{DSACK[1:0]}}$, $\overline{\text{BERR}}$, $\overline{\text{AVEC}}$, $\overline{\text{HALT}}$	t_{AIST}	5	—	ns
47B	Asynchronous Input Hold Time	t_{AIHT}	15	—	ns
48	$\overline{\text{DSACK[1:0]}}$ Asserted to $\overline{\text{BERR}}$, $\overline{\text{HALT}}$ Asserted[9]	t_{DABA}	—	30	ns
53	Data Out Hold from Clock High	t_{DOCH}	0	—	ns
54	Clock High to Data Out High Impedance	t_{CHDH}	—	28	ns
55	R/W Asserted to Data Bus Impedance Change	t_{RADC}	40	—	ns
70	Clock Low to Data Bus Driven (Show Cycle)	t_{SCLDD}	0	29	ns
71	Data Setup Time to Clock Low (Show Cycle)	t_{SCLDS}	15	—	ns
72	Data Hold from Clock Low (Show Cycle)	t_{SCLDH}	10	—	ns
73	$\overline{\text{BKPT}}$ Input Setup Time	t_{BKST}	15	—	ns
74	$\overline{\text{BKPT}}$ Input Hold Time	t_{BKHT}	10	—	ns
75	Mode Select Setup Time	t_{MSS}	20	—	t_{cyc}
76	Mode Select Hold Time	t_{MSH}	0	—	ns
77	$\overline{\text{RESET}}$ Assertion Time[10]	t_{RSTA}	4	—	t_{cyc}
78	$\overline{\text{RESET}}$ Rise Time[11,12]	t_{RSTR}	—	10	t_{cyc}

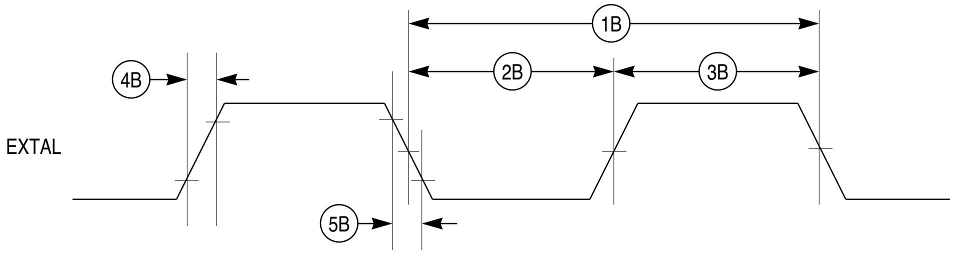
NOTES:

1. All AC timing is shown with respect to 20% V_{DD} and 70% V_{DD} levels unless otherwise noted.
2. When an external clock is used, minimum high and low times are based on a 50% duty cycle. The minimum allowable t_{Xcyc} period is reduced when the duty cycle of the external clock varies. The relationship between external clock input duty cycle and minimum t_{Xcyc} is expressed:
   Minimum t_{Xcyc} period = minimum t_{XCHL} / (50% – external clock input duty cycle tolerance).
3. Specification 9A is the worst-case skew between $\overline{\text{AS}}$ and $\overline{\text{DS}}$ or $\overline{\text{CS}}$. The amount of skew depends on the relative loading of these signals. When loads are kept within specified limits, skew will not cause $\overline{\text{AS}}$ and $\overline{\text{DS}}$ to fall outside the limits shown in specification 9.
4. If multiple chip selects are used, $\overline{\text{CS}}$ width negated (specification 15) applies to the time from the negation of a heavily loaded chip select to the assertion of a lightly loaded chip select. The $\overline{\text{CS}}$ width negated specification between multiple chip selects does not apply to chip selects being used for synchronous ECLK cycles.
5. Hold times are specified with respect to $\overline{\text{DS}}$ or $\overline{\text{CS}}$ on asynchronous reads and with respect to CLKOUT on fast cycle reads. The user is free to use either hold time.
6. Maximum value is equal to (t_{cyc} / 2) + 25 ns.
7. If the asynchronous setup time (specification 47A) requirements are satisfied, the $\overline{\text{DSACK[1:0]}}$ low to data setup time (specification 31) and $\overline{\text{DSACK[1:0]}}$ low to $\overline{\text{BERR}}$ low setup time (specification 48) can be ignored. The data must only satisfy the data-in to clock low setup time (specification 27) for the following clock cycle. $\overline{\text{BERR}}$ must satisfy only the late $\overline{\text{BERR}}$ low to clock low setup time (specification 27A) for the following clock cycle.
8. To ensure coherency during every operand transfer, $\overline{\text{BG}}$ is not asserted in response to $\overline{\text{BR}}$ until after all cycles of the current operand transfer are complete.
9. In the absence of $\overline{\text{DSACK[1:0]}}$, $\overline{\text{BERR}}$ is an asynchronous input using the asynchronous setup time (specification 47A).
10. After external $\overline{\text{RESET}}$ negation is detected, a short transition period (approximately 2) t_{cyc} elapses, then the SIM drives $\overline{\text{RESET}}$ low for 512 t_{cyc}.
11. External assertion of the $\overline{\text{RESET}}$ input can overlap internally-generated resets. To insure that an external reset is recognized in all cases, $\overline{\text{RESET}}$ must be asserted for at least 590 CLKOUT cycles.
12. External logic must pull $\overline{\text{RESET}}$ high during this period in order for normal MCU operation to begin.



68300 CLKOUT TIM

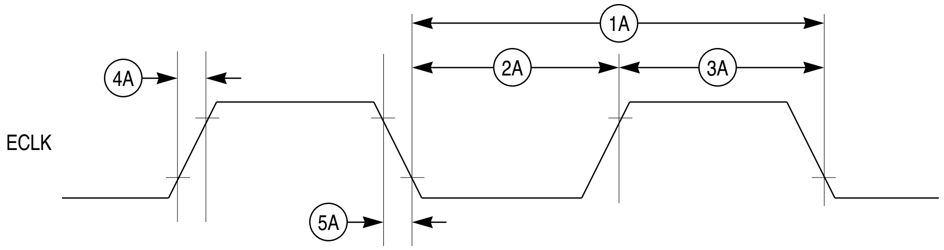
Figure 1 CLKOUT Output Timing Diagram



NOTE: TIMING SHOWN WITH RESPECT TO 20% AND 70% V_{DD}.
PULSE WIDTH SHOWN WITH RESPECT TO 50% V_{DD}.

68300 EXT CLK INPUT TIM

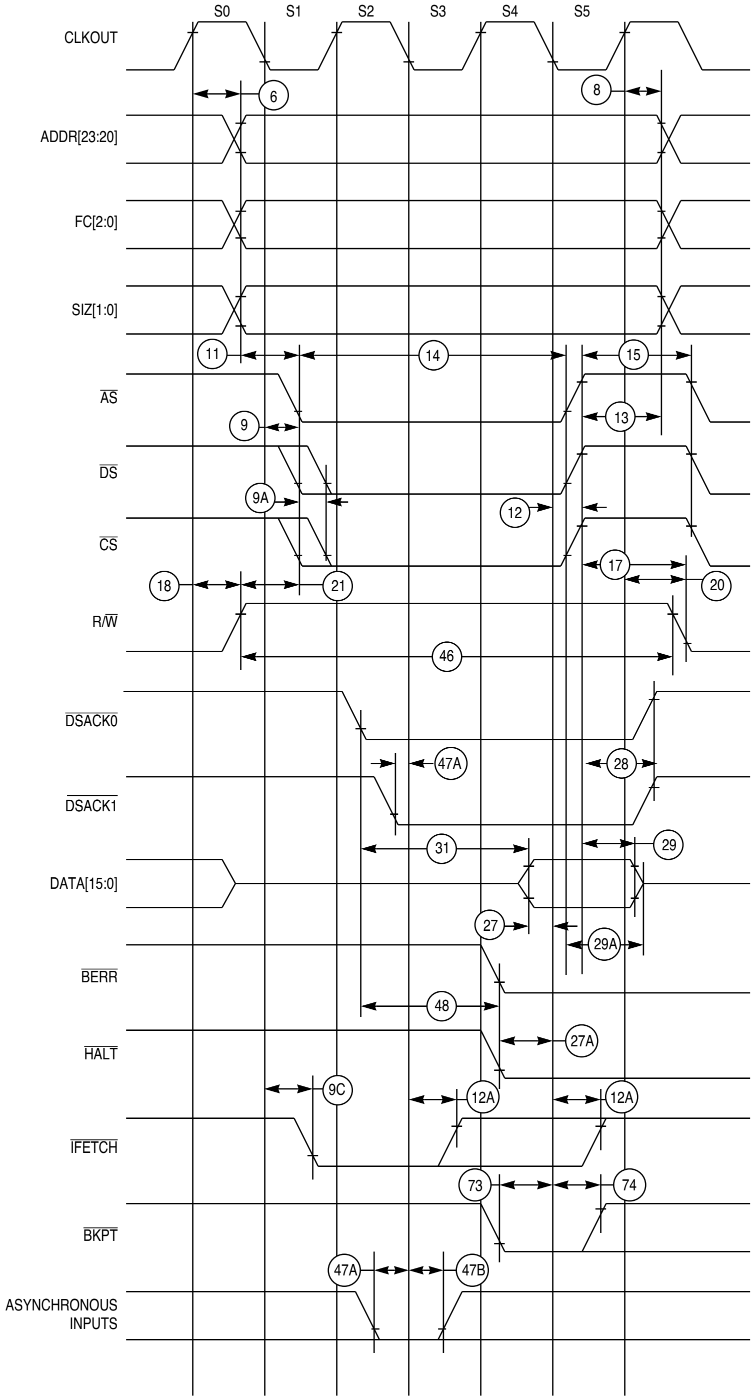
Figure 2 External Clock Input Timing Diagram



NOTE: TIMING SHOWN WITH RESPECT TO 20% AND 70% V_{DD}.

68300 ECLK OUTPUT TIM

Figure 3 ECLK Output Timing Diagram



68300 RD CYC TIM

Figure 4 Read Cycle Timing Diagram

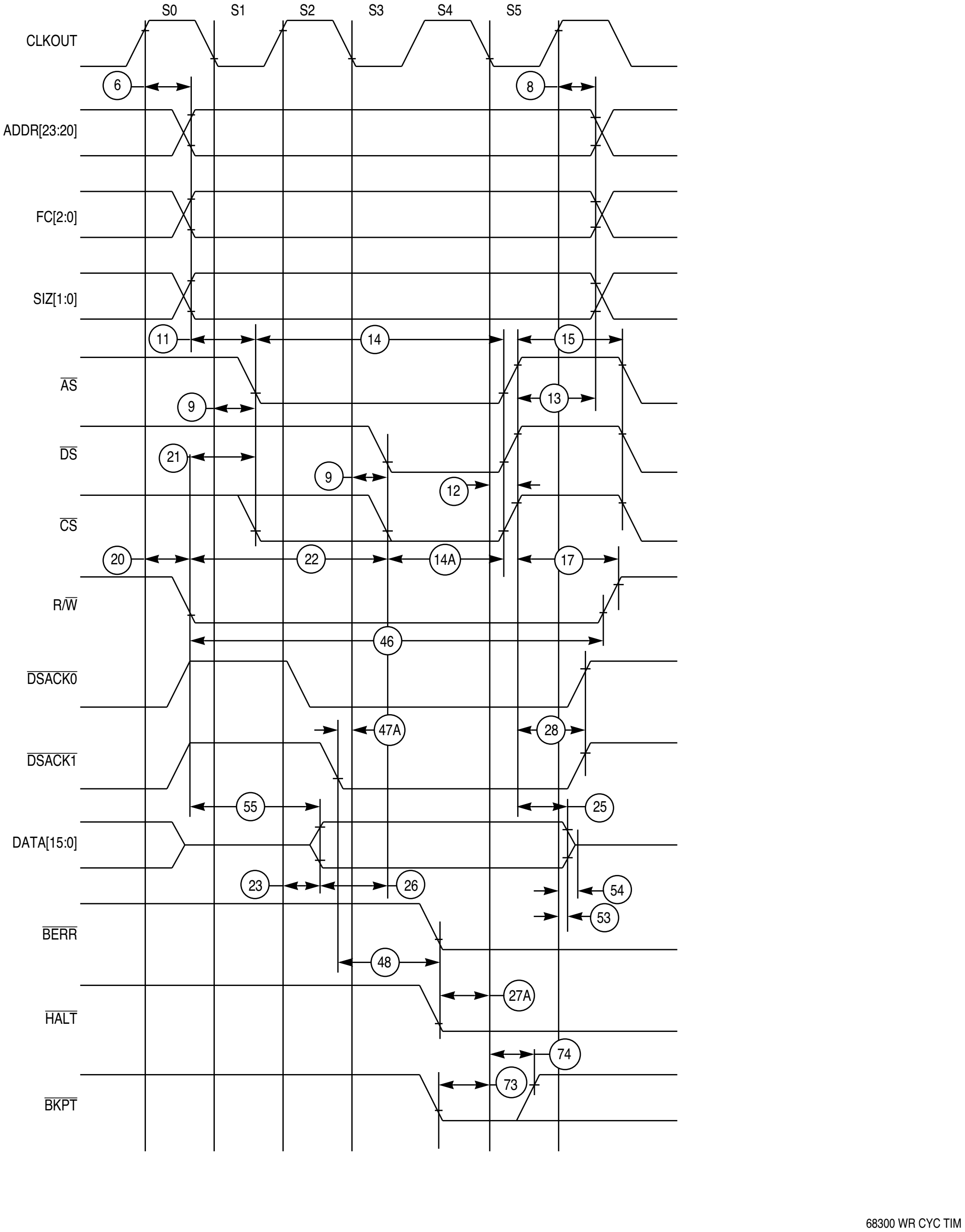


Figure 5 Write Cycle Timing Diagram

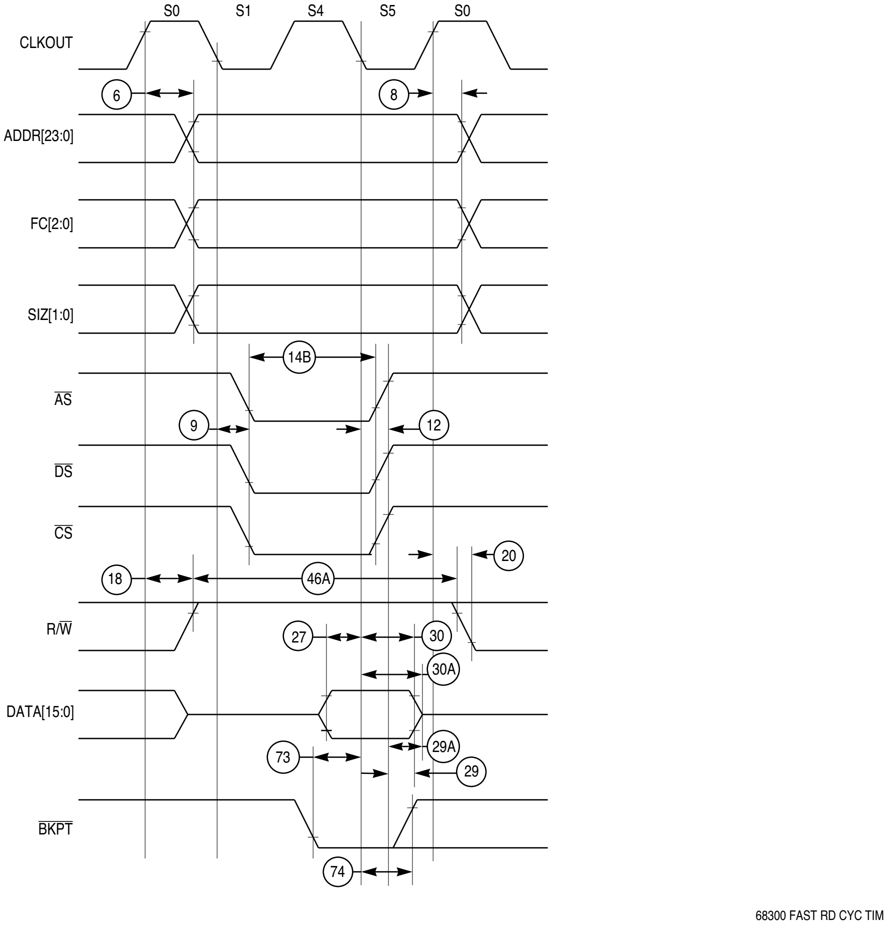


Figure 6 Fast Termination Read Cycle Timing Diagram

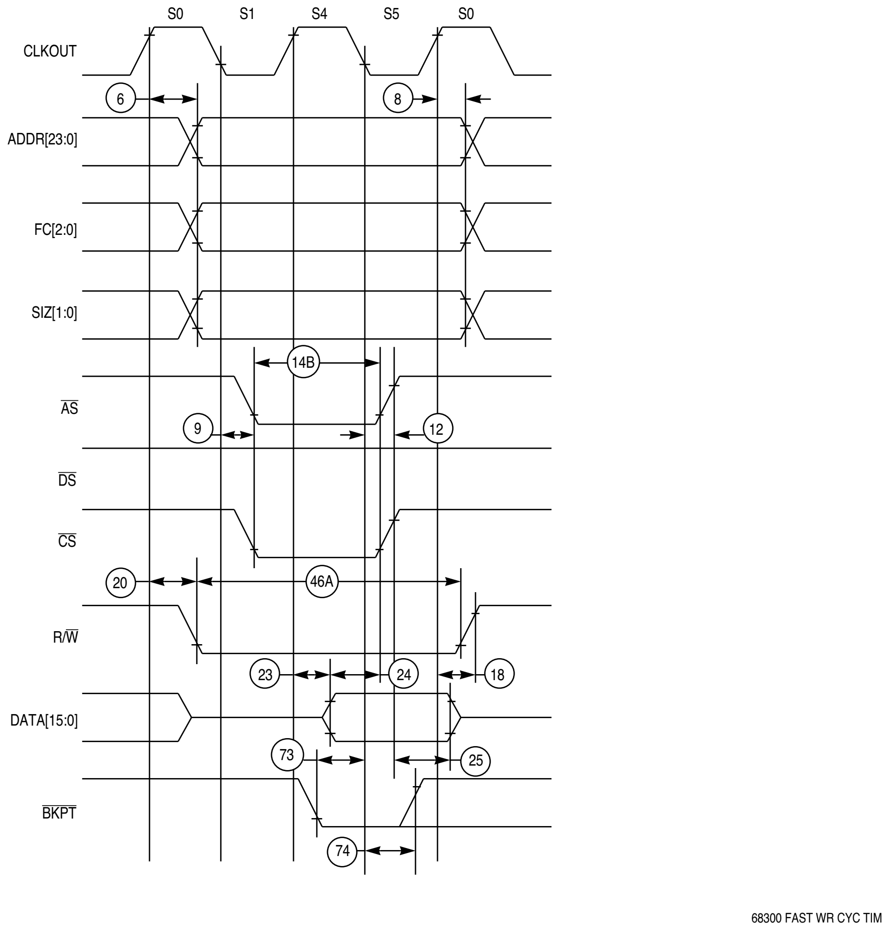


Figure 7 Fast Termination Write Cycle Timing Diagram

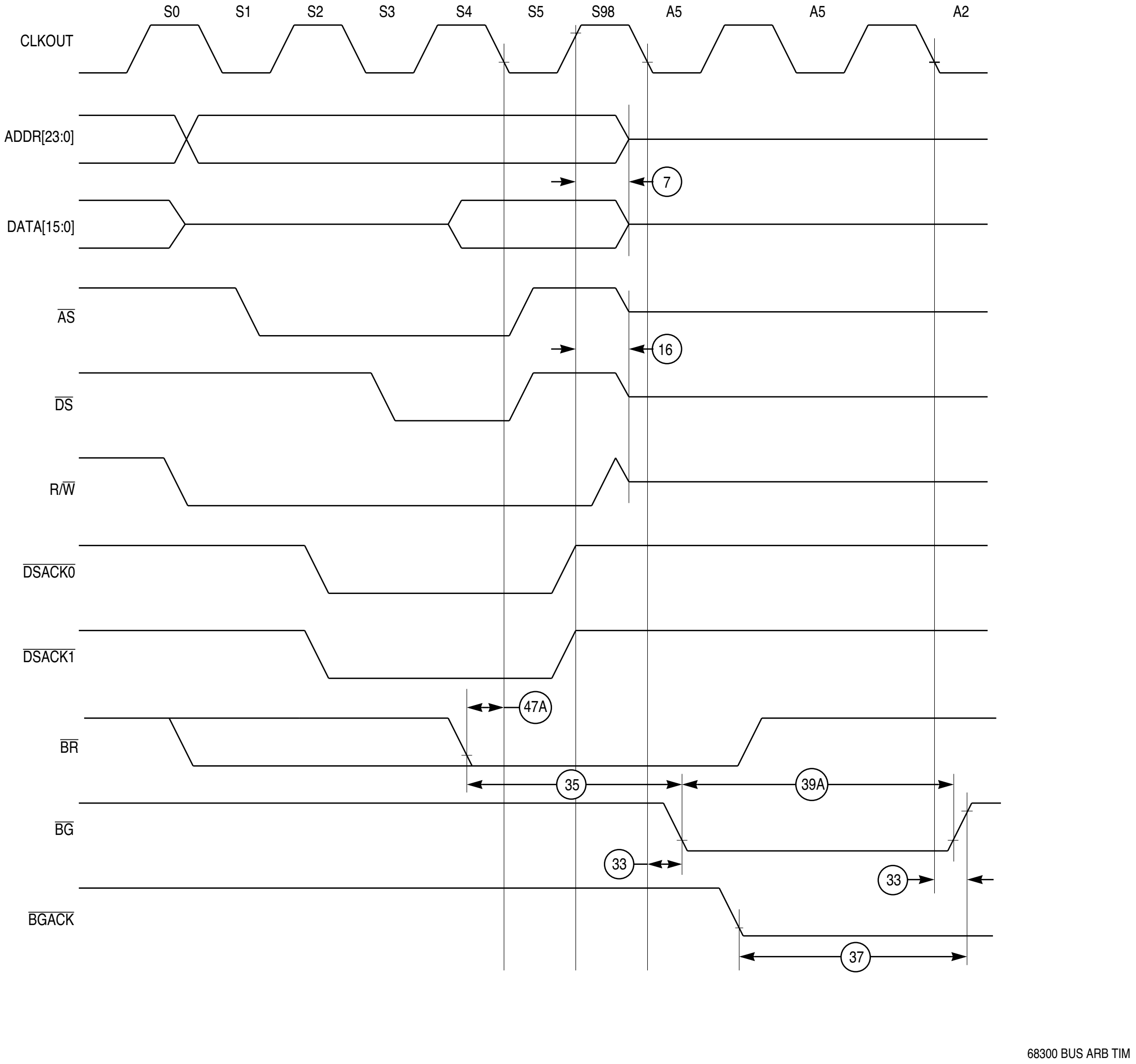


Figure 8 Bus Arbitration Timing Diagram — Active Bus Case

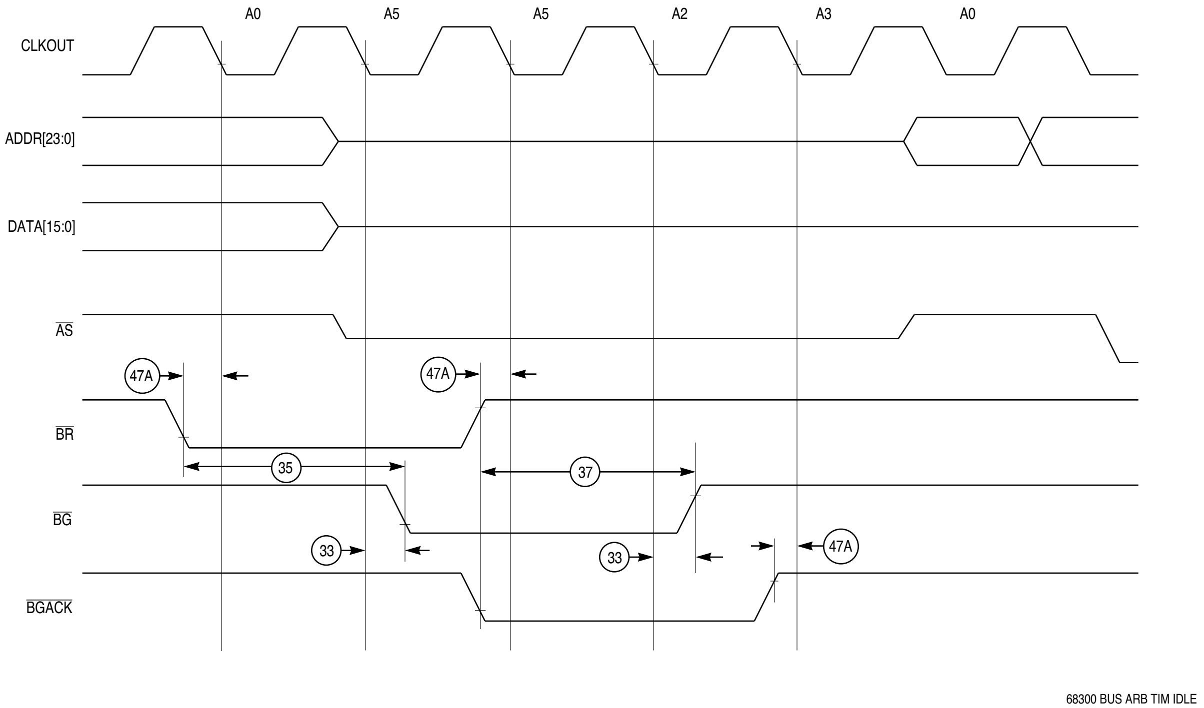
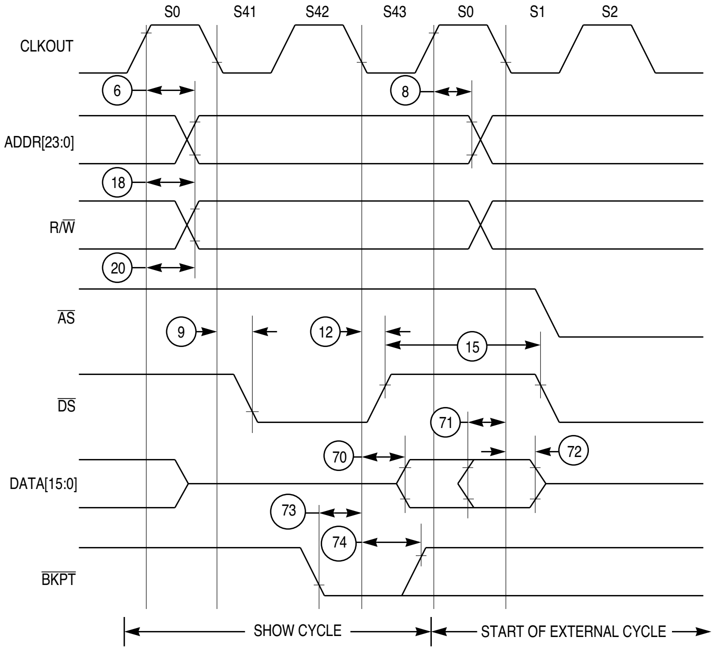


Figure 9 Bus Arbitration Timing Diagram — Idle Bus Case



NOTE:
Show cycles can stretch during clock phase S42 when bus accesses take longer than two cycles due to IMB module wait-state insertion.

Figure 10 Show Cycle Timing Diagram

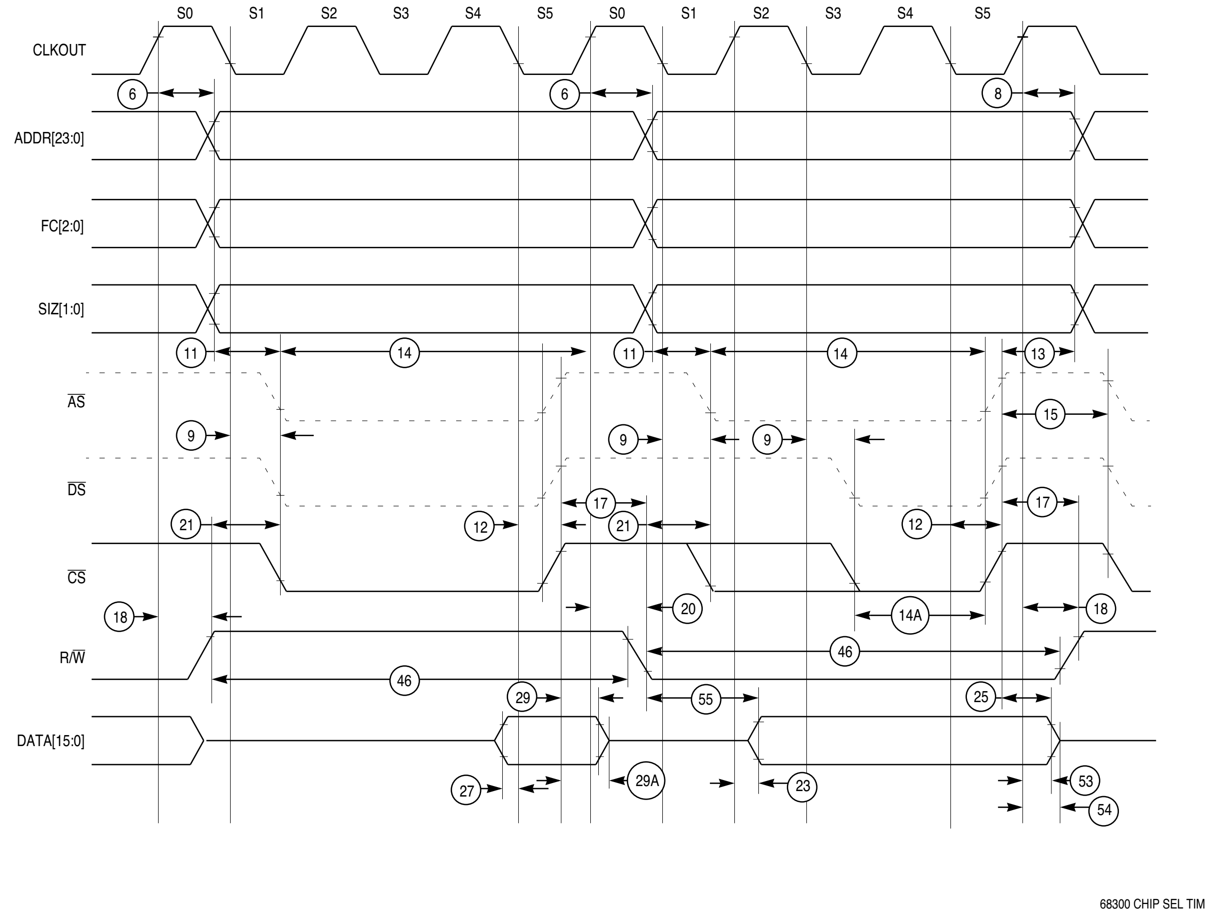


Figure 11 Chip-Select Timing Diagram

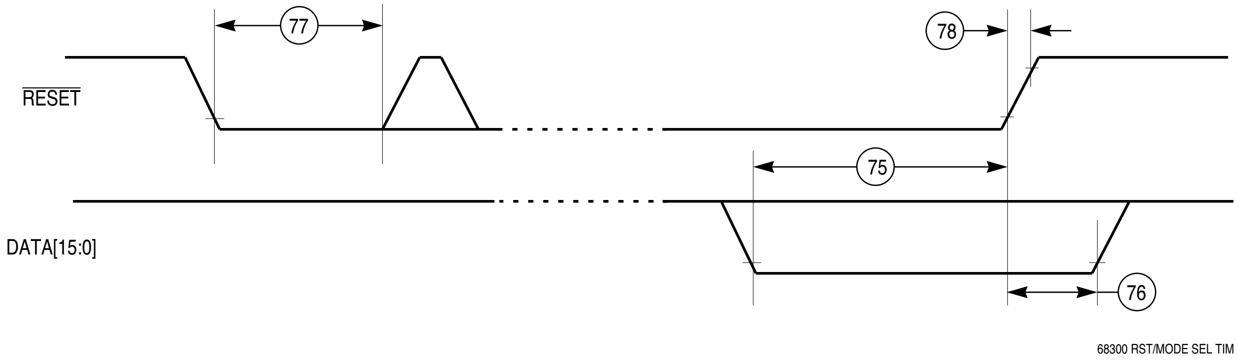


Figure 12 Reset and Mode Select Timing Diagram

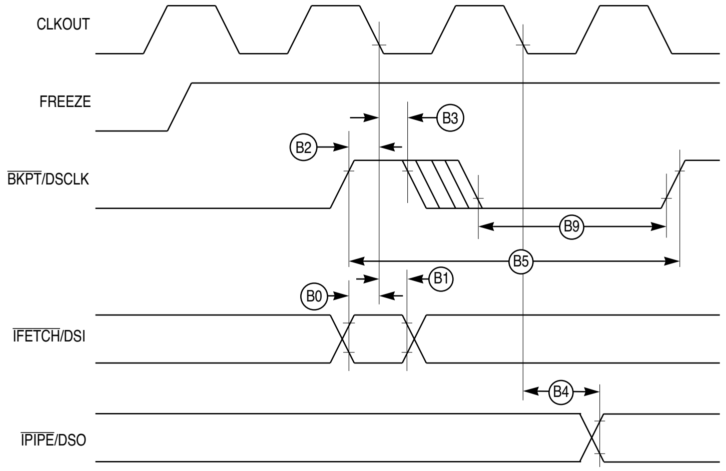
Table 7 Background Debugging Mode Timing

(V_{DD} and V_{DDSYN} = 3.0 to 3.6Vdc, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)[1]

Num	Characteristic	Symbol	Min	Max	Unit
B0	DSI Input Setup Time	t_{DSISU}	15	—	ns
B1	DSI Input Hold Time	t_{DSIH}	10	—	ns
B2	DSCLK Setup Time	t_{DSCSU}	15	—	ns
B3	DSCLK Hold Time	t_{DSCH}	10	—	ns
B4	DSO Delay Time	t_{DSOD}	—	25	ns
B5	DSCLK Cycle Time	t_{DSCCYC}	2	—	t_{cyc}
B6	CLKOUT Low to FREEZE Asserted/Negated	t_{FRZAN}	—	50	ns
B7	CLKOUT High to $\overline{\text{IFETCH}}$ High Impedance	t_{IPZ}	—	50	ns
B8	CLKOUT High to $\overline{\text{IFETCH}}$ Valid	t_{IP}	—	50	ns
B9	DSCLK Low Time	t_{DSCLO}	1	—	t_{cyc}

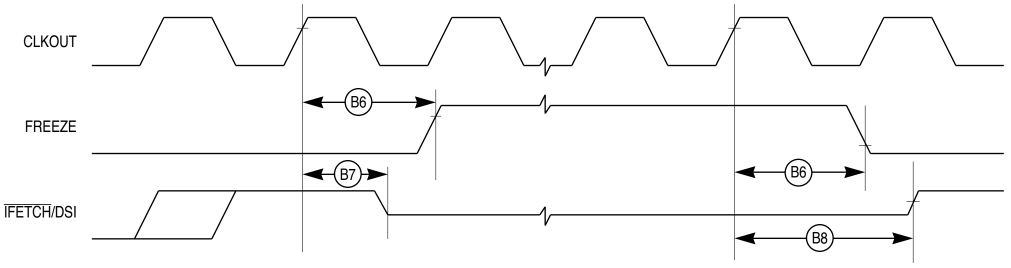
NOTES:

1. All AC timing is shown with respect to 20% V_{DD} and 70% V_{DD} levels unless otherwise noted.



68300 BKGD DBM SER COM TIM

Figure 13 BDM Serial Communication Timing Diagram



68300 BDM FRZ TIM

Figure 14 BDM Freeze Assertion Timing Diagram

Table 8 ECLK Bus Timing

(V_{DD} and V_{DDSYN} = 3.0 to 3.6Vdc, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)[1]

Num	Characteristic	Symbol	Min	Max	Unit
E1	ECLK Low to Address Valid[2]	t_{EAD}	—	60	ns
E2	ECLK Low to Address Hold	t_{EAH}	15	—	ns
E3	ECLK Low to $\overline{\text{CS}}$ Valid ($\overline{\text{CS}}$ Delay)	t_{ECSD}	—	150	ns
E4	ECLK Low to $\overline{\text{CS}}$ Hold	t_{ECSH}	15	—	ns
E5	$\overline{\text{CS}}$ Negated Width	t_{ECSN}	30	—	ns
E6	Read Data Setup Time	t_{EDSR}	30	—	ns
E7	Read Data Hold Time	t_{EDHR}	5	—	ns
E8	ECLK Low to Data High Impedance	t_{EDHZ}	—	60	ns
E9	$\overline{\text{CS}}$ Negated to Data Hold (Read)	t_{ECDH}	0	—	ns
E10	$\overline{\text{CS}}$ Negated to Data High Impedance	t_{ECDZ}	—	1	t_{cyc}
E11	ECLK Low to Data Valid (Write)	t_{EDDW}	—	2	t_{cyc}
E12	ECLK Low to Data Hold (Write)	t_{EDHW}	15	—	ns
E13	Address Access Time (Read)[3]	t_{EACC}	386	—	ns
E14	Chip-Select Access Time (Read)[4]	t_{EACS}	296	—	ns
E15	Address Setup Time	t_{EAS}	1/2	—	t_{cyc}

NOTES:

1. All AC timing is shown with respect to 20% V_{DD} and 70% V_{DD} levels unless otherwise noted.
2. When previous bus cycle is not an ECLK cycle, the address may be valid before ECLK goes low.
3. Address access time = $t_{Ecyc} - t_{EAD} - t_{EDSR}$.
4. Chip select access time = $t_{Ecyc} - t_{ECSD} - t_{EDSR}$.

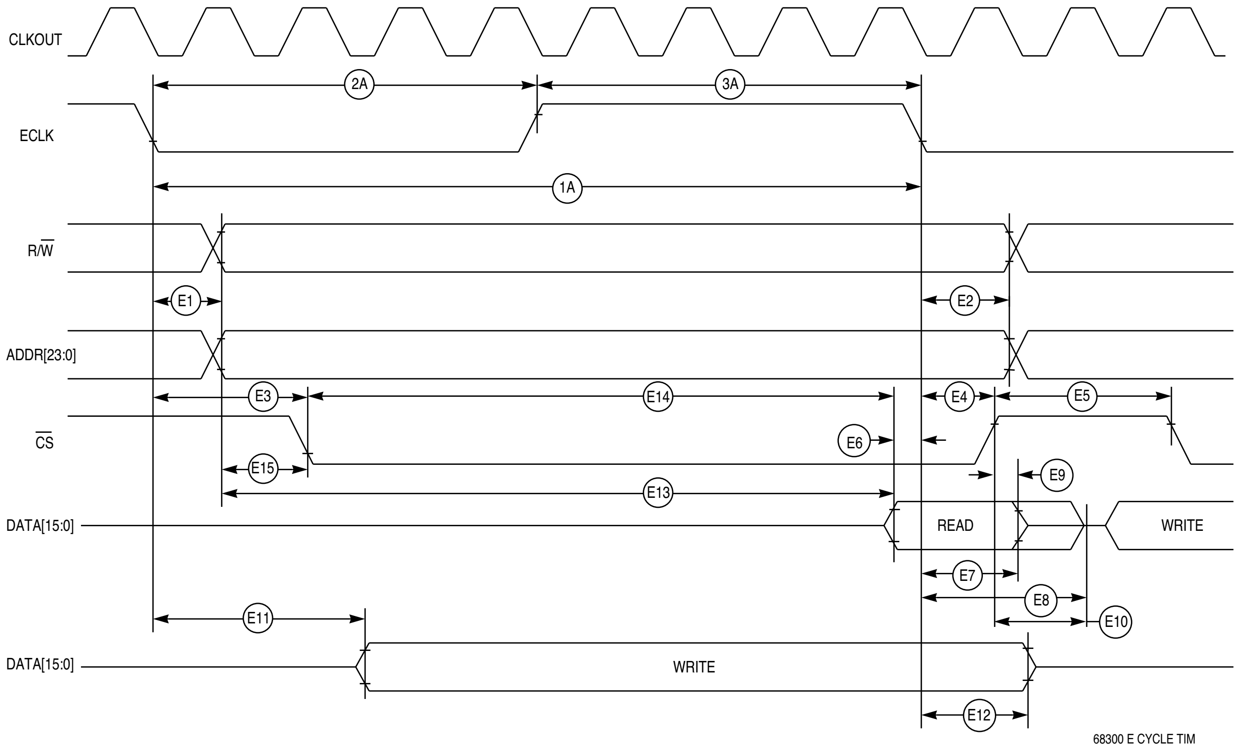


Figure 15 ECLK Timing Diagram

Table 9 QSPI Timing

(V_{DD} and V_{DDSYN} = 3.0 to 3.6Vdc, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H , 100 pF load on all QSPI pins)[1]

Num	Function	Symbol	Min	Max	Unit
1	Operating Frequency Master Slave	f_{op}	DC DC	1/4 1/4	f_{sys} f_{sys}
2	Cycle Time Master Slave	t_{qcyc}	4 4	510 —	t_{cyc} t_{cyc}
3	Enable Lead Time Master Slave	t_{lead}	2 2	128 —	t_{cyc} t_{cyc}
4	Enable Lag Time Master Slave	t_{lag}	— 2	1/2 —	SCK t_{cyc}
5	Clock (SCK) High or Low Time Master Slave[2]	t_{sw}	$2\ t_{cyc} - 60$ $2\ t_{cyc} - n$	$255\ t_{cyc}$ —	ns ns
6	Sequential Transfer Delay Master Slave (Does Not Require Deselect)	t_{td}	17 13	8192 —	t_{cyc} t_{cyc}
7	Data Setup Time (Inputs) Master Slave	t_{su}	30 20	— —	ns ns
8	Data Hold Time (Inputs) Master Slave	t_{hi}	0 20	— —	ns ns
9	Slave Access Time	t_a	—	1	t_{cyc}
10	Slave MISO Disable Time	t_{dis}	—	2	t_{cyc}
11	Data Valid (after SCK Edge) Master Slave	t_v	— —	50 50	ns ns
12	Data Hold Time (Outputs) Master Slave	t_{ho}	0 0	— —	ns ns
13	Rise Time Input Output	t_{ri} t_{ro}	— —	2 30	µs ns
14	Fall Time Input Output	t_{fi} t_{fo}	— —	2 30	µs ns

NOTES:

1. All AC timing is shown with respect to 20% V_{DD} and 70% V_{DD} levels unless otherwise noted.
2. For high time, n = External SCK rise time; for low time, n = External SCK fall time.

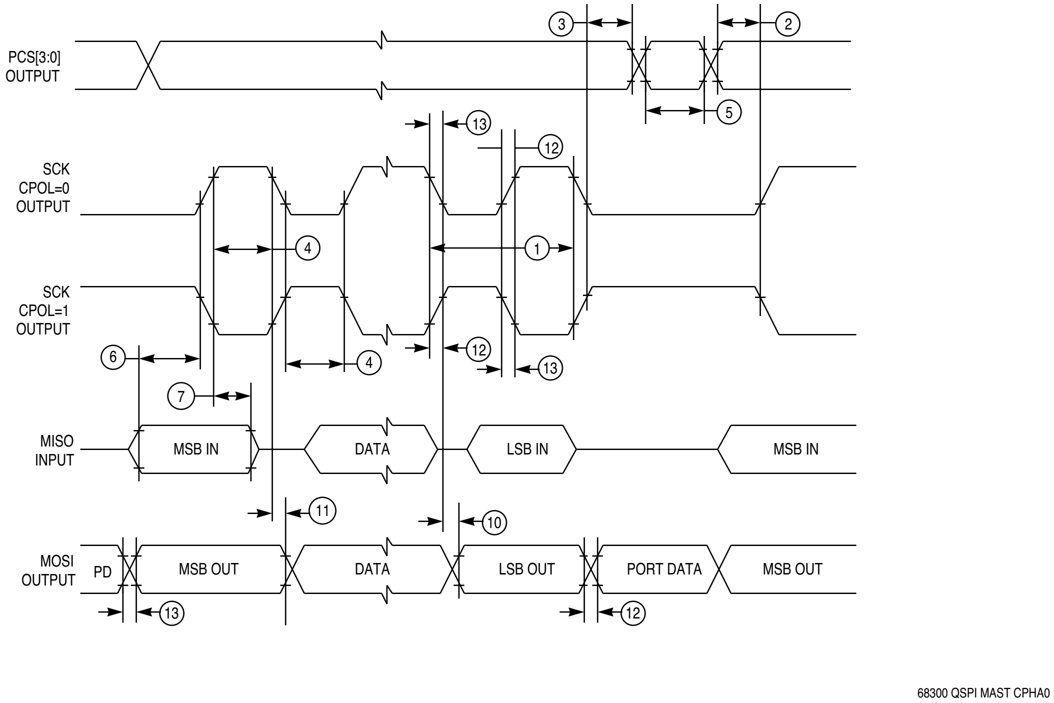


Figure 16 QSPI Timing — Master, CPHA = 0

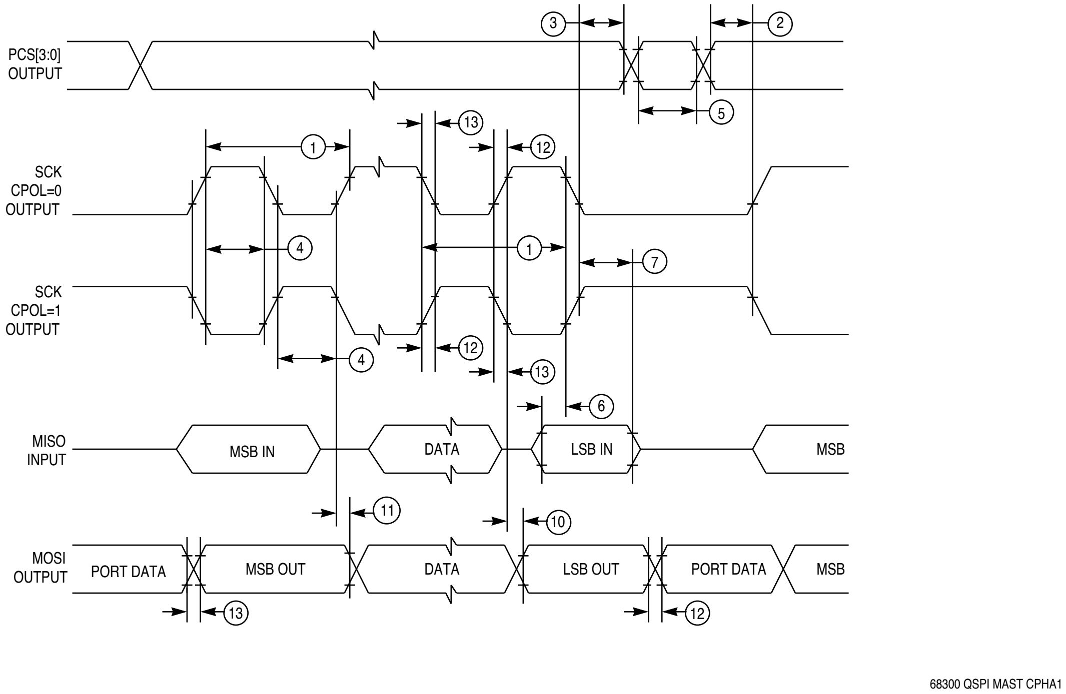


Figure 17 QSPI Timing — Master, CPHA = 1

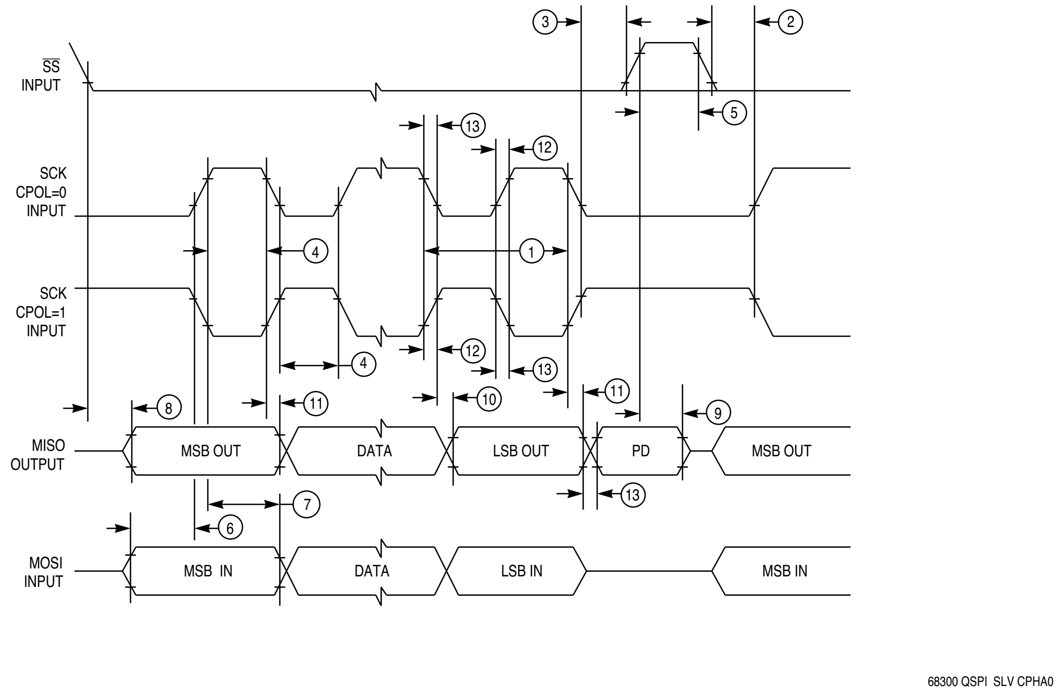


Figure 18 QSPI Timing — Slave, CPHA = 0

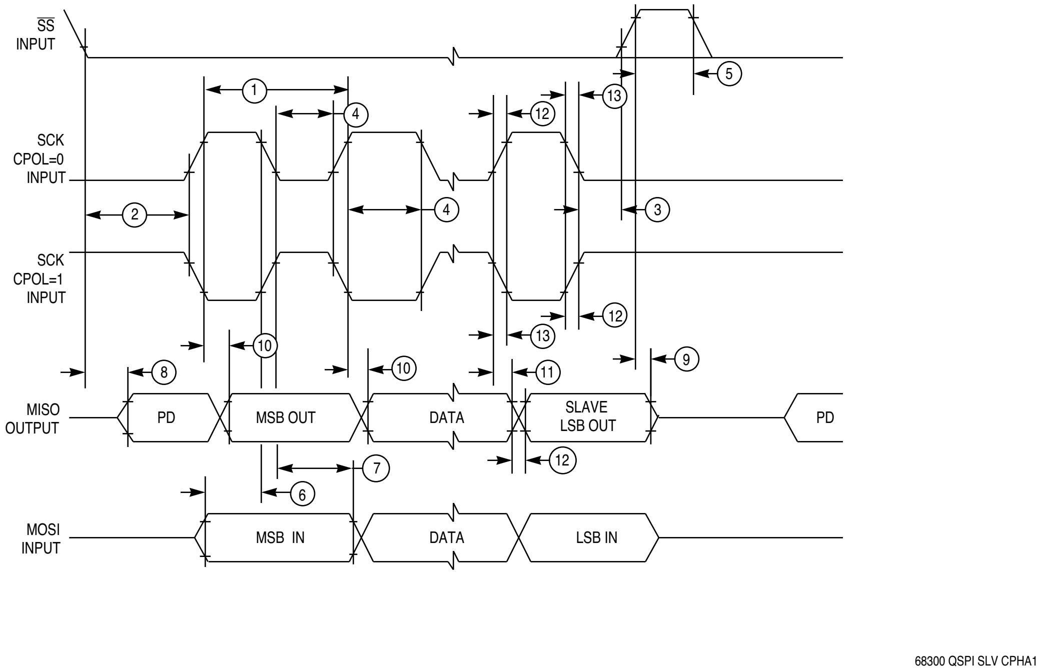


Figure 19 QSPI Timing — Slave, CPHA = 1

Table 10 Time Processor Unit Timing

(V_{DD} and V_{DDA} = 3.0 to 3.6Vdc, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)[1]

Num	Parameter	Symbol	Min	Max	Unit
1	CLKOUT High to TPU Output Channel Valid[2, 3, 4]	t_{CHTOV}	2	23	ns
2	CLKOUT High to TPU Output Channel Hold	t_{CHTOH}	0	20	ns
3	TPU Input Channel Pulse Width	t_{TIPW}	4	—	t_{cyc}

NOTES:

1. AC Timing is shown with respect to 20% V_{DD} and 70% V_{DD} levels.
2. Timing not valid for external T2CLK input.
3. Maximum load capacitance for CLKOUT pin is 90 pF.
4. Maximum load capacitance for TPU output pins is 100 pF.

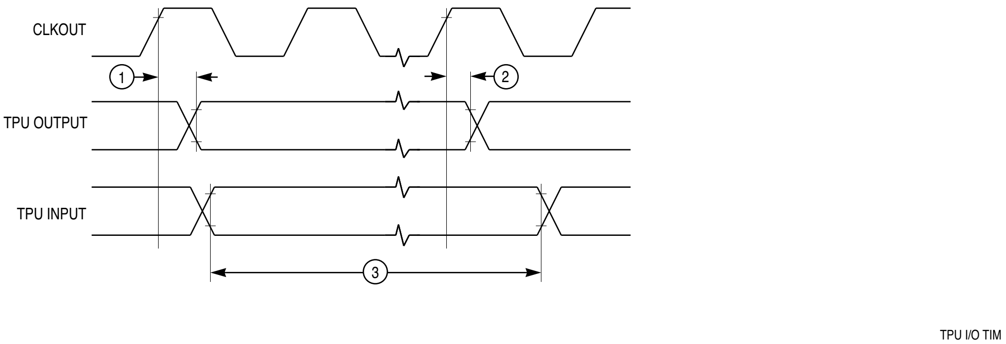
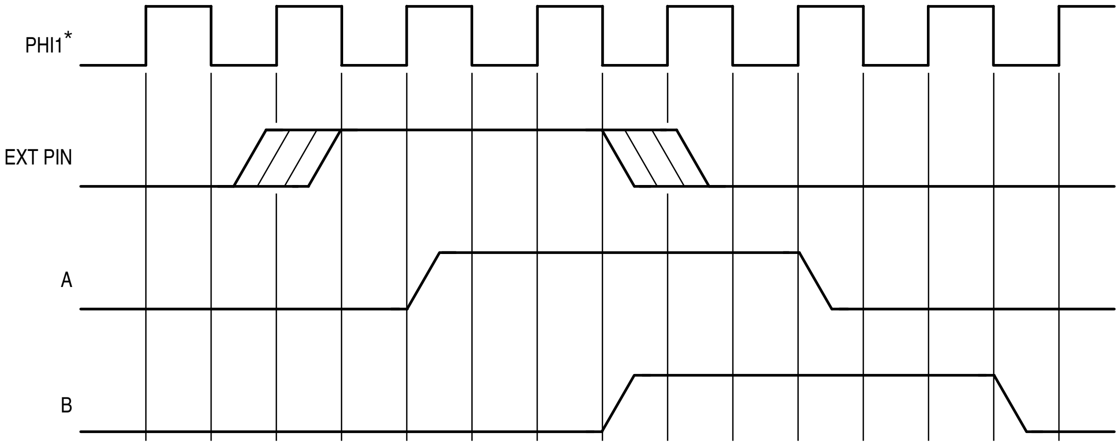


Figure 20 TPU Timing Diagram

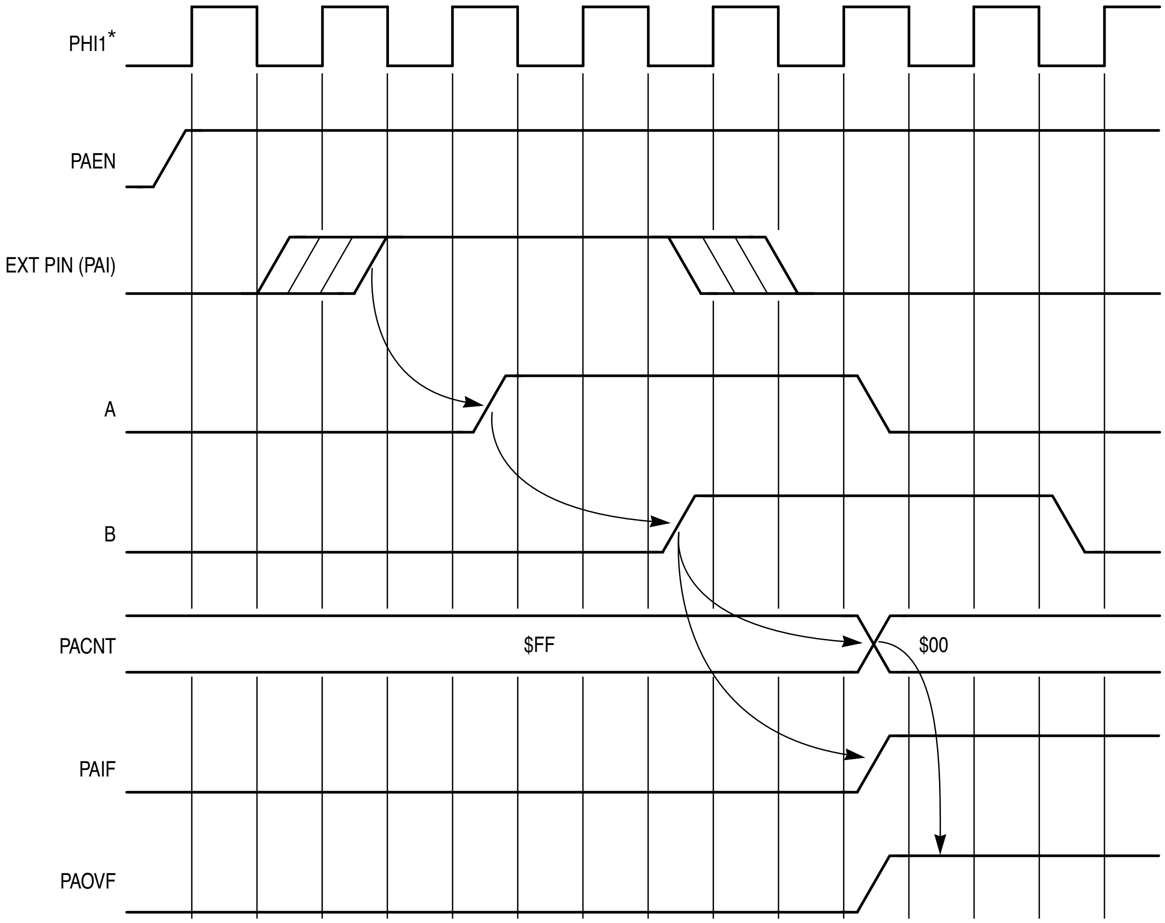
Table 11 General-Purpose Timer AC Characteristics

Num	Parameter	Symbol	Min	Max	Unit
1	Operating Frequency	Fclock	0	16.77	MHz
2	PCLK Frequency	Fpclk	0	1/4 Fclock	MHz
3	Pulse Width Input Capture	PWtim	2/Fclock	—	—
4	PWM Resolution	—	2/Fclock	—	—
5	IC/OC Resolution	—	4/Fclock	—	—
6	PCLK Width (PWM)	—	4/Fclock	—	—
7	PCLK Width (IC/OC)	—	4/Fclock	—	—
8	PAI Pulse Width	—	2/Fclock	—	—



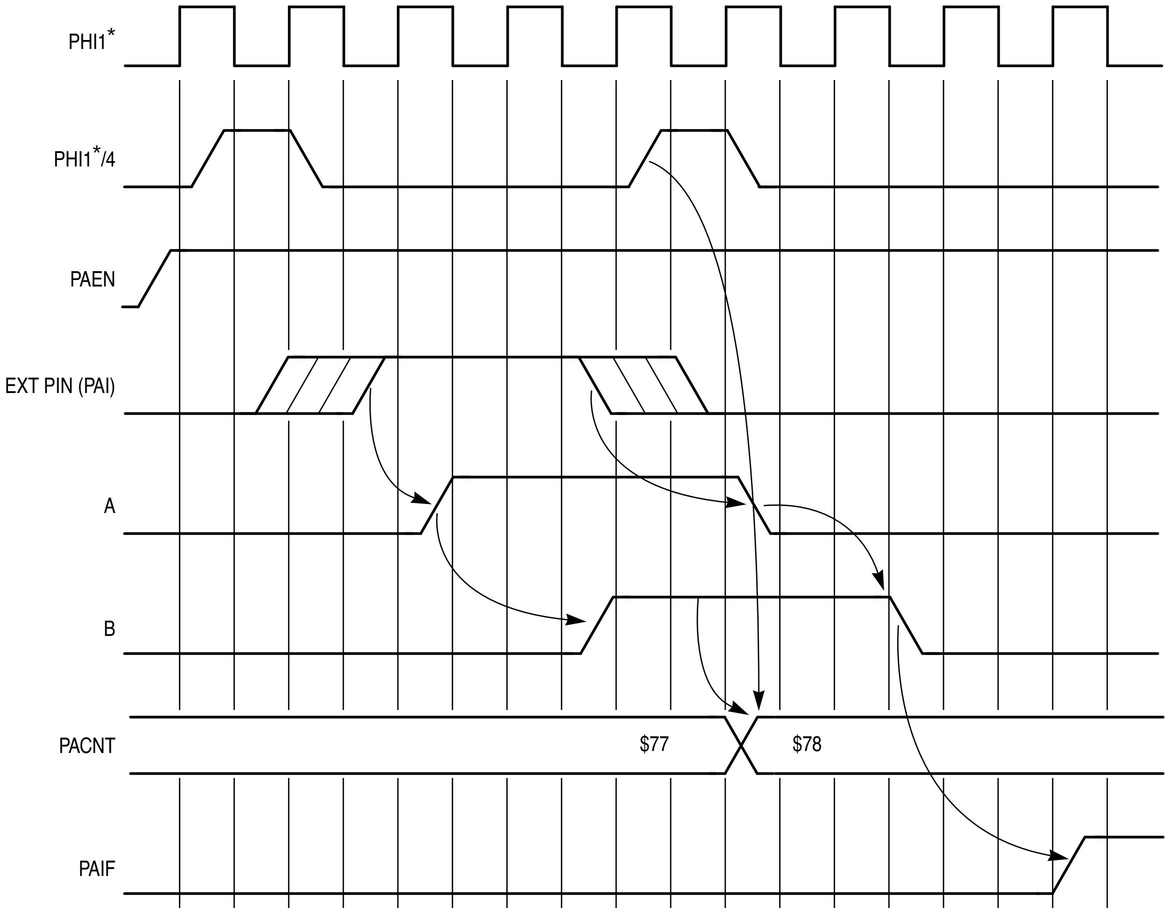
NOTE: 1. A = Input signal after the synchronizer
2. B = “A” after the digital filter
3. *PHI1 is the same frequency as system clock; however, it does not have the same timing.

Figure 21 Input Signal Conditioner Timing



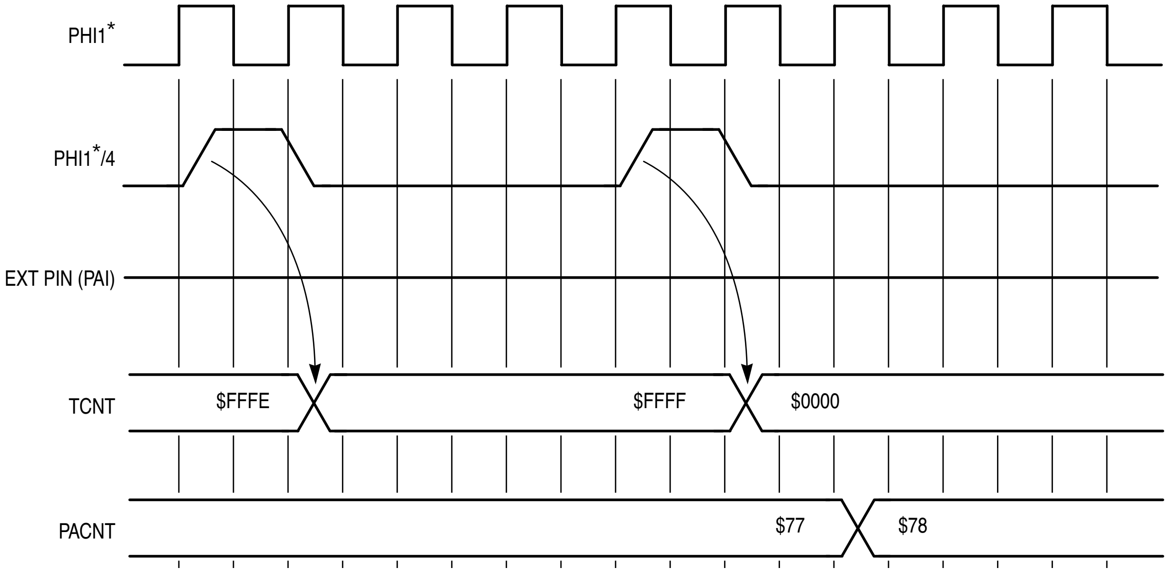
NOTE: 1. A = PAI signal after the synchronizer
2. B = “A” after the digital filter
3. *PHI1 is the same frequency as system clock; however, it does not have the same timing.
4. The external leading edge causes the pulse accumulator to increment and the PAIF flag to be set.
5. The counter transition from $FF to $00 causes the PAOVF flag to be set.

Figure 22 Pulse Accumulator — Event Counting Mode (Leading Edge)



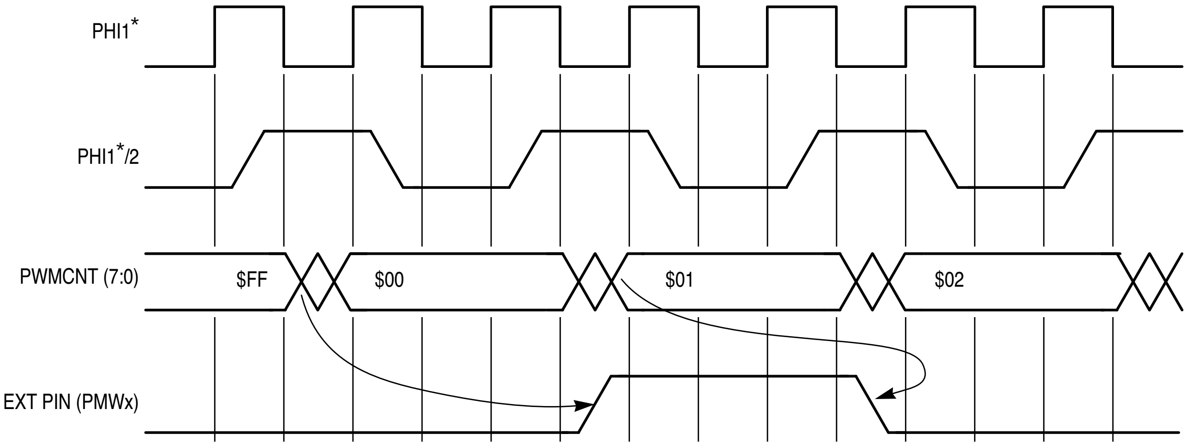
NOTE: 1. A = PAI signal after the synchronizer
2. B = “A” after the digital filter
3. PHI1*/4 clocks PACNT when GT-PAIF is asserted.
4. PAIF is asserted when PAI is negated.
5. *PHI1 has the same frequency as the system clock; however, it does not have the same timing.

Figure 23 Pulse Accumulator — Gated Mode (Count While Pin High)



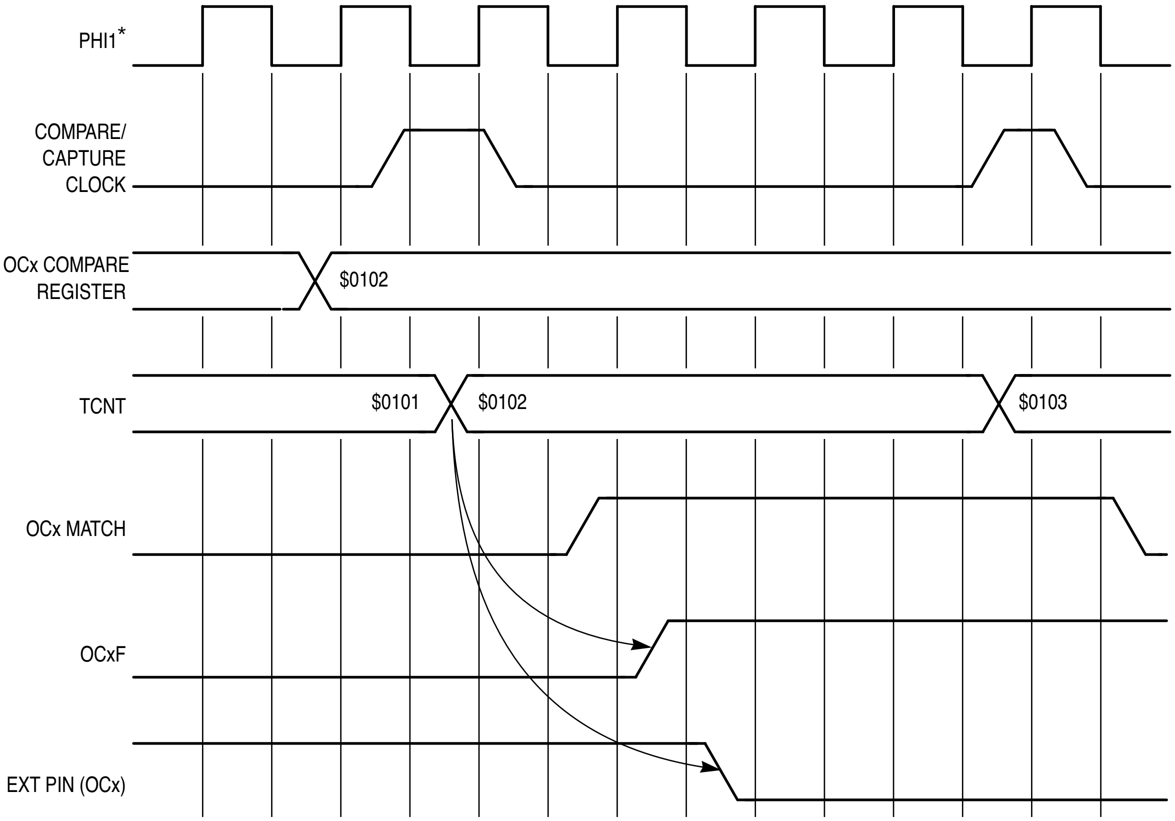
NOTE: 1. TCNT counts as a result of PHI1*/4; PACNT counts when TCNT overflows from $FFFF to $0000 and the conditioned PAI signal is asserted.
2. *PHI1 has the same frequency as the system clock; however, it does not have the same timing.

Figure 24 Pulse Accumulator — Using TOF as Gated Mode Clock



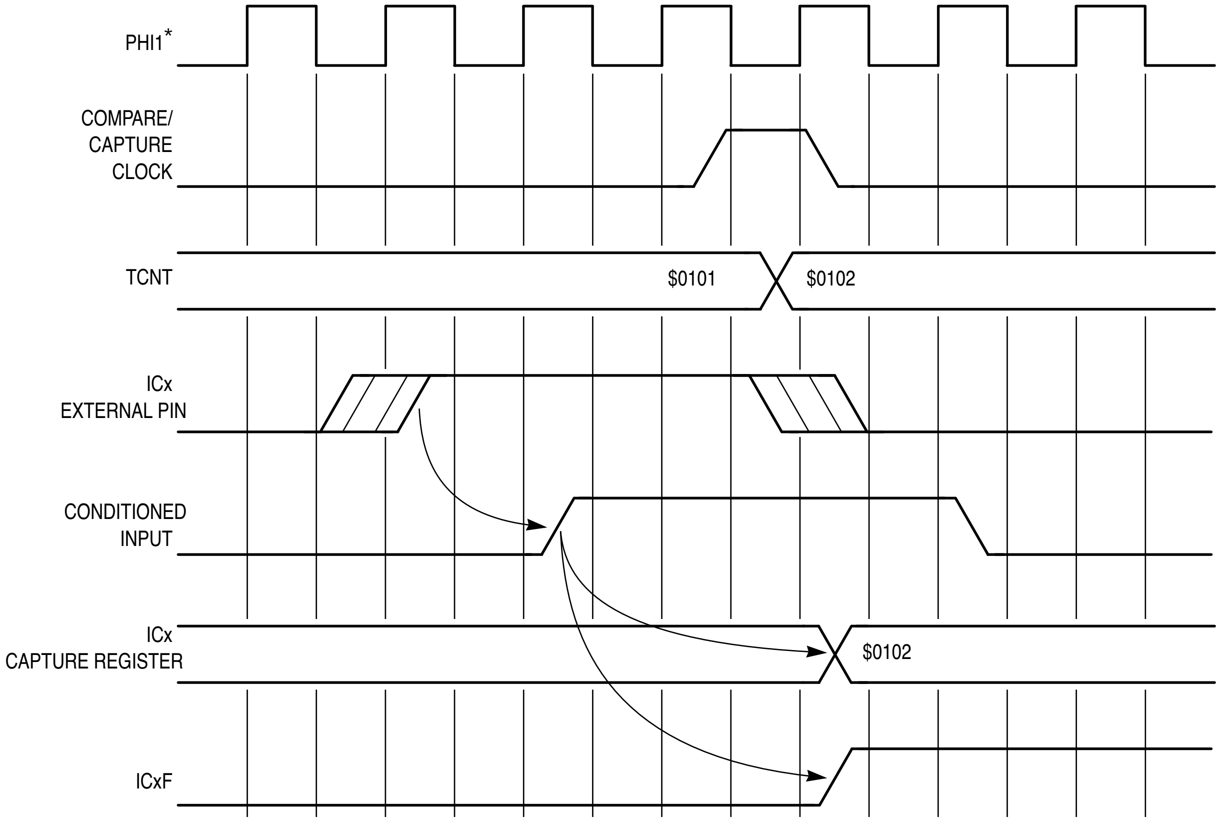
NOTE: 1. *PAI1 is the same frequency as the system clock; however, it does not have the same timing.
2. When the counter rolls over from $FF to $00, the PWM pin is set to logic level one.
3. When the counter equals the PWM register, the PWM pin is cleared to a logic level zero.

Figure 25 PWMx (PWMx Register = 01, Fast Mode)



NOTE: 1. When the TCNT matches the OCx compare register, the OCxF flag is set followed by the OCx pin changing state.
2. *PAI1 is the same frequency as the system clock; however, it does not have the same timing.

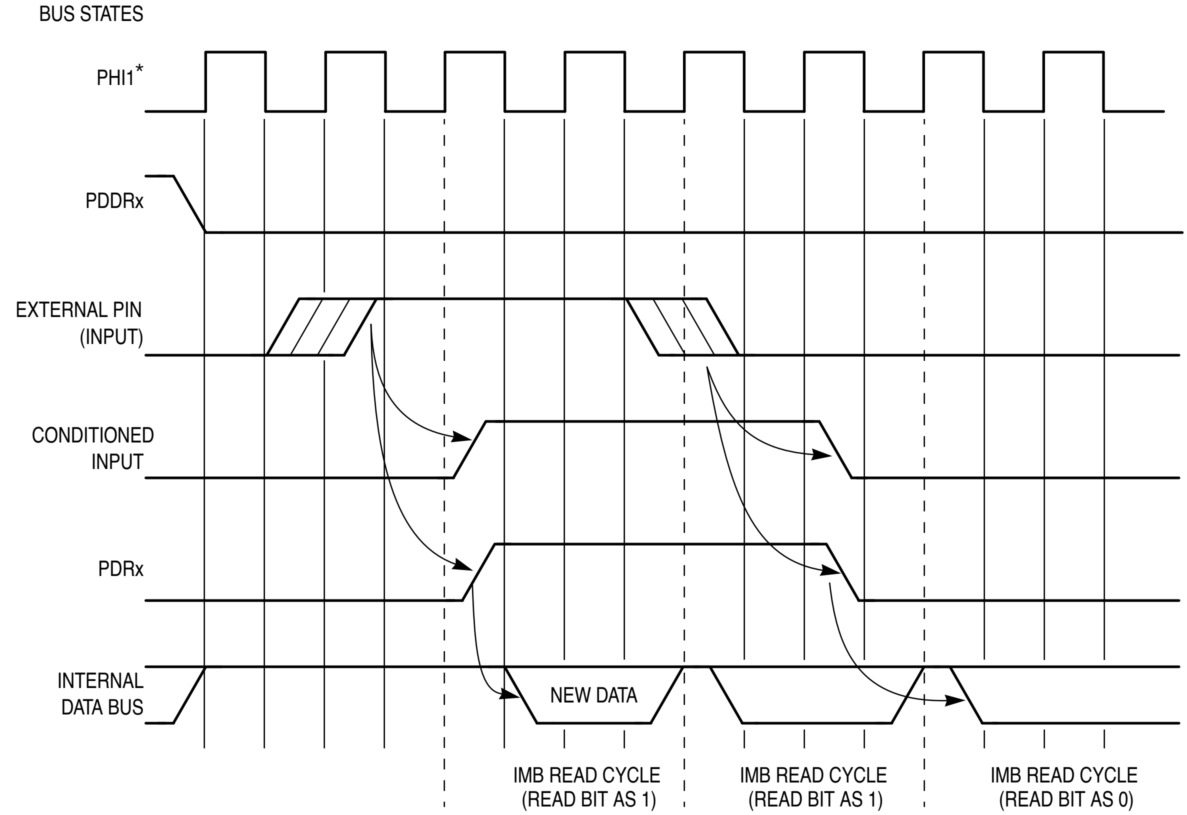
Figure 26 Output Compare (Toggle Pin State)



NOTE: 1. The conditioned input signal causes the current value of the TCNT to be latched by the ICx capture register. The ICxF flag is set at the same time.

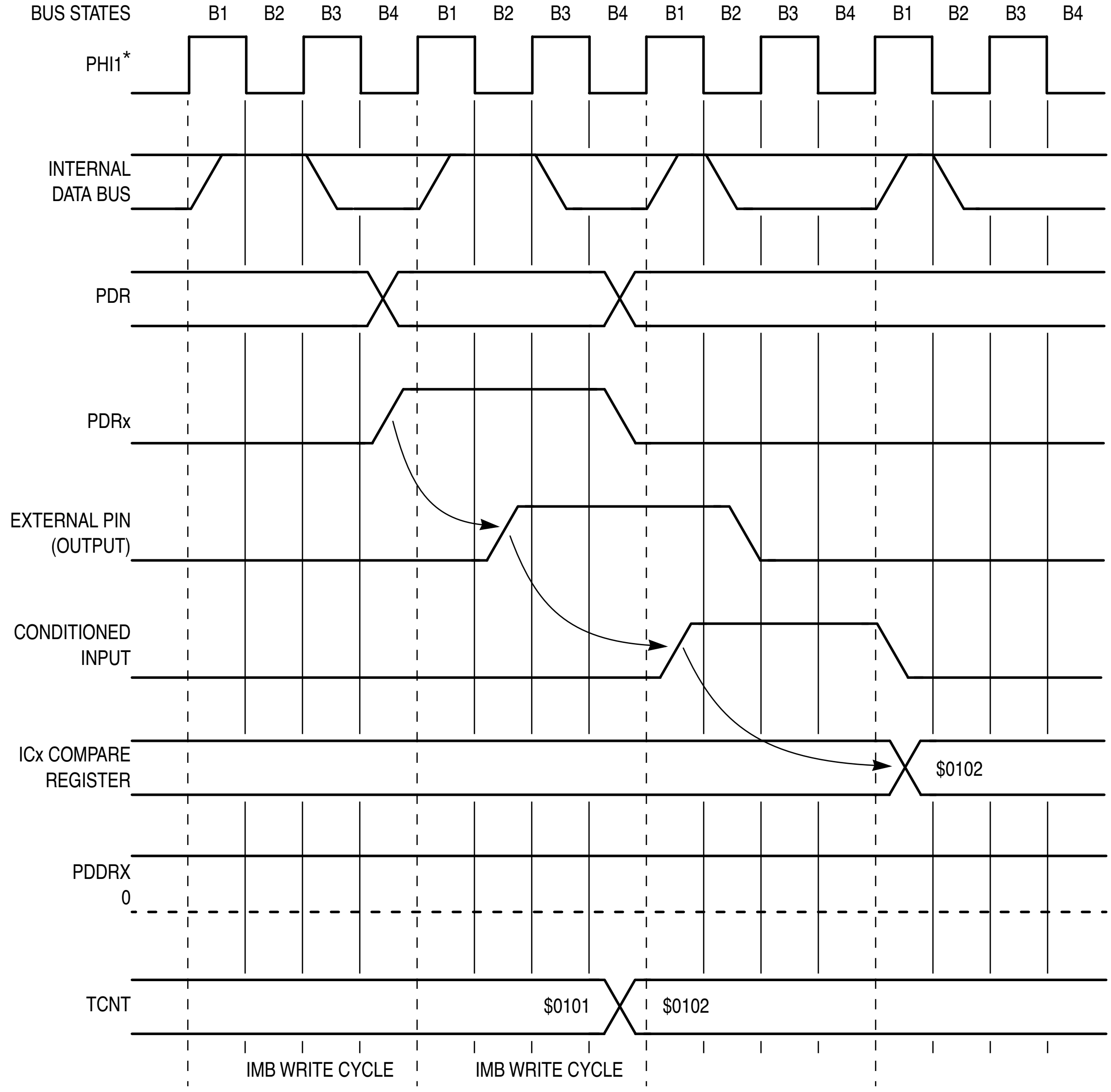
2. *PAI1 is the same frequency as the system clock; however, it does not have the same timing.

Figure 27 Input Capture (Capture on Rising Edge)



NOTE: 1. *PAI1 is the same frequency as the system clock; however, it does not have the same timing.

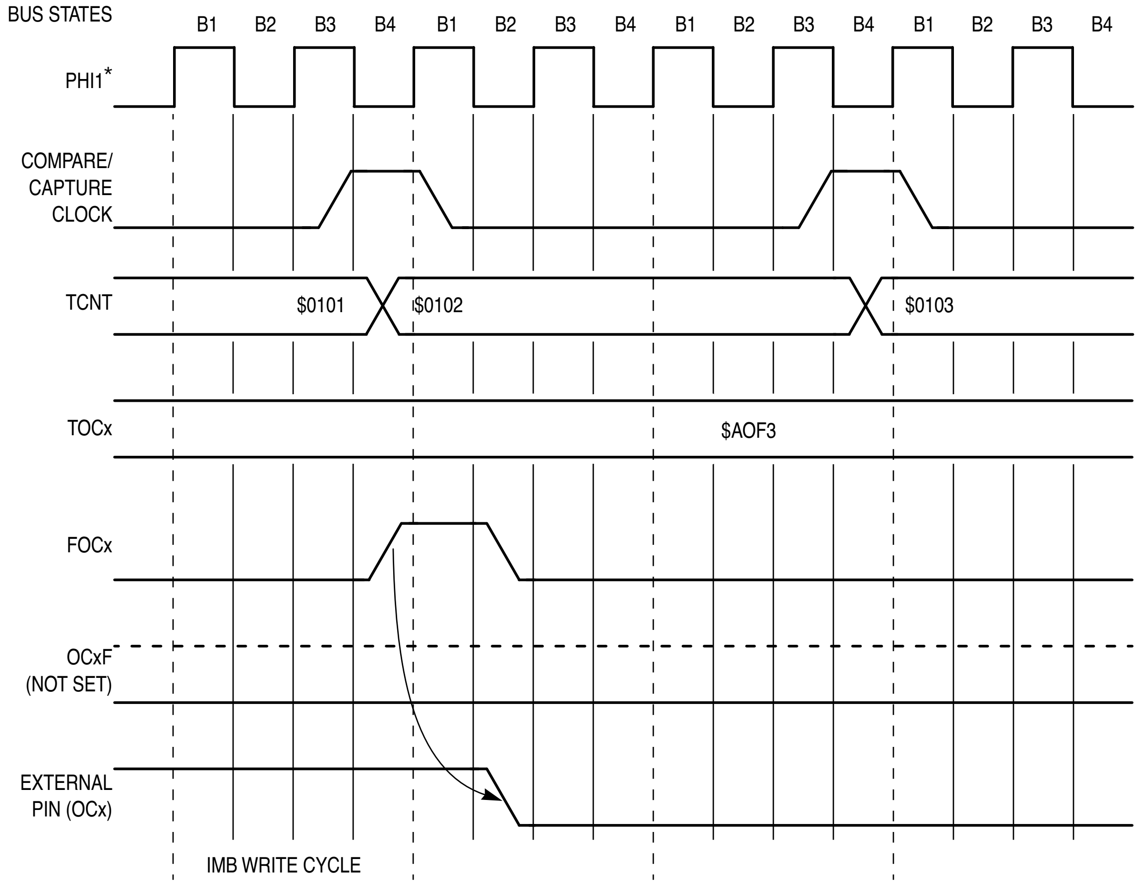
Figure 28 General-Purpose Input



NOTE: 1. *PAI1 is the same frequency as the system clock; however, it does not have the same timing.

2. When the bit value is driven on the pin, the input circuit sees the signal. After it is conditioned it causes the contents of the TCNT to be latched into the ICx compare register.

Figure 29 General-Purpose Output (Causes Input Capture)



NOTE: 1. *PAI1 is the same frequency as the system clock; however, it does not have the same timing.

Figure 30 Force Compare (CLEAR)

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