

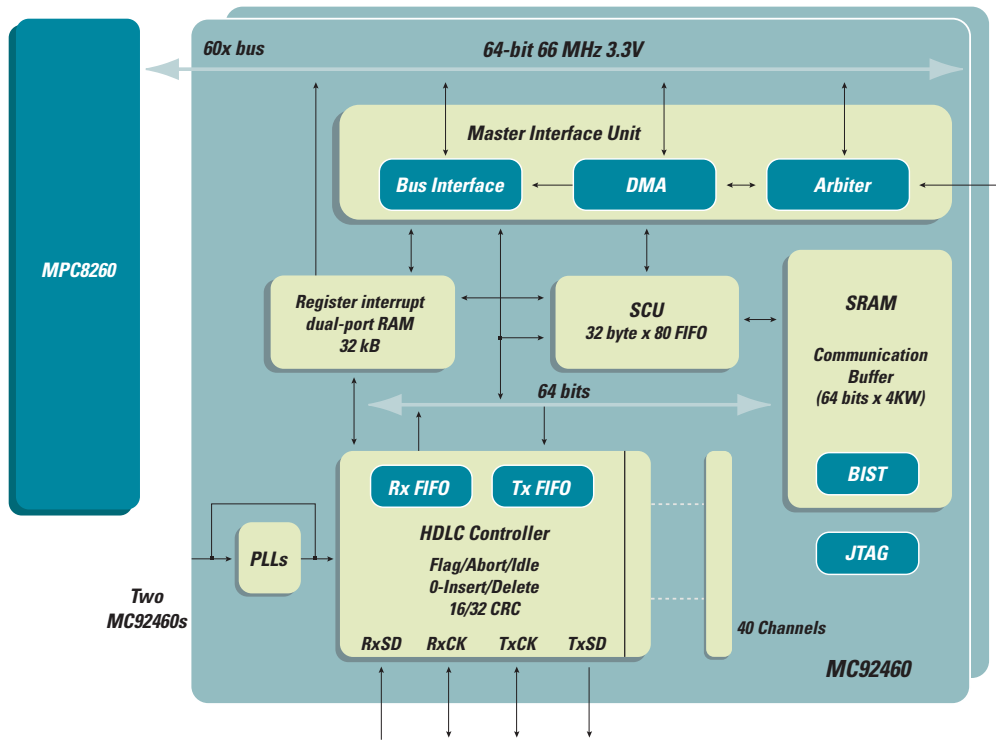
**MC92460:
MULTICHANNEL
HDLC CONTROLLER
PERIPHERAL**



The MC92460 is a 40-channel, high-level data link controller (HDLC) with an aggregate throughput of up to 1.9 Gbps across a synchronous optical network (SONET). A total of four of these peripheral devices can be connected to the 60x bus of the MPC8260 or the MPC603e.

Applications for the MC92460 include remote access concentrators, frame relay switches, high-speed direct links, regional office routers, DSLAM (xDSL) Internet access equipment, and network management in SONET/SDH systems.

Freescale Semiconductor, Inc.



MC92460 BLOCK DIAGRAM

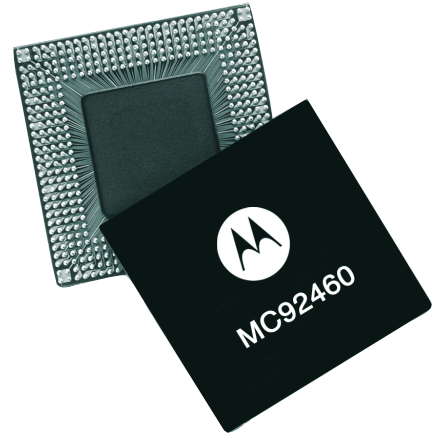
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Go to: www.freescale.com**

MC92460 FEATURES

Major features of the MC92460 include:

- Controllers
 - Maximum throughput of up to 1.9 Gbps; individual controllers operating up to 66.7 Mbps
 - All communication controllers operating in asynchronous mode
- HDLC channels
 - 40 dedicated full-duplex HDLC channels
 - Each HDLC channel supporting a maximum of 66.7 Mbps
 - A default of 64 buffer descriptors per channel (32 TxBD plus 32 RxBD) or 4096 total buffer descriptors
 - Configurable number of buffer descriptors in each channel (minimum of 0, maximum of 4096)
- Buffering
 - 32 kB on-chip dual-port RAM for buffer descriptors
 - A default of 64 buffer descriptors per channel (32 TxBD plus 32 RxBD) or 4096 total buffer descriptors
 - 256 kilobits on-chip memory for data buffers
 - 256-kilobit communication buffer storing up to 819 bytes per frame
 - Maximum buffer length of 64 kB
 - 80-channel virtual DMA functionality executing between off-chip memory and the communications buffer
- Framing
 - Programmable frame size (maximum 64 kB)
 - Flexible buffers and multiple buffers per frame
 - Separate interrupts for frames and buffers (Tx and Rx)
 - Received frames threshold to reduce interrupt overhead
 - Flag/abort/idle generation and detection
 - Zero insertion and deletion
 - 16- or 32-bit CRC-CCITT generation and checking
 - Detection of non-octet aligned frames
 - Detection of too-long frames
 - Programmable flags (0–15) between successive frames
 - Echo and local loopback mode for testing
- Master interface unit
 - Directly connects with 64-bit data, 32-bit address 60x bus
 - Supports 66 MHz 60x bus speed
 - Virtual DMA supports an 80-channel HDLC master
 - Virtual DMA functionality executing off-chip memory to internal memory
 - Either the master or the slave MC92460 may be selected as the 60x bus master
 - Bus supports multimaster design
 - Up to four devices may be connected in parallel on the 60x bus
 - Supports single-beat and burst accesses

- Baud rate generator (BRG)
 - 40 independent and identical baud rate generators, one per channel
 - On-chip PLL for configurable baud rate generation (maximum of 66.7 MHz)
 - A 16x divider option allows slow baud rates at high system frequencies
 - Each BGR output can be routed to a pin (TxCKn and RxCKn)
 - On-the-fly changes allowed
- 480-pin TBGA, 1.27 mm pitch packaging
- Applications
 - Supports IEEE1149.1 JTAG controller standard
 - Separate power supplies for core (1.8 volts) and internal logic (3.3 volts)



MC92460 PARAMETRICS

Description: Multichannel HDLC Controller Peripheral

Package: 480-pin TBGA

Comments: Peripheral to the MPC826x processors

MC92460 DOCUMENTATION

Literature order number: MC92460TS/D

Description: MC92460 HDLC Controller Technical Summary

Literature order number: MC92460UM/D

Description: MC92460 HDLC Controller User's Manual

Literature order number: MC92460IBIS

Description: MC92460 IBIS Model

CONTACT INFORMATION

Motorola offers user's manuals, application notes, and sample code for all of its communications processors and components. In addition, local support for these products is also provided. This information can be found at:

www.motorola.com/smartnetworks

For all other inquiries about Motorola products, please contact the Motorola Customer Response Center at: (800) 521-6274.



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MC92460FACT/D

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