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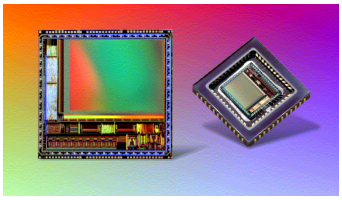
SCM20025

Product Data Sheet

Color CIF 1/4" Digital Image Sensor
352 x 288 pixel progressive scan solid state image sensor with integrated CDS/PGA/ADC, digital programming, control, timing, and pixel correction features



Features:

- CIF resolution, active CMOS image sensor with square pixel unit cells
- 7.8µm pitch pixels with patented pinned photodiode architecture
- Bayer-RGB color filter array with optional micro lenses
- High sensitivity, quantum efficiency, and charge conversion efficiency
- Low fixed pattern noise / Wide dynamic range
- Antiblooming and continuous variable speed shutter
- Single master clock operation
- Digitally programmable via I^2C interface
- Integrated on-chip timing/logic circuitry
- CDS sample and hold for suppression of low frequency and correlated reset noise
- 28X programmable variable gain to optimize dynamic range and facilitate white balance and iris adjustment
- 8-bit, pipelined algorithmic RSD ADC (DNL ±0.5 LSB, INL ±1.0 LSB)
- Automatic column offset correction for noise suppression
- Pixel addressability to support 'Window of Interest' windowing, resolution, and subsampling
- 30 fps full CIF at 3Mhz Master Clock Rate
- Single 3.3V power supply
- 28 pin CLCC package

Ordering Information	
Device	**Package**
SCM20025IBMN Monochrome	
SCM20025IBBN Color	

The SCM20025 is a fully integrated, high performance CMOS image sensor with features such as integrated timing, control, and analog signal processing for digital imaging applications. The part provides designers a complete imaging solution with a monolithic image capture and processing engine thus making it a true "camera on a chip". System benefits enable design of smaller, portable, low cost and low power systems. Thereby making the product suitable for a variety of consumer applications including still/full motion imaging, security/surveillance, and automotive among others.

The imaging pixels are based on active CMOS pixels using pinned photodiodes that are realized using Motorola's sub-micron ImageMOS™ technology. A maximum frame rate of 130 FPS at full resolution can be achieved, further the frame rate is completely adjustable independently of the system clock. Each pixel on the sensor is individually addressable allowing the user to control "Window of Interest" (WOI) panning and zooming. Control of sub-sampling, resolution, exposure, gain, and other image processing features is accomplished via a two pin I^2C interface. The sensor is run by supplying a single Master Clock. The sensor output is 8 digital bits providing wide dynamic range images.

This document contains information on a new product.
Specifications and information herein are subject to change without notice.
May 2000

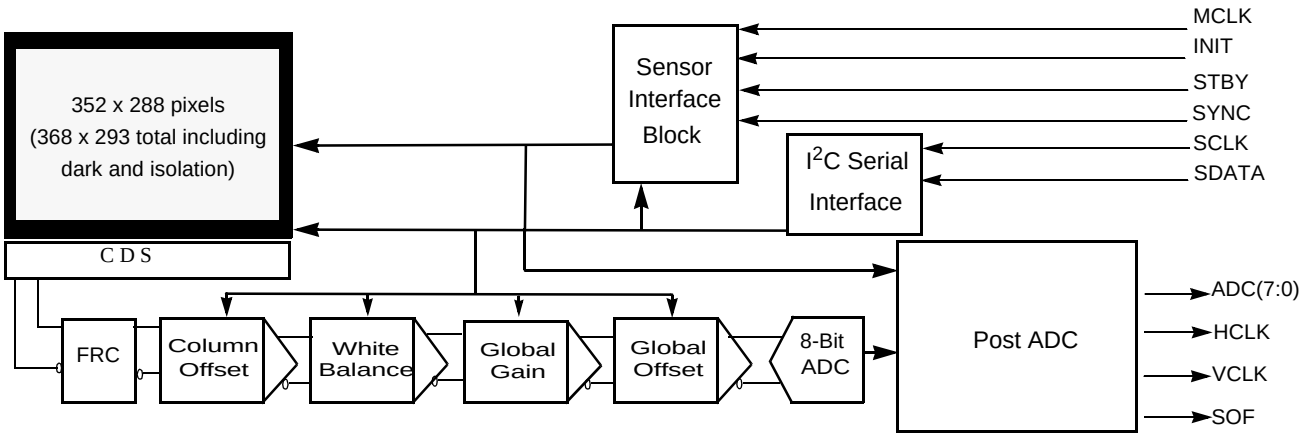


Figure 1. SCM20025 Simplified Block Diagram

Specifications

Image Size: 2.75mm x 2.25mm (1/4")

Resolution: 352 x 284 pixels, available digital zoom and region of interest (ROI) windowing

Pixel Size: 7.8µm x 7.8µm

Monochrome Sensitivity: 3 V/Lux-sec

Min. Detectable Light Level: 5 Lux at 30FPS/F2 lens

Scan Modes: Progressive

Shutter Modes: Continuous (Video) / Single (Still) - available in all modes

Readout Rate: 13.5MSPS

Frame Rate: 0-130 frames per second

Max Master Clock Frequency: 13.5MHz

System Dynamic Range: 42dB

On Chip programmable gain: -4.5dB to 24dB

On Chip Image Correction: Column offset calibration

Analog to Digital Converter: 8-bit, RSD ADC (DNL +/-0.5 LSB, INL +/-1.0 LSB)

Power Dissipation: 200mW (dynamic)

Package: 28 pin ceramic LCC

Temperature Operating Range: 0-40^{o}C

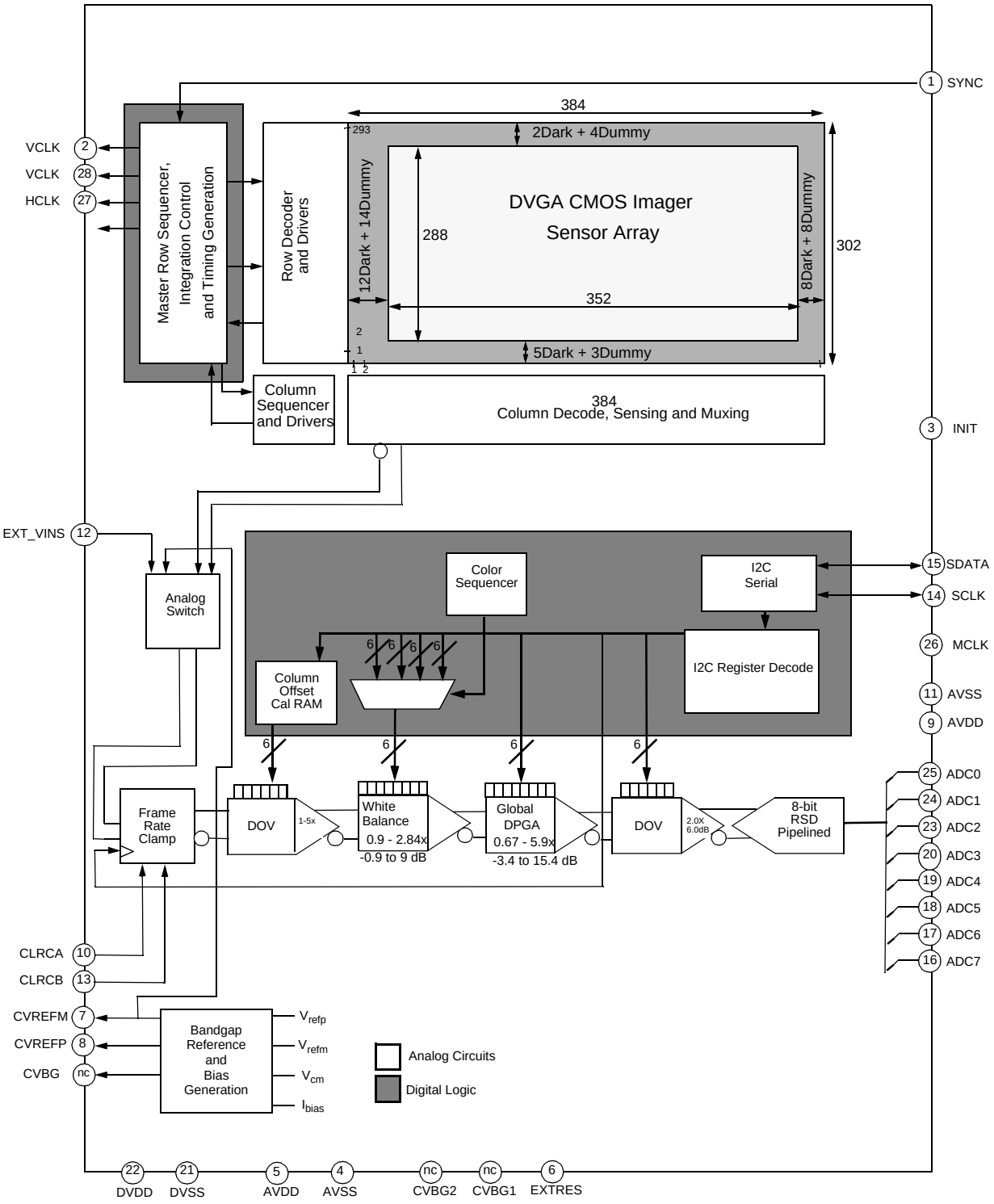


Figure 2. SCM20025 Detailed Block Diagram

1.0 SCM20025 Overview

The SCM20025 is a solid state CMOS Active CMOS Imager (ACI™) that integrates the functionality of a complete analog image acquisition, digitizer, and digital signal processing system on a single chip. The image sensor comprises a 1/4" format pixel array with 352x288 (VGA) active elements. The image size is fully programmable to user defined windows of interest. The pixels are on a 7.8µm pitch. High sensitivity and low noise are a characteristic of the pinned photodiode architecture utilized in the pixels. Optional microlenses are available to further enhance the sensitivity. The sensor is available with Bayer patterned Color Filter Arrays (CFAs) for color output or as a monochrome imager.

Integrated timing and programming controls allow video (CFCM) or still (SFCM) image capture mode supporting progressive or interlace scan modes. Frame rates are programmable while keeping Master Clock frequency constant. User programmable row and column start/stop allow windowing to a minimum 1x1 pixel window. Windowing can also be performed by subsampling in multiple pixel increments to allow digital zoom.

A high performance analog signal processing chain helps establish a new benchmark for digital image capture. The sensor has an unprecedented level of integration. The analog video output of the pixel array is processed by an on chip processing pipeline. Correlated Double Sampling (CDS) eliminates low frequency correlated noise. The Frame Rate Clamp (FRC) enables real time optical black level calibration and offset correction. Digitally Programmable Amplifiers (DPGAs) allow real time color gain correction for Auto White Balance (AWB) as well as global gain adjustment; offset calibration can be done on a per column basis or globally. This per-column offset correction can be applied by using stored values in the on chip SRAM. A 8-bit Redundant Signed Digit (RSD) ADC converts the analog data to a 8-bit digital word stream. The fully differential analog signal processing pipeline serves to improve noise immunity, signal to noise ratio, and system dynamic range.

The sensor uses an industry standard two line I^2C serial interface. It operates with a single 3.3V power supply with no additional biases and requires only a single Master Clock for operation up to 13.5MHz. It is housed in a 28 pin ceramic LCC package.

The SCM20025 is designed taking into consideration interfacing requirements to standard video encoders. In addition to the 8-bit bayer encoded data stream, the sensor outputs the valid frame, line and pixel sync signals needed for encoding. The sensor interfaces with a variety of commercially available video image processors to allow encoding into various standard video formats.

The SCM20025 is an elegant and extremely flexible single chip solution that simplifies a system designer's tasks of image sensing, processing, digital conversion, and digital signal processing to a high performance, low cost, low power IC. One that supports among others a wide range of low power, portable consumer digital imaging applications.

2.0 SCM20025 Theory of Operation

This section reviews the concepts behind the operation of the image sensing and capture mechanisms employed in the SCM20025.

2.1 Sensor Interface

2.1.1 Pixel Architecture

The SCM20025 ImageMOS™ (1) sensor comprises a 352x288active pixel array and supports progressive scan readout mode. The basic operation of the pixel relies on the photoelectric effect where due to its physical properties silicon is able to detect photons of light. The photons generate electron-hole pairs in direct proportion to the intensity and wavelength of the incident illumination. The application of an appropriate bias allows the user to collect the electrons and meter the charge in the form of a useful parameter such as voltage.

The pixel architecture is based on a four transistor (4T) Advanced CMOS Imager™(2) pixel which requires all pixels in a row to have common Reset, Transfer, and Row Select controls. In addition all pixels have common supply (V_{DD}) and ground (V_{SS}) connections. An optimized cell architecture provides enhancements such as noise reduction, fill factor maximizations, and antiblooming. The use of pinned photodiodes and proprietary transfer gate devices in the photoelements enables enhanced sensitivity in the entire visual spectral range and a lag free operation.

1. ImageMOS is a Motorola trademark
2. Advanced CMOS Imager is a Kodak trademark

The nominal photoresponse of the SCM20025 is shown in Figure 3.

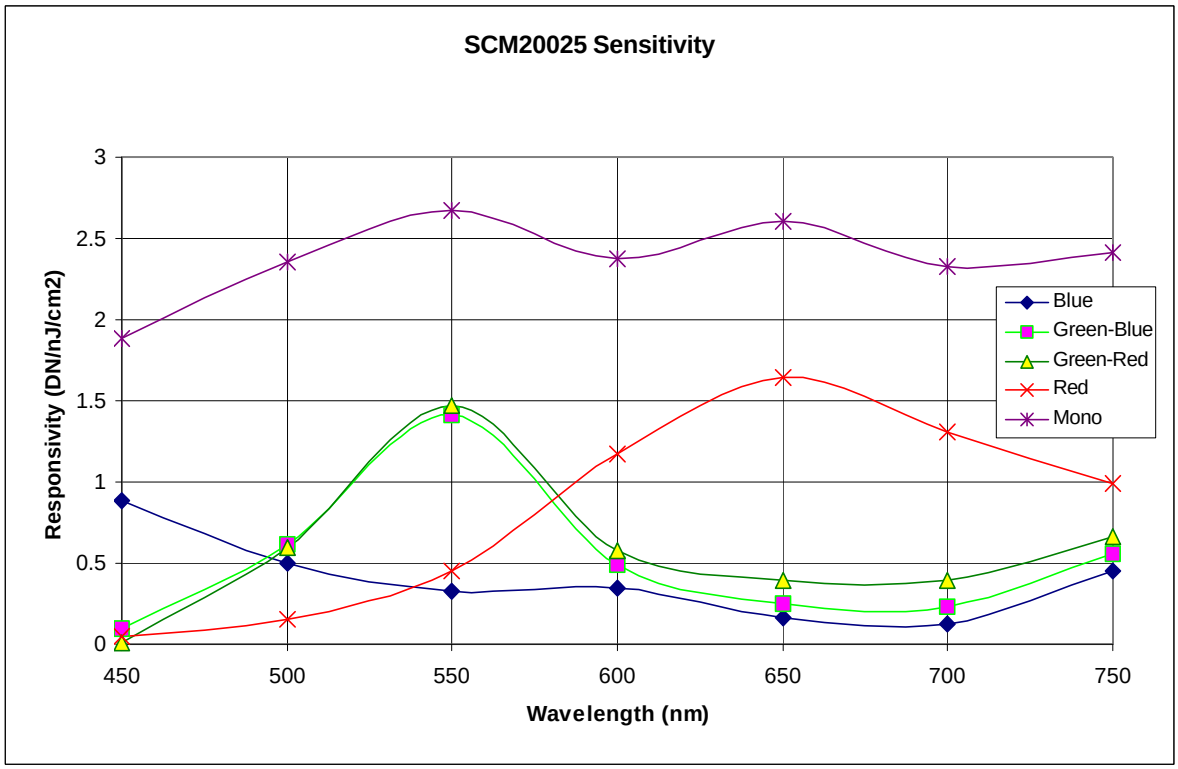


Figure 3. SCM20025 Nominal spectral response

In addition to the imaging pixels, there are additional pixels called dark and dummy pixels at the periphery of the imaging section (see Figure 2). The dark pixels are covered by a light blocking shield rendering the pixels underneath insensitive to photons. These pixels provide the sensor means to measure the dark level offset which is used downstream in the signal processing chain to perform auto black level calibration. The dummy pixels are provided at the array's periphery to eliminate inexact measurements due to light piping into the dark pixels adjacent to active pixels. The output of these pixels should be discarded.

Electronic shuttering, also known as electronic exposure timing in photographic terms, is a standard feature. The pixel integration time can be widely varied from a small fraction of a given frame readout time to the entire frame time. This feature can be especially useful in situations such as imaging of fast moving objects where maximum available integration time is long enough to cause smear or blurring or when imaging a bright scene where there are enough photons to cause an early saturation of the pixel.

2.1.2 Color Separation and Fill Factor Enhancement

The SCM20025 family is offered with the option of monolithic polymer color filter arrays (CFAs). The combination of an extremely planarized process and proprietary color filter technology result in CFAs with superior spectral and transmission properties. The standard option (Part # SCM20025IBBN) is a primary (RGB) "Bayer" pattern (see Figure 4), however, facility to produce customized CFAs including complementary (CMYG) mosaics also exists. Depending on the application, the choice between primary or complementary filter mosaics should be made. In general, primary mosaics are used in still video while complementary are used in real time video applications.

Applications requiring higher sensitivity can benefit from the optional micro-lens arrays shown in Figure 5. The lenslet arrays can improve the fill factor (aperture ratio) of the sensor by 1.5-2x depending on the F number of the main lens used in the camera system. Microlenses yield greatest benefits when the main lens has a high F number. As a caution, unoptimized F numbers can lead to optical aberrations hence, care should be taken when

incorporating microlens equipped imagers into camera systems/heads. The fill factor of the pixels without microlenses is 35%.

G1	R	G1	R
B	G2	B	G2
G1	R	G1	R
B	G2	B	G2

Figure 4. Optional on-chip Bayer CFA

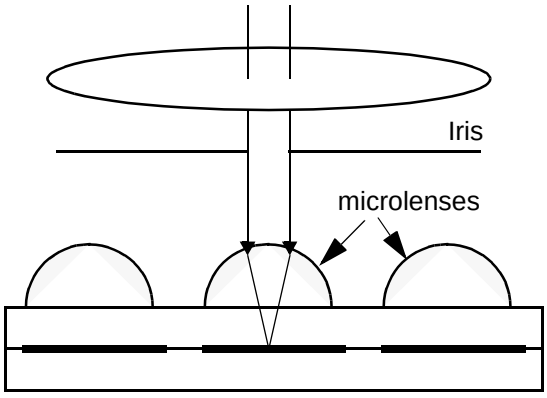


Figure 5. Improvement in pixel sensitivity results from focusing incident light on photo sensitive portions of the pixel by using microlenses.

2.1.3 Frame Capture Modes

Depending on the application the user may choose between the two available Frame Capture Modes (FCMs). An overview of the operation of the two modes and suggested guidelines for selection are given in this section.

The default mode of image capture is the Continuous Frame Capture Mode (CFCM). This mode is most suitable for full motion video capture and will yield CIF sized frame rates over 100fps at 13.5 MHz MCLK. In this mode the image integration and row readout take place in parallel. While a row of pixels is being read out, another row or rows are being integrated. Since the integration time (T_{int}) is equal for all rows, the start of the integration periods for rows is staggered out. This mode relies on the integration periods of the rows being long enough to produce a reasonable overlap of the sequential rows. If this is not the case then image artifacts may be produced in instances where the target is moving very fast or the illumination varies.

The second available capture mode is called Single Frame Capture Mode (SFCM). This mode consists of global integration of all pixels, next a simultaneous transfer to the Floating Diffusion (FD) node of all pixels followed by a sequential read out of all rows. This mode is best suited for still or “single snap shot” capture of an image where a flash illumination is utilized.

SFCM should only be used when the ambient lighting will not cause the pixels to saturate during the readout time.

The user chooses the scan mode via the Capture Mode Control Register, (Table 22), on page 28.

2.1.4 Image Scan Modes

The SCM20025 has two available image scanning modes: interlaced and progressive.

Interlacing is a technique used in TV systems that is used to enhance the vertical resolution of the picture without increasing the bandwidth of the transmission system. A spatial offset is introduced on the display system between the odd and even fields. An odd field consists of rows 1,3,5,7,9.... while an even field comprises rows 2,4,6,8..... Since the spatial offset is exactly half the vertical pitch of the sensor, the even and odd fields appear interdigitated when displayed on top of one another, thus appearing to improve the sensor’s vertical resolution. By definition two interlaced fields comprise a frame. It should be noted that at high frame rates, motion between fields in interlaced video can cause smear and/or serrations to appear in the image.

Progressive scanning refers to non-interlaced or sequential row by row scanning of the entire sensor in a single pass. The image capture happens at one instant of time. This mode is primarily used in applications where vertical resolution is of prime importance and available bandwidth of the transmission system does not impose any limitations.

The user chooses the scan mode via the Sub-sample Control Register, (Table 23), on page 29.

2.1.5 Window of Interest Control

The pixel data to be read out of the device is defined as a ‘Window of Interest’ (WOI). The window of interest can be defined anywhere on the pixel array at any size. The user provides the upper-left pixel location and the size in both rows and columns to define the WOI. The

WOI is defined using the WOI Pointer, WOI Depth, and WOI Width registers, (Table 27, page 31 through Table 34, page 34). Please refer to Figure 6 for a pictorial representation of the WOI within the active pixel array.

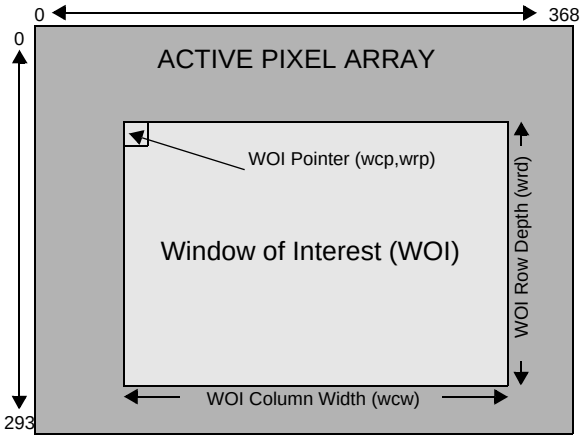


Figure 6. WOI Definition

2.1.6 WOI Sub-sampling Control

The WOI can be sub-sampled per user control. The user can read out the pixel data in either monochrome or bayer pixel space in four different sampling rates in each direction: full, 1/2, 1/4, or 1/8. The user controls the subsampling via the Sub-sample Control Register, (Table 23), on page 29. An example of Bayer space sub-sampling is shown in Figure 7.

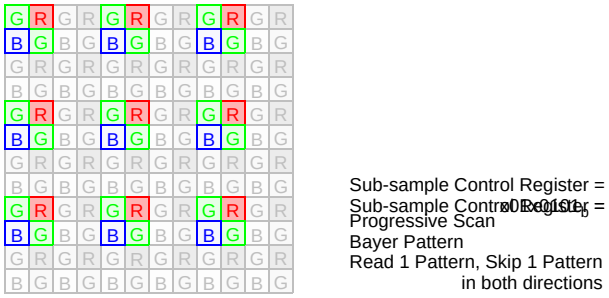


Figure 7. Bayer Space Sub-sampling Example

2.1.7 CFCM Frame Rate and Integration Time Control

In addition to the minimum time required to readout the selected resolution and WOI, the user has the ability to control the frame rates while operating in CFCM. This is done by varying the size of a Virtual Frame surrounding the WOI. Please refer to Figure 8 for a pictorial description of the Virtual Frame and its relationship to the WOI.

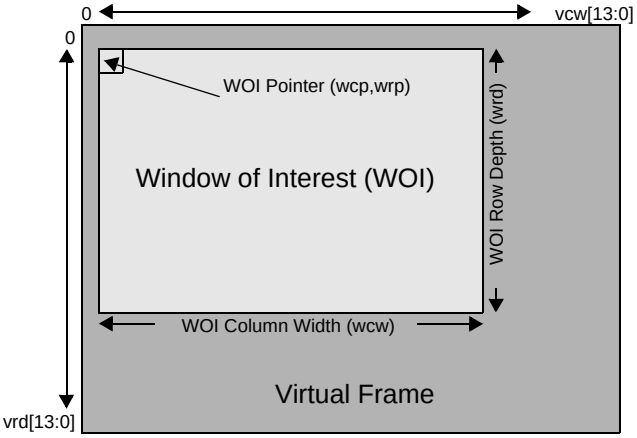


Figure 8. Virtual Frame Definition

The frame rate (time required to readout an entire frame of data plus the required boundary timing) is completely defined by the size of the Virtual Frame and can be expressed as:

$$\textbf{Frame Time} = \textbf{vrd}_d * \textbf{T}_{row} + \textbf{T}_{fc} \quad \text{for } T_{row} < T_{lim}$$

$$\textbf{Frame Time} = (\textbf{vrd}_d + 1) * \textbf{T}_{row} \quad \text{for } T_{row} \geq T_{lim}$$

where vrd_d defines the number of rows in the virtual frame. The user controls vrd_d via the CFCM Virtual Frame Row Depth registers (Table 38, page 36 and Table 39, page 37).

Row Time (T_{row}) is the length of time required to read one row of the virtual frame and can be defined as:

$$\textbf{T}_{row} = (\textbf{vcw}_d + \textbf{shs}_d + \textbf{shr}_d + 19) * \textbf{MCLK}_{period}$$

where vcwd defines the number of columns in the virtual frame and shs_d and shr_d are internal timing control registers. The user controls vcw_d via the CFCM Virtual Frame Column Width registers (Table 40, page 37 and Table 41, page 38). The user controls the shs_d and shr_d values via the Internal Timing Control Register; Table 26 and is strongly encouraged to write an 00_h to this register.

T_{lim} is the minimum amount of time required for the internally generated frame clamp signal and is defined as:

$$\textbf{T}_{lim} = 399 * \textbf{MCLK}_{period}$$

T_{fc} is the minimum amount of time required to perform a frame clamp with timing overhead and is defined as:

$$\textbf{T}_{fc} = (399 + \textbf{shs}_d + \textbf{shr}_d + 19) * \textbf{MCLK}_{period}$$

The Integration Time for CFCM is defined by a combination of the width of the virtual frame and the integration time register, (Table 36, page 35 and Table 37, page 36); and can be expressed as:

Integration Time = ($cint_d$ + 1) * T_{row}

where $cint_d$ is the number of virtual frame row times desired for integration time. Therefore, the integration time in CFCM mode can be adjusted in steps of virtual frame row times. This equation for Integration Time is valid only for $T_{row} \geq T_{lim}$. For virtual frames where $T_{row} < T_{lim}$, the integration time is different for the first $cint_d$ rows and is defined as:

Integration $Time_{cintdrows}$ = T_{fc} + ($cint_d$ * T_{row})

By using the default values in the Virtual Frame definition and Integration Time registers, an 00_h loaded into the Internal Timing Control Register, and assuming a standard video square pixel clock rate of 12.27Mhz, we can calculate the frame rate and integration time as:

Row Time = (368 + 16 + 16 + 19) / 12.27e6 =34.14µs

Frame Time = (499 + 1) * 34.14µs = 17.07ms which results in a Frame Rate of 58 frames per second.

Integration Time = (499 + 1) * 34.14µs = 17.07ms.

2.1.8 SFCM Integration Time Control

The Integration Time for the SFCM is defined by the integration time register (Table 35, page 35 through Table 37, page 36) and can be expressed as:

Integration Time = $sint_d$ * 16 * $MCLK_{period}$

where $sint_d$ is a number. Therefore, the user can adjust integration time in steps of 16 MCLK periods.

2.2 Analog Signal Processing Chain Overview

The SCM20025's analog signal processing (ASP) chain incorporates Correlated Double Sampling (CDS), Frame Rate Clamp (FRC), two Digitally Programmable Gain Amplifiers (DPGA), Offset Correction (DOVA), and a 8-bit Analog to Digital Converter (ADC).

2.2.1 Correlated Double Sampling (CDS)

The uncertainty associated with the reset action of a capacitive node results in a reset noise which is equal to kTC; C being the capacitance of the node, T the temperature and k the Boltzmann constant. A common way of eliminating this noise source in all image sensors is to use Correlated Double Sampling. The output signal is sampled twice, once for its reset (reference) level and once for the actual video signal. These values are sampled and held while a difference amplifier subtracts the reference level from the signal output. Double sampling of the signal eliminates correlated noise sources.

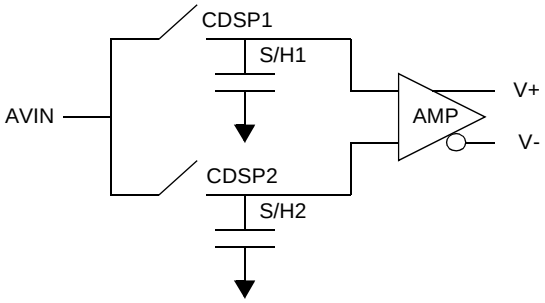


Figure 9. Conceptual block diagram of CDS implementation.

2.2.2 Frame Rate Clamp (FRC)

The FRC (Figure 10) is designed to provide a feed forward dark level subtract reference level measurement. In the automatic FRC mode, the optical black level reference is re-established each time the image sensor begins a new frame. The SCM20025 uses optical black (dark) pixels to aid in establishing this reference.

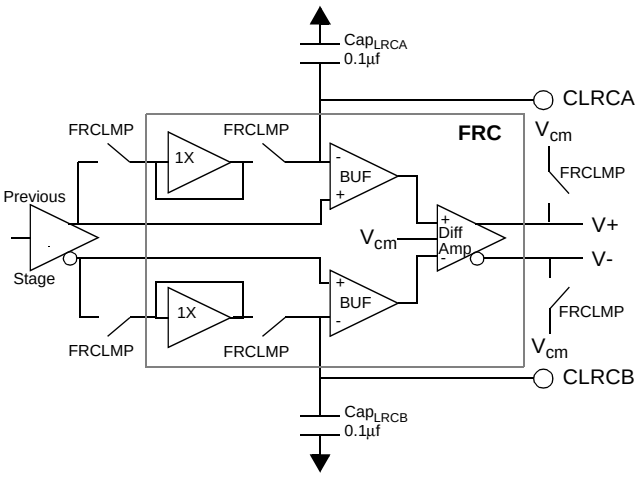


Figure 10. FRC Conceptual Block Diagram

On the SCM20025, dark pixel input signals should be sampled for a minimum of 137µs to allow the two 0.1µF capacitors at the CLRCA and CLRCB pins sufficient time to charge for 8-bit accuracy. The imager typically require first few frames to establish the dark pixel reference for subsequent active pixel processing. The dark pixel sample period is automatically controlled internally and it is set to skip the first 2 dark rows and then sample the next dark row. When "dark clamping" is active, each dark pixel is processed and held to establish pixel reference level at the CLRCA and CLRCB pins. During this period, the FRC's differential outputs (V+ and V- on the

Diff Amp, Figure 10) are clamped to V_{cm}. Together, these actions help to eliminate the dark level offset, simultaneously establishing the desired zero code at the ADC output.

Care should be exercised in choosing the capacitors for the CLRCA, B pins to reflect different frame rates.

The user can disable this function via the Capture Mode Control Register, (Table 22), on page 28 which will allow the ASP chain to drift in offsetPer-Column Digital Offset Voltage Adjust (DOVA)

The architecture of the sensor is based on blocks of 64 columns that are repeated across the array. As a result a certain source of column based noise in this block of 64 columns has a higher probability of repeating itself across the entire array. In order to allow users to correct for such offset errors, the sensor supports up to 4 column address locations that can be specified from 0 to 63. The offset value to be used at these four locations is next programmed onto an onchip RAM that stores 4, 4 bit words representing offset coefficients for these columns. Figure 11 depicts a conceptual view of how the automatic generation of the per-column offsets is accomplished.

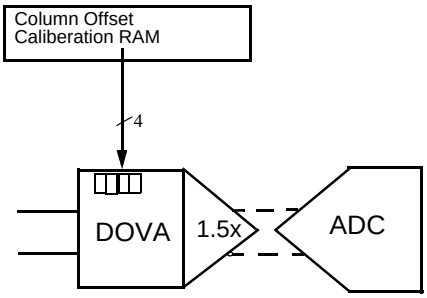


Figure 11. Conceptual illustration of the per column calibration scheme for offset adjustment

The user can generate and load data for this function as well. A dark frame can be analyzed to determine the appropriate values to be loaded into the Per-Column DOVA RAM (Column DOVA RAM, (Table 20), on page 26).

When the per-column feature is not used or necessary, the user loads a 5-bit value into the Column DOVA DC Register, (Table 18), on page 25 to perform a global offset adjust prior to the gain stages of the ASP.

2.2.3 Digitally Programmable Gain Amplifiers (DPGA)

Two DPGAs are available in the analog signal processing chain. These are used to perform white balance and exposure gain functions. Both are linearly programmable via 6-bit registers.

2.2.3.1 White Balance Control PGA

The sensor produces three primary color outputs, Red, Green and Blue. These are monochrome signals that represent luminance values in each of the primary colors. When added in equal amounts they mix to make neutral color. White balancing is a technique where the gain coefficients of the green(1), red, blue, and green(2) pixels comprising the Bayer pattern (see Figure 12.) are set so as to equalize their outputs for neutral color scenes. Since the sensitivity of the two green pixels in the Bayer pattern may not be equal, an individual color gain register is provided for each component of the Bayer pattern.

Once all color gain registers are loaded with the desired gain coefficients, white balance is achieved in real time and in analog space. The appropriate values are selected and applied to the pixel output via a high speed path, the delay of which is much shorter than the pixel clock rate. Real time updates can be performed to any of the gain registers; however, latency associated with the I^2C interface should be taken into consideration before changes occur. In most applications, users will be able to assign predefined settings such as daylight, fluorescent, tungsten, and halogen to cover a wide gamut of illumination conditions.

Both DPGA designs use switched capacitors to minimize accumulated offset and improve measurement accuracy and dynamic range. The white balance gain registers are 6-bits and can be programmed to allow gain of 0.9x to 2.84x in steps of 0.03x.

The user programs the individual gain coefficients into the SCM20025 via the Color Gain Registers (Table 3 through Table 6). For the default Bayer configuration of the color filter array; Figure 4, the Color Gain Register addresses are as follows: Reg (01h): green pixel of a green-red row; Reg (00h): red pixel; Reg (03h): blue pixel; and Reg (02h): green pixel of a blue-green row.

The SCM20025 is presently available with only a Bayer CFA, however, it is designed to support other novel color configurations. This is accomplished via the Color Tile Configuration Register, (Table 7), on page 19 and the Color Tile Row Definition registers (Table 8 through Table 11).

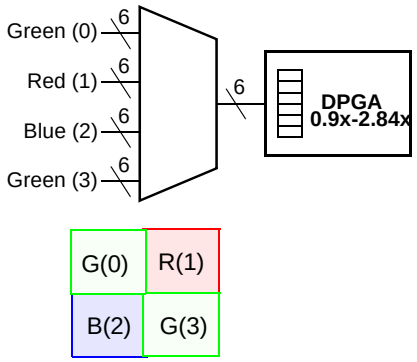


Figure 12. Color Gain Register Selection

2.2.3.2 Global Gain PGA

The global gain DPGA provides a 0.67x to 5.9x programmable gain adjustment for dynamic range. The gain of the amplifier is linearly programmable using a six bit gain coefficient in steps of 0.08x. The user programs the global gain via the DPGA Global Gain Register, (Table 16), on page 24.

2.2.4 Global Digital Offset Voltage Adjust (DOVA)

A programmable global offset adjustment is available on the SCM20025. A user defined offset value is loaded via a 6-bit signed magnitude programming code via the Global DOVA Register, (Table 21), on page 27.

Offset correction allows fine-tuning of the signal to remove any additional residual error which may have accumulated in the analog signal path. This function is performed directly before analog to digital conversion and introduces a fixed gain of 2.0X. This feature is useful in applications that need to insert a desired offset to adjust for a known system noise floor relative to AVSS and offsets of amplifiers in the analog chain.

2.2.5 Analog to Digital Converter (ADC)

The ADC is a fully differential, low power circuit. A pipelined, Redundant Signed Digit (RSD) algorithmic technique is used to yield an ADC with superior characteristics for imaging applications.

Integral Noise Linearity (INL) and Differential Noise Linearity (DNL) performance is specified at $\pm$1.0 and $\pm$0.5, respectively, with no missing codes. The input voltage resolution is 9.76mV with a full-scale 2.5 V_{pp} input (2.5 $V_{pp}/2^8$). The input dynamic range of the ADC is programmed via a Programmable Voltage Reference Generator. The positive reference voltage (VREFP) and negative reference voltages (VREFM) can be programmed from 2.5V to 1.25V and 0V to 1.25V respectively in steps of 5mV via the Reference Voltage Registers (Table 12 and Table 13). This feature is used independently or in conjunction with the DPGAs to maximize the system dynamic range based on incident illumination. The default input range for the ADC is 1.9V for VREFP and 0.6V for VREFM hence allowing a 8-bit digitization of a 1.3V peak to peak signal.

2.3 Additional Operational Conditions

The SCM20025 includes initialization, standby modes, and external reference voltage outputs to afford the user additional applications flexibility.

2.3.1 Initialization

The INIT input pin (#3) controls reinitialization of the SCM20025. This serves to assure controlled chip and system startup. Control is asserted via a logic high input. This state must be held a minimum of 1 ms and a 1 ms “wait period” should be allowed before chip processing to ensure that the start-up routines within the SCM20025 have run to completion, and to guarantee that all holding and bypass capacitors, etc. have achieved their required steady state values.

Tasks which are accomplished during startup include: reset of the utility programming registers and initialization to their default values (please refer to previous section for settings), reset of all internal counters and latches, and setup of the analog signal processing chain.

2.3.2 Standby Mode

The standby mode option is implemented to allow the user to reduce system power consumption during periods which do not require operation of the SCM20025. This feature allows the user to extend battery life in low power applications.

By utilizing this mode, the user may reduce dynamic power consumption from 200mW, in the active processing, 13 Million Samples per Second mode, to $\leq$50 mW in the standby mode (note that dynamic power consumption is also reduced in slower conversion speed applications).

The sensor can be put in the stand by mode via bit <0> on the Power Configuration Register (OC_h)

The user may also reduce power consumption in the active processing mode by placing the SCM20025’s outputs in the tri-state mode. This action can be accomplished by setting the **sby** bit on the Power Configuration Register; Table 14, ($0C_h$).

2.3.3 References CVREFP, CVREFM

The SCM20025 contains all internally generated references and biases on-chip for system simplification. An internally generated differential bandgap regulator derives all the ADC and other analog signal processing required references. The user should connect 0.1µF capacitors to the CVREFP and CVREFM pins (#8 and #7 respectively) to accurately hold the biases.

2.3.4 Internal Timing Control Register

The Internal Timing Control Register; Table 26 allows control over pulse widths of critical internal timing signals. The user must write an 00_h into this address location to assure proper operation of the SCM20025.

2.3.5 Internal Bias Current Control

The ASP chain has internally generated bias currents that result in an operating power consumption of nearly 200mW. By attaching a resistor between pin 6, EXTRES; and ground, the user can reduce the power consumption of the device. This feature is enabled by writing a 1_b to bit **res** of the Power Configuration Register. Additional power savings can be achieved at lower clock rates.

3.0 SCM20025 Waveform Diagrams

The following set of diagrams depict the input/output waveform relationships for the pixel data.

3.1 CFCM Data Waveforms

The following set of waveforms depict the CFCM output data stream from a complete frame down to individual signal relationships. Figure 13 depicts a complete frame of a CFCM output data stream in default mode. Figure 14 depicts the first row of data in the frame.

Figure 15 and Figure 16 depict the same CFCM waveforms with the Internal Timing Control Register loaded with an 00_h.

Figure 17 depicts a single frame output using CFCM. This is created by setting the **cms** bit of the Capture Mode Control Register, (Table 22), on page 28 to1_b.

Figure 3.2 depicts the CFCM in interlaced output mode. This is created by setting the **sm** bit of the Sub-sample Control Register, (Table 23), on page 29 to1_b.

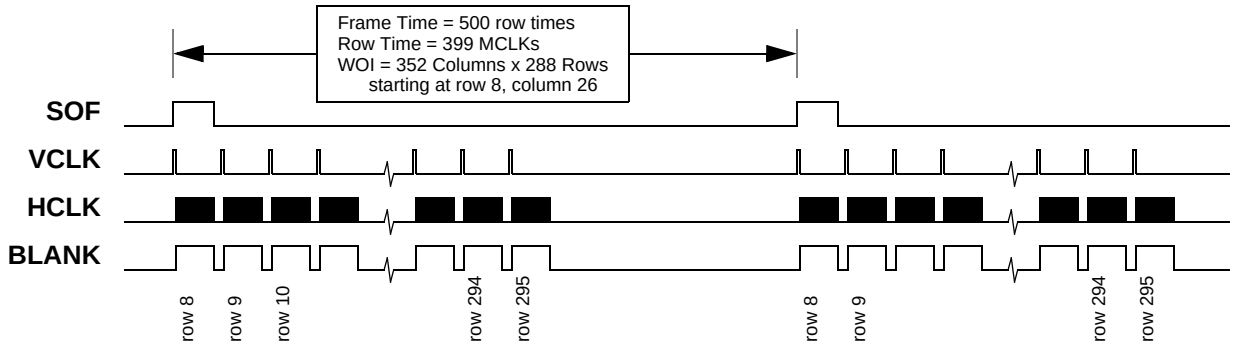


Figure 13. CFCM Default Frame Waveform

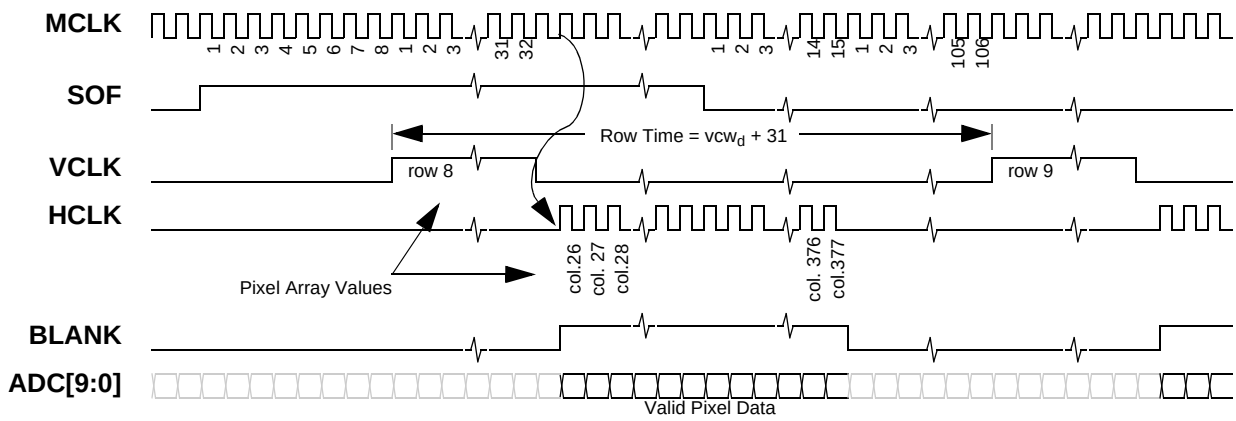


Figure 14. CFCM Default Line Waveform

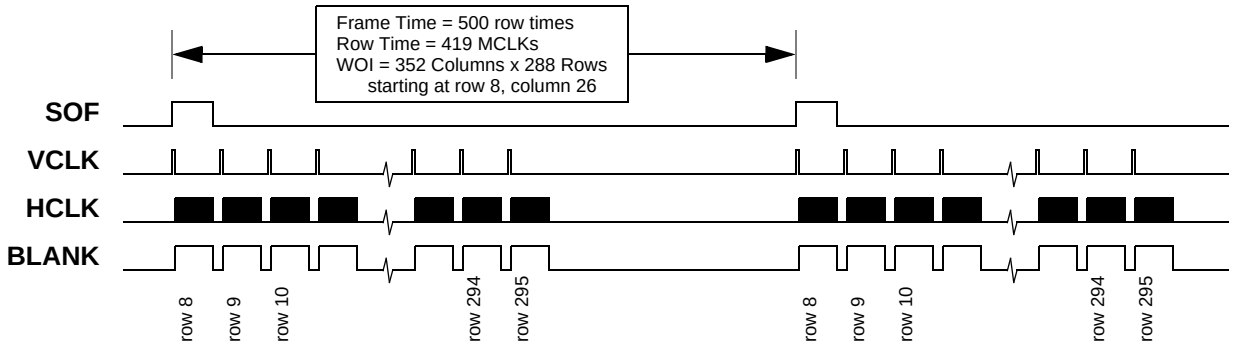


Figure 15. CFCM Frame Waveform with Internal Timing Control Register = 00_h

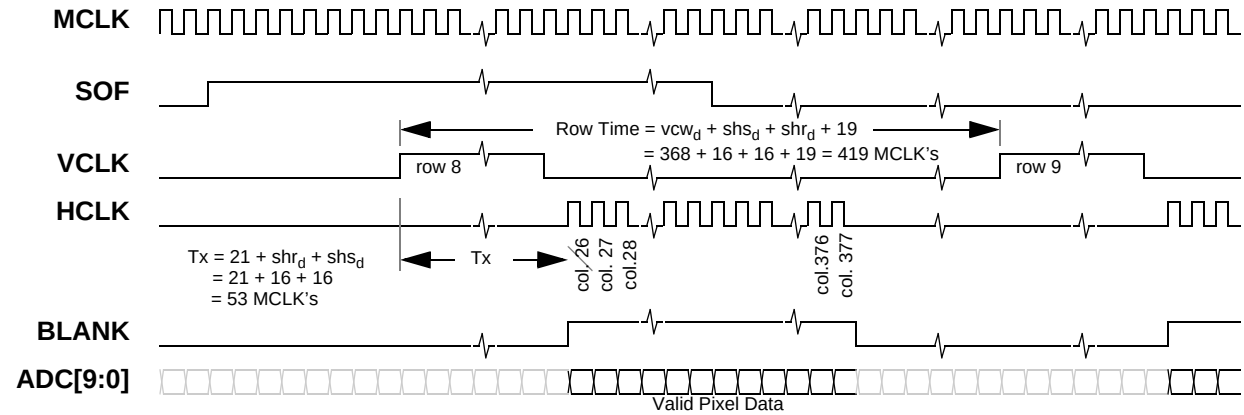


Figure 16. CFCM Line Waveform with Internal Timing Control Register = 00_h

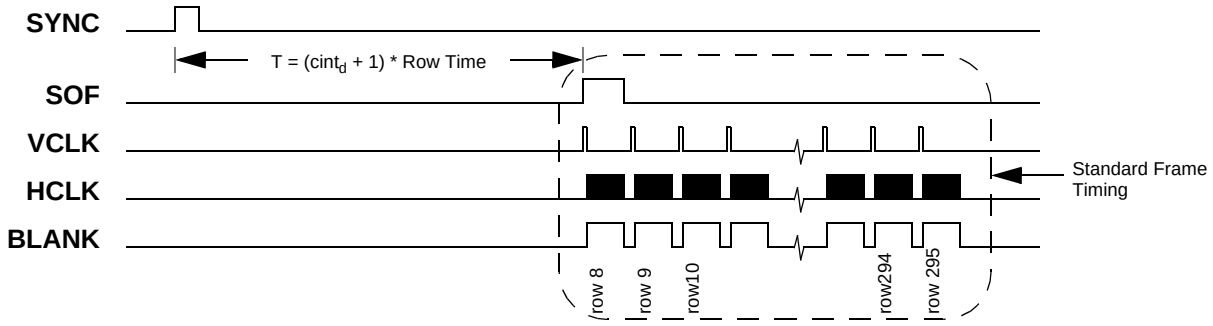


Figure 17. CFCM Single Frame Mode Waveform

3.2 SFCM Data Waveforms

The following set of wave forms depict the SFCM output data stream from a complete frame down to individual signal relationships. Figure 18 depicts a complete frame of a SFCM output data stream in default mode. Figure 19 depicts the first row of data in the frame.

Figure 20 and Figure 21 depict the same SFCM waveforms with the Internal Timing Control Register loaded with an 00_h.

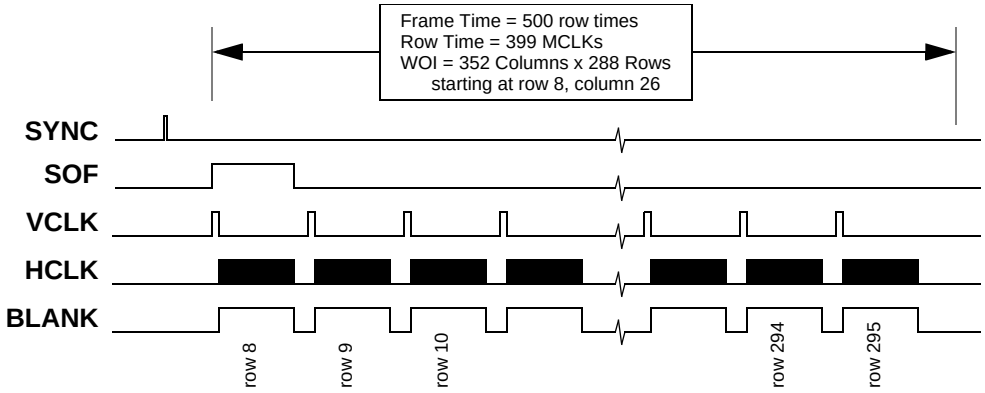


Figure 18. SFCM Default Frame Waveform

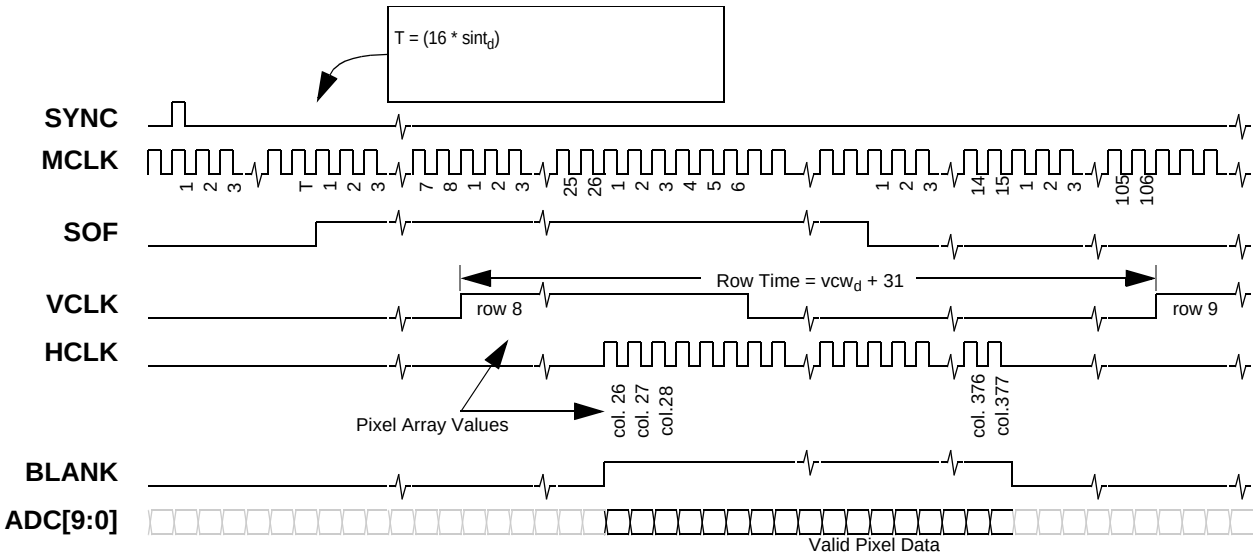


Figure 19. SFCM Default Line Waveform

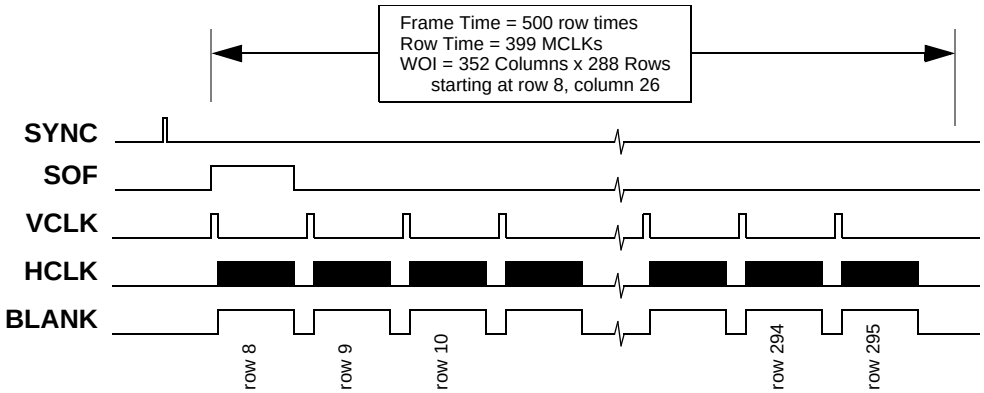


Figure 20. SFCM Frame Waveform with Internal Timing Control Register = 00_h

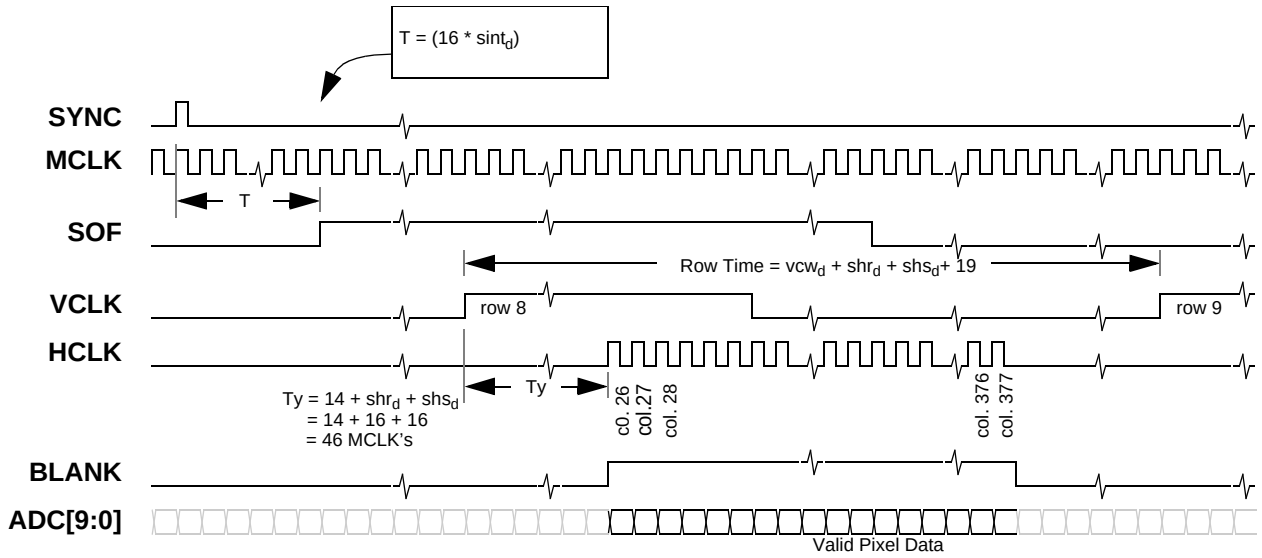


Figure 21. SFCM Line Waveform with Internal Timing Control Register = 00_h

4.0 SCM20025 Utility Programming Registers

4.1 Register Reference Map

The I^2C addressing is broken up into groups of 16 and assigned to a specific digital block. The designated block is responsible for driving the internal control bus, when the assigned range of addresses are present on the internal address bus. The grouping designation and assigned range are listed in Table 1. Each block contains registers which are loaded and read by the digital and analog blocks to provide configuration control via the I^2C serial interface.

Address Range	Block Name
00_h - $0F_h$	Analog Register Interface
10_h - $1F_h$	Global Gain
20_h - $2F_h$	Offset Calibration
40_h - 60_h	Sensor Interface
61_h - FF_h	Factory Use

Table 1. I^2C Address Range Assignments

Table 2 contains all the I^2C address assignments. The table includes a column indicating whether the register values are shadowed with respect to the sensor interface. If the register is shadowed, the sensor interface will only be updated upon frame boundaries, thereby eliminating intraframe artifacts resulting from register changes.

Hex Address	Register Function	Default	Ref. Table	Shadowed?
00_h	DPGA Color 1 Gain Register (Red)	02_h	Table 3, page 18	Yes
01_h	DPGA Color 2 Gain Register (Green of Green-Red Row)	02_h	Table 4, page 18	Yes
02_h	DPGA Color 3 Gain Register (Green of Blue-Green Row)	02_h	Table 5, page 19	Yes
03_h	DPGA Color 4 Gain Register (Blue)	02_h	Table 6, page 19	Yes
04_h	*Unused*			

Table 2. I^2C Address Assignments

Hex Address	Register Function	Default	Ref. Table	Shadowed?
05_h	Color Tile Configuration Register	05_h	Table 7, page 19	No
06_h	Color Tile Row 1 Definition Register	44_h	Table 8, page 20	No
07_h	Color Tile Row 2 Definition Register	EE_h	Table 9, page 21	No
08_h	Color Tile Row 3 Definition Register	00_h	Table 10, page 21	No
09_h	Color Tile Row 4 Definition Register	00_h	Table 11, page 22	No
$0A_h$	Negative Voltage Reference Code Register	76_h	Table 12, page 22	No
$0B_h$	Positive Voltage Reference Code Register	80_h	Table 13, page 23	No
$0C_h$	Power Configuration Register	00_h	Table 14, page 23	No
$0D_h$	*Factory Use Only (set to 00h)*	*00_h*		
$0E_h$	Reset Control Register	00_h	Table 15, page 24	No
$0F_h$	Device Identification (read only)	70_h		No
10_h	DPGA Global Gain Register	00_h	Table 16, page 24	Yes
11_h - $1F_h$	*Unused*			
12_h	Tristate Output Enable	$C0_h$	Table 17, page 25	Yes
13_h - $1F_h$	*Unused*			
20_h	Column DOVA DC Register	00_h	Table 18, page 25	Yes
21_h	Column DOVA Control Register	00_h	Table 19, page 26	No
22_h	Global DOVA Register	00_h	Table 21, page 27	Yes
23_h	Per Column DC offset Mod 64 Address #1	00_h	page 25	Yes
24_h	Per Column DC offset Mod 64 Address #2	00_h	page 25	Yes
25_h	Per Column DC offset Mod 64 Address #3	00_h	page 25	Yes
26_h	Per Column DC offset Mod 64 Address #4	00_h	page 25	Yes
27_h	Per Column DC offset Mod 64 Value at Address #1	00_h	Table 20, page 26	Yes
28_h	Per Column DC offset Mod 64 Value at Address #2	00_h	Table 20, page 26	Yes
29_h	Per Column DC offset Mod 64 Value at Address #3	00_h	Table 20, page 26	Yes
$2A_h$	Per Column DC offset Mod 64 Value at Address #4	00_h	Table 20, page 26	Yes

Table 2. I^2C Address Assignments (Continued)

Hex Address	Register Function	Default	Ref. Table	Shadowed?
2B - 3F$_h$	*Unused*			
40$_h$	Capture Mode Control Register	AA$_h$	Table 22, page 28	Yes
42$_h$	Frame Request Sync Control Register	04$_h$		Yes
43$_h$	Sub-sample Control Register	00$_h$	Table 23, page 29	Yes
44$_h$	*Unused*			
45$_h$	WOI Row Pointer MSB Register	00$_h$	Table 27, page 31	Yes
46$_h$	WOI Row Pointer LSB Register	08$_h$	Table 28, page 32	Yes
47$_h$	WOI Row Depth MSB Register	01$_h$	Table 31, page 33	Yes
48$_h$	WOI Row Depth LSB Register	1F$_h$	Table 32, page 33	Yes
49$_h$	WOI Column Pointer MSB Register	00$_h$	Table 29, page 32	Yes
4A$_h$	WOI Column Pointer LSB Register	1A$_h$	Table 30, page 33	Yes
4B$_h$	WOI Column Width MSB Register	01$_h$	Table 33, page 34	Yes
4C$_h$	WOI Column Width LSB Register	5F$_h$	Table 34, page 34	Yes
4D$_h$	Integration Time MSB Register	00$_h$	Table 35, page 35	Yes
4E$_h$	Integration Time ISB Register	01$_h$	Table 36, page 35	Yes
4F$_h$	Integration Time LSB Register	F3$_h$	Table 37, page 36	Yes
50$_h$	CFCM Virtual Frame Row Depth MSB Register	01$_h$	Table 38, page 36	Yes
51$_h$	CFCM Virtual Frame Row Depth LSB Register	F3$_h$	Table 39, page 37	Yes
52$_h$	CFCM Virtual Frame Column Width MSB Register	01$_h$	Table 40, page 37	Yes
53$_h$	CFCM Virtual Frame Column Width LSB Register	70$_h$	Table 41, page 38	Yes
54$_h$	SOF Control Register	C2$_h$	Table 24, page 29	No
55$_h$	VCLK Control Register	98$_h$	Table 25, page 30	No
56$_h$	Reverse Readout Register	00$_h$	Table ?	No
60$_h$	Internal Timing Control Register	66$_h$	Table 26, page 31	Yes
61$_h$ *- 65*$_h$	*Factory Use Only*			
66$_h$ *- FF*$_h$	*Unused*			

Table 2. I^{2}C Address Assignments (Continued)

5.0 Detailed Register Block Assignments

This section describes in further detail the functional operation of the various SCM20025 programmable registers. The registers are subdivided into various blocks for ease of addressability and use (see Table 1).

In each table where a suffix code is used; h = hex, b = binary, and d = decimal.

5.1 Analog Register Interface Block

The address range for this block is 00_h to $0F_h$.

5.1.1 Analog Color Configuration

The four Color Gain Registers, Color Tile Configuration Register, and four Color Tile Row definitions define how white balance is achieved on the device. Six-bit gain codes can be selected for four separate colors: Table 3, Table 4, Table 5, and Table 6. Gain for each individual color register is programmable given the gain function defined in the table. The user programs these registers to account for changing light conditions to assure a white balanced output. The default value in each register is provides for a unity gain. In addition, the default CFA pattern color is listed in the title of each register.

Address 00_h	DPGA Color 1 Gain Code Red						Default 02_h
msb (7)	6	5	4	3	2	1	lsb (0)
x	x	cg1[5]	cg1[4]	cg1[3]	cg1[2]	cg1[1]	cg1[0]

Bit Number	Function	Description	Reset State
7 - 6	Unused	Unused	xx
5 - 0	Gain	Gain = 0.88 + (0.03 * $cg1_d$)	000010_b

Table 3. DPGA Color 1 Gain Register

Address 01_h	DPGA Color 2 Gain Code Green (of Green-Red Row)						Default 02_h
msb (7)	6	5	4	3	2	1	lsb (0)
x	x	cg2[5]	cg2[4]	cg2[3]	cg2[2]	cg2[1]	cg2[0]

Bit Number	Function	Description	Reset State
7 - 6	Unused	Unused	xx
5 - 0	Gain	Gain = 0.88 + (0.03 * $cg2_d$)	000010_b

Table 4. DPGA Color 2 Gain Register

Address 02_h	DPGA Color 3 Gain Code Green (of Green-Blue Row)						Default 02_h
msb (7)	6	5	4	3	2	1	lsb (0)
x	x	cg3[5]	cg3[4]	cg3[3]	cg3[2]	cg3[1]	cg3[0]
Bit Number	**Function**	**Description**					**Reset State**
7 - 6	Unused	Unused					xx
5 - 0	Gain	Gain = 0.88 + (0.03 * $cg3_d$)					000010_b

Table 5. DPGA Color 3 Gain Register

Address 03_h	DPGA Color 4 Gain Code Blue						Default 02_h
msb (7)	6	5	4	3	2	1	lsb (0)
x	x	cg4[5]	cg4[4]	cg4[3]	cg4[2]	cg4[1]	cg4[0]
Bit Number	**Function**	**Description**					**Reset State**
7 - 6	Unused	Unused					xx
5 - 0	Gain	Gain = 0.88 + (0.03 * $cg4_d$)					000010_b

Table 6. DPGA Color 4 Gain Register

The Color Tile Configuration Register; Table 7, defines the maximum number of lines and the maximum number of colors per line. A maximum of four row and four column definitions are permitted. The Color Tile Configuration Register defaults to two lines and two colors per line. The user should leave this register in default unless a unique CFA option has been ordered.

This register can be configured to any pattern combination of 1, 2, or 4 rows and 1, 2, or 4 columns.

Address 05_h	Color Tile Configuration						Default 05_h
msb (7)	6	5	4	3	2	1	lsb (0)
x	x	x	x	nc[1]	nc[0]	nr[1]	nr[0]
Bit Number	**Function**	**Description**					**Reset State**
7 - 4	Unused	Unused					xxxx

Table 7. Color Tile Configuration Register

Address 05_h	Color Tile Configuration						Default 05_h
msb (7)	6	5	4	3	2	1	lsb (0)
x	x	x	x	nc[1]	nc[0]	nr[1]	nr[0]
3 - 2	Columns	00_b = 1 Column in tile. 01_b = 2 Columns in tile. $1x_b$ = 4 Columns in tile.					01_b
1 - 0	Rows	00_b = 1 Row in tile. 01_b = 2 Rows in tile. $1x_b$ = 4 Rows in tile.					01_b

Table 7. Color Tile Configuration Register

The Color Tile Row Definition registers; Table 8, Table 9, Table 10, and Table 11 define the sequence of colors for each respective line. Each byte wide line definition allows a maximum of four unique color definitions using 2 bits per color in a given line. Gain programming for each color was described earlier in this section. The default line definitions are colors 00_b, 01_b, 00_b, 01_b for row 1 and 10_b, 11_b, 10_b, 11_b for row 2 which supports a Bayer pattern as defined in section 2.1.2. The user should leave these registers in default unless a unique CFA option has been ordered.

For the default Bayer configuration of the color filter array; Figure 4, the Color Gain Register addresses are as follows: Reg (01_h): green pixel of a green-red row; Reg (00_h): red pixel; Reg (03_h): blue pixel; and Reg (02_h): green pixel of a blue-green row. The predefined gain values programmed in the respective registers are applied to pixel outputs as they are being read.

Address 06_h	Color Tile Row 1 Definition Green - Red Row						Default 44_h
msb (7)	6	5	4	3	2	1	lsb (0)
r1c4[1]	r1c4[0]	r1c3[1]	r1c3[0]	r1c2[1]	r1c2[0]	r1c1[1]	r1c1[0]
Bit Number	**Function**	**Description**					**Reset State**
7 - 6	Color 4	Fourth Color in Row 1(Green)					01_b
5 - 4	Color 3	Third Color in Row 1 (Red)					00_b
3 - 2	Color 2	Second Color in Row 1 (Green)					01_b
1 - 0	Color 1	First Color in Row 1 (Red)					00_b

Table 8. Color Tile Row 1 Definition Register

Address 07_h	Color Tile Row 2 Definition Blue - Green Row						Default EE_h
msb (7)	6	5	4	3	2	1	lsb (0)
r2c4[1]	r2c4[0]	r2c3[1]	r2c3[0]	r2c2[1]	r2c2[0]	r2c1[1]	r2c1[0]

Bit Number	Function	Description	Reset State
7 - 6	Color 4	Fourth Color in Row 2 (Blue)	11_b
5 - 4	Color 3	Third Color in Row 2 (Green)	10_b
3 - 2	Color 2	Second Color in Row 2 (Blue)	11_b
1 - 0	Color 1	First Color in Row 2 (Green)	10_b

Table 9. Color Tile Row 2 Definition Register

Address 08_h	Color Tile Row 3 Definition Unused						Default 00_h
msb (7)	6	5	4	3	2	1	lsb (0)
r3c4[1]	r3c4[0]	r3c3[1]	r3c3[0]	r3c2[1]	r3c2[0]	r3c1[1]	r3c1[0]

Bit Number	Function	Description	Reset State
7 - 6	Color 4	Fourth Color in Row 3	00_b
5 - 4	Color 3	Third Color in Row 3	00_b
3 - 2	Color 2	Second Color in Row 3	00_b
1 - 0	Color 1	First Color in Row 3	00_b

Table 10. Color Tile Row 3 Definition Register

Address 09_h	Color Tile Row 4 Definition Unused						Default 00_h
msb (7)	6	5	4	3	2	1	lsb (0)
r4c4[1]	r4c4[0]	r4c3[1]	r4c3[0]	r4c2[1]	r4c2[0]	r4c1[1]	r4c1[0]

Bit Number	Function	Description	Reset State
7 - 6	Color 4	Fourth Color in Row 4	00_b
5 - 4	Color 3	Third Color in Row 4	00_b
3 - 2	Color 2	Second Color in Row 4	00_b
1 - 0	Color 1	First Color in Row 4	00_b

Table 11. Color Tile Row 4 Definition Register

5.1.2 Reference Voltage Adjust Registers

The analog register block allows programming the input voltage range of the analog to digital converter to match the saturation voltage of the pixel array. The voltage reference generator can be programmed via two registers; **nrv** (0 to 1.25V) Table 12, **prv** (2.5V to 1.25V) Table 13, in 5mV steps. A 00_h value in the **prv** register represents a reference output voltage of 2.5V. A 00_h value in the **nrv** register represents output voltage of 0V. The default settings for the two registers produce a 1.9V reference on **prv** and 0.6V on **nrv** outputs. When adjusting these values, the user should keep the voltage range centered around 1.25V.

Address $0A_h$	Voltage Reference "Negative" Code						Default 76_h
msb (7)	6	5	4	3	2	1	lsb (0)
nrv[7]	nrv[6]	nrv[5]	nrv[4]	nrv[3]	nrv[2]	nrv[1]	nrv[0]

Bit Number	Function	Description	Reset State
7 - 0	Reference	Voltage = 0.0 + (5mV * nrc_d)	01110110_b (0.6V)

Table 12. Negative Voltage Reference Code Register

Address $0B_h$	Voltage Reference "Positive" Code						Default 80_h
msb (7)	6	5	4	3	2	1	lsb (0)
prv[7]	prv[6]	prv[5]	prv[4]	prv[3]	prv[2]	prv[1]	prv[0]
Bit Number	**Function**	**Description**					**Reset State**
7 - 0	Reference	Voltage = 2.5 - (5mV * prv_d)					10000000_b (1.9V)

Table 13. Positive Voltage Reference Code Register

5.1.3 Analog Control Registers

The Analog Register Block also contains a Power Configuration Register; Table 14, and a Reset Control Register; Table 15.

The Power Configuration Register controls the internal analog functionality that directly effect power consumption of the device. An external precision resistor pin is available on the SCM20025 that may be used to more accurately regulate the internal current sources. This serves to minimize variations in power consumption that are caused by variations in internal resistor values as well as offer a method to reduce the power consumption of the device. The default for this control uses the internally provided resistor which is nominally 12.5kΩ. This feature is enabled by setting the **res** bit of the Power Configuration Register and placing a resistor between the pin; EXTRES, and ground. Figure 13 depicts the power savings that can be achieved with an external resistor at a specific clock rate. Power is further reduced at lower clock rates.

The SCM20025 is put into a standby mode via the I^2C interface by setting the **sby** bit of the Power Configuration Register.

Address $0C_h$	Power Configuration						Default 00_h
msb (7)	6	5	4	3	2	1	lsb (0)
x	x	x	x	res	fuo	fuo	sby
Bit Number	**Function**	**Description**					**Reset State**
7 - 4	Unused	Unused					x
3	Int/Ext Resistor	0_b = Internal Resistor 1_b = External Resistor					0_b
2 - 1	FUO	Factory Use Only					0000_b
0	Software Standby	0_b = Soft Standby inactive 1_b = Soft Standby active					0_b

Table 14. Power Configuration Register

Additional control of the SCM20025 can be had using the Reset Control Register; Reset Control Register; Table 15. Setting the appropriate bit will reset only specific

blocks of the sensor. This is especially useful when aonly a specific functional block needs to be reset without affecting others. .

Address $0E_h$	Reset Control						Default 00_h
msb (7)	6	5	4	3	2	1	lsb (0)
x	x	x	x	asr	sir	ssr	sit

Bit Number	Function	Description	Reset State
7 - 4	Unused	Unused	xxxxx
3	ASP	0_b = normal 1_b = Reset	0_b
2	Sensor Interface	0_b = normal 1_b = Reset	0_b
1	State Reset	0_b = Normal Mode 1_b = Reset all non-programmable registers to the default state	0_b
0	Program-mable Reg	0_b = Normal Mode 1_b = Reset all registers to default state	0_b

Table 15. Reset Control Register

5.2 Gain Calibration Block

The DPGA Global Gain Register; Table 16, allows the user to set a global gain via a 6 bit register this is applied universally to all the pixel outputs. This enables the user to account for varying light conditions using a gain range of 0.67x to 5.9x in steps of 0.08x. The default value for this register results in unity gain.

Address 10_h	Global Gain						Default 00_h
msb (7)	6	5	4	3	2	1	lsb (0)
x	x	gg[5]	gg[4]	gg[3]	gg[2]	gg[1]	gg[0]

Bit Number	Function	Description	Reset State
7 - 6	Unused	Unused	xx
5 - 0	Gain	Gain = 0.67 + (0.08 * gg_d)	000000_b

Table 16. DPGA Global Gain Register

Address 12_h	Tristate Output Enable						Default $C0_h$
msb (7)	6	5	4	3	2	1	lsb (0)
snc	pix	fuo	fuo	fuo	fuo	fuo	fuo

Bit Number	Function	Description	Reset State
7	Tristate Enable	0_b = SOF, VCLK, and HCLK Output in Tristate 1_b = SOF, VCLK, and HCLK Output Enabled	1_b
6	Tristate Enable	0_b = Output Data Bus in Tristate 1_b = Output Data Bus Enabled	1_b
5 - 0	FUO	Factory Use Only	0000_b

Table 17. Tri-State Control Register

5.3 Offset Calibration Block

Offset adjustments for the SCM20025 are done in separate sections of the ASP to facilitate FPN removal and final image black level set.

The Column DOVA DC Register; Table 18, is used to set the initial offset of the pixel output in a range that will facilitate per-column offset data generation for varying operational conditions. In most operational scenarios, this register can be left in its default state of 00_h.

This register can also be used to apply a global offset adjust. In this case, the user must take into account the Color Gain and Global Gain registers to determine the resulting offset at the output.

Address 20_h	Column DOVA DC						Default 00_h
msb (7)	6	5	4	3	2	1	lsb (0)
x	x	cdd[5]	cdd[4]	cdd[3]	cdd[2]	cdd[1]	cdd[0]

Bit Number	Function	Description	Reset State
7 - 6	Unused	Unused	xx
5	Sign	0_b = Positive Offset 1_b = Negative Offset	0_b
4 - 0	Column DC Offset	Offset = 2 * cdd_d	00000_b

Table 18. Column DOVA DC Register

The Column DOVA Control Register; Table 19, is used to select between column wise application of offset or a global offset value. Setting the **cal** bit allows application of specified offset values at specified column addresses. All of which can be programmed via registers (25-2D)h . This feature is especially useful for repetitive column fixed pattern noise that occurs at a given spatial frequency. The user can calculate the column offset

data using their own algorithm and load this data via the I^2C bus as defined in this section.

Address 21_h	Column DOVA Control						Default 00_h
msb (7)	6	5	4	3	2	1	lsb (0)
fuo	fuo	fuo	fuo	fuo	fuo	fuo	cal

Bit Number	Function	Description	Reset State
7 - 1	FUO	Factory Use Only	0000000_b
0	Column DOVA Enable	0_b = Column DOVA disabled/Global DOVA enabled 1_b = Column DOVA enabled	0_b

Table 19. Column DOVA Control Register

The architecture of the sensor is based on blocks of 64 columns that are repeated across the array. As a result a certain source of column based noise in this block of 64 columns has a higher probability of repeating itself across the entire array. In order to allow users to correct for such offset errors, the sensor supports up to 4 column address locations that can be specified from 0 to 63 via registers (24-27)h. Further Registers (28-2B)h can be programmed with corressponding offset levels that desire to be applied at these address locations. The Column DOVA RAM; Table 20, is are 4-bit words that contains the offset adjustment used to eliminate the aforementioned column based offset FPN. When the user is calculating values to be loaded, the fixed gain of 2x in the ASP after the Column DOVA circuit must be taken into account. Therefore, each code value in the DOVA RAM represents 2 code values in the 8-bit ADC output.

Address $28\text{-}2B_h$	Column DOVA RAM						Default 00_h
msb (7)	6	5	4	3	2	1	lsb (0)
x	x	x	x	cor[3]	cor[2]	cor[1]	cor[0]

Bit Number	Function	Description	Reset State
7 - 4	Unused	Unused	xxx
3	Sign	0_b = Positive Offset 1_b = Negative Offset	auto
2 - 0	Offset	Offset = 2 * cor_d	auto

Table 20. Column DOVA RAM

The Global DOVA Register; Table 21 performs a final offset adjustment in analog space prior to the ADC. The 6-bit register uses its MSB to indicate positive or nega-

tive offset. Each bit value changes the offset value by 1 LSB code levels hence giving an offset range of +/-31 LSB. .

Address 23_h	Global DOVA						Default 00_h
msb (7)	6	5	4	3	2	1	lsb (0)
x	x	gd[5]	gd[4]	gd[3]	gd[2]	gd[1]	gd[0]

Bit Number	Function	Description	Reset State
7 - 6	Unused	Unused	xx
5	Sign	0_b = Positive Offset 1_b = Negative Offset	0_b
5 - 0	Offset	Offset = gd_d	00000_b

Table 21. Global DOVA Register

5.4 Sensor Interface Block

5.4.1 Sensor Output Control

The sensor output control registers define how the window of interest is captured and what data is output from the SCM20025.

The Capture Mode Control Register; Table 22, defines how the data is captured and how the data is to be provided at the output.

The **sms** bit defines the shutter mode, CFCM or SFCM, of the device as described in section 2.1.3. CFCM is the default mode.

Setting the **cms** bit will stop the current CFCM output data stream at the end of the current frame. Unsetting this bit (**cms** = 0_b) will resume the output of the frame stream. The SCM20025 is in CFCM in default. The user may use this bit to capture data in the CFCM mode while using the SYNC pin. The SYNC pin triggers a single frame of data to be output from the device in the CFCM mode. Please refer to Figure 17, on page 13 for a timing diagram of this mode.

The **frc** bit is used to enable or disable the Frame Rate Clamp. Unsetting this bit will turn off the frame rate clamp and the output dark level will begin to drift over frames. The frame rate clamp is enabled in default mode.

The **sp** bit is used to define whether SOF is active high or low. SOF is active high in default.

The **ve** bit is used to determine whether VCLK is output at the beginning of all the rows including virtual frame rows or for the WOI rows only. The default is WOI only.

The **vp** bit is used to define whether VCLK is active high or low. VCLK is active high in default.

The **he** bit is used to determine whether HCLK is output continuously or for the WOI pixels only. The default is WOI only.

The **hp** bit is used to define whether HCLK is active high or low. HCLK is active high in default.

Address 40_h	Capture Mode Control						Default AA_h
msb (7)	6	5	4	3	2	1	lsb (0)
sms	cms	sp	ve	vp	he	hp	hm

Bit Number	Function	Description	Reset State
7	Shutter Mode	0_b = CFCM 1_b = SFCM	1_b
6	CFCM Mode	0_b = Continuos Frame Stream 1_b = Single Frame	0_b
5	SOF Phase	1_b = SOF active high 0_b = SOF active low	1_b
4	VCLK Enable	1_b = All virtual frame rows 0_b = Window of Interest rows only	0
3	VCLK Phase	1_b = Active high 0_b = Active low	1
2	HCLK Enable	1_b = Continuos 0_b = Window of Interest Pixels only	0_b
1	HCLK Phase	1_b = Active high 0_b = Active low	1_b
0	HCLK Mode	1_b = Continous 0_b = Toggle	0_b

Table 22. Capture Mode Control Register

The Sub-sample Control Register; Table 23, is used to define what pixels of the WOI are read and the method they are read.

The **sm** bit determines the readout mode, defined in section 2.1.4, of the SCM20025, progressive scan or interlaced. In default, data is read out in progressive scan mode.

Using the **cm** bit, the user can sample the pixel array in either monochrome or Bayer pattern color space. This means that when sampling the rows or columns, the set of pixels read will be gathered as individual pixels (monochrome) or in color tiles of pixels (Bayer pattern). The pixels will be read in monochrome mode in default.

The **ptm** bit is used to define how the pixels are output in time. Setting this bit to a 1_b will cause the SCM20025 to output the pixels at the same point in time it would have if the pixel array was fully sampled. Setting this bit to a 0_b (default) will cause the device to burst each row of pixels out at the normal MCLK rate.

The row sampling rate is defined by **rf**[1:0] while the column sampling rate is defined by **cf**[1:0]. The pixel array is fully sampled in default.

Address 43_h	Sub-sample Control						Default 10_h
msb (7)	6	5	4	3	2	1	lsb (0)
x	sm	cm	ptm	rf[1]	rf[0]	cf[1]	cf[0]

Bit Number	Function	Description	Reset State
7-5	Unused	Unused	x
4	Color Mode	1_b = Bayer Pattern Sampling 0_b = Monochrome Pattern Sampling	0_b
3 - 2	Row Frequency	11_b = read one pattern, skip 7 (1/8 sampled) 10_b = read one pattern, skip 3 (1/4 sampled) 01_b = read one pattern, skip one (1/2 sampled) 00_b = full sampling	00_b
1 - 0	Column Frequency	11_b = read one pattern, skip 7 (1/8 sampled) 10_b = read one pattern, skip 3 (1/4 sampled) 01_b = read one pattern, skip one (1/2 sampled) 00_b = full sampling	00_b

Table 23. Sub-sample Control Register

The SOF Control Register and VCLK Control Register; Table 24 and Table 25 respectively, are used to define the size of the SOF and VCLK signals. In default, SOF is one row wide while VLCK is 32 MCLKs wide.

Address 54_h	SOF Control						Default $C2_h$
msb (7)	6	5	4	3	2	1	lsb (0)
sof[7]	sof[6]	sof[5]	sof[4]	sof[3]	sof[2]	sof[1]	sof[0]

Bit Number	Function	Description	Reset State
7 - 6	SOF Control	sof[7:6] = 00_b = 1 MCLK Wide sof[7:6] = 01_b = 8 MCLKs Wide sof[7:6] = 10_b = 32 MCLKs Wide sof[7:6] = 11_b = Full Row Wide	11_b
5 - 0	SOF Start Delay	sof[5:0] = $0x00_b$ = min delay from line transfer time sof[7:6] = $0x01\text{-}1x11_b$ Delay SOF in increments of 1/2 MCLKs	000010_b

Table 24. SOF Control Register

Address 55_h	VCLK Control						Default 98_h
msb (7)	6	5	4	3	2	1	lsb (0)
vck[7]	vck[6]	vck[5]	vck[4]	vck[3]	vck[2]	vck[1]	vck[0]

Bit Number	Function	Description	Reset State
7 - 6	VCLK Control	vck[7:6] = 00_b = 1 MCLK Wide vck[7:6] = 01_b = 8 MCLKs Wide vck[7:6] = 10_b = 32 MCLKs Wide vck[7:6] = 11_b = Full Row Wide	10_b
5 - 0	VCLK Start Delay	sof[5:0] = $0x00_b$ = min delay from SOF start sof[7:6] = 0x01-1x11_b Delay VCLK in increments of 1/2 MCLKs	011000_b

Table 25. VCLK Control Register

The Internal Timing Control Register; Table 26, is used to define the size of internal timing pulse widths. In default, both **shs** and **shr** are 6 MCLK's wide. The user is strongly encouraged to write an 00_h to this register; thus making these pulse widths 16 MCLKs wide.

Address 60_h	**Internal Timing Control**						**Default 66_h**
msb (7)	**6**	**5**	**4**	**3**	**2**	**1**	**lsb (0)**
shs[3]	**shs[2]**	**shs[1]**	**shs[0]**	**shr[3]**	**shr[2]**	**shr[1]**	**shr[0]**
Bit Number	**Function**	**Description**					**Reset State**
7 - 4	shs	shs[3:0] = 000_b = 16 MCLKs Wide shs[3:0] = $1xx_b$ = shs_d MCLKs Wide shs[3:0] = $x1x_b$ = shs_d MCLKs Wide shs[3:0] = $xx1_b$ = shs_d MCLKs Wide					0110_b
3 - 0	shr	shr[3:0] = 000_b = 16 MCLKs Wide shr[3:0] = $1xx_b$ = shr_d MCLKs Wide shr[3:0] = $x1x_b$ = shr_d MCLKs Wide shr[3:0] = $xx1_b$ = shr_d MCLKs Wide					0110_b

Table 26. Internal Timing Control Register

5.4.2 Programmable "Window of Interest"

The WOI is defined by a set of registers that indicate the upper-left starting point for the window and another set of registers that define the size of the window. Please refer to Figure 6, on page 7 for a pictorial representation of the WOI within the active pixel array.

The WOI Row Pointer; **wrp**[8:0] (Table 27 and Table 28), and the WOI Column Pointer; **wcp**[8:0] (Table 29 and Table 30), mark the upper-left starting point for the WOI.

The WOI Row Pointer; **wrp**[8:0], has a valid range of 0_d to 292_d whereas the WOI Column Pointer; **wcp**[8:0] has a usable range of 0_d to 383_d. The pointer can be placed anywhere within the active pixel array.

The WOI Row Depth; **wrd**[8:0] (Table 27 and Table 28), and the WOI Column Depth; **wcd**[8:0] (Table 29 and Table 30), indicate the size of the WOI.

The WOI Row Depth; **wrd**[8:0], has a range of 0_d to 292_d whereas the WOI Column Depth; **wcd**[9:0], has a range of 0_d to 383_d.

The user should be careful to create a WOI that contains active pixels only. There is no logic in the sensor interface to prevent the user from defining an WOI that addresses non-existent pixels.

Address 45_h	**WOI Row Pointer MSB**						**Default 00_h**
msb (7)	**6**	**5**	**4**	**3**	**2**	**1**	**lsb (0)**
x	**x**	**x**	**x**	**x**	**x**	**x**	**wrp[8]**
Bit Number	**Function**	**Description**					**Reset State**
7 - 1	Unused	Unused					xxxxxxxx

Table 27. WOI Row Pointer MSB Register

Address 45_h	WOI Row Pointer MSB						Default 00_h
msb (7)	6	5	4	3	2	1	lsb (0)
x	x	x	x	x	x	x	wrp[8]
0	WOI Row Pointer	In conjunction with the WOI Row Pointer LSB Register (Table 28), forms the 9-bit WOI Row Pointer wrp[8:0]					0_b

Table 27. WOI Row Pointer MSB Register

Address 46_h	WOI Row Pointer LSB						Default 08_h
msb (7)	6	5	4	3	2	1	lsb (0)
wrp[7]	wrp[6]	wrp[5]	wrp[4]	wrp[3]	wrp[2]	wrp[1]	wrp[0]
Bit Number	**Function**	**Description**					**Reset State**
7 - 0	WOI Row Pointer	In conjunction with the WOI Row Pointer MSB Register (Table 27), forms the 9-bit WOI Row Pointer wrp[8:0]					00001000_b (row 8)

Table 28. WOI Row Pointer LSB Register

Address 49_h	WOI Column Pointer MSB						Default 00_h
msb (7)	6	5	4	3	2	1	lsb (0)
x	x	x	x	x	x	x]	wcp[8]
Bit Number	**Function**	**Description**					**Reset State**
7 - 1	Unused	Unused					xxxxxx
0	WOI Col. Pointer	In conjunction with the WOI Column Pointer LSB Register (Table 30), forms the 8-bit WOI Column Pointer wcp[8:0]					00_b

Table 29. WOI Column Pointer MSB Register

Address $4A_h$	WOI Column Pointer LSB						Default $1A_h$
msb (7)	6	5	4	3	2	1	lsb (0)
wcp[7]	wcp[6]	wcp5]	wcp[4]	wcp[3]	wcp[2]	wcp[1]	wcp[0]
Bit Number	**Function**	**Description**					**Reset State**
7 - 0	WOI Col. Pointer	In conjunction with the WOI Column Pointer MSB Register (Table 29), forms the 8-bit WOI Column Pointer wcp[8:0]					00011010_b (col. 26)

Table 30. WOI Column Pointer LSB Register

Address 47_h	WOI Row Depth MSB						Default 01_h
msb (7)	6	5	4	3	2	1	lsb (0)
x	x	x	x	x	x	x	wrd[8]
Bit Number	**Function**	**Description**					**Reset State**
7 - 1	Unused	Unused					xxxxxxx
0	WOI Row Depth	In conjunction with the WOI Row Depth LSB Register (Table 32), forms the 9-bit WOI Row Depth wrd[8:0].					1_b

Table 31. WOI Row Depth MSB Register

Address 48_h	WOI Row Depth LSB						Default $1F_h$
msb (7)	6	5	4	3	2	1	lsb (0)
wrd[7]	wrd[6]	wrd[5]	wrd[4]	wrd[3]	wrd[2]	wrd[1]	wrd[0]
Bit Number	**Function**	**Description**					**Reset State**
7 - 0	WOI Row Pointer	In conjunction with the WOI Row Depth MSB Register (Table 31), forms the 9-bit WOI Row Depth wrd[8:0]. Desired = $wrd_d + 1$.					00011111_b (287+1 rows)

Table 32. WOI Row Depth LSB Register

Address $4B_h$	WOI Column Width MSB						Default 02_h
msb (7)	6	5	4	3	2	1	lsb (0)
x	x	x	x	x	x	x	wcw[8]
Bit Number	**Function**	**Description**					**Reset State**
7 - 1	Unused	Unused					xxxxxx
0	WOI Col. Width	In conjunction with the WOI Column Width LSB Register (Table 34), forms the 8-bit WOI Column Width wcw[8:0].					1_b

Table 33. WOI Column Width MSB Register

Address $4C_h$	WOI Column Width LSB						Default $6F_h$
msb (7)	6	5	4	3	2	1	lsb (0)
wcw[7]	wcw[6]	wcw[5]	wcw[4]	wcw[3]	wcw[2]	wcw[1]	wcw[0]
Bit Number	**Function**	**Description**					**Reset State**
7 - 0	WOI Row Pointer	In conjunction with the WOI Column Width MSB Register (Table 33), forms the 8-bit WOI Column Width wcw[9:0]. Desired = $wcw_d + 1$.					01011111_b (351+1 col.)

Table 34. WOI Column Width LSB Register

5.4.3 Integration Time Control

The Integration Time registers; Table 35, Table 36, and Table 37, control the integration time for the pixel array. Integration time for SFCM; **sint**[20:0], is measured in MCLK cycles while the integration time for CFCM; **cint**[15:0], is measured in Virtual Row times. Please refer to Figure 8 for a pictorial description of the Virtual Frame and its relationship to the WOI.

A virtual frame is the mechanism by which the user controls the integration time and frame time for the output data stream. By adding additional rows or columns as 'blanking' to the WOI to form the Virtual Frame, the user can control the amount of blanking in both horizontal and vertical space.

Both the Virtual Frame Row Depth; **vrd**[13:0], and the Virtual Frame Column Width; **vcw**[9:0] have a range of 0_d to 16384_d.

The user should be careful to create a Virtual Frame that is larger than the WOI. There is no logic in the sensor interface to prevent the user from defining a Virtual Frame smaller than the WOI. Therefore, pixel data may be lost.

The Virtual Frame must be 1 row and 6 columns larger than the WOI.

The Virtual Frame completely defines the integration time in CFCM. Any changes to the WOI or how the WOI is sampled has no effect on integration time.

Address $4D_h$	Integration Time MSB						Default 00_h
msb (7)	6	5	4	3	2	1	lsb (0)
x	x	x	x	sint[19]	sint[18]	sint[17]	sint[16]

Bit Number	Function	Description	Reset State
7 - 4	Unused	Unused	xxxx
3 - 0	Integration Time	**SFCM**: In conjunction with the Integration Time ISB (Table 36) and Integration Time LSB (Table 37) Registers, forms the 20-bit Integration Time sint[19:0]. **CFCM**: Unused	0000_b

Table 35. Integration Time MSB Register

Address $4E_h$	Integration Time ISB						Default 01_h
msb (7)	6	5	4	3	2	1	lsb (0)
sint[15] cint[15]	sint[14] cint[14]	sint[13] cint[13]	sint[12] cint[12]	sint[11] cint[11]	sint[10] cint[10]	sint[9] cint[9]	sint[8] cint[8]

Bit Number	Function	Description	Reset State
7 - 0	Integration Time	**SFCM**: In conjunction with the Integration Time MSB (Table 35) and Integration Time LSB (Table 37) Registers, forms the 20-bit Integration Time sint[19:0]. **CFCM**: In conjunction with the Integration Time LSB (Table 37) Register, forms the 16-bit Integration Time cint[15:0].	00000001_b

Table 36. Integration Time ISB Register

Address $4F_h$	Integration Time LSB						Default $F3_h$
msb (7)	6	5	4	3	2	1	lsb (0)
sint[7] cint[7]	sint[6] cint[6]	sint[5] cint[5]	sint[4] cint[4]	sint[3] cint[3]	sint[2] cint[2]	sint[1] cint[1]	sint[0] cint[0]
Bit Number	**Function**	**Description**					**Reset State**
7 - 0	Integration Time	**SFCM**: In conjunction with the Integration Time MSB (Table 35) and Integration Time ISB (Table 36) Registers, forms the 20-bit Integration Time sint[19:0]. Integration Time = $sint_d$ * 16 * MCLKperiod. **CFCM**: In conjunction with the Integration Time ISB (Table 36) Register, forms the 16-bit Integration Time cint[15:0]. Integration Time = ($cint_d$ + 1) * T_{row}						11110011_b (**SFCM**: 7984 MCLKs **CFCM**: 500 Rows)

Table 37. Integration Time LSB Register

Address 50_h	CFCM Virtual Frame Row Depth MSB						Default 01_h
msb (7)	6	5	4	3	2	1	lsb (0)
x	x	vrd[13]	vrd[12]	vrd[11]	vrd[10]	vrd[9]	vrd[8]
Bit Number	**Function**	**Description**					**Reset State**
7 - 6	Unused	Unused					xx
5 - 0	Virtual Row Depth	In conjunction with the CFCM Virtual Frame Row Depth LSB (Table 39) Register, forms the 14-bit Virtual Frame Row Depth vrd[13:0].					000001_b

Table 38. CFCM Virtual Frame Row Depth MSB Register

Address 51_h	CFCM Virtual Frame Row Depth LSB						Default $F3_h$
msb (7)	6	5	4	3	2	1	lsb (0)
vrd[7]	vrd[6]	vrd[5]	vrd[4]	vrd[3]	vrd[2]	vrd[1]	vrd[0]
Bit Number	**Function**	**Description**					**Reset State**
7 - 0	Virtual Row Depth	In conjunction with the CFCM Virtual Frame Row Depth MSB (Table 38) Register, forms the 14-bit Virtual Frame Row Depth vrd[13:0]. WOI is always top-left justified in Virtual Frame. vrd_d minimum = wrd_d + 1					11110011_b (500 rows)

Table 39. CFCM Virtual Frame Row Depth LSB Register

Address 52_h	CFCM Virtual Frame Column Width MSB						Default 01_h
msb (7)	6	5	4	3	2	1	lsb (0)
x	x	vcw[13]	vcw[12]	vcw[11]	vcw[10]	vcw[9]	vcw[8]
Bit Number	**Function**	**Description**					**Reset State**
7 - 6	Unused	Unused					xx
5 - 0	Virtual Column Width	In conjunction with the CFCM Virtual Frame Column Width LSB (Table 41) Register, forms the 14-bit Virtual Frame Column Width vcw[13:0].					000001_b

Table 40. CFCM Virtual Frame Column Width MSB Register

Address 53_h	CFCM Virtual Frame Column Width LSB						Default 70_h
msb (7)	6	5	4	3	2	1	lsb (0)
vcw[7]	vcw[6]	vcw[5]	vcw[4]	vcw[3]	vcw[2]	vcw[1]	vcw[0]
Bit Number	**Function**	**Description**					**Reset State**
7 - 0	Virtual Column Width	In conjunction with the CFCM Virtual Frame Column Width MSB (Table 40) Register, forms the 14-bit Virtual Frame Column Width vcw[13:0]. WOI is always top-left justified in Virtual Frame. vcw_d minimum = wcw_d + 11 (CFCM) vcw_d minimum = wcw_d + 14 (SFCM)					011100001 b (368 col.)

Table 41. CFCM Virtual Frame Column Width LSB Register

6.0 I²C Serial Interface

The I²C is an industry standard which is also compatible with the Motorola bus (called M-Bus) available on many microprocessor products. The I²C contains a serial two-wire half-duplex interface that features bidirectional operation, master or slave modes, and multi-master environment support. The clock frequency on the system is governed by the slowest device on the board. The SDATA and SCLK are the bidirectional data and clock pins, respectively. These pins are open drain and will require a pull-up resistor to VDD of 1.5 kΩ to 10 kΩ (see page 45).

The I²C is used to write the required user system data into the Program Control Registers in the SCM20025. The I²C bus can also read the data in the Program Control Register for verification or test considerations. The SCM20025 is a slave only device that supports a maximum clock rate (SCLK) of 100 kHz while reading or writing only one register address per I²C start/stop cycle. The following sections will be limited to the methods for writing and reading data into the SCM20025 register.

For a complete reference to I²C, see *The I²C Bus from Theory to Practice*, by Dominique Paret and Carll-Fenger, published by John Wiley & Sons, ISBN 0471962686.

6.1 SCM20025 I²C Bus Protocol

The SCM20025 uses the I²C bus to write or read one register byte per start/stop I²C cycle as shown in Figure 22 and Figure 23. These figures will be used to describe the various parts of the I²C protocol communications as it applies to the SCM20025.

SCM20025 I²C bus communication is basically composed of following parts: START signal, SCM20025 slave address (0111000_b) transmission followed by a R/W bit, an acknowledgment signal from the slave, 8 bit data transfer followed by another acknowledgment signal, STOP signal, repeated START signal, and clock synchronization.

6.2 START Signal

When the bus is free, i.e. no master device is engaging the bus (both SCLK and SDATA lines are at logical “1”), a master may initiate communication by sending a START signal. As shown in Figure 22, a START signal is defined as a high-to-low transition of SDATA while SCLK is high. This signal denotes the beginning of a new data transfer and wakes up all the slaves on the bus.

6.3 Slave Address Transmission

The first byte of a data transfer, immediately after the START signal, is the slave address transmitted by the master. This is a 7-bit calling address followed by a R/W bit. The seven-bit address for the SCM20025, starting with the MSB (AD7) is 0111000_b. The transmitted calling address on the SDATA line may only be changed while SCLK is low as shown in Figure 22. The data on the SDATA line is valid on the High to Low signal transition on the SCLK line. The R/W bit following the 7-bit tells the slave the desired direction of data transfer:

- 1 = Read transfer, the slave transitions to a slave transmitter and sends the data to the master
- 0 = Write transfer, the master transmits data to the slave

6.4 Acknowledgment

Only the slave with a calling address that matches the one transmitted by the master will respond by sending back an acknowledge bit. This is done by pulling the SDATA line low at the 9th clock (see Figure 22). If a transmitted slave address is acknowledged, successful slave addressing is said to have been achieved. No two slaves in the system may have the same address. The SCM20025 is configured to be a slave only.

6.5 Data Transfer

Once successful slave addressing is achieved, data transfer can proceed between the master and the selected slave in a direction specified by the R/W bit sent by the calling master. Note that for the first byte after a start signal (in Figure 22 and Figure 23), the R/W bit is always a “0” designating a write transfer. This is required since the next data transfer will contain the register address to be read or written.

All transfers that come after a calling address cycle are referred to as data transfers, even if they carry sub-address information for the slave device.

Each data byte is 8 bits long. Data may be changed only while SCLK is low and must be held stable while SCLK is high as shown in Figure 22. There is one clock pulse on SCLK for each data bit, the MSB being transferred first.

Each data byte has to be followed by an acknowledge bit, which is signalled from the receiving device by pulling the SDATA low at the ninth clock. So one complete data byte transfer needs nine clock pulses. If the slave receiver does not acknowledge the master, the SDATA line must be left high by the slave. The master can then generate a stop signal to abort the data transfer or a start signal (repeated start) to commence a new calling.

If the master receiver does not acknowledge the slave transmitter after a byte transmission, it means 'end of data' to the slave, so the slave releases the SDATA line for the master to generate STOP or START signal.

6.6 Stop Signal

The master can terminate the communication by generating a STOP signal to free the bus. However, the master may generate a START signal followed by a calling command without generating a STOP signal first. This is called a Repeated START. A STOP signal is defined as a low-to-high transition of SDATA while SCLK is at logical “1” (see Figure 22).

The master can generate a STOP even if the slave has generated an acknowledge bit at which point the slave must release the bus.

6.7 Repeated START Signal

A Repeated START signal is a START signal generated without first generating a STOP signal to terminate the communication. This is used by the master to communicate with another slave or with the same slave in a different mode (transmit/receive mode) without releasing the bus.

As shown in Figure 23, a Repeated START signal is being used during the read cycle and to redirect the data transfer from a write cycle (master transmits the register address to the slave) to a read cycle (slave transmits the data from the designated register to the slave).

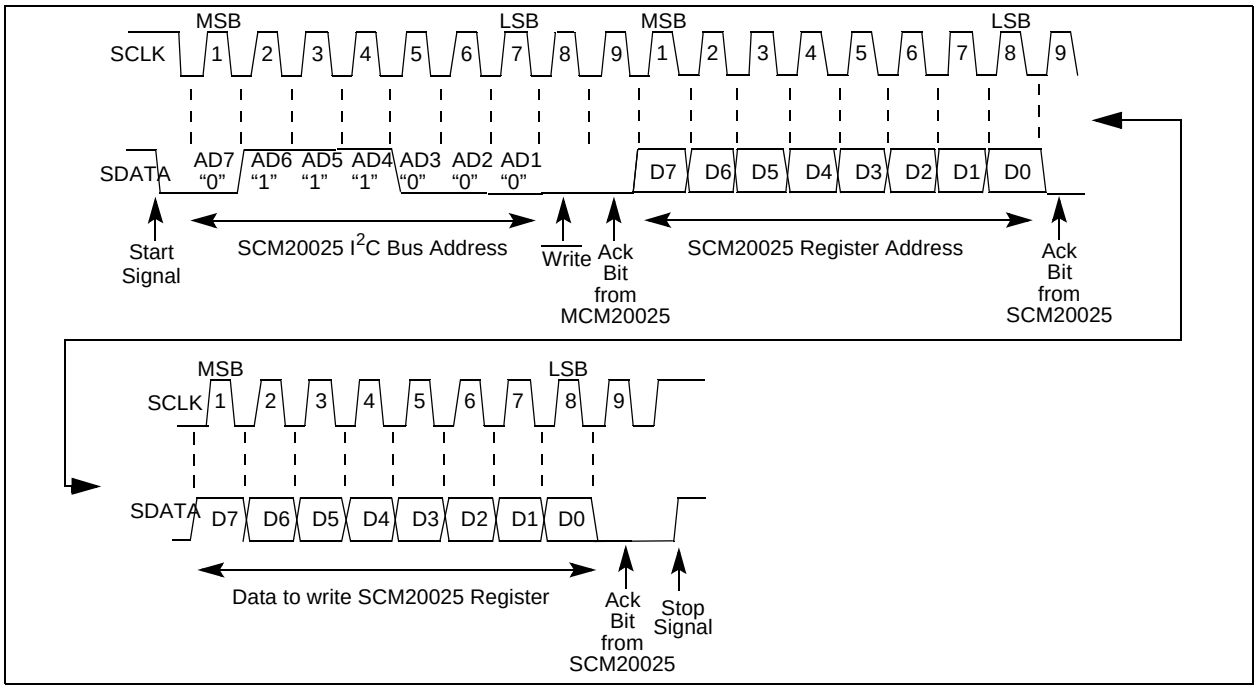


Figure 22. WRITE Cycle using I2C Bus

6.8 I2C Bus Clocking and Synchronization

Open drain outputs are used on the SCLK outputs of all master and slave devices so that the clock can be synchronized and stretched using wire-AND logic. This means that the slowest device will keep the bus from going faster than it is capable of receiving or transmitting data.

After the master has driven SCLK from High to Low, all the slaves drive SCLK Low for the required period that is needed by each slave device and then releases the SCLK bus. If the slave SCLK Low period is greater than the master SCLK Low period, the resulting SCLK bus signal Low period is stretched. Therefore, synchronized clocking occurs since the SCLK is held low by the device with the longest Low period. Also, this method can be used by the slaves to slow down the bit rate of a transfer. The master controls the length of time that the SCLK line is in the High state. The data on the SDATA line is valid when the master switches the SCLK line from a High to a Low.

Slave devices may hold the SCLK low after completion of one byte transfer (9 bits). In such case, it halts the bus clock and forces the master clock into wait states until the slave releases the SCLK line.

6.9 Register Write

Writing the SCM20025 registers is accomplished with the following I2C transactions (see Figure 22):

- Master transmits a START
- Master transmits the SCM20025 Slave Calling Address with "WRITE" indicated (BYTE=70_h, 112_d, 01110000_b)
- SCM20025 slave sends acknowledgment by forcing the SDATA Low during the 9th clock, if the Calling Address was received
- Master transmits the SCM20025 Register Address
- SCM20025 slave sends acknowledgment by forcing the SDATA Low during the 9th clock after receiving the Register Address
- Master transmits the data to be written into the register at the previously received Register Address
- SCM20025 slave sends acknowledgment by forcing the SDATA Low during the 9th clock after receiving the data to be written into the Register Address
- Master transmits STOP to end the write cycle

6.10 Register Read

Reading the SCM20025 registers is accomplished with the following I2C transactions (see Figure 23):

- Master transmits a START
- Master transmits the SCM20025 Slave Calling Address with “WRITE” indicated (BYTE=70_h, 112_d, 01110000_b)
- SCM20025 slave sends acknowledgment by forcing the SData Low during the 9th clock, if the Calling Address was received
- Master transmits the SCM20025 Register Address
- SCM20025 slave sends acknowledgment by forcing the SData Low during the 9th clock after receiving the Register Address
- Master transmits a Repeated START
- Master transmits the SCM20025 Slave Calling Address with “READ” indicated (BYTE = 71_h, 113_d, 01110001_b)
- SCM20025 slave sends acknowledgment by forcing the SDATA Low during the 9th clock, if the Calling Address was received
- At this point, the SCM20025 transitions from a “Slave-Receiver” to a “Slave-Transmitter”
- SCM20025 sends the SCLK and the Register Data contained in the Register Address that was previously received from the master; SCM20025 transitions to slave-receiver
- Master does not send an acknowledgment (NAK)
- Master transmits STOP to end the read cycle

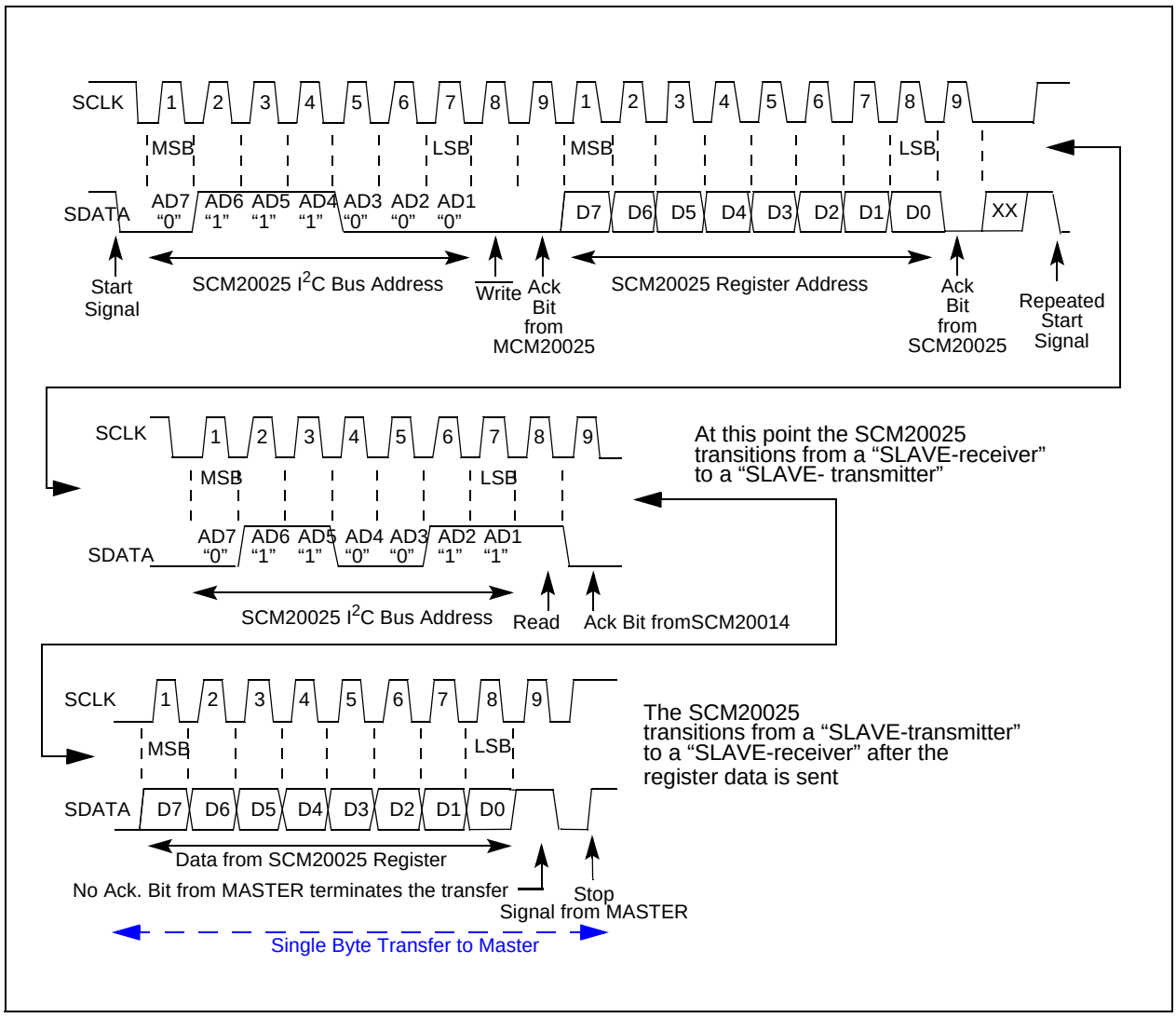


Figure 23. READ Cycle using I2C Bus

7.0 Electrical Characteristics

ABSOLUTE MAXIMUM RATINGS[1] (Voltages Referenced to VSS)			
Symbol	**Parameter**	**Value**	**Unit**
V_{DD}	DC Supply Voltage	-0.5 to 3.8	V
V_{in}	DC Input Voltage	0.5 to V_{DD} + 0.5	V
V_{out}	DC Output Voltage	-0.5 to V_{DD} + 0.5	V
I	DC Current Drain per Pin, Any Single Input or Output	±50	mA
I	DC Current Drain, V_{DD} and V_{SS} Pins	±100	mA
T_{STG}	Storage Temperature Range	-65 to +150	°C
T_L	Lead Temperature (10 second soldering)	300	°C

[1] Maximum Ratings are those values beyond which damage to the device may occur.

$V_{SS} = AV_{SS} = DV_{SS} = V_{SSO}$ ($DV_{SS} = V_{SS}$ of Digital circuit, $AV_{SS} = V_{SS}$ of Analog Circuit)
$V_{DD} = AV_{DD} = DV_{DD} = V_{DDO}$ ($DV_{DD} = V_{DD}$ of Digital circuit, $AV_{DD} = V_{DD}$ of Analog Circuit)

RECOMMENDED OPERATING CONDITIONS (to guarantee functionality; voltage referenced to VSS)				
Symbol	Parameter	Min	Max	Unit
V_{DD}	DC Supply Voltage, V_{DD} = 3.3V (Nominal)	3.0	3.6	V
T_A	Commercial Operating Temperature	0	40	°C
T_J	Junction Temperature	0	55	°C

Notes:
- All parameters are characterized for DC conditions after thermal equilibrium has been established.
- Unused inputs must always be tied to an appropriate logic level, e.g., either V_{SS} or V_{DD}.
- This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than the maximum rated voltages to this high impedance circuit.
- For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

DC ELECTRICAL CHARACTERISTICS (V_{DD} = 3.3V ± 0.3V; V_{DD} referenced to V_{SS}; T_a = 0°C to 40°C)					
			T_A = 0°C to 40°C		
Symbol	Characteristic	Condition	Min	Max	Unit
V_{IH}	Input High Voltage		2.0	V_{DD}+0.3	V
V_{IL}	Input Low Voltage		-0.3	0.8	V
I_{in}	Input Leakage Current, No Pull-up Resistor	$V_{in} = V_{DD}$ or V_{SS}	-5	5	µA
I_{OH}	Output High Current	V_{DD} = Min, V_{OH} Min = 0.8 * V_{DD}	-3		mA
I_{OL}	Output Low Current	V_{DD} = Min, V_{OL} Max = 0.4 V	3		mA
V_{OH}	Output High Voltage	V_{DD} = Min, I_{OH} = -100µA	V_{DD} - 0.2		V
V_{OL}	Output Low Voltage	V_{DD} = Min, I_{OL} = 100µA		0.2	V
I_{OZ}	3-State Output Leakage Current	Output = High Impedance, $V_{out} = V_{DD}$ or V_{SS}	-10	10	µA
I_{DD}	Maximum Standby Supply Current	I_{out} = 0mA, $V_{in} = V_{DD}$ or V_{SS}	0	15.0	mA

POWER DISSIPATION (VDD = 3.0V, VDD referenced to VSS; Ta = 25°C)				
Symbol	Parameter	Condition	Typ	Unit
P_{DYN}	Dynamic Power	13.5 MHz MCLK Clock frequency	200	mW
P_{STDBY}	Standby Power	STDBY Pin Logic High	50	mW
P_{AVG}	Average Power	13.5 MHz Operation (using STDBY)	100	mW

SCM20025 MONOCHROME CMOS IMAGE SENSOR ELECTRO-OPTICAL CHARACTERISTICS				
Symbol	Parameter	Typ	Unit	Notes
E_{sat}	Saturation Exposure	0.14	$\mu J/cm^2$	1
QE	Peak Quantum Efficiency (@550nm)	18	%	2
PRNU	Photoresponse Non-uniformity	12	% pk-pk	3

Notes:
1.For λ = 550 nm wavelength.
2.Refer to typical values from Figure 3, SCM20025 nominal spectral response.
3.For a 100 x 100 pixel region under uniform illumination with output signal equal to 80% of saturation signal.

SCM20025 COLOR CMOS IMAGE SENSOR ELECTRO-OPTICAL CHARACTERISTICS				
Symbol	Parameter	Typ	Unit	Notes
E_{sat}	Saturation Exposure	0.3	$\mu J/cm^2$	1
QE_r	Red Peak Quantum Efficiency @ λ = 650 nm	12	%	2
QE_g	Green Peak Quantum Efficiency @ λ = 550 nm	11	%	2
QE_b	Blue Peak Quantum Efficiency @ λ = 450 nm	8	%	2

Notes:
1.For λ = 550 nm wavelength.
2.Refer to typical values from Figure 3, SCM20025 nominal spectral response.

CMOS IMAGE SENSOR CHARACTERISTICS				
Symbol	Parameter	Typ	Unit	Notes
	Sensitivity	3.0	V/lux-sec	
I_d	Photodiode Dark Current	0.2	nA/cm^2	
DSNU	Dark Signal Non-Uniformity (Entire Field)	0.4	% rms	
CTE	Pixel Charge Transfer Efficiency	0.9995	%	1
f_H	Horizontal Imager Frequency	11.5	MHz	4
X_{ab}	Blooming Margin - shuttered light	200		2,3

Notes:
1. Transfer efficiency of photosite
2. X_{ab} represents the increase above the saturation-irradiance level (H_{sat}) that the device can be exposed to before blooming of the pixel will occur.
3. No column streaking
4. At 110fps CIF

GENERAL				
Symbol	Parameter	Typ	Unit	Notes
$n_{e^- total}$	Total System (equivalent) Noise Floor	70	e^- rms	1
DR	System Dynamic Range	42	dB	

Notes:
1.Includes amplifier noise, dark pattern noise and dark current shot noise at 13.5 MHz data rates.

ANALOG SIGNAL PROCESSOR CHARACTERISTICS

Analog to Digital Converter (ADC)					
Symbol	Parameter	Min	Typ	Max	Units
	Resolution		8		bits
V_{IN}	Input Dynamic Range[8]		2.5		Vpp
INL	Integral Non-Linearity		±1.0		LSB
DNL	Differential Non-Linearity		±0.5		LSB
f_{max}	ADC Clock Rate			13.5	MHz

Notes:
[8] Effective differential signal dynamic range
9. INL & DNL test limits are adjusted to compensate for the effects of the FRC, DOVA and DPGA stages between the EXT_VINS input and the input of the ADC.

I²C SERIAL INTERFACE[6] TIMING SPECIFICATIONS (see Figure 24)				
Symbol	**Characteristic**	**Min**	**Max**	**Unit**
f_{max}	SCLK maximum frequency	50	400	KHz
M1	Start condition SCLK hold time	4	-	T_{MCLK}[7]
M2	SCLK low period	8	-	T_{MCLK}
M3	SCLK/SDATA rise time [from V_{IL} = (0.2)*VDD to V_{IH} = (.8)*VDD]	-	.3	µs[8]
M4	SDATA hold time	4	-	T_{MCLK}[7]
M5	SCLK/SDATA fall time (from Vh = 2.4V to Vl = 0.5V)	-	.3	µs[8]
M6	SCLK high period	4	-	T_{MCLK}
M7	SDATA setup time	4	-	T_{MCLK}[7]
M8	Start / Repeated Start condition SCLK setup time	4	-	T_{MCLK}
M9	Stop condition SCLK setup time	4	-	T_{MCLK}
C_I	Capacitive for each I/O pin	-	10	pF
Cbus	Capacitive bus load for SCLK and SDATA	-	200	pF
Rp	Pull-up Resistor on SCLK and SDATA	1.5	10	kΩ[9]

[6] I²C is a proprietary Philips interface bus
[7] The unit T_{MCLK} is the period of the input master clock; The frequency of MCLK is assumed 13.5 MHz
[8] The capacitive load is 200 pF
[9] A pull-up resistor to VDD is required on each of the SCLK and SDATA lines; for a maximum bus capacitive load of 200 pf, the minimum value of Rp should be selected in order to meet specifications

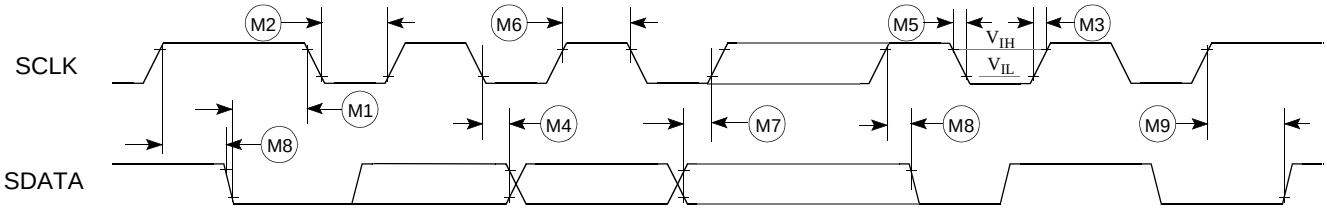


Figure 24. I²C Bus Timing Diagram

PIXEL DATA BUS INTERFACE TIMING SPECIFICATIONS (see Figure 25)

Symbol	Characteristic	Min	Typ	Max	Unit
f_{max}	MCLK maximum frequency	1	11.5	13.5	MHz
t_{hsync}	SYNC hold time w.r.t MCLK	3.5	-	9	ns
t_{susync}	SYNC setup time w.r.t MCLK	3.0	-	8.5	ns
t_{dsof}	MCLK to SOF delay time	8	13	21.5	ns
t_{dvclk}	MCLK to VCLK delay time	8.5	13.5	22	ns
t_{drhclk}	Rising edge of MCLK to rising edge of HCLK delay time	7.5	13	22	ns
t_{dfhclk}	Falling edge of MCLK to falling edge of HCLK delay time	3	5	10.5	ns
t_{dadc}	MCLK to ADC[9:0] delay time	8	13	21.5	ns
t_{dblank}	MCLK to BLANK delay time	8	13	21.5	ns

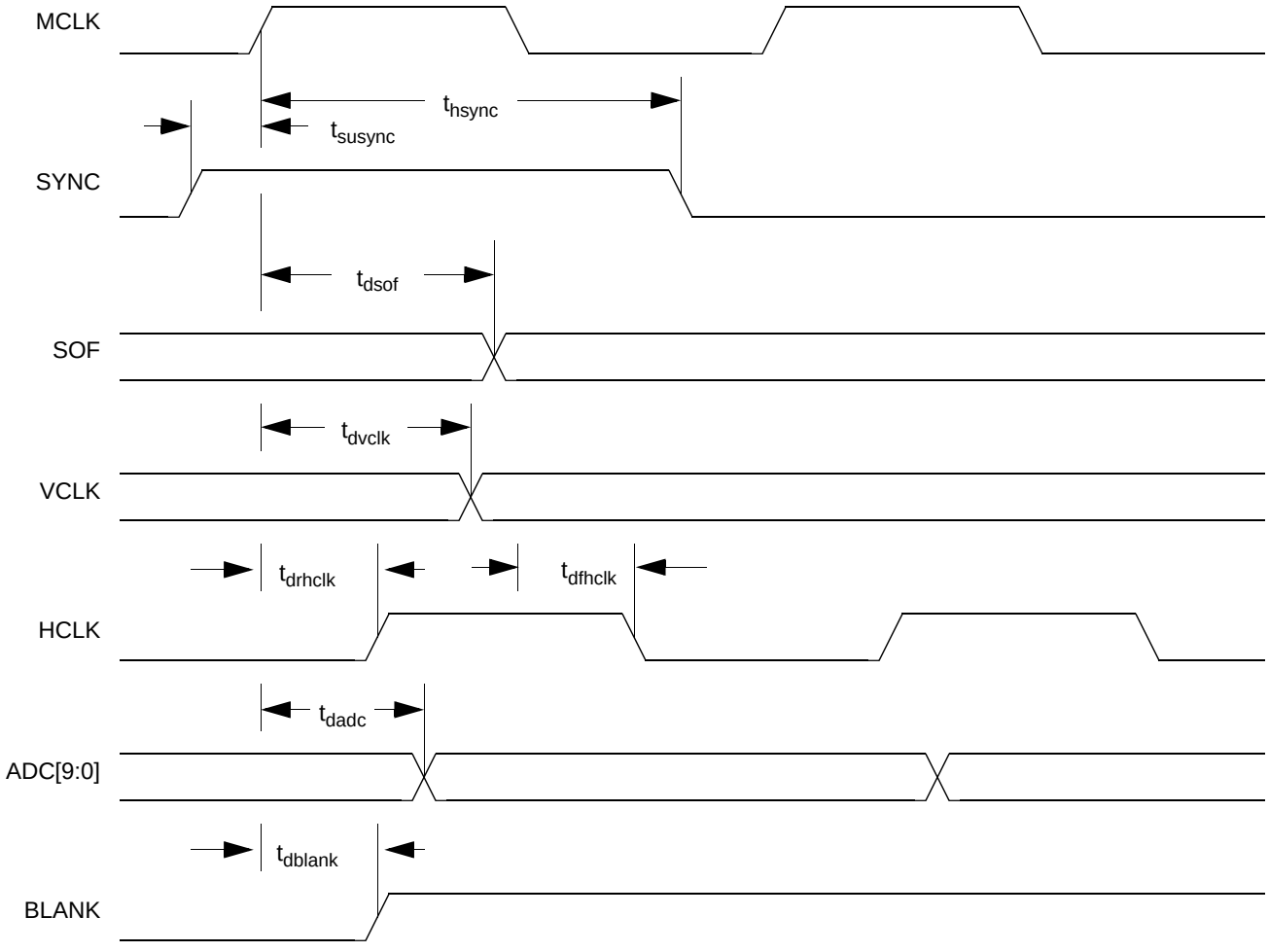


Figure 25. Pixel Data Bus Timing Diagram

Table 42. SCM20025 Pin Definitions

Pin No.	Pin Name	Description	Pin Type	Power
1	SYNC	Sensor Sync Signal	I	
2	SOF	Start Of Frame	O	
3	INIT	Sensor Initialize	I	
4	AVSS	Analog Ground	G	A
5	AVDD	Analog Power	P	A
6	EXTRES	External Bias Resistor Input	I	
7	CVREFM	Bias Reference Bottom Output	O	
8	CVREFP	Bias Reference Top Output	O	
9	AVDD	Analog Power	P	A
10	CLRCA	Line Rate Clamp Output	O	
11	AVSS	Analog Ground	G	A
12	TEST_AI	Test Analog Chain Input	I	
13	CLRCB	Line Rate Clamp Output	O	
14	SCLK	I2C Serial Clock	I/O	

Pin No.	Pin Name	Description	Pin Type	Power
15	SDATA	I2C Serial Data	I/O	
16	ADC7	Output Bit 7 = 128_{10} Weight	O	
17	ADC6	Output Bit 7 = 64_{10} Weight	O	
18	ADC5	Output Bit 7 = 32_{10} Weight	O	
19	ADC4	Output Bit 7 = 16_{10} Weight	O	
20	ADC3	Output Bit 7 = 8_{10} Weight	O	
21	DVSS	Digital Ground	G	D
22	DVDD	Digital Power	P	D
23	ADC2	Output Bit 7 = 4_{10} Weight	O	
24	ADC1	Output Bit 7 = 2_{10} Weight	O	
25	ADC0	Output Bit 7 = 1_{10} Weight	O	
26	MCLK	Master Clock	I	
27	HCLK	Pixel Sync	O	
28	VCLK	Line Sync	O	

note: pins 1 should
be pulled down when not in use
pins 14,15 should be pulled high
pins 7,8,10,13 should have 0.1uF
or appropriate value capacitors

Legend:
P = V_{DD}
G = V_{SS}
I = Input
O = Output
D = Digital
A = Analog

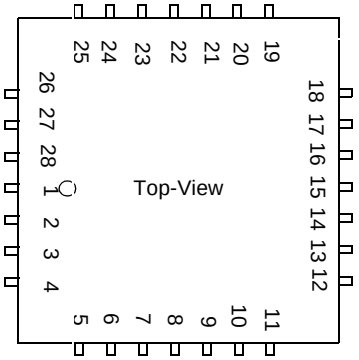


Figure 26. SCM20025 Pinout Diagram

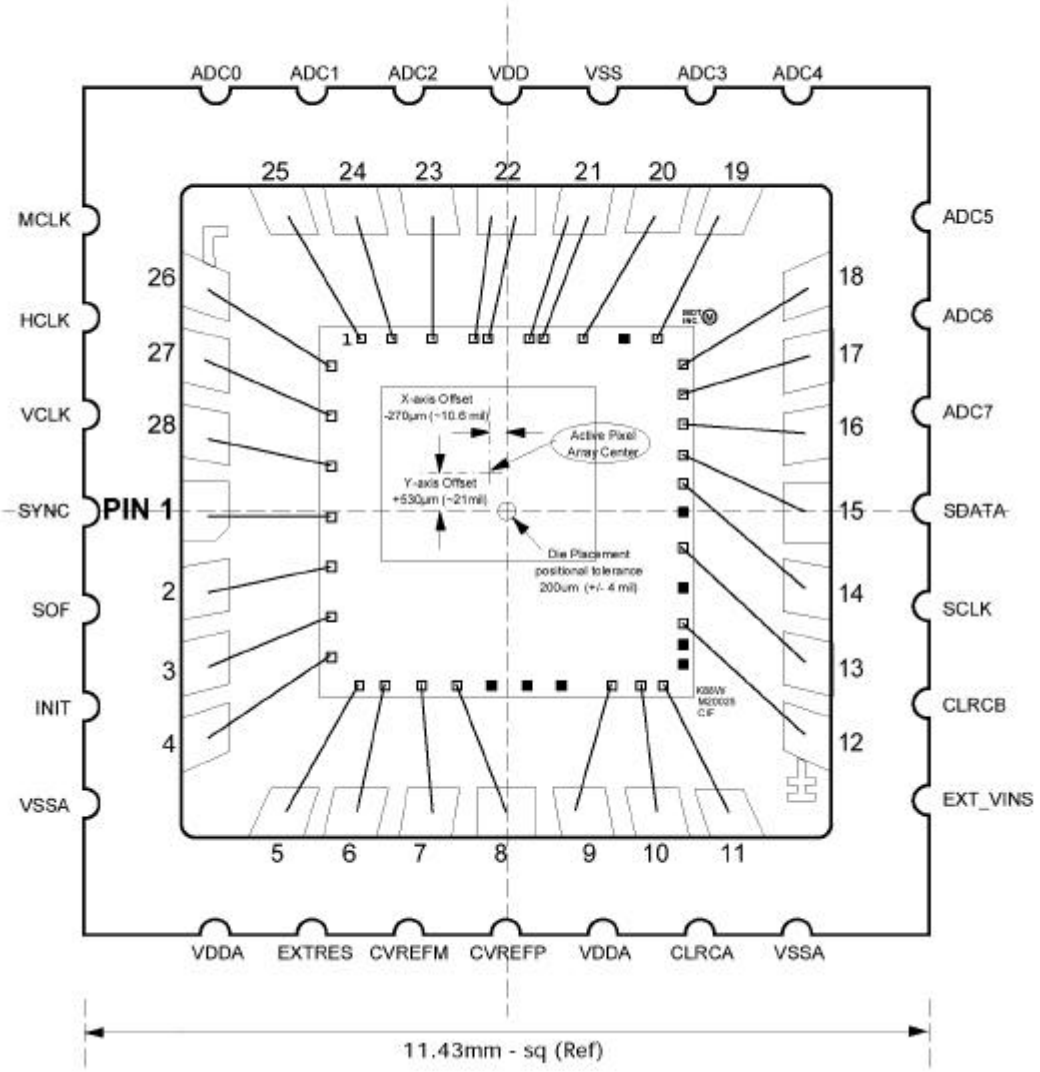


Figure 27. 28 Terminal ceramic leadless chip carrier (bottom view)

Note: For the most current information regarding this product, contact Motorola on the World Wide Web at http://www.motorola.com/adc/Image_Capture/

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