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Advance Information

PowerPC 602™ RISC Microprocessor Hardware Specification

The PowerPC 602 microprocessor is an implementation of the PowerPC™ family of reduced instruction set computing (RISC) microprocessors. This document contains pertinent information on the physical characteristics of the 602. For functional characteristics of the processor, refer to the *PowerPC 602 RISC Microprocessor User's Manual.*

This document contains the following topics:

In this document, the term "602" is used as an abbreviation for the phrase "PowerPC 602 microprocessor." The PowerPC 602 microprocessors are available from Motorola as MPC602 and from IBM as PPC602 and EMPPC602.

1.1 Overview

The 602 is a low-cost, low-power implementation of the PowerPC microprocessor family of reduced instruction set computing (RISC) microprocessors. The 602 implements the 32-bit portion of the PowerPC architecture, which provides 32-bit effective addresses, integer data types of 8, 16, and 32 bits, and floating-point data types of 32 and 64 bits. Floating-point operations involving 64-bit data types are not implemented in the 602. Double-precision floating point operations are trapped for emulation in software.

The 602 provides four software controllable power-saving modes. Three of the modes (the nap, doze, and sleep modes) are static in nature, and progressively reduce the amount of power dissipated by the processor. The fourth is a dynamic power management mode that causes the functional units in the 602 to automatically enter a low-power mode when the functional units are idle without affecting operational performance, software execution, or any external hardware.

The 602 is a superscalar processor capable of issuing two instructions (which includes one branch). Branches are folded out, and the 602 retires one instruction per clock. Instructions can execute out of order for increased performance; however, the 602 makes completion appear sequential.

The 602 integrates four execution units—an integer unit (IU), a floating-point unit (FPU), a branch processing unit (BPU), and a load/store unit (LSU). The ability to execute four instructions in parallel and the use of simple instructions with rapid execution times yield high efficiency and throughput for 602-based systems. Most integer instructions execute in one clock cycle. The FPU is pipelined so a single-precision multiply-add instruction can be issued every clock cycle.

The 602 provides independent on-chip, 4-Kbyte, two-way set-associative, physically addressed caches for instructions and data as well as on-chip instruction and data memory management units (MMUs). The 602 MMUs contain 32-entry, two-way set-associative, data and instruction translation lookaside buffers (DTLB and ITLB). The TLBs and caches use a least recently used (LRU) replacement algorithm. The 602 also supports block address translation through the use of two independent instruction and data block address translation (IBAT and DBAT) arrays of four entries each. Effective addresses are compared simultaneously with all four entries in the BAT array during block translation. If an effective address matches against any entry in the BATs, the BAT entry takes priority over any potential matches in the TLBs.

The 602 offers an optional configuration (referred to as protection-only mode) of its TLBs under user control on reset. Applications that do not require address translation through the TLBs can use this configuration to protect up to 4-Mbytes of memory per TLB. The 602 BATs are available in this optional configuration for protection and translation of the effective address.

The 602 has a single bus interface used for transferring both 32-bit addresses and 64-bit or 32-bit data. This bus is time-multiplexed. First the address is driven on the bus, and then the data. During each address phase, the 602 samples the $\overline{\text{T32}}$ input pin to determine if the data phase will use a 32-bit bus or a 64-bit bus. The 602 interface protocol allows multiple masters to compete for system resources through a central external arbiter. The 602 provides a three-state coherency protocol that supports the modified, exclusive, and invalid (MEI) cache states. This protocol is a compatible subset of the MESI (modified/exclusive/shared/invalid) four-state protocol and operates coherently in systems that contain four-state caches. The 602 supports single-beat and burst data transfers for memory accesses and memory-mapped I/O.

The 602 uses an advanced, 3.3-V CMOS process technology and maintains full interface compatibility with TTL devices.

1.1.1 Features

This section describes details of the 602 implementation of the PowerPC architecture. Major features of the 602 are as follows:

- High-performance, superscalar microprocessor
  - As many as two instructions are fetched from the instruction queue per clock
  - One instruction can be issued and one retired per clock
  - As many as four instructions in execution per clock
  - Single-cycle execution for most instructions
- Four independent execution units and two register files
  - BPU performs architecturally-defined static branch prediction
  - A 32-bit IU
  - Fully IEEE 754-compliant FPU for single-precision operations
  - Emulation support for double-precision operations
  - An implementation of the non-IEEE floating-point mode
  - Thirty-two 32-bit general-purpose registers (GPRs) for integer operands
  - Thirty-two 32-bit floating-point registers (FPRs) for single-precision operands
  - LSU for data transfer between data cache and GPRs and FPRs
- Instruction pipelining and split cache organization
  - Zero-cycle branch capability (branch folding)
  - Programmable static branch prediction on unresolved conditional branches
  - BPU that performs CR lookahead operations
  - Instruction fetch unit capable of fetching two instructions per clock from the instruction cache (one of which is a branch instruction)
  - A four-entry instruction queue that provides lookahead capability
  - Independent pipelines with feed-forwarding that reduces data dependencies in hardware
  - 4-Kbyte data cache—two-way set-associative, physically addressed; LRU replacement algorithm
  - 4-Kbyte instruction cache—two-way set-associative, physically addressed; LRU replacement algorithm
  - Cache write-back or write-through operation programmable on a per page or per block basis
- Memory managament features
  - Address translation facilities for 4-Kbyte page size, variable block size, and 256-Mbyte segment size
  - A 32-entry, two-way set-associative ITLB
  - A 32-entry, two-way set-associative DTLB
  - Four-entry data and instruction BAT arrays providing 128-Kbyte to 256-Mbyte blocks
  - Software table search operations and updates supported through fast trap mechanism
  - 52-bit virtual address; 32-bit physical address
  - Optional configuration of the TLBs that offers protection for up to 4-Mbytes of memory per TLB, but no effective address translation

- Facilities for enhanced system performance
  - A 64-bit (address and data multiplexed) external data bus with burst transfers
  - Support for injected snoops by other devices during ownership of bus tenure
  - Ability to broadcast a line-fill address, during the address tenure of a writeback transaction on the bus
- Integrated power management
  - Low-power 3.3-volt design
  - Internal processor/bus clock multiplier that provides 2/1 and 3/1 ratios
  - Three static power-saving modes—doze, nap, and sleep
  - Automatic dynamic power reduction when internal functional units are idle
- Data bus externally selectable as either 32 or 64 bits
- In-system testability and debugging features through JTAG port
- Three power saving modes
  - Doze—All the functional units of the 602 are disabled except for the time base/decrementer registers and the bus snooping logic. When the processor is in doze mode, an external asynchronous interrupt, a system management interrupt, a decrementer exception, a hard or soft reset, or machine check brings the 602 into the full-power state. The 602 in doze mode maintains the PLL in a fully-powered state and locked to the system external clock input (SYSCLK) so a transition to the full-power state takes only a few processor clock cycles.
  - Nap—The nap mode further reduces power consumption by disabling bus snooping, leaving only the time base register and the PLL in a powered state. The 602 returns to the full-power state upon receipt of an external asynchronous interrupt, a system management interrupt, a decrementer exception, a hard or soft reset, or a machine check input ($\overline{\text{MCP}}$). A return to full-power state from a nap state takes only a few processor clock cycles.
  - Sleep—Sleep mode reduces power consumption to a minimum by disabling all internal functional units, after which external system logic may disable the PLL and SYSCLK. Returning the 602 to the full-power state requires the enabling of the PLL and SYSCLK, followed by the assertion of an external asynchronous interrupt, a system management interrupt, a hard or soft reset, or a machine check input ($\overline{\text{MCP}}$) signal after the time required to relock the PLL.

1.2 General Parameters

The following list provides a summary of the general parameters of the 602.

Technology	CMOS (four-level metal)
Die size	7.07 mm x 7.07 mm
Processor performance	66.67 MHz, 80 MHz
Package	Surface mount, 144-pin plastic quad flat pack (PQFP)
Power supplies	3.3 V (± 10% V dc)

1.3 Electrical and Thermal Characteristics

This section provides both the AC and DC electrical specifications and thermal characteristics for the 602. The following specifications are preliminary and subject to change without notice.

1.3.1 DC Electrical Characteristics

Table 1, Table 2, and Table 3 provide the absolute maximum rating and thermal characteristics for the 602.

Table 1. Absolute Maximum Ratings

Characteristic	Symbol	Value	Unit
Core Supply voltage	Vdd	–0.3 to 4.0	V
I/O Supply voltage	OVdd	–0.3 to 4.0	V
PLL Supply voltage	AVdd	–0.3 to 4.0	V
Input voltage	V_{in}	–0.3 to 5.5	V
Storage temperature range	T_{stg}	–55 to 150	°C

Notes:

1. Functional operating conditions are given in AC and DC electrical specifications. Stresses beyond the maximums listed may affect device reliability or cause permanent damage to the device.
2. **Caution**: Input voltage must not be greater than the supply voltage by more than 2.5 V at all times including during power-on reset.

Table 2. Recommended Operating Conditions

Characteristic	Symbol	Value	Unit
Core Supply voltage	Vdd	2.97 to 3.63	V
I/O Supply voltage	OVdd	2.97 to 3.63	V
PLL Supply voltage	AVdd	2.97 to 3.63	V
Input voltage	V_{in}	GND to 5.5	V

Table 2. Recommended Operating Conditions

Characteristic	Symbol	Value	Unit
Junction Temperature	T_J	0 to 105	°C

Notes:

1. These are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.
2. **Caution**: V_{in} must not exceed OVdd by more than 2.5 V at all times, including during power-on reset.
3. **Caution**: OVdd must not exceed Vdd by more than 2.5 V at all times, including during power-on reset.
4. **Caution**: Vdd/Avdd must not exceed OVdd by more than 0.4 V at all times, including during power-on reset.

Table 3. Thermal Characteristics

Characteristic	Symbol	Value	Rating
Motorola PQFP package thermal resistance, junction-to-case (typical)	θ_{JC}	2.8	°C/W
IBM PQFP package thermal resistance, junction-to-case (typical)	θ_{JC}	2.8	°C/W

Notes:

1. $T_J = T_A + P_D \times \theta_{JA}$ where $\theta_{JA} = \theta_{JC} + \theta_{CA}$
2. Refer to Section 1.7, “System Design Information,” for more information about thermal management.

Table 4 provides the DC electrical characteristics for the 602.

Table 4. DC Electrical Specifications

Vdd = 3.3 ± 10% V dc, GND = 0 V dc

Characteristic	Symbol	Min	Max	Unit
Input high voltage (all inputs except SYSCLK)	V_{IH}	2	5.5	V
Input low voltage (all inputs except SYSCLK)	V_{IL}	GND	0.8	V
SYSCLK input high voltage	CV_{IH}	2.4	5.5	V
SYSCLK input low voltage	CV_{IL}	GND	0.4	V
Input leakage current, V_{in} = 3.63 V[1,2]	I_{in}	—	10	µA
Output three-state leakage, V_{in} = 3.63 V[2]	I_{TSO}	—	10	µA
Bidirectional three-state leakage, V_{in} = 3.63 V[3]	I_{TSB}	—	500	µA
Output high voltage, I_{OH} = -9mA	V_{OH}	2.4	—	V
Output low voltage, I_{OL} = 9mA	V_{OL}	—	0.4	V

Table 4. DC Electrical Specifications (Continued)

Vdd = 3.3 ± 10% V dc, GND = 0 V dc

Characteristic	Symbol	Min	Max	Unit
Capacitance, V_{in} = 0 V, f = 1 MHz[4]	C_{in}	—	15	pF

Notes:

1. Excludes test signal pins $\overline{\text{LSSD\_MODE}}$, L1_TSTCLK, L2_TSTCLK, TDI, TMS, TCK, $\overline{\text{TRST}}$. These pins contain weak active pull up devices and may typically draw 600 µA current.
2. Inputs and outputs contain protective diodes which may typically draw 600 µA at 5.5 V when three-stated.
3. Bidirectional pins contain internal bus keeper circuits which may typically draw 700 µA current at 5.5 V when three-stated.
4. Capacitance is guaranteed by design.

Table 5 provides the power dissipation for the 602. These are typical values from a limited sample size.

Table 5. Power Dissipation

Vdd = 3.3 ± 10% V dc, GND = 0 V dc, $0 \le T_J \le 105$ °C

CPU Clock		66.67 MHz	80 MHz	Unit
Full-On Mode				
2:1	Typical	1.2	1.4	W
	Maximum	1.8	2.0	W
3:1	Typical	1.2	1.4	W
	Maximum	1.8	2.0	W
Doze Mode				
2:1	Typical	150	165	mW
3:1	Typical	150	165	mW
Nap Mode[1]				
2:1	Typical	75	100	mW
3:1	Typical	75	100	mW

Table 5. Power Dissipation (Continued)

Vdd = 3.3 ± 10% V dc, GND = 0 V dc, 0 ≤ T_J ≤ 105 °C

CPU Clock	66.67 MHz	80 MHz	Unit
Sleep Mode[1]			
2:1 Typical	8.0	12.0	mW
3:1 Typical	8.0	12.0	mW
Sleep Mode—PLL Disabled[1]			
2:1 Typical	2	2.2	mW
3:1 Typical	2	2.2	mW
Sleep Mode—PLL and SYSCLK Disabled[1]			
2:1 Typical	2	2	mW
3:1 Typical	2	2	mW

Notes:

1. The values provided for this mode do not include pad driver power (OVdd).
2. Power dissipation values assume C_L = 50pF.

1.3.2 AC Electrical Characteristics

This section provides the clock AC electrical characteristics for the 602.

1.3.2.1 Clock AC Specifications

Table 6 provides the clock AC timing specifications as defined in Figure 1.

Table 6. Clock AC Timing Specifications

Vdd = 3.3 ± 10% V dc, GND = 0 V dc, 0 ≤ T_J ≤ 105 °C

Num	Characteristic	66.67 MHz CPU Clock		80 MHz CPU Clock		Unit	Notes
		Min	Max	Min	Max		
	VCO frequency	120	300	180	360	MHz	2
	SYSCLK (bus) frequency	22	33.33	26.6	40	MHz	
1	SYSCLK cycle time	30	45	25	37.5	ns	
2,3	SYSCLK rise and fall time	—	2.0	—	2.0	ns	3
4	SYSCLK duty cycle measured at 1.4 V	40.0	60.0	40.0	60.0	%	5

Table 6. Clock AC Timing Specifications (Continued)

Vdd = 3.3 ± 10% V dc, GND = 0 V dc, 0 ≤ T_J ≤ 105 °C

Num	Characteristic	66.67 MHz CPU Clock		80 MHz CPU Clock		Unit	Notes
		Min	Max	Min	Max		
8	SYSCLK short-term jitter (cycle-to-cycle)	—	±150	—	±150	ps	4
9	602 internal PLL relock time	—	100	—	100	µs	5,6

Notes:

1. Times shown in specifications are only valid for a 66.67 MHz processor frequency.
2. PLL_CFG settings that cause the VCO or processor to operate outside of specified range are not guaranteed. Recommended PLL_CFG0–PLL_CFG3 settings for 2:1 mode are—66 MHz - 0101; 80 MHz - 0101. Recommended PLL_CFG0–PLL_CFG3 settings for 3:1 mode are—66 MHz - 1001; 80 MHz - 1001.
3. Rise and fall times for the SYSCLK input are measured from 0.4 V to 2.4 V.
4. This parameter shows the sum of short- and long-term jitter. Short- and long-term jitter are guaranteed by design.
5. Timing is guaranteed by design and characterization, and is not tested.
6. PLL-relock is the maximum time required for the PLL to lock after Vdd and SYSCLK become stable during power-on reset or wake-up from sleep mode. During the power-on-reset sequence, $\overline{\text{HRESET}}$ must be asserted for a minimum of 255 bus clocks after the PLL-relock time.

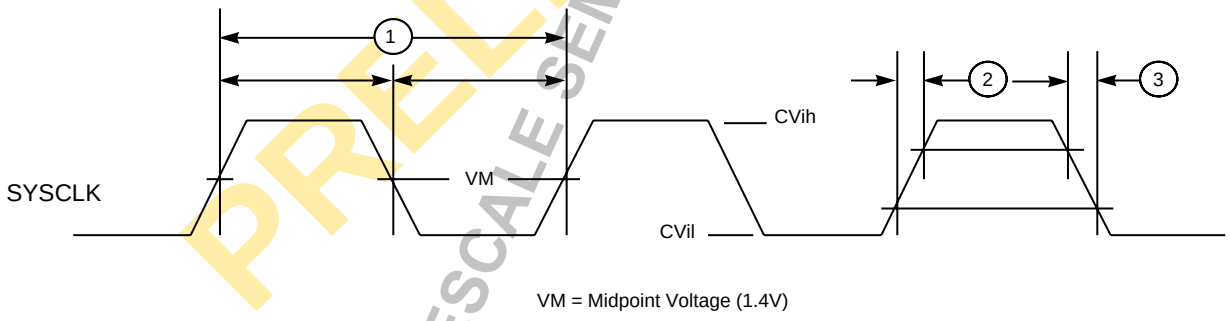


Figure 1. SYSCLK Input Timing Diagram

1.3.2.2 Input AC Specifications

Table 7 provides the input AC timing specifications for the 602.

Table 7. Input AC Timing Specifications

Vdd = 3.3 ± 10% V dc, GND = 0 V dc, 0 ≤ T_J ≤ 105 °C

Num	Characteristic	66.67 MHz CPU Clock		80 MHz CPU Clock		Unit	Notes
		Min	Max	Min	Max		
10a	Inputs valid to SYSCLK (input setup)	6	—	6	—	ns	1
10b	Mode select inputs valid to $\overline{\text{HRESET}}$ (input setup) (for $\overline{\text{QACK}}$)	8 * t_{sys}	—	8 * t_{sys}	—	ns	1,2,3,4,5
11a	Inputs invalid (input hold)	3.0	—	3.0	—	ns	1

Table 7. Input AC Timing Specifications (Continued)

Vdd = 3.3 ± 10% V dc, GND = 0 V dc, 0 ≤ T_J ≤ 105 °C

Num	Characteristic	66.67 MHz CPU Clock		80 MHz CPU Clock		Unit	Notes
		Min	Max	Min	Max		
11b	$\overline{\text{HRESET}}$ to mode select inputs invalid (input hold) (for $\overline{\text{QACK}}$)	0	—	0	—	ns	2,4,5

Notes:

1. All input specifications are measured from the TTL level (0.8 or 2.0 V) of the signal in question to the 1.4 V of the rising edge of the input SYSCLK. Both input and output timings are measured at the pin; see Figure 2.
2. The setup and hold time is with respect to the rising edge of $\overline{\text{HRESET}}$; see Figure 3.
3. t_{SYS} is the period of the external clock (SYSCLK) in nanoseconds.
4. These values are guaranteed by design, and are not tested.
5. This specification is for configuration-mode only. Also note that $\overline{\text{HRESET}}$ must be held asserted for a minimum of 255 bus clocks after the PLL-relock time (100 µs) during the power-on reset sequence.

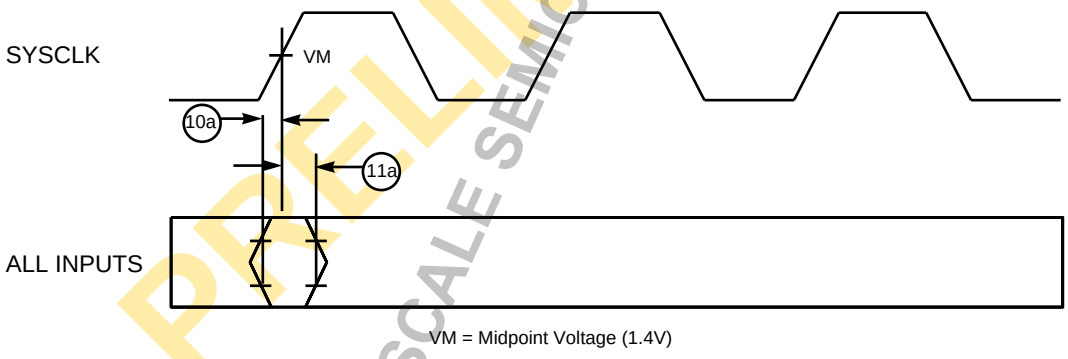


Figure 2. Input Timing Diagram

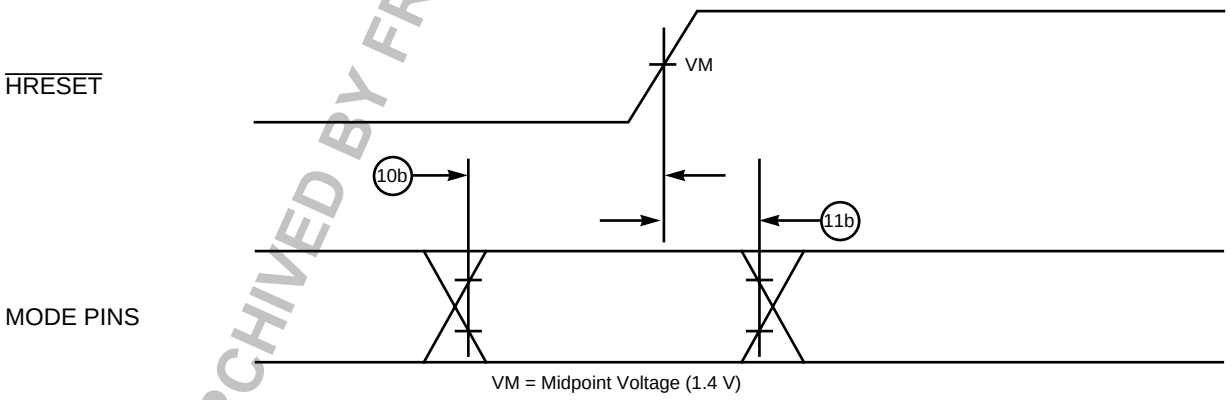


Figure 3. Mode Select Input Timing Diagram

1.3.2.3 Output AC Specifications

Table 8 provides the output AC timing specifications for the 602.

Table 8. Output AC Timing Specifications

Vdd = 3.3 ± 10% V dc, GND = 0 V dc, C_L = 50 pF, 0 ≤ T_J ≤ 105 °C

Num	Characteristic	33.33 MHz Bus Clock/ 66.67 MHz CPU Clock		40 MHz Bus Clock/ 80 MHz CPU Clock		Unit	Notes
		Min	Max	Min	Max		
12	SYSCLK to output driven (output enable time)(AD0–AD63, TS, BB, BR, ARTRY)	1.0	—	1.0	—	ns	1,3
13	SYSCLK to output valid (all outputs)	—	17	—	17	ns	1
14	SYSCLK to output invalid (output hold) (AD0–AD63), TS, BB, BR, ARTRY)	4	—	4	—	ns	1
15	SYSCLK to output high impedance (AD0–AD63, TS, BB, BR, ARTRY)	—	18	—	18	ns	1,2
16	SYSCLK to output driven (output enable time) (RESETO, QREQ, CKSTP_OUT, TDO)	1.0	—	1.0	—	ns	1,2,3
17	SYSCLK to output invalid (output hold) (RESETO, QREQ, CKSTP_OUT)	1.0	—	1.0	—	ns	1,2
18	SYSCLK to output high impedance (RESETO, QREQ, CKSTP_OUT)	—	18	—	18	ns	1,2

Notes:

1. All output specifications are measured from the 1.4 V of the rising edge of SYSCLK to 1.4 V. Both input and output timings are measured at the pin.
2. All maximum timing specifications assume C_L = 50 pF.
3. These values are guaranteed by design and are not tested.

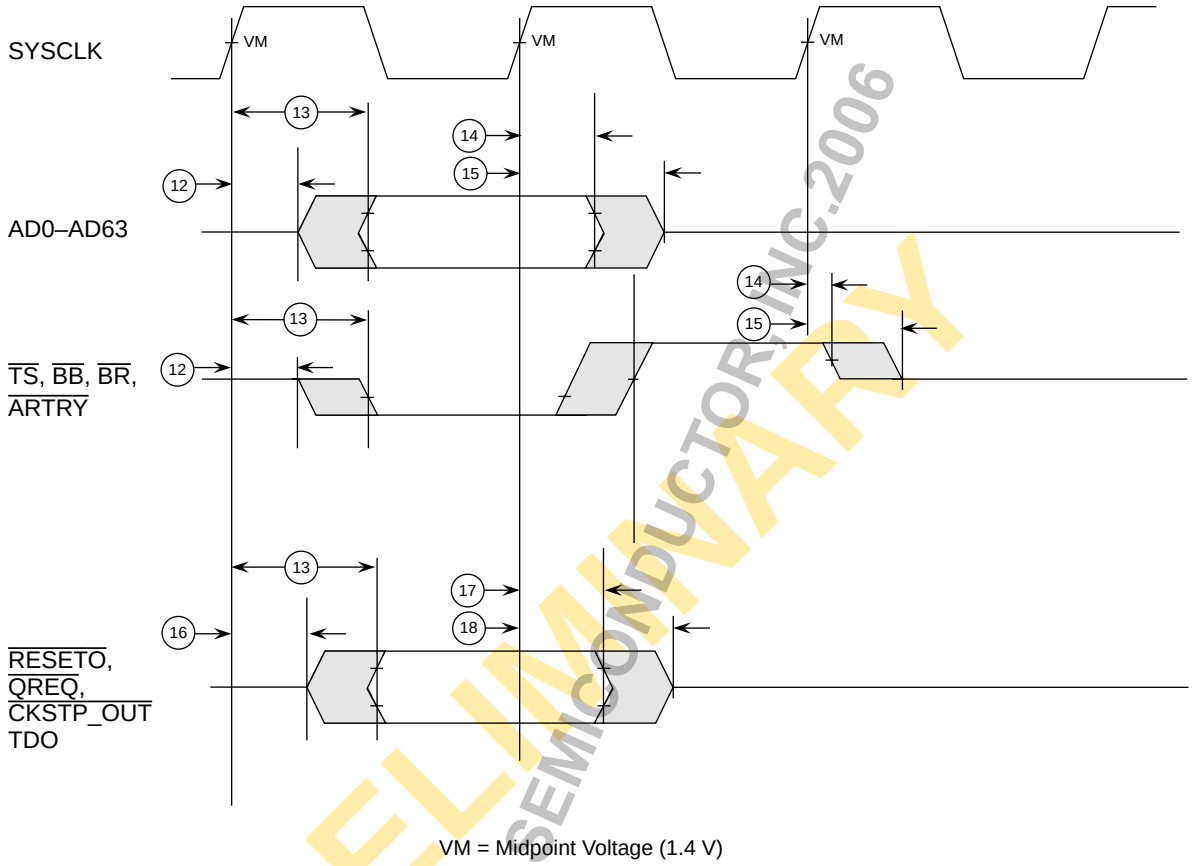


Figure 4. Output Timing Diagram

1.3.3 JTAG AC Timing Specifications

Table 9 provides the JTAG AC timing specifications.

Table 9. JTAG AC Timing Specifications (Independent of SYSCLK)

Vdd = 3.3 ± 10% V dc, GND = 0 V dc, C_L = 50 pF, 0 ≤ T_J ≤ 105 °C

Num	Characteristic	Min	Max	Unit	Notes
	TCK frequency of operation	0	16	MHz	
1	TCK cycle time	62.5	—	ns	
2	TCK clock pulse width measured at 1.4 V	25	—	ns	
3	TCK rise and fall times	0	3	ns	
4	$\overline{\text{TRST}}$ setup time to TCK rising edge	13	—	ns	1
5	$\overline{\text{TRST}}$ assert time	40	—	ns	
6	Boundary-scan input data setup time	6	—	ns	2
7	Boundary-scan input data hold time	27	—	ns	2
8	TCK to output data valid	4	25	ns	3

Table 9. JTAG AC Timing Specifications (Independent of SYSCLK) (Continued)

Vdd = 3.3 ± 10% V dc, GND = 0 V dc, C_L = 50 pF, 0 ≤ T_J ≤ 105 °C

Num	Characteristic	Min	Max	Unit	Notes
9	TCK to output high impedance	3	24	ns	3
10	TMS, TDI data setup time	0	—	ns	
11	TMS, TDI data hold time	25	—	ns	
12	TCK to TDO data valid	4	24	ns	
13	TCK to TDO high impedance	3	18	ns	

Notes:

1. $\overline{\text{TRST}}$ is an asynchronous signal. The setup time is for test purposes only.
2. Non-test signal input timing with respect to TCK.
3. Non-test signal output timing with respect to TCK.

Figure 5 provides the JTAG clock input timing diagram.

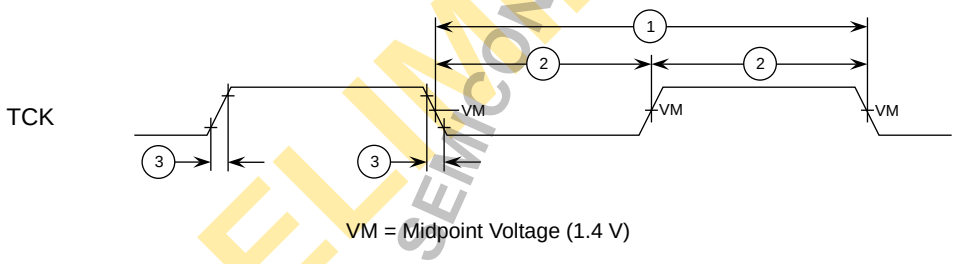


Figure 5. Clock Input Timing Diagram

Figure 6 provides the $\overline{\text{TRST}}$ timing diagram.

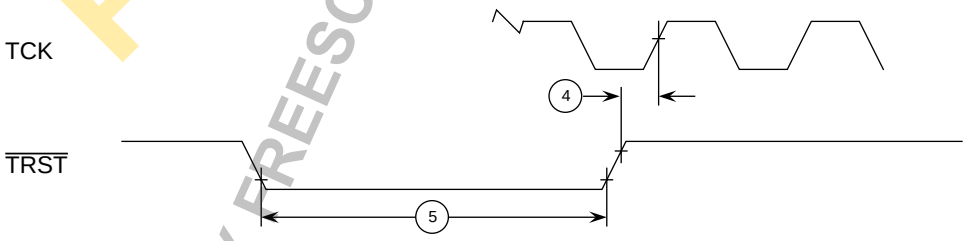


Figure 6. $\overline{\text{TRST}}$ Timing Diagram

Figure 7 provides the boundary-scan timing diagram.

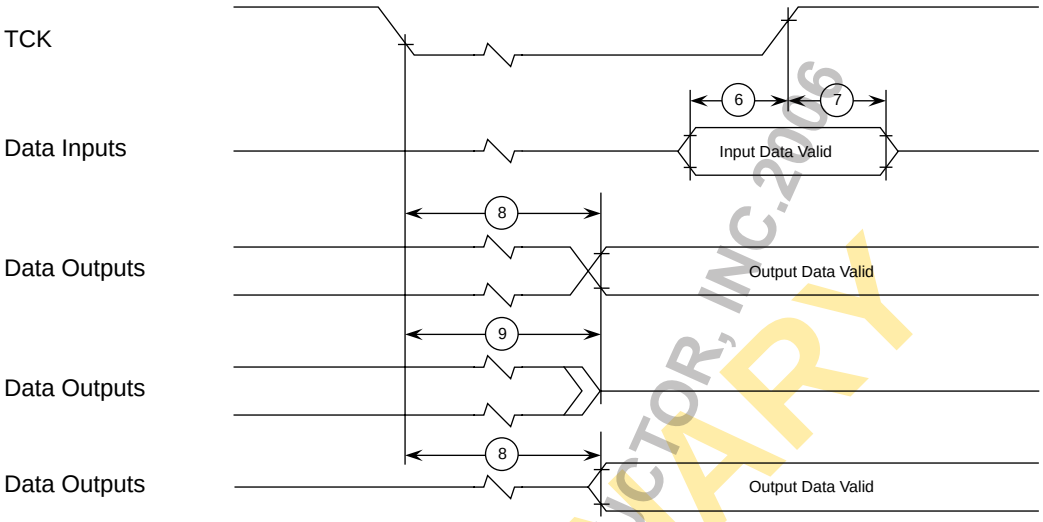


Figure 7. Boundary-Scan Timing Diagram

Figure 8 provides the test access port timing diagram.

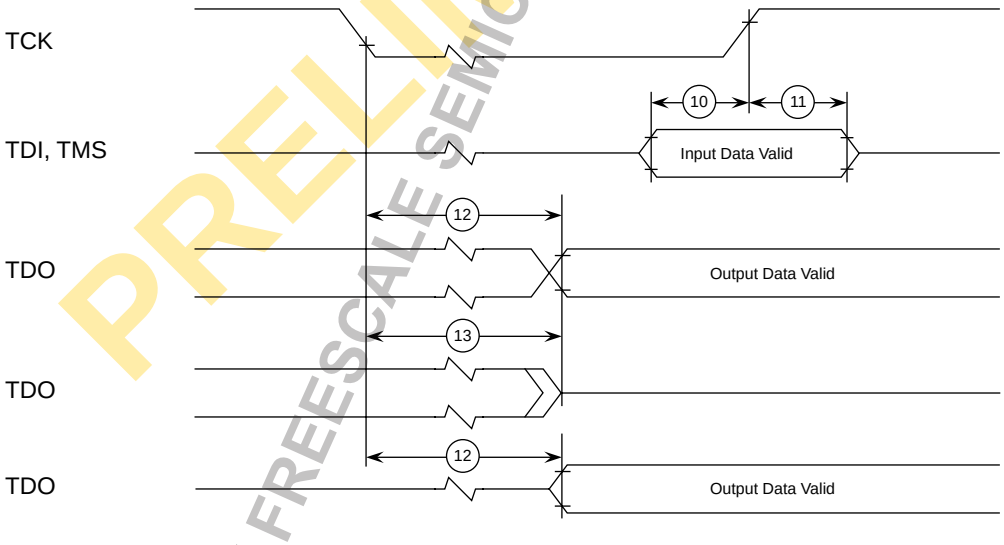
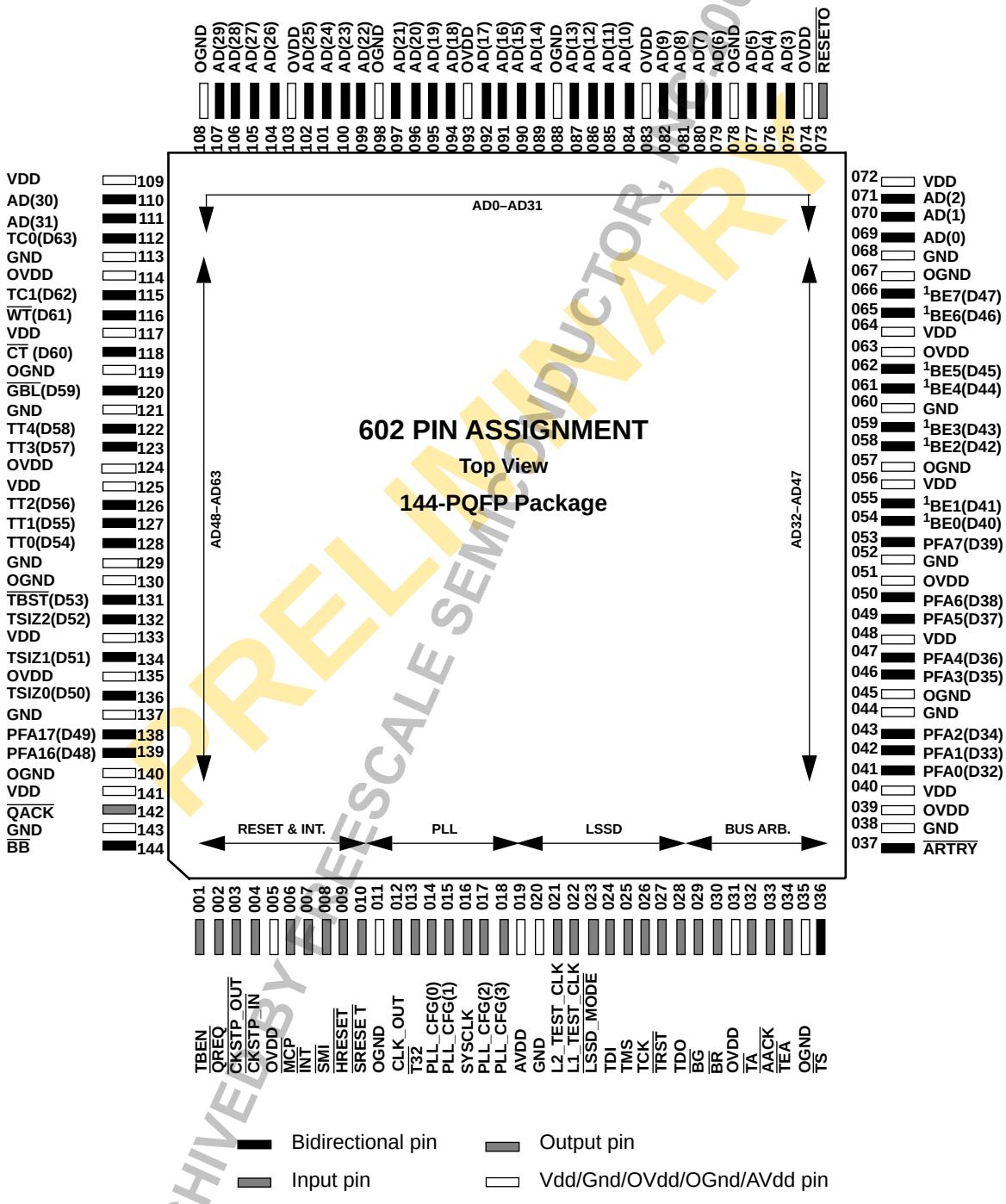


Figure 8. Test Access Port Timing Diagram

1.4 Pinout Diagram

Figure 9 contains the pin assignments for the 602.



Note: These signals also contain PFA8-PFA15.

Figure 9. PowerPC 602 Pin Assignment

1.5 Pinout Listing

Table 10 provides the pinout listing for the 602

Table 10. PowerPC 602 Microprocessor Pinout Listing

Signal Name	Pin Number	Active	I/O
AD0–AD31	69, 70, 71, 75, 76, 77, 79, 80, 81, 82, 84, 85, 86, 87, 89, 90, 91, 92, 94, 95, 96, 97, 99, 100, 101, 102, 104, 105, 106, 107, 110, 111	High	I/O
AACK	33	Low	Input
ARTRY	37	Low	I/O
AVDD	19	High	Input
BB	144	Low	I/O
BE0–BE7 (D40–D47) (PFA8–PFA15)	54, 55, 58, 59, 61, 62, 65, 66	High High High	Output I/O Output
BG	29	Low	Input
BR	30	Low	Output
CI (D60)	118	Low High	Output I/O
CLK_OUT	12	—	Output
CKSTP_IN	4	Low	Input
CKSTP_OUT	3	Low	Output
GBL (D59)	120	Low High	I/O I/O
GND	20, 38, 44, 52, 60, 68, 113, 121, 129, 137, 143	Low	Input
HRESET	9	Low	Input
INT	7	Low	Input
LSSD_MODE*	23	Low	Input
L1_TSTCLK*	22	—	Input
L2_TSTCLK*	21	—	Input
MCP	6	Low	Input
OGND	11, 35, 45, 57, 67, 78, 88, 98, 108, 119, 130, 140	Low	Input
OVDD	5, 31, 39, 51, 63, 74, 83, 93, 103, 114, 124, 135	High	Input
PFA0–PFA7 (D32–D39)	41, 42, 43, 46, 47, 49, 50, 53	High High	I/O I/O
PFA16–PFA17 (D48–D49)	138,139	High High	Output I/O

Table 10. PowerPC 602 Microprocessor Pinout Listing (Continued)

Signal Name	Pin Number	Active	I/O
PLL_CFG0–PLL_CFG3	14,15,17,18	High	Input
QACK	142	Low	Input
QREQ	2	Low	Output
RESETO	73	Low	Output
SMI	8	Low	Input
SRESET	10	Low	Input
SYSCLK	16	—	Input
T32	13	Low	Input
TA	32	Low	Input
TBEN	1	High	Input
TBST (D53)	131	Low High	I/O I/O
TC0–TC1 (D62, D63)	115,112	High High	Output I/O
TCK	26	—	Input
TDI	24	High	Input
TDO	28	High	Output
TEA	34	Low	Input
TMS	25	High	Input
TRST	27	Low	Input
TSIZ0–TSIZ2 (D50–D52) (PFA18–PFA20)	136,134,132	High High High	I/O I/O Output
TS	36	Low	I/O
TT0–TT4 (D54–D58)	128, 127, 126, 123, 122	High High	I/O I/O
VDD	40, 48, 56, 64, 72, 109, 117, 125, 133, 141	High	Input
WT (D61)	116	Low High	Output

Note: These are test signals for factory use only and must be pulled up to VDD for normal machine operation.

1.6 Package Description

The following sections provide the package parameters and the mechanical dimensions for the 602. Note that the 602 is currently offered in PQFP packages—the Motorola PQFP and the IBM PQFP.

1.6.1 Motorola Wire-Bond PQFP Package Description

The following sections provide the package parameters and mechanical dimensions for the Motorola wire-bond PQFP package.

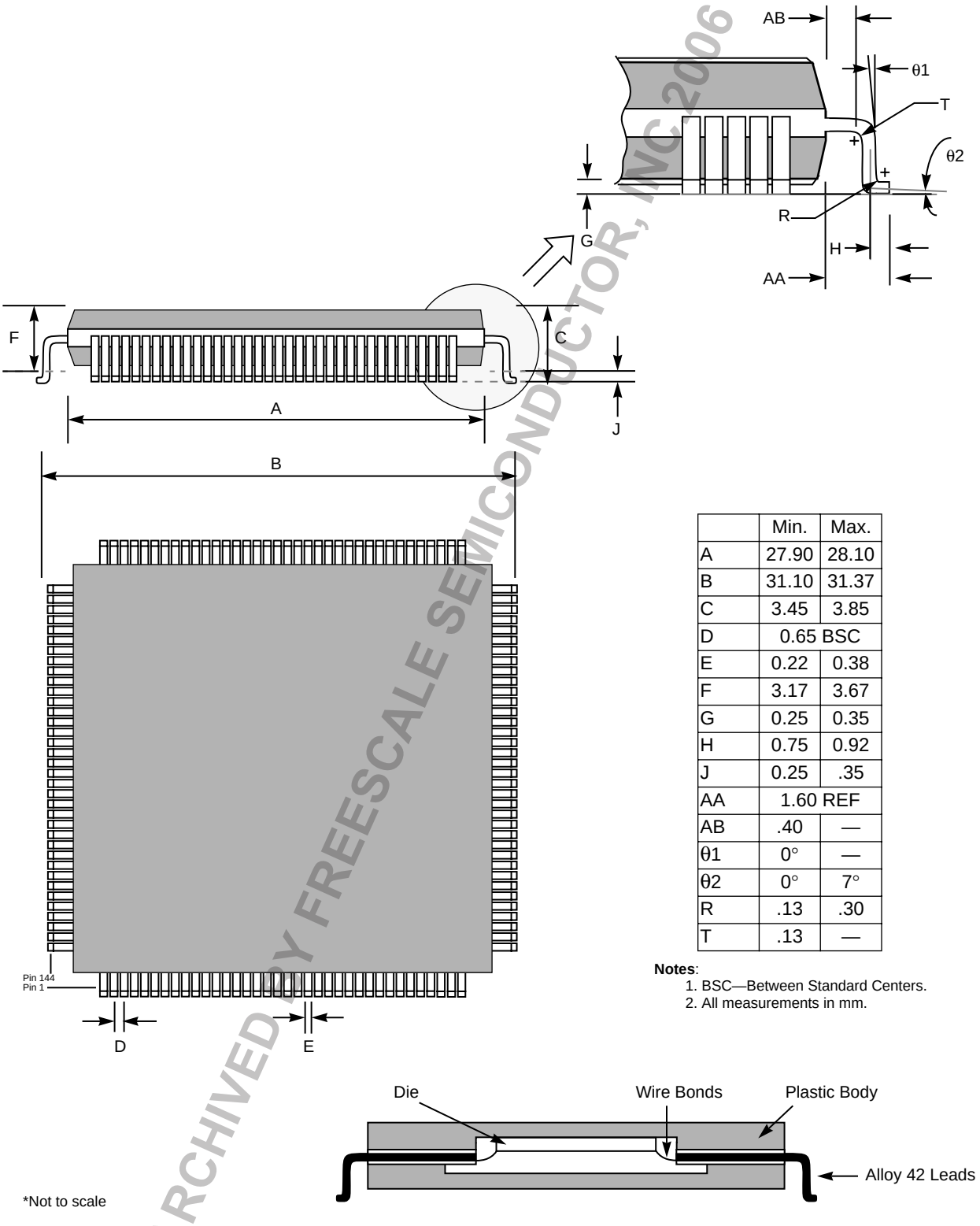
1.6.1.1 Package Parameters

The package parameters are as provided in the following list. The package type is mm x mm, 144-pin plastic quad flat pack.

Package outline	28 mm x 28 mm
Interconnects	144
Pitch	0.65 mm

1.6.1.2 Mechanical Dimensions of the Motorola Wire-Bond PQFP Package

Figure 10 shows the mechanical dimensions for the Motorola wire-bond PQFP package.



	Min.	Max.
A	27.90	28.10
B	31.10	31.37
C	3.45	3.85
D	0.65 BSC	
E	0.22	0.38
F	3.17	3.67
G	0.25	0.35
H	0.75	0.92
J	0.25	.35
AA	1.60 REF	
AB	.40	—
θ1	0°	—
θ2	0°	7°
R	.13	.30
T	.13	—

Notes:
1. BSC—Between Standard Centers.
2. All measurements in mm.

Figure 10. Mechanical Dimensions of the Motorola Wire-Bond PQFP Package

1.6.2 IBM PQFP Package Description

The following sections provide the package parameters and mechanical dimensions for the IBM PQFP package.

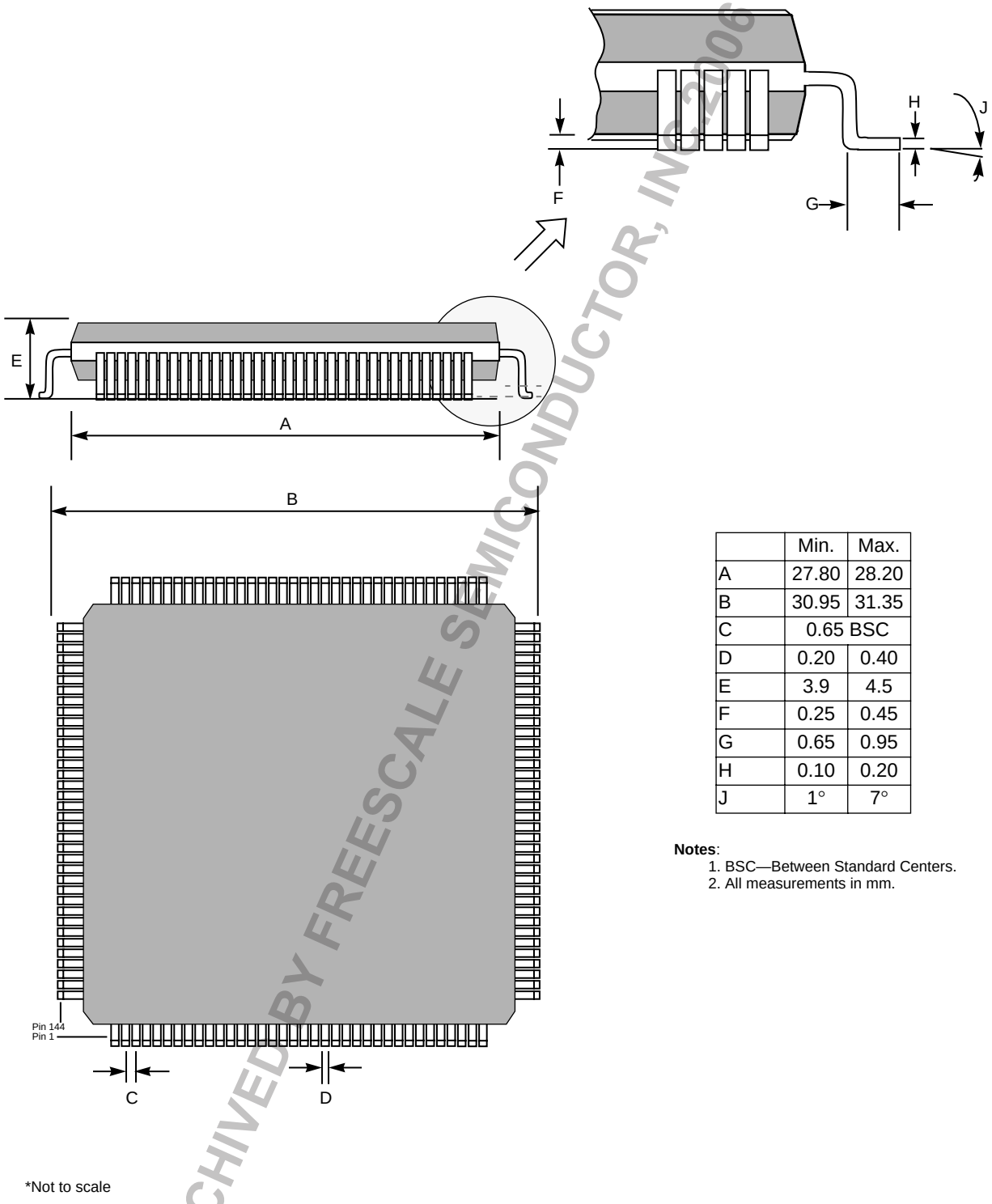
1.6.2.1 Package Parameters

The package parameters are as provided in the following list. The package type is mm x mm, 144-pin plastic quad flat pack.

Package outline	28 mm x 28 mm
Interconnects	144
Pitch	0.65 mm
Lead plating	Ni Au

1.6.2.2 Mechanical Dimensions of the IBM PQFP Package

Figure 11 shows the mechanical dimensions for the IBM wire-bond PQFP package.



	Min.	Max.
A	27.80	28.20
B	30.95	31.35
C	0.65 BSC	
D	0.20	0.40
E	3.9	4.5
F	0.25	0.45
G	0.65	0.95
H	0.10	0.20
J	1°	7°

Notes:
1. BSC—Between Standard Centers.
2. All measurements in mm.

Figure 11. Mechanical Dimensions of the IBM Wire-Bond PQFP Package

1.7 System Design Information

This section provides electrical and thermal design recommendations for successful application of the 602.

1.7.1 PLL Configuration

The 602 has an internal programmable phased-lock loop (PLL). The PLL is programmed using the PLL_CFG0–PLL_CFG3 pins. The PLL contains a voltage controlled oscillator (VCO) which is locked to the incoming SYSCLK. The VCO is divided down to the CPU frequency (internal) and to the bus frequency (SYSCLK). The PLL_CFG0–PLL_CFG3 pins are used to determine these frequency divisions. The 602 has two bus modes (CPU/bus ratio), 2:1 and 3:1. The 602 also has two VCO divider ratios (VCO/CPU), ÷2 and ÷4.

In a system application, the bus frequency and bus mode is selected based on system requirements (for example, 33 MHz, 2:1) and then the VCO divider is selected such that the VCO frequency is within the typical lock range identified in Table 6 (for example, 66 MHz CPU, ÷4 such that VCO = 264 MHz).

The first two PLL_CFG pins, PLL_CFG0 and PLL_CFG1, determine the bus mode while the second two pins, PLL_CFG2 and PLL_CFG3, determine the VCO divider ratio as shown in Table 11.

Table 11. PLL Configuration

PLL_CFG0–PLL_CFG3 Setting	Bus Mode	VCO Divider
0100	2:1	÷2
0101	2:1	÷4
1000	3:1	÷2
1001	3:1	÷4

Note: It is important that the VCO frequency be selected such that it falls within the typical VCO lock range identified in Table 6.

1.7.2 PLL Power Supply Filtering

The AVdd power signal is provided on the 602 to supply power to the clock generation phased-lock loop. To ensure stability of the internal clock, the power supplied to the AVdd input signal should be filtered using a circuit similar to the one shown in Figure 12. The circuit should be placed as close as possible to the AVdd pin to ensure it filters out as much noise as possible.

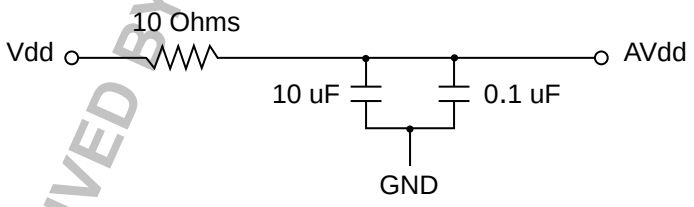


Figure 12. PLL Power Supply Filter Circuit

1.7.3 Decoupling Recommendations

Due to the 602's dynamic power management feature, large address and data buses, and high operating frequencies, the 602 can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the 602 system, and the 602 itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place a decoupling capacitor with a low ESR (effective series resistance) rating at every other Vdd and OVdd pin of the 602.

These capacitors should range in value from 220 pF to 10 µF to provide both high and low frequency filtering, and should be placed as close as possible to their associated Vdd pin. Surface-mount tantulum or ceramic devices are preferred. It is also recommended that these decoupling capacitors receive their power from Vdd and GND power planes in the PCB, utilizing short traces to minimize inductance. Power or ground connections must be made to all external Vdd and GND pins of the 602.

1.7.4 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unused active-low inputs should be connected to Vdd. Unused active-high inputs should be connected to GND.

1.7.5 Thermal Management Information for the Motorola Package

This section provides a thermal management example for the 602; this example is based on a typical desktop configuration using a 144 lead, 28 mm x 28 mm, Motorola wire-bond PQFP package.

1.7.5.1 Thermal Characteristics for the Motorola Wire-Bond PQFP Package

The thermal characteristics for a wire-bond PQFP package are as follows:

Thermal resistance (junction-to-case) = $R_{\theta jc}$ or θ_{jc} = 2.8°C/Watt (junction-to-case)

1.7.5.2 Thermal Management Example

The junction temperature can be calculated from the junction-to-ambient thermal resistance, as follows:

Junction temperature: $T_j = T_a + R_{\theta ja} * P$

or

$$T_j = T_a + (R_{\theta jc} + R_{cs} + R_{sa}) * P$$

Where:

T_a is the ambient temperature in the vicinity of the device
$R_{\theta ja}$ is the junction-to-ambient thermal resistance
$R_{\theta jc}$ is the junction-to-case thermal resistance of the device
R_{cs} is the case-to-heat sink thermal resistance of the interface material
R_{sa} is the heat sink-to-ambient thermal resistance
P is the power dissipated by the device

In this environment, it can be assumed that all the heat is dissipated to the ambient through the heat sink, so the junction-to-ambient thermal resistance is the sum of the resistances from the junction to the case, from the case to the heat sink, and from the heat sink to the ambient.

Note that verification of external thermal resistance and case temperature should be performed for each application. Thermal resistance can vary considerably due to many factors including degree of air turbulence.

For a power dissipation of 2.5 Watts in an ambient temperature of 40 °C at 1 m/sec with the heat sink

measured above, the junction temperature of the device would be as follows:

$T_j = T_a + R_{\theta ja} * P$
$T_j = 40\ °C + (10\ °C/Watt * 2.5\ Watts) = 65\ °C$

which is well within the reliability limits of the device.

Notes:

1. Junction-to-ambient thermal resistance is based on measurements on single-sided printed circuit boards per SEMI (Semiconductor Equipment and Materials International) G38-87 in natural convection.

2. Junction-to-case thermal resistance is based on measurements using a cold plate per SEMI G30-88 with the exception that the cold plate temperature is used for the case temperature.

The vendors who supply heat sinks are Aavid Engineering, IERC, Thermalloy, and Wakefield Engineering. Any of these vendors can supply heat sinks with sufficient thermal performance.

1.7.6 Thermal Management Information for the IBM Package

This section provides a thermal management example for the 602; this example is based on a typical desktop configuration using a 144-lead, mm x mm, IBM PQFP package.

1.7.6.1 Thermal Characteristics for the IBM PQFP Package

The thermal characteristics for a PQFP package are as follows:

Thermal resistance (junction to heat sink) = $R_{\theta js}$ or θ_{js} = 2.8°C/Watt (junction to heat sink)

1.7.6.2 Thermal Management Example

The following example is based on a typical desktop configuration using an IBM PQFP package. The heat sink used for this data is a pinfin heat sink #2338 attached to the PQFP package with 2-stage epoxy.

The junction temperature can be calculated from the junction-to-ambient thermal resistance, as follows:

Junction temperature = $T_j = T_a + R_{\theta ja} * P$

or

$$T_j = T_a + (R_{\theta js} + R_{sa}) * P$$

Where:

T_a is the ambient temperature in the vicinity of the device
$R_{\theta ja}$ is the junction-to-ambient thermal resistance
$R_{\theta js}$ is the junction-to-heat sink thermal resistance
R_{sa} is the heat sink-to-ambient thermal resistance
P is the power dissipated by the device

Note: $R_{\theta js}$ includes the resistance of a typical layer of thermal compound. If a lower conductivity material is used, its thermal resistance must be included.

In this environment, it can be assumed that all the heat is dissipated to the ambient through the heat sink, so the junction-to-ambient thermal resistance is the sum of the resistances from the junction to the heat sink and from the heat sink to the ambient.

Note that verification of external thermal resistance and case temperature should be performed for each application. Thermal resistance can vary considerably due to many factors including degree of air turbulence.

1.8 Ordering Information

This section provides the ordering information for the 602. Note that the individual part numbers correspond to a specific combination of 602 internal/bus frequencies, which must be observed to ensure proper operation of the device. For other frequency combinations, temperature ranges, power-supply tolerances package types, etc., contact your local Motorola or IBM sales office.

1.8.1 Motorola Part Number Key

Figure 13 provides a detailed description of the Motorola part number for the 602.

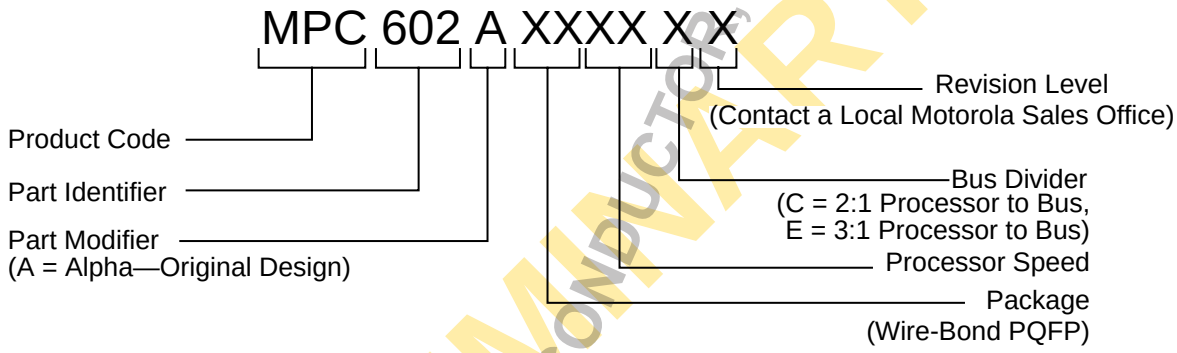


Figure 13. Motorola Part Number Key

1.8.2 IBM Part Number Key

Figure 14 provides a detailed description of the IBM part number for the 602.

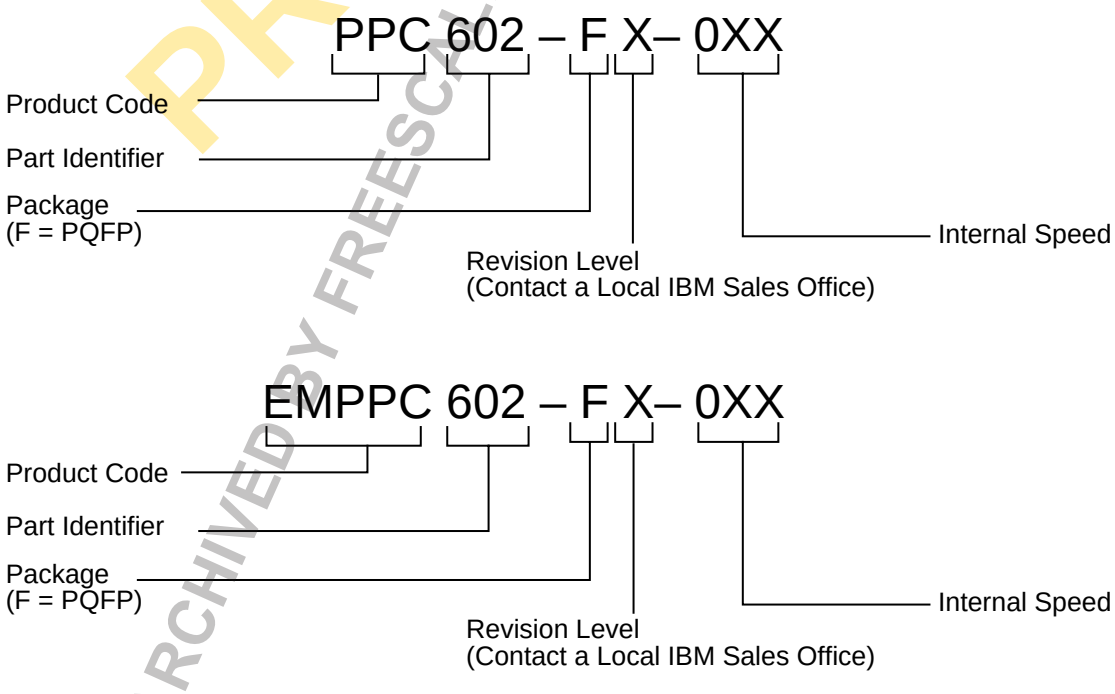


Figure 14. IBM Part Number Key

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