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MPC860

Product Brief

MPC860 Microprocessor

INTRODUCTION

The MPC860 PowerQUICC™ is a versatile one-chip integrated microprocessor and peripheral combination that can be used in a variety of controller applications, excelling particularly in communications and networking products. The PowerQUICC can be described as a next-generation MC68360 QUICC™ for network and data communication applications, providing higher performance in all areas of device operation including flexibility, extensions in capability, and integration. The MPC860 PowerQUICC, like the MC68360 QUICC integrates two processing blocks. One block is the Embedded PowerPC Core and the second block is a Communication Processor Module (CPM) that closely resembles the MC68360 CPM. The CPM supports four serial communications controllers (SCCs) on the device; however, there are actually eight serial channels: four SCCs, two serial management controllers (SMCs), one serial peripheral interface (SPI) and one I^2C interface. This dual-processor architecture provides lower power consumption than traditional architectures because the CPM off-loads peripheral tasks from the Embedded PowerPC Core.

MPC860 POWERQUICC KEY FEATURES

The following list summarizes the key MPC860 PowerQUICC features:

- Embedded PowerPC Core with 52 MIPS at 40 MHz (using Dhrystone 2.1)
- Single Issue, 32-Bit Version of the Embedded PowerPC Core (Fully Compatible with Book 1 of the PowerPC Architecture Definition) with 32 x 32 - Bit Fixed Point Registers
  - Embedded PowerPC Core Performs Branch Folding, Branch Prediction with Conditional Pre-Fetch, without Conditional Execution
  - 4 Kbyte Data Cache and 4 Kbyte Instruction Cache
  - Instruction and Data Caches are Two Way, Set-Associative, Physical Address, 4 Word Line Burst, Least Recently Used (LRU) Replacement, Lockable On-Line Granularity
  - MMUs with 32 Entry TLB, Fully Associative Instruction and Data TLBs
  - MMUs Support Multiple Page Sizes of 4 kB, 16 kB, 512 kB and 8 MB; 16 Virtual Address Spaces and 16 Protection Groups
  - Advanced On-Chip-Emulation Debug Mode
- Up to 32-Bit Data Bus (Dynamic Bus Sizing for 8,16, and 32 Bits)
- 32 Address Lines
- Complete Static Design (0–40 MHz Operation)

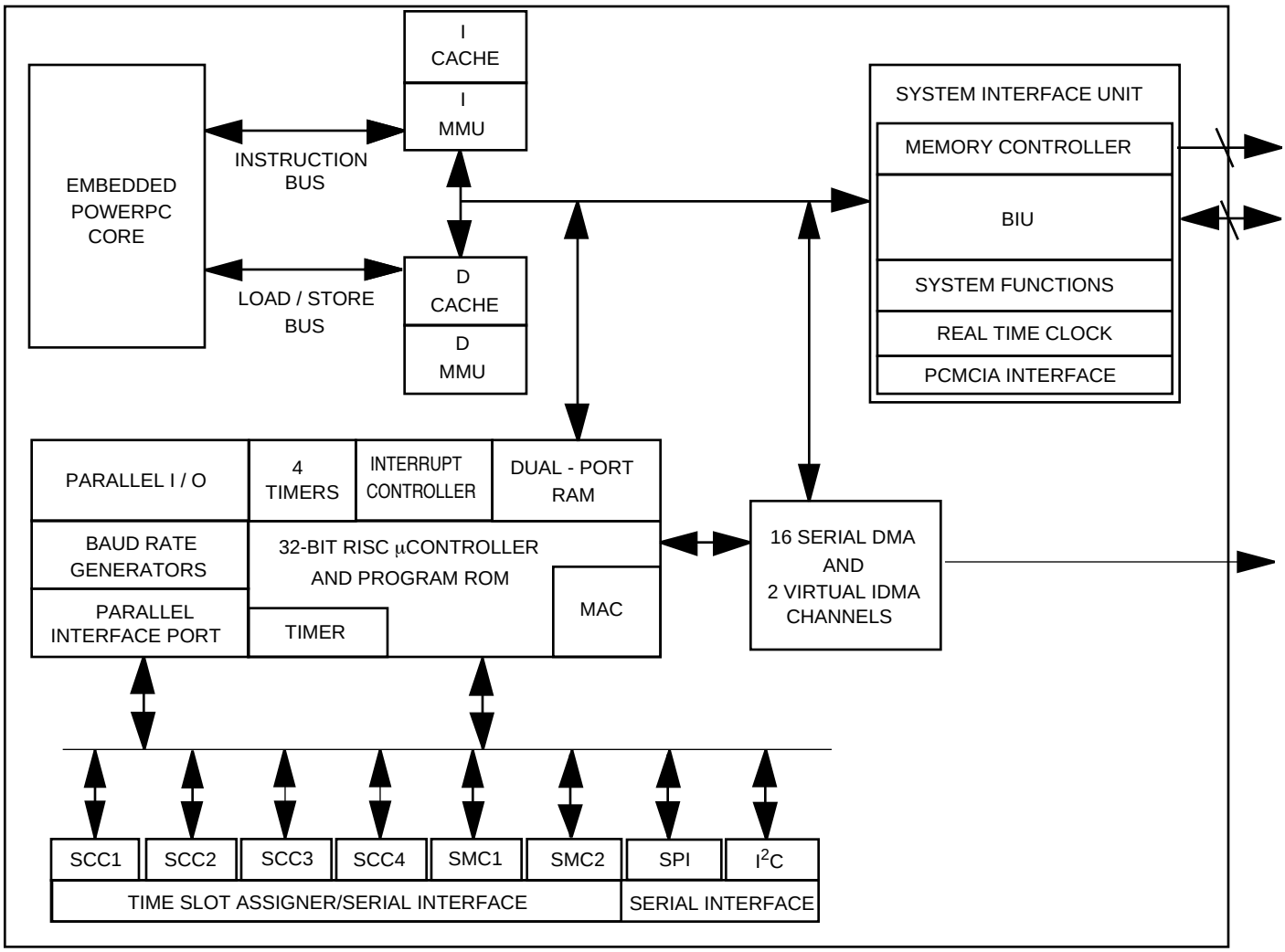

Figure 1. MPC860 PowerQUICC Block Diagram

- Memory Controller (Eight Banks)
  - Contains Complete Dynamic Random-Access Memory (DRAM) Controller
  - Each Bank Can Be a Chip Select or $\overline{RAS}$ to Support a DRAM Bank
  - Up to 15 Wait States Programmable per Memory Bank
  - Glueless Interface to DRAM Single In-Line Memory Modules (SIMMs), Static Random-Access Memory (SRAM), Electrically Programmable Read-Only Memory (EPROM), Flash EPROM, etc.
  - DRAM Controller Programmable to Support most Size and Speed Memory Interfaces
  - Four $\overline{CAS}$ lines, Four $\overline{WE}$ lines, One $\overline{OE}$ line
  - Boot Chip Select Available at Reset (Options for 8-, 16-, or 32-Bit Memory)
  - Variable Block Sizes, 32 kB to 256MB
  - Selectable Write Protection
  - On-Chip Bus Arbitration Logic
- General-Purpose Timers
  - Four 16-Bit Timers or Two 32-Bit Timers
  - Gate Mode Can Enable/Disable Counting

— Interrupt can be Masked on Reference Match and Event Capture

- System Integration Unit (SIU)
  - — Bus Monitor
  - — Software Watchdog
  - — Periodic Interrupt Timer
  - — Low Power Stop Mode
  - — Clock Synthesizer
  - — PowerPC Decrementer
  - — PowerPC Time Base and RTC
  - — Reset Controller
  - — IEEE 1149.1 Test Access Port (JTAG)
- Interrupts
  - — Seven External Interrupt Request (IRQ) Lines
  - — 12 Port Pins with Interrupt Capability
  - — 23 Internal Interrupt Sources
  - — Programmable Priority Between SCCs
  - — Programmable Highest Priority Request
- Communications Processor Module (CPM)
  - — RISC Controller
  - — Communication Specific Commands (e.g., Graceful Stop Transmit, Close Receive Buffer Descriptor, RxBD)
  - — Up to 384 Buffer Descriptors
  - — Supports Continuous Mode Transmission and Reception on All Serial Channels
  - — Up to 5 kbytes of Dual-Port RAM
  - — 16 Serial DMA (SDMA) Channels
  - — Three Parallel I/O Registers with Open-Drain Capability
- On Chip 16x16 Multiply Accumulate Controller (MAC)
  - — One Operation per Clock (Two Clock Latency, One Clock Blockage)
  - — MAC Operates Concurrently with Other Instructions
  - — FIR Loop: Four Clocks per Four Multiplies
- Four Baud Rate Generators
  - — Independent (Can Be Connected to Any SCC or SMC)
  - — Allow Changes During Operation
  - — Autobaud Support Option
- Four SCCs (Serial Communication Controllers)
  - — Ethernet/IEEE 802.3 Optional on SCC1-4, Supporting Full 10-Mbps Operation *(Available only on Specially Programmed Devices)*
  - — HDLC/SDLC[1] (All Channels Supported at 2 Mbps)
  - — HDLC Bus (Implements an HDLC-Based Local Area Network (LAN))
  - — Asynchronous HDLC to Support PPP (Point-to-Point Protocol)
  - — AppleTalk[2]
  - — Universal Asynchronous Receiver Transmitter (UART)
  - — Synchronous UART
  - — Serial Infrared (IrDA)
  - — Binary Synchronous Communication (BISYNC)

1. SDLC is a trademark of International Business Machines.

2. AppleTalk is a registered trademark of Apple Computer, Inc.

  - Totally Transparent (Bit Streams)
  - Totally Transparent (Frame Based with Optional Cyclic Redundancy Check (CRC))
- Two SMCs (Serial Management Channels)
  - UART
  - Transparent
  - General Circuit Interface (GCI) Controller
  - Can Be Connected to the Time-Division Multiplexed (TDM) Channels
- One SPI (Serial Peripheral Interface)
  - Supports Master and Slave Modes
  - Supports Multimaster Operation on the Same Bus
- One I^2C (Inter-Integrated Circuit) Port
  - Supports Master and Slave Modes
  - Multi-Master Environment Support
- Time-Slot Assigner
  - Allows SCCs and SMCs to run in Multiplexed and/or Non-Multiplexed Operation
  - Supports T1, CEPT, PCM Highway, ISDN Basic Rate, ISDN Primary Rate, User Defined
  - 1- or 8-Bit Resolution
  - Allows Independent Transmit and Receive Routing, Frame Syncs, Clocking
  - Allows Dynamic Changes
  - Can Be internally Connected to Six Serial Channels (Four SCCs and Two SMCs)
- Parallel Interface Port
  - Centronics[3] Interface Support
  - Supports Fast Connection Between Compatible Ports on MPC860 or MC68360
- PCMCIA Interface
  - Master (Socket) Interface, Release 2.1 Compliant
  - Supports Two Independent PCMCIA Sockets
  - 8 Memory or I/O Windows supported
- Low Power Support
  - Full On–All Units Fully Powered
  - Doze–Core Functional Units Disabled Except Time Base Decrementer, PLL, Memory Controller, RTC, and CPM in Low Power Standby
  - Sleep–All Units Disabled Except RTC and PIT, PLL Active for Fast Wake-Up
  - Deep Sleep–All Units Disabled Including PLL Except RTC and PIT
  - Power Down Mode– All units powered down except PLL, RTC, PIT, Time Base and Decrementer
- Debug Interface
  - Eight Comparators: Four Operate on Instruction Address, Two Operate on Data Address, and Two Operate on Data
  - Supports Conditions: = ≠ < >
  - Each Watchpoint can Generate a Breakpoint Internally
- 3.3 V Operation with 5V TTL Compatibility
- 357-Pin Ball Grid Array (BGA) Package

3. Centronics is a trademark of Centronics, Inc.

ARCHITECTURE OVERVIEW

The MPC860 PowerQUICC integrates the Embedded PowerPC Core with high performance, low power peripherals to extend the Freescale Data Communications family of embedded processors even farther into high end communications and networking products.

The MPC860 PowerQUICC is comprised of three modules which all use the 32-bit internal bus: the Embedded PowerPC Core, the System Integration Unit (SIU), and the Communication Processor Module (CPM). The MPC860 PowerQUICC block diagram is shown in Figure 1.

EMBEDDED POWERPC CORE

The Embedded PowerPC Core is compliant with the Book 1 specification for the PowerPC architecture. The Embedded PowerPC Core is a fully static design that consists of two functional blocks; the integer block and the load/store block. It executes all integer and load/store operations directly on the hardware. The core supports integer operations on a 32-bit internal data path and 32-bit arithmetic hardware. The core interface to the internal and external buses is 32 bits. The core uses a two instruction load/store queue, a four instruction prefetch queue, and a six instruction history buffer. The core does branch folding and branch prediction with conditional pre-fetch but without conditional execution. The Embedded PowerPC Core can operate on 32-bit external operands with one bus cycle.

The PowerPC integer block supports 32 x 32-bit fixed point general purpose registers. It can execute one integer instruction each clock cycle.

The Embedded PowerPC Core is integrated with MMU's as well as 4 kbyte instruction and data caches. Each MMU provides a 32 entry, fully associative instruction and data TLB, with multiple page sizes of: 4 kB, 16 kB, 512 kB, and 8 MB. It will support 16 virtual address spaces with 16 protection groups. Three special registers are available as scratch registers to support software table walk and update.

The instruction cache is 4 kilobytes, two-way, set associative with physical addressing. It allows single cycle access on hit with no added latency for miss. It has four words per line, supporting burst line fill using Least Recently Used (LRU) replacement. The cache can be locked on a per line basis for application critical routines. The cache inhibit mode can be programmed per MMU page.

The data cache is 4 kilobytes, two-way, set associative with physical addressing. It allows single cycle access on hit with one added clock latency for miss. It has four words per line, supporting burst line fill using LRU replacement. The cache can be locked on a per line basis for application critical data. the data cache can be programmed to support copy-back or write-through via the MMU. The cache inhibit mode can be programmed per MMU page.

The Embedded PowerPC Core with its Instruction and data caches delivers approximately 52 MIPS at 40 MHz, using Dhrystone 2.1

The Embedded PowerPC Core contains a much improved debug interface that provides superior debug capabilities without causing any degradation in the speed of operation. This interface supports six watchpoint pins that are used to detect software events. Internally it has eight comparators, four of which operate on the effective address on the address bus. The remaining four comparators are split, with two comparators operating on the effective address on the data address bus, and two comparators operating on the data bus. The Embedded PowerPC Core can compare using =, ≠, <, > conditions to generate watchpoints. Each watchpoint can then generate a breakpoint that can be programmed to trigger in a programmable number of events.

SYSTEM INTERFACE UNIT (SIU)

The SIU on the MPC860 PowerQUICC integrates general-purpose features useful in almost any 32-bit processor system, enhancing the performance provided by the system integration module (SIM) on the MC68360 QUICC device.

Dynamic bus sizing is supported. Bus sizing allows 8-, 16-, and 32-bit peripherals and memory to exist in the 32-bit system bus mode.

The SIU also provides power management functions, Reset control, PowerPC decrementer, PowerPC time base and the real time clock.

The memory controller will support up to eight memory banks with glueless interfaces to DRAM, SRAM, SSRAM, EPROM, Flash EPROM, SRDRAM, EDO and other peripherals with two-clock access to external SRAM and bursting support. It provides variable block sizes from 32 kilobytes to 256 megabytes. The memory controller will provide 0 to 30 wait states for each bank of memory and can use address type matching to qualify each memory bank access. It provides four byte enable signals, one output enable signal and one boot chip select available at reset.

The DRAM interface supports port sizes of 8, 16, and 32 bits. Memory banks can be defined in depths of 256k, 512k, 1M, 2M, 4M, 8M, 16M, 32M, or 64M for all port sizes. In addition the memory depth can be defined as 64k and 128k for 8-bit memory or 128M and 256M for 32-bit memory. The DRAM controller supports page mode access for successive transfers within bursts. The MPC860 will support a glueless interface to one bank of DRAM while external buffers are required for additional memory banks. The refresh unit provides $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$, a programmable refresh timer, refresh active during external reset, disable refresh mode, and stacking up to 7 refresh cycles. The DRAM interface uses a programmable state machine to support almost any memory interface.

PCMCIA CONTROLLER

The PCMCIA interface is a master (socket) controller and is compliant with release 2.1. The interface will support up to two independent PCMCIA sockets requiring only external transceivers/buffers. The interface provides 8 memory or I/O windows where each window can be allocated to a particular socket. If only one PCMCIA port is being used, the unused PCMCIA port may be used as general-purpose input with interrupt capability.

POWER MANAGEMENT

The MPC860 PowerQUICC supports a wide range of power management features including Full On, Doze, Sleep, Deep Sleep, and Low Power Stop. In Full On mode the MPC860 processor is fully powered with all internal units operating at the full speed of the processor. A Gear mode is provided which is determined by a clock divider, allowing the OS to reduce the operational frequency of the processor. Doze mode disables core functional units other than the time base decrementer, PLL, memory controller, RTC, and then places the CPM in low power standby mode. Sleep mode disables everything except the RTC and PIT, leaving the PLL active for quick wake-up. The Deep Sleep mode disables the PLL for lower power but slower wake-up. Low Power Stop disables all logic in the processor except the minimum logic required to restart the device, providing the lowest power consumption but requiring the longest wake-up time.

COMMUNICATIONS PROCESSOR MODULE (CPM)

The MPC860 PowerQUICC is the next generation MC68360 QUICC and like its predecessor implements a dual processor architecture. This dual processor architecture provides both a high performance general purpose processor for application programming use as well as a special purpose communication processor (CPM) uniquely designed for communications needs.

The CPM contains features that allow the MPC860 PowerQUICC to excel in communications and networking products as did the MC68360 QUICC which preceded it. These features may be divided into three sub-groups:

- Communications Processor (CP)
- Sixteen Independent DMA (SDMA) Controllers
- Four General-Purpose Timers

The CP provides the communication features of the MPC860 PowerQUICC. Included are a RISC processor, four Serial Communication Controllers (SCC), four Serial Management Controllers (SMC), one Serial Peripheral Interface (SPI), one I^2C Interface, 5 kilobytes of dual-port RAM, an interrupt controller, a time slot assigner, three parallel ports, a parallel interface port, four independent baud rate generators, and sixteen serial DMA channels to support the SCCs, SMCs, SPI, and I^2C.

The SDMAs provide two channels of general-purpose DMA capability for each communications channel. They offer high-speed transfers, 32-bit data movement, buffer chaining, and independent request and acknowledge logic.

The four general-purpose timers on the CPM are identical to the timers found on the MC68360 and still support the internal cascading of two timers to form a 32-bit timer.

The MPC860 PowerQUICC maintains the best features of the MC68360 QUICC, while making changes required to provide for the increased flexibility, integration, and performance requested by customers demanding the performance of the PowerPC architecture. The addition of a Multiply-And-Accumulate (MAC) function on the CPM further enhances the MPC860 PowerQUICC, enabling various modem and DSP applications. Because the CPM architectural approach remains intact between the MPC860 PowerQUICC and the MC68360 QUICC, a user of the MC68360 QUICC can easily become familiar with the MPC860 PowerQUICC.

Software Compatibility Issues

The following list summarizes the major software differences between the MC68360 QUICC and the MPC860 PowerQUICC:

- Since the MPC860 PowerQUICC uses an Embedded PowerPC Core, code written for the MC68360 must be recompiled for the PowerPC instruction set. Code which accesses the MC68360 peripherals requires only minor modifications for use with the MPC860. Although the functions performed by the PowerQUICC SIU are similar to those performed by the QUICC SIM, the initialization sequence for the SIU is different and therefore code that accesses the SIU must be rewritten. Many developers of 68K compilers now provide compilers which also support the PowerPC architecture.
- The addition of the MAC function to the MPC860 CPM block to support the needs of higher performance communication software is the only major difference between the CPM on the MC68360 and that on the MPC860. Therefore the registers used to initialize the QUICC CPM are similar to the MPC860 CPM, but there are some minor changes necessary for supporting the MAC function.
- When porting code from the MC68360 CPM to the MPC860 CPM, the software writer will find new options for hardware breakpoint on CPU commands, address, and serial request which are useful for software debugging. Support for single step operation with all the registers of the CPM visible makes software development for the CPM on the MPC860 processor even simpler.

MPC860 POWERQUICC GLUELESS SYSTEM DESIGN

A fundamental design goal of the MPC860 PowerQUICC was ease of interface to other system components. Figure 2 shows a system configuration that offers one EPROM, one flash EPROM, and supports two DRAM SIMMs. Depending on the capacitance on the system bus, external buffers may be required. From a logic standpoint, however, a glueless system is maintained.

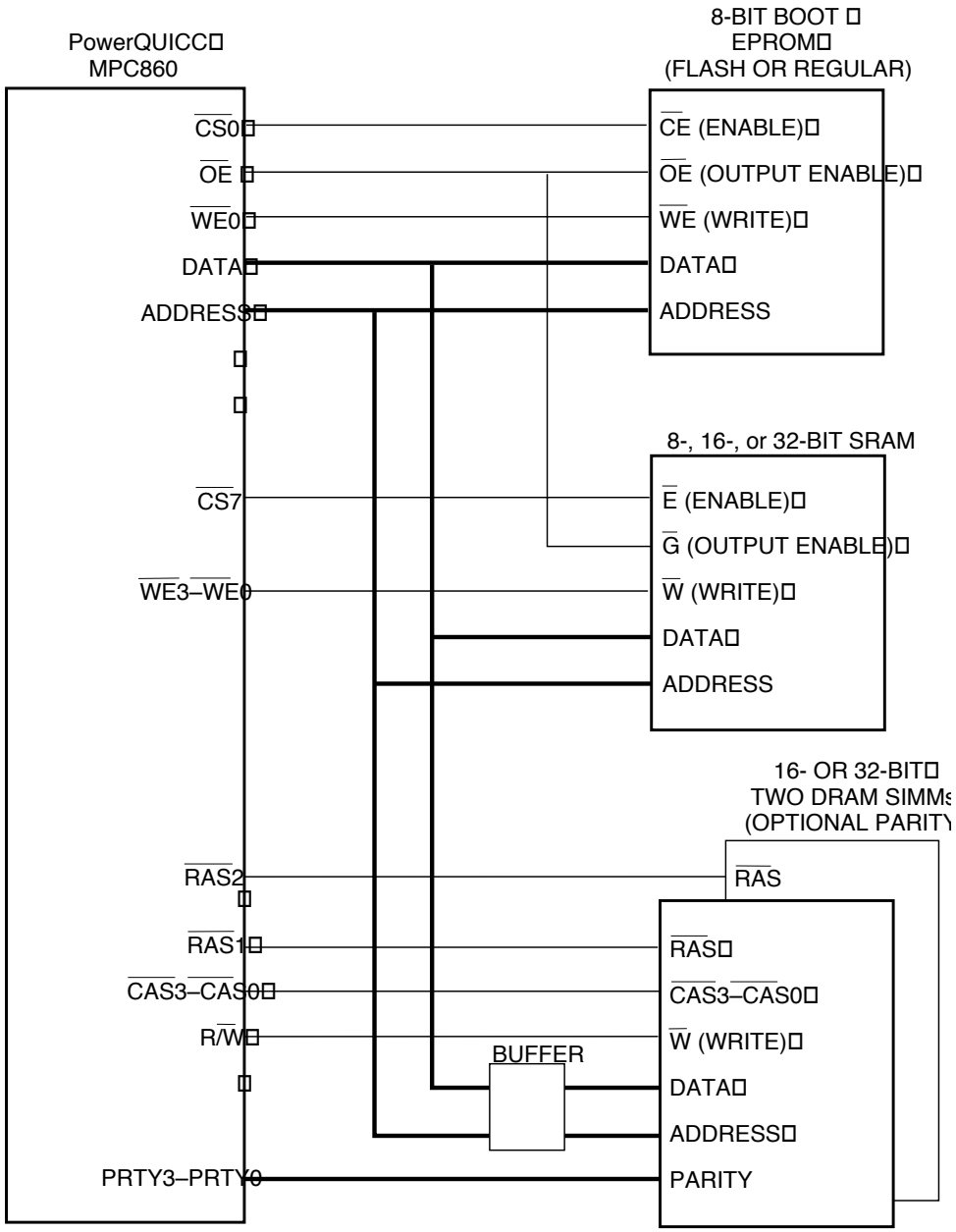

Figure 2. MPC860 System Configuration

ORDERING INFORMATION

The following table identifies the packages and operating frequencies available for the MPC860 Device.

Table 1. MPC860 Package/Frequency Availability

PACKAGE TYPE	FREQUENCY (MHZ)	TEMPERATURE	ORDER NUMBER
Ball Grid Array (ZP Suffix)	25	0°C to 70°C	XPC860ZP25
	25	0°C to 70°C	XPC860ENZP25
	25	0°C to 70°C	XPC860MHZP25
	25	0°C to 70°C	XPC860DCZP25
	25	0°C to 70°C	XPC860DEZP25
	40	0°C to 70°C	XPC860ZP40
	40	0°C to 70°C	XPC860ENZP40
	40	0°C to 70°C	XPC860MHZP40
	40	0°C to 70°C	XPC860DCZP40
	40	0°C to 70°C	XPC860DEZP40
Ball Grid Array (CZP Suffix)	TBD	-40°C to 85°C	TBD

Five different versions of the MPC860 PowerQUICC will be made available. The table below summarizes the different versions. Pricing and availability vary depending on the derivative.

Table 2. MPC860 Version Availability

DEVICE	ETHERNET SUPPORT	NUMBER OF SCCS	32-CHANNEL HDLC SUPPORT
MPC860	N/A	Four	N/A
MPC860EN	Yes	Four	N/A
MPC860DC	N/A	Two	N/A
MPC860DE	Yes	Two	N/A
MPC860MH	Yes	Four	Yes

The documents listed in the following table contain detailed information on the MPC860.

Table 3. MPC860 Documentation

DOCUMENT TITLE	ORDER NUMBER	CONTENTS
MPC860 User's Manual	MPC860UM/AD	Detailed information for design
PowerPC Programmer's Reference Guide	MPCPRG/D	POWERPC Instruction Set
High-Performance Embedded Systems PowerPC Source	POWERPCDIR/D	Independent vendor listing supporting software and development tools

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