MPCPCMEC/D
(Motorola Order Number)

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PowerPC™

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Advance Information

Processor and Cache Module Hardware Specifications

The Processor and Cache Module (PCM) is a 17 x 17 pin grid array (PGA) circuit assembly which combines a PowerPC® microprocessor and SRAM components into a CPU subsystem. The PCM provides a standard mechanical, electrical, and functional interface which can be socketed on a computer system board and allow many combinations of processors and optional components to be easily interchanged. This document describes the general characteristics for a module consisting of a single PowerPC microprocessor and two SRAM devices for L2 cache. The PCM packaging and PGA signal definition also accomodates single processors without SRAM, and multiple processors.

This document must be used in conjunction with a Motorola part number specification, located on the Motorola PowerPC website at http://www.mot.com/SPS/PowerPC/. The part number specifications describe the configuration and ordering information, and provide references to the appropriate processor and SRAM hardware specifications to describe the component parts on a particular PCM. The order of precedence is such that the microprocessor or SRAM component documents such as user's manuals and hardware specifications take precedence unless otherwise indicated by this document (for example, in packaging or pinout). The part number specifications take precedence over this document in the areas it addresses (for example, specifics of part numbers, configurations, and any requisite application relief on electrical parameters.)

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This document contains the following topics:

To locate any published errata or updates for this document, refer to the website at http://www.mot.com/SPS/PowerPC/.

1.1 Overview

The PCM is a circuit assembly which combines a PowerPC microprocessor and two SRAM components into a CPU subsystem. The PCM consists of an epoxy-glass (FR4) substrate which adapts a processor in a ceramic ball grid array (CBGA) package with 50 mil spacing to a 288-pin PGA with 100 mil spacing that can be easily socketed and hence, easily upgraded. The FR4 substrate can be extended beyond the area of the 17 x 17 pin grid array to provide an interconnect area for SRAM components configured as closely coupled L2 cache. The resulting PCM provides numerous flexible configurations of processor and cache for various price/performance system designs.

1.2 Features

This section summarizes features of the PCM. Major features of the PCM are as follows:

- The same signals and system interface operation as the attached PowerPC processor would provide in a 255-pin (16 x 16) CBGA package.
- An FR4 PCM to connect a 360-lead CBGA PowerPC microprocessor to the 288-pin PGA.
- An interconnection area between the processor and SRAM memory when configured with an L2 cache. (When the MPC750 microprocessor is configured to support an L2 cache, the L2address and data buses are entirely contained on the processor module without any increase in the number of PGA pins or complexity for the system designer.)
- Additional power supply filtering on the processor module
  - PLL voltage supply (AVdd) filtering on the PGA PCM close to the processor improves noise immunity.
  - Core voltage (Vdd) filtering on PCM reduces voltage variations.
- PCM signals determine selection of processor voltage and identification of module type
  - Direct encoding and control of power supply modules
    - Four voltage ID pins select operating core voltage from 1.3V to 3.5V.
    - Encodings match industry-standard power-controllers.
  - Self-identification of the module
    - 3-pin encoding for simple modules.
    - Serial EEPROM encoding for complex modules.

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1.3 General Parameters

The following list provides a summary of the general parameters of the PCM with an MPC750 processor and 256 Kbytes, 512 Kbytes, or 1 Mbyte of SRAM:

Technology	See General Parameters of individual components.
Die Size	See General Parameters of individual components.
Transistor Count	See General Parameters of individual components.
Package	17 x 17 pin grid array
Core Power Supply	Generally 2.6 + 5% V dc but refer to the part number specifications for a specific part for accurate information
I/O Power Supply	3.3 + 5% V dc

1.4 Electrical and Thermal Characteristics

The AC and DC electrical specifications for the PCM are identical to the electrical specifications for the attached microprocessor unless otherwise specified in the part number specifications for a particular module.

The thermal characteristics for the PCM are generally the composite of the thermal characteristics for the attached microprocessor and SRAMs. The variety of processor and SRAM speeds possible dictate that thermal characteristics are unique to a particular module and therefore are described in its associated part number specifications.

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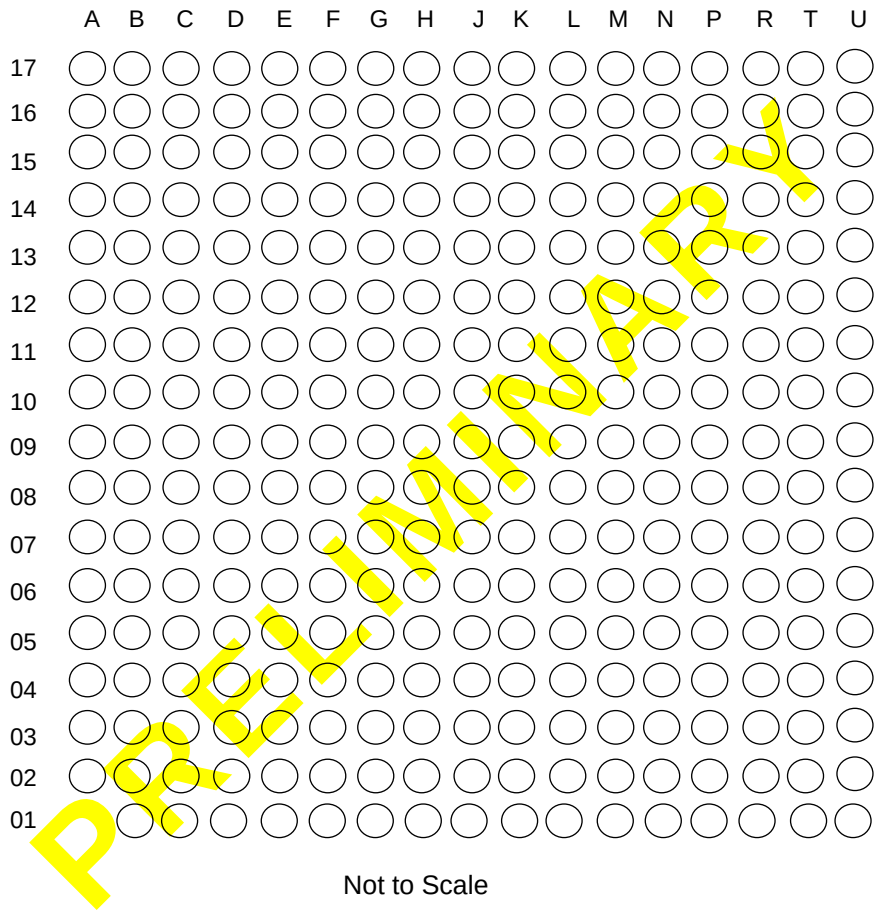
1.5 Pin Assignments

Figure 1 (in part A) shows the pinout of the PCM as viewed from the top surface. Part B shows the side profile of the module to indicate the direction of the top surface view.

Part A



Part B

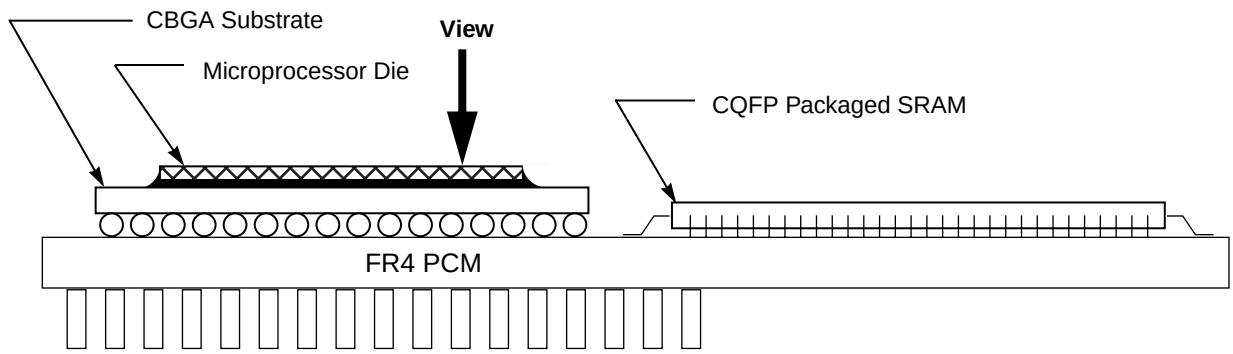


Figure 1. 17 x 17 PGA Processor + Cache Module Pinout

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1.6 Pinout Listings

Table 1 provides the pinout listing for the 17 x 17 PGA PCM. This pinout is the superset of all 17 x 17 PCMs and should be followed for maximum interchangeability between modules; however, particular implementations may not connect all signals between the PGA pins and the PowerPC microprocessor. See the individual part number specifications for specific pinouts by part number.

Table 1. Pinout Listing for the 17 x 17 PGA Module

Signal Name	Pin Number	Active	I/O
A[0–31]	F13, E1, D17, F3, E16,F1, E17, G5, F15, G4, G13, G3, F17, G2, G14, G1, G15, H1, G16, H3, G17, J1, H13, H5, H15, J2, H17, J3, J13, L1, K13, M1	High	I/O
$\overline{\text{AACK}}$	K3	Low	Input
$\overline{\text{ABB}}$	L3	Low	I/O
AP[0–3]	E6, C4, C5, A4	High	I/O
$\overline{\text{APE}}$	C8	Low	Output
$\overline{\text{ARRAY\_WR}}$[2]	A8	Low	Input
$\overline{\text{ARTRY}}$	K5	Low	I/O
AVDD	A11	High	Input
$\overline{\text{BG}}$	J5	Low	Input
$\overline{\text{BG2}}$	E13	Low	Input
$\overline{\text{BR}}$	E8	Low	Output
$\overline{\text{BR2}}$	A17	Low	Output
$\overline{\text{CI}}$	E2	Low	Output
CLK_OUT	A6	—	Output
$\overline{\text{CKSTP\_IN}}$	C9	Low	Input
$\overline{\text{CKSTP\_OUT}}$	E9	Low	Output
CSE0–CSE1[1]	E7, B5	High	Output
$\overline{\text{DBB}}$	L17	Low	I/O
DBDIS	J15	Low	Input
$\overline{\text{DBG}}$	K1	Low	Input
$\overline{\text{DBG2}}$	R15	Low	Input
$\overline{\text{DBWO}}$	J4	Low	Input
DH[0–31]	P13, N12, T15, U15, R13, U14, N10,P11, T11, U11, R10, U10, U9, T9, N9,P9, R9, U8, R8, U7, N8, P7, T7,U6, R7, R6, N7, U5, T5, U4, R5,U3	High	I/O
DL[0–31]	L16, K15, M17, L14, N17, M15, N16, L13, M13, N15, P17, R17, N14, P15, R16, U16, R14, N11, T13, R12, U13, R11, U12, N3, P3, N4, R2, T1, T3, R4, P5, N6	High	I/O
DP[0–7]	L4, N1, M3, N2, P1, L5, R1, M5	High	I/O

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Table 1. Pinout Listing for the 17 x 17 PGA Module (Continued)

Signal Name	Pin Number	Active	I/O
$\overline{\text{DPE}}$	B7	Low	Output
$\overline{\text{DRTRY}}$	J17	Low	Input
DRVMOD[0–1]	E3, D3	—	Input
$\overline{\text{GBL}}$	F5	Low	I/O
GND	B4, B8, B10, B14, D2, D6, D12, D16,F4, F6, F8, F10, F12, F14, G7, G9, G11, H2, H6, H8, H10, H12, H16, J7, J9, J11, K2, K6, K8, K10, K12, K16, L7, L9, L11, M4, M6, M8, M10, M12, M14, P2, P6, P12, P16, T4, T8, T10, T14	Low	Input
HALTED	D9	High	Output
$\overline{\text{HRESET}}$	B9	Low	Input
$\overline{\text{INT}}$	E14	Low	Input
$\overline{\text{INT2}}$	U17	Low	Input
LSSD_MODE[2]	D11	Low	Input
L1_TSTCLK[2]	B11	—	Input
L2_INT	A7	High	Input
L2_TSTCLK[2]	E10	—	Input
$\overline{\text{MCP}}$	D15	Low	Input
NAP_RUN	D7	High	Input
NC[5]	N13	—	-
OVDD[3]	B2, B6, B12, B16, D4, D8, D10, D14, F2, F9, F16, H4, H14, J6, J12, K4, K14, M2, M9, M16, P4, P8, P10, P14, T2, T6, T12, T16	High	Input
PID[0–2]	U1, U2, R3	High	I/O
PLL_CFG[0–3]	A9, A10, A13, C11	High	Input
$\overline{\text{QACK}}$	E5	Low	Input
$\overline{\text{QREQ}}$	N5	Low	Output
$\overline{\text{RSRV}}$	D5	Low	Output
SCLK	A3	—	Input
SDATA	C1	—	I/O
$\overline{\text{SHD}}$	L2	Low	I/O
$\overline{\text{SMI}}$	B17	Low	Input
$\overline{\text{SRESET}}$	D13	Low	Input
SYSCLK	C10	—	Input
SYSCLK2	T17	—	Input
$\overline{\text{TA}}$	J16	Low	Input

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Table 1. Pinout Listing for the 17 x 17 PGA Module (Continued)

Signal Name	Pin Number	Active	I/O
TBEN	E4	High	Input
$\overline{\text{TBST}}$	E12	Low	I/O
TC[0–2][4]	C6, A5, C7	High	Output
TCK	C12	—	Input
TDI	B13	High	Input
TDO	A14	High	Output
$\overline{\text{TEA}}$	J14	Low	Input
TLBISYNC	C15	Low	Input
TMS	C13	High	Input
TRST	A12	Low	Input
TSIZ[0–2]	E11, A15, B15	High	I/O
$\overline{\text{TS}}$	L15	Low	I/O
TT[0–4]	A16, C14, C16, C17, E15	High	I/O
VDD[3]	F7, F11, G6, G8, G10, G12, H7, H9, H11, J8, J10, K7, K9, K11, L6, L8, L10, L12, M7, M11	High	Input
VID[0–4]	B1, C2, A2, B3, C3	High	Input
$\overline{\text{WT}}$	D1	Low	Output
$\overline{\text{XATS}}$[1]	K17	Low	Output

Notes:

1. Not recommended for new designs.
2. These are test signals for factory use only and must be pulled up to Vdd for normal machine operation.
3. OVdd inputs supply power to the I/O drivers and Vdd inputs supply power to the processor core.
4. TC2 defined for PowerPC 604™-class processors only.
5. These signals are undefined and must be left disconnected.

Many of the PCM signals have the same definition and timing as that of the attached processor. The actual signals present vary depending upon the type of the PowerPC microprocessor used; refer to the corresponding processor hardware specifications for details.

The PCM implements several signals that are not part of the PowerPC 60x bus specification, nor of any particular PowerPC processor. These pins are unique to the PCM and are used to set operational parameters or indicate the features the PCM provides. Table 2 describes the functions of the signals provided for identification or configuration of the PCM.

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Table 2. PCM Unique/Redefined Pins

Pin Name	Definitions	Notes
VID[4–0]	The VID pins encode the voltage encoding as described in Section 1.8.6, “Voltage Encoding.” Note the little-endian bit ordering, used for compatibility with industry standard parts.	These pins must be pulled up by the power controller for proper operation. The pullups must be wired to a voltage level which is stable while the power controller ramps up after power up. Many power controllers include internal pullups to handle this.
PID[0–2]	The PID pins carry the presence detect codes as described in Section 1.8.7, “Presence Detect.”	These pins must be pulled up by the system with 1K to 10K pullup resistors.
PLL[0–3]	Specified PLL setting to use.	These PLL pins may be connected to VDD or ground on the PCM if a PLL-encoded PCM is ordered; otherwise, the motherboard may control the CPU’s PLL pins directly as usual with PowerPC CPUs.
SYSCLK2	Clock for second processor. Same timing as SYSCLK for PowerPC CPUs.	Unused signal—Reserved for future function; signal should remain disconnected
INT2	Interrupt for second processor. Same timing as $\overline{\text{INT}}$ for PowerPC CPUs.	Unused signal—Reserved for future function; signal should remain disconnected
BR2	Bus request for second processor. Same timing as $\overline{\text{BR}}$ for PowerPC CPUs.	Unused signal—Reserved for future function; signal should remain disconnected
BG2	Bus grant for second processor. Same timing as $\overline{\text{BG}}$ for PowerPC CPUs.	Unused signal—Reserved for future function; signal should remain disconnected
DBG2	Data Bus grant for second processor. Same timing as $\overline{\text{DBG}}$ for PowerPC CPUs.	Unused signal—Reserved for future function; signal should remain disconnected
SCLK	I^2C serial clock input	Connected when EEPROM presence detect mode is implemented.
SDATA	I^2C command input/ data output	Connected when EEPROM presence detect mode is implemented.

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1.7 Package Description

The following sections provide the package parameters and the mechanical dimensions for the PCM.

1.7.1 Package Parameters

The package parameters are as provided in the following list. The package consists of a 288-lead pin grid array (PGA) on the bottom of a 1.75 x 2.5 inch glass-epoxy (FR4) substrate with a PowerPC microprocessor in a ceramic ball grid array (CBGA) package and two fast static RAMs (FSRAMs) in ceramic quad flat pack (CQFP) or plastic ball grid array (PBGA) packages attached on the top. The package parameters for the PGA PCM are:

Package outline	1.75 in. by 2.50 in.
Interconnects	288
Pitch	0.1 in
Pin Diameter	0.018 in
Pin Length	.180 in
Lead Plating	Au
Module Height without pins	.215 in

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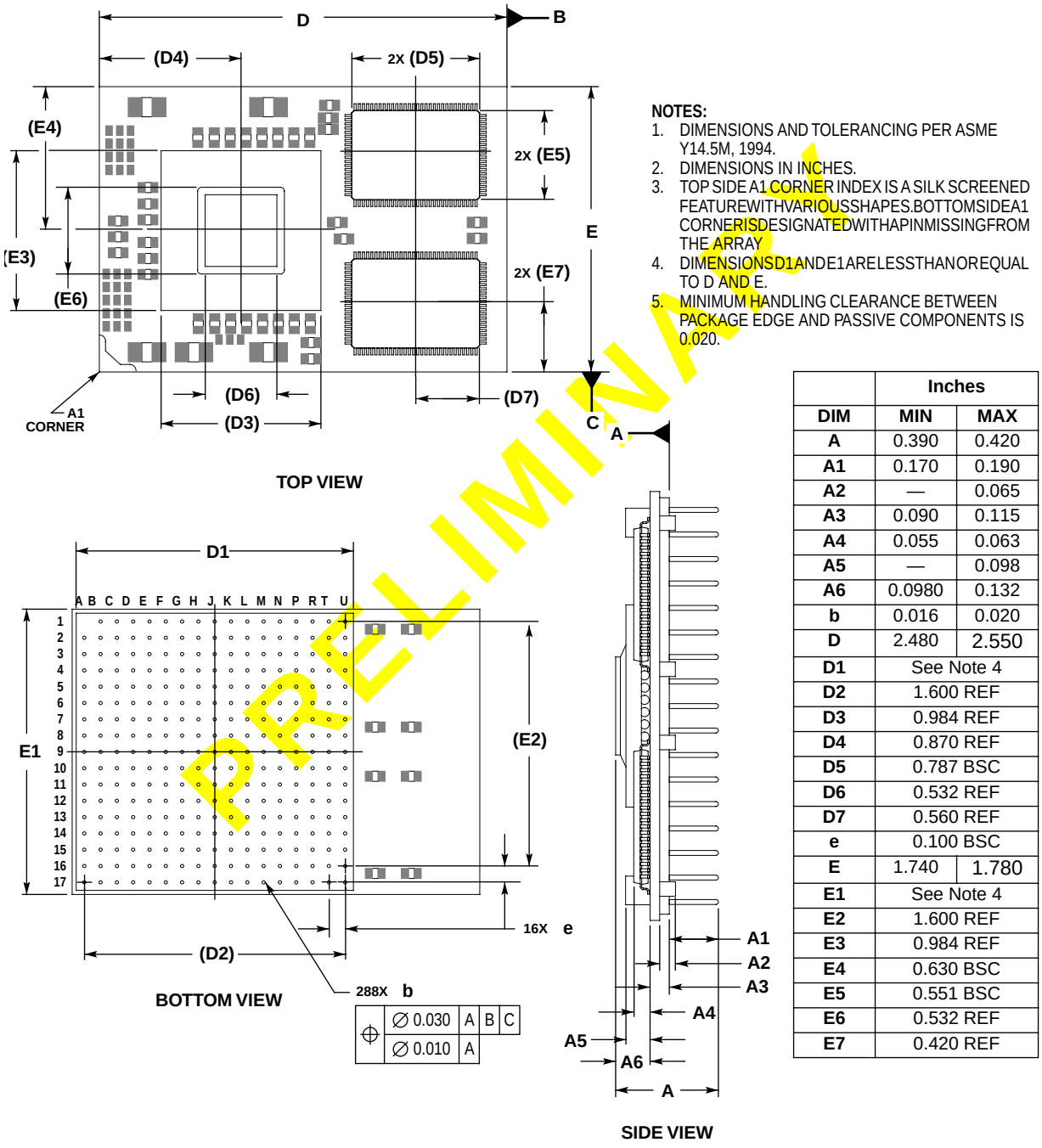
1.7.2 Mechanical Dimensions

Figure 2 provides the mechanical dimensions for the PCM.



NOTES:

1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN INCHES.
3. TOP SIDE A1 CORNER INDEX IS A SILK SCREENED FEATUREWITHVARIOUSSHAPES.BOTTOMSIDEA1 CORNERISDESIGNATEDWITHAPINMISSINGFROM THE ARRAY
4. DIMENSIONSD1ANDE1ARELESSTHANOREQUAL TO D AND E.
5. MINIMUM HANDLING CLEARANCE BETWEEN PACKAGE EDGE AND PASSIVE COMPONENTS IS 0.020.

	Inches	
DIM	MIN	MAX
A	0.390	0.420
A1	0.170	0.190
A2	—	0.065
A3	0.090	0.115
A4	0.055	0.063
A5	—	0.098
A6	0.0980	0.132
b	0.016	0.020
D	2.480	2.550
D1	See Note 4	
D2	1.600 REF	
D3	0.984 REF	
D4	0.870 REF	
D5	0.787 BSC	
D6	0.532 REF	
D7	0.560 REF	
e	0.100 BSC	
E	1.740	1.780
E1	See Note 4	
E2	1.600 REF	
E3	0.984 REF	
E4	0.630 BSC	
E5	0.551 BSC	
E6	0.532 REF	
E7	0.420 REF	

Figure 2. Mechanical Dimensions and Bottom Surface Nomenclature of the PCM

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1.8 System Design Information

Refer to the device-specific user's manuals and hardware specifications for system design information about the processor and SRAM attached to the module. This section provides descriptions of functionality and electrical or thermal design recommendations unique to the PCM.

1.8.1 PLL Configuration

The system utilizing the PCM is expected to configure the processor PLL by the PLL_CFG[0–3] signals appropriate to the attached processor. For a given SYSCLK (bus) frequency, the PLL configuration signals set the internal CPU and VCO frequency of operation. Refer to the system design information of the appropriate processor's hardware specifications for appropriate PLL settings. It is possible during manufacture to fix the settings of PLL_CFG[0–3] via jumpers on the substrate to one particular combination that will be independent of the signals asserted by the system on the pins; if this is done for a particular part number, it will be noted in the part number specifications for that specific part.

The interface between the processor and the SRAMs on the module will operate at CPU-to-L2 frequency divisors of ÷1, ÷1.5, ÷2, ÷2.5, and ÷3. These ratios will have to be programmed into the L2 cache control registers on the processor by the operating system and the L2 cache enabled before the SRAM will be functional on the module. See the part number specifications for the CPU-to-L2 frequency divisor(s) supported on a particular part.

1.8.2 PLL Power Supply Filtering

The AVdd power signal provides power to the clock generation phase-locked loop. To ensure stability of the internal clock, the power supplied to the AVdd input signal of the microprocessor should be as electrically quiet as possible. For maximum effectiveness the filter circuit of Figure 3 which is normally recommended for inclusion in the system design has been included on the PCM itself.

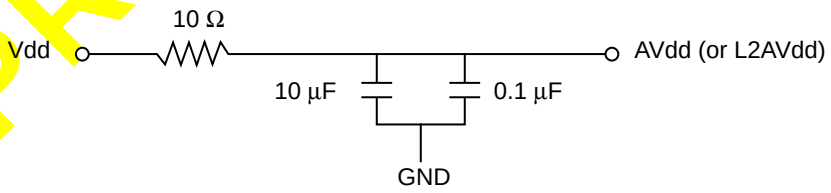

Figure 3. PLL Power Supply Filter Circuit

The PCM resistors are used to program the connection between the external signals and the microprocessor PLL supply as shown in Figure 4. If required, the system can provide additional power supply filtering for the AVdd signal, shown in Figure 3, to the PCM AVdd signal. The PCM provides AVdd power supply filtering as shown in Figure 4.

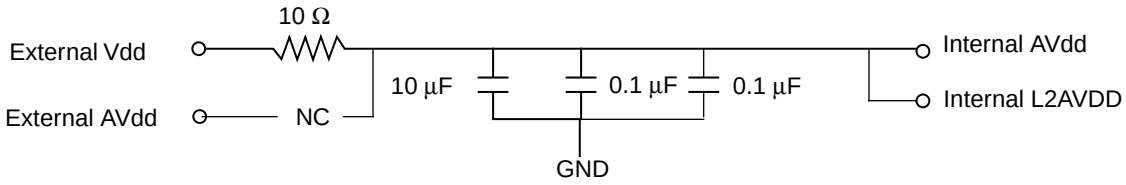

Figure 4. PCM PLL Power Supply Filter Circuit

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1.8.3 Decoupling Recommendations

The microprocessor and cache on the PCM can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the system, and the module itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each Vdd and OVdd pin of the module. It is also recommended that these decoupling capacitors receive their power from separate Vdd, OVdd, and GND power planes in the PCB, utilizing short traces to minimize inductance.

The module will provide some bulk decoupling and high frequency decoupling capacitors on the module itself to improve the overall system noise immunity.

1.8.4 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to Vdd. Unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external Vdd, OVdd, and GND pins of the PCM.

1.8.5 Socketing

The PCM is specifically designed for the flexibility of a socket. The PGA footprint is compatible with the widely available Socket #3 footprint popular in the PC industry. Several vendors provide this socket, including Amp Incorporated (part number: 916668-1).

1.8.6 Voltage Encoding

The core operating voltage (Vdd and AVdd) for PowerPC processors has varied with semiconductor process technology. Within a narrow range determined by the process technology, Motorola has specified non-standard core voltages for some processors in device-specific part number specifications.

The PCM provides additional pins to communicate the attached processor's preferred core voltage. The desired voltage setting is encoded on the VID[4–0] signals. This 5-bit bus encodes various voltage settings which match existing industry standards. In most systems these signals are connected directly to a Voltage Regulator Module (VRM) or to an on-board power supply which accepts the VID encoded voltage setting.

The encoding for the VID voltage levels supported by the PCM are shown in Table 3.

Table 3. Voltage Encoding

VID[4–0] Output	Voltage (V)	VID[4–0] Output	Voltage (V)
01111	1.30 V	10000	3.50 V
01110	1.35 V	10001	3.40 V
01101	1.40 V	10010	3.30 V
01100	1.45 V	10011	3.20 V
01011	1.50 V	10100	3.10 V
01010	1.55 V	10101	3.00 V
01001	1.60 V	10110	2.90 V
01000	1.65 V	10111	2.80 V

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Table 3. Voltage Encoding (Continued)

VID[4–0] Output	Voltage (V)	VID[4–0] Output	Voltage (V)
00111	1.70 V	11000	2.70 V
00110	1.75 V	11001	2.60 V
00101	1.80 V	11010	2.50 V
00100	1.85 V	11011	2.40 V
00011	1.90 V	11100	2.30 V
00010	1.95 V	11101	2.20 V
00001	2.00 V	11110	2.10 V
00000	2.05 V	11111	No CPU

Note: The bit numbering shown here is little-endian due to pre-existing standards. This differs from most other PowerPC bus numbering conventions.

The PCM encodes the voltage setting by selectively installing 0-ohm resistors on the VID bus. The regulator must have internal pullups to properly encode the settings (this is true of all known 5-bit encoded switching controllers).

1.8.7 Presence Detect

The PCM provides a means of self-identification (called presence detection after the method(s) used to identify memory and cache modules). The module implements a three-wire solution which combines the inexpensive parallel encoding of Single In-line Memory Modules (SIMMs) with the more flexible serial solution found on Dual In-line Memory Modules (DIMMs). Figure 5 shows the architecture of the presence detection:

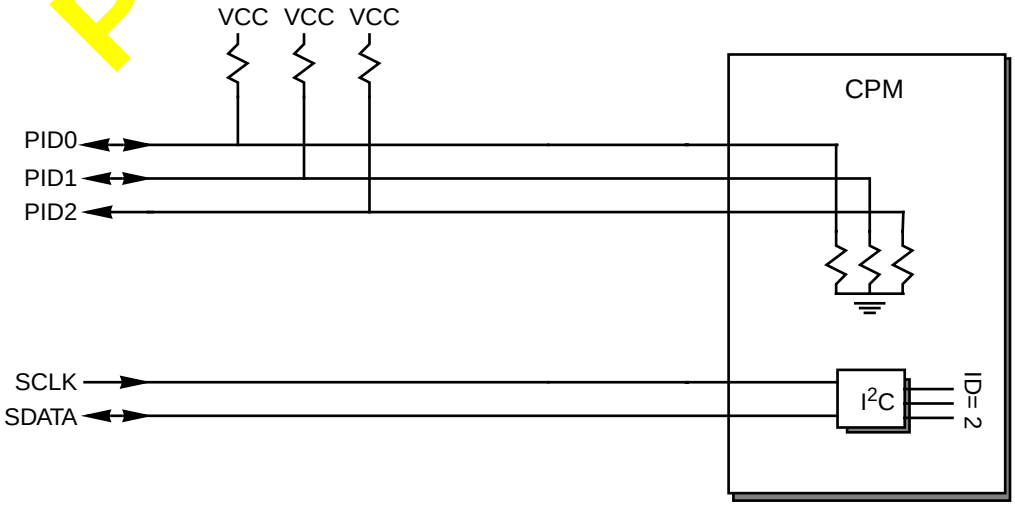

Figure 5. CPU Present Detect Hardware

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Note that either the pull-down resistors are installed, or the I^2C EEPROM, but not both.

For the simplest case, the three presence detect pins encode seven specific configurations of processor or processor/cache combinations, with one reserved for identification of the serial EEPROM method. The motherboard requires pullups on the parallel lines (1K to 10K ohms), and the PCM selectively pulls down the PID lines to create the PID encoding.

The possible combinations of processor and cache with all the attendant settings are too numerous to directly encode in the three bits allotted, so predefined configurations are assigned an identifier. Additionally, the table used will be associated with the processor attached (determined by reading the processor PVR). Together, the processor ID register and PID bits are used to determine the most difficult cache settings, with the remainder handled by software, as shown in Table 4.

Table 4. Processor Presence Detect (PPD) Information

Parameter	Determined by
Cache size	PPD encoding
Processor core/cache bus clock ratio	PPD encoding
Cache type	PPD encoding
Cache enable	Software
Cache parity	Software, or always off
Cache write-through/copyback	Software, or always copyback
Cache output hold	Always 0.5 ns
Cache clock type	If late-write: differential If pipelined: single-ended

Table 5 shows example settings for an MPC750-based PCM with cache:

Table 5. MPC750 Presence Detect Table

PID[0–2]	Cache/Core Ratio	SRAM Type	Hold (ns)	Size	Example Module CPU/Cache	SRAM Speed
0 0 0	3:2	Late-write	0.5	1 M	300/200	200
0 0 1	2:1	Pipelined	0.5	512 K	300/150 266/133 233/117	150 133 117
0 1 0	2:1	Pipelined	0.5	1 M	300/150 266/133 233/117 200/100	150 133 117 100
0 1 1	5:2	Pipelined	0.5	512 K	300/120 266/106 233/ 93	120 117 100
1 0 0	5:2	Pipelined	0.5	1 M	300/120 266/106 233/ 93	120 117 100

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Table 5. MPC750 Presence Detect Table (Continued)

PID[0–2]	Cache/Core Ratio	SRAM Type	Hold (ns)	Size	Example Module CPU/Cache	SRAM Speed
1 0 1	3:1	Pipelined	0.5	512 K	300/100 266/ 88	100 90
1 1 0	3:1	Pipelined	0.5	1 M	300/100 266/88	100 90
1 1 1	No Module ID				This indicates the presence of a serial EEPROM or non-cache PCM.	

Note that there are various cache speeds for each entry. The processor does not need to know the actual speed of its cache, only the proper ratio of core:cache, in order to properly configure the cache controller. If the cache speed is of interest, the bus frequency and PLL settings must be determined via software.

For each new processor with cache a similar table will be created. If a PCM needs a particular combination that was not pre-defined in this table, then a serial presence detect EEPROM will be used. A serial EEPROM is detected when all ones are sensed on the PID lines. To determine the system configuration, software will have to read the data from the EEPROM, as shown in Figure 5.

Either software or an I^2C controller may be used to address EEPROM #2 (the address of the presence detect EEPROM) and load the configuration data.

1.8.7.1 Presence Detect EEPROM Format

The data within presence detect EEPROM memory generally follows JEDEC DIMM outline and reuses the same data formats. The format is not JEDEC approved, and will not be since it cannot be shared with DIMM memory presence detect lines.

The format of the data is based upon the following criteria:

- The Software Presence Detect (SPD) describes the PCM but does not tell the software what register bits to use (interfaces change over time).
- Minimize software impact by re-using memory SPD data formats. This also implies that little-endian multi-byte ordering is retained.
- Keep the block/length structure so that I^2C readers can be re-used.
- The first few bytes should not be all ones, so that the I^2C EEPROM reader routine can easily detect the presence/absence of data.

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Table 6 shows the PCM SPD format.

Table 6. PCM SPD Data Format

Byte	Field	Description	Range of Values	Example
0	NO	Number of bytes written into EEPROM	64, 128, 255	80
1	SIZE	Total number blocks of SPD RAM	4, 8, 16	08
2	TYPE	Module type	CPU	00
5, 6	WIDTH	Data width of module	1–65536	80, 00
7	VID	Voltage level of module (Mirrors VID encoding)	3.3V	12
			2.5V	1A
8	SIGLEV	Signaling level	1:LVTTL	01
			2:SSTL	02
			3:GTL	03
9	TAU0	TAU calibration, 0 °C	–128..127	00
10	TAU100	TAU calibration, 100 °C	–128..127	00
11–15		Reserved for other general information		
16	CTYPE	Cache type	0:None	00
			1:Flow-through	01
			2:Pipelined	02
			3:Late-write	03
17, 18	CSIZE	Cache size LSB, MSB (K)	0	00, 00
			512K	00, 02
			1M	00, 04
			2M	00, 08
19, 20	CSPEED	Cache speed LSB, MSB (MHz)	0	00, 00
			180	B4, 00
			200	C8, 00
21	CCLOCK	Cache clock type	0:Single-ended	00
			1:Differential	01
22	CHOLD	Cache output hold	0.0 ns	00
			0.5 ns	05
			1.0 ns	10
			1.5 ns	15
23–31		Reserved for other cache information		
32	CPUS	CPU count	0–n	01

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Table 6. PCM SPD Data Format (Continued)

Byte	Field	Description	Range of Values	Example
33	SPEED	CPU speed LSB, MSB (MHz)	66	42, 00
			200	C8, 00
			333	4D, 01
34, 35	BUSSPD	Bus speed LSB, MSB (MHz)	66	42, 00
			100	64, 00
36–63		Reserved for other CPU information		
64–67	MANUF	Manufacturers ID	Stock name	“MOT“
68–90	CPUID	CPU ID	Part marking	“MCM603RRX 366LARX”
91–127		Manufacturers data	TBD	FF
128–nnn		Unused		FF

The first eight bytes are fairly similar to the DIMM SPDs in the hope that it will enable the EEPROM access software to retrieve a block from either SPD with minimal effort. Thereafter, the formats diverge but should allow the re-use of existing DIMM data conversion routines (for example, the format for output hold).

The fields of the EEPROM are described in detail as follows:

NO This field contains the total number of bytes written during manufacture. This field is retained for compatibility with existing SPD standards.

SIZE This field contains the number of 16-byte blocks available in the EEPROM. A value of 0x10 indicates the EEPROM is 16 x 16 = 256 bytes long. This field is retained for compatibility with existing SPD standards.

TYPE The type encoding field is zero to indicate that it is not a memory DIMM. This field is retained for compatibility with existing SPD standards.

WIDTH This field describes the width of the module. The value is the width of the PCM, either 0x0080 (64-bit) or 0x0100 (128-bit). This field is retained for compatibility with existing SPD standards.

VID The VID field contains a copy of the encoding presented to the motherboard via the VID pins. Refer to the VRM table for the encoded values.

SIGLEV The SIGLEV field contains an encoded description of the PCM interface level; see Table 7.

Table 7. PCM Interface Level

Interface Level	Code
LVTTL	01
SSTL	02
GTL	03

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TAU This field describes the calibration factors necessary to temperature compensate a thermal assist unit (TAU), such as found on MPC750 processors. The current TAU units have a high relative accuracy, but an absolute accuracy of ±12˚C. With the appropriate compensation factors stored in EEPROM, the TAU-handling software can determine the temperature to the specified accuracy.

The parameters describe the numerical offset applied at 0˚C and 100˚C. The software can elect to adjust the temperature over the described interval for greatest accuracy (using linear interpolation), or apply only the 100˚C factor for faster compensation (with less accuracy).

CTYPE The CTYPE field contains an encoding which indicates the type of cache attached to the processor dedicated L2 interface, if any. If zero is present, indicating no cache, none of the other cache parameters have any meaning; see Table 8.

Table 8. CTYPE Field Encoding

CTYPE	Cache Type
0	None
1	Flow-through
2	Pipelined
3	Late-write

CSIZE The CSIZE field contains the size of the cache, in kilobytes.

CSPEED The CSPEED field contains the speed of the cache, in megahertz.

CCLOCK The CCLOCK field is used to configure the L2 clock signals as single-ended (0 value) or differential (1 value).

CHOLD The CHOLD field contains the hold time needed for the cache memories, encoded in the pseudo-BCD method used for SPD data values. The lower nibble ranges from 0..9, and describes fractions of nanoseconds. The upper range is from 0..15, and is in nanoseconds. The lower nibble may be used as-is, or simply to round up the upper nibble, as needed.

CPUS The CPUS field contains the number of CPUs present on the PCM.

SPEED The SPEED field contains the maximum specified core operating speed of the CPU(s), in megahertz.

BUSSPD The BUSSPD field contains the maximum specified bus operating speed of the CPU(s), in megahertz.

MANUF The MANUF field contains the stock ticker symbol of the manufacturer of the CPU. The encoding method is ASCII; unused bytes are filled with zero.

CPUID The CPUID field contains the literal ASCII name (part ordering number) of the CPU(s) installed. For example, a 300 MHz PowerPC 603e™ would be encoded as MPC603RRX300LA. Unused bytes are filled with zeroes.

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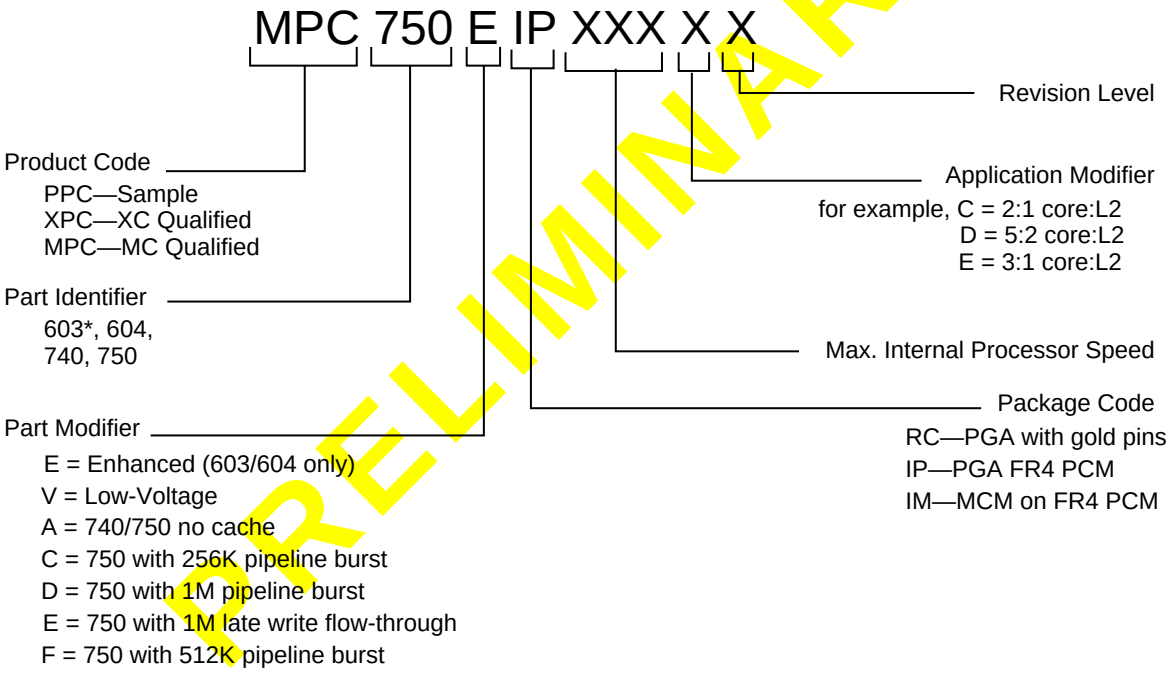
1.9 Ordering Information

This section provides the part numbering nomenclature for the PCM. Note that the individual part numbers correspond to a particular PowerPC microprocessor at a maximum core frequency and a certain size of SRAM. Often the ratio of core to L2 frequency is called out in the part number also because this ratio and the maximum core frequency set the maximum frequency of the attached SRAM. These details for a particular part are provided in the part number specifications available from the Motorola PowerPC website at: http://www.mot.com/SPS/PowerPC/.

1.9.1 Part Number Key

Figure 6 provides an example of the part numbering scheme for the PCM.



Note: The term ‘603’ is used as an abbreviation for ‘PowerPC 603™’ .

Figure 6. Motorola Part Number Key

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