SmartMX2 P40 family P40C012/040/072

Secure smart card controller

Rev. 3.0 — 24 April 2015
262830

Product short data sheet
COMPANY PUBLIC

1. Introduction

1.1 Product overview

SmartMX2-P40 family is a secure microcontroller family designed and manufactured by NXP Semiconductors. It is part of the SmartMX2-IC family produced in 90 nm CMOS technology. SmartMX2-P40 is an ISO/IEC 7816 compliant contact secure microcontroller platform, built around the proven and powerful MRK3-SC RISC core. The overall architecture of P40 has been streamlined to meet the performance requirements of payment and eGovernment contact smart card applications.

NXP's SmartMX2 P40 security architecture is built on more than 15 years of experience in this area. The SmartMX2-P40 product family provides embedded firmware forming a Hardware Abstraction Layer (HAL). The use of this HAL makes it easier to efficiently develop embedded software for the device.

SmartMX2-P40 supports DES, AES, ECC, RSA cryptography, hash computation, and random-number generation. For asymmetric RSA and ECC cryptography, a dedicated coprocessor supports RSA key lengths up to 4096 bits and ECC key lengths up to 521 bits. Coprocessors for symmetric ciphers support DES (single DES, 2-key 3DES, and 3-key 3DES), plus AES cryptography with bit lengths of 128-bit, 192-bit, or 256-bit. The memory configuration, which combines up to 265 KB User ROM, 6 KB RAM, up to 72 KB EEPROM, handles static code and dynamic data separately, and enables fast code execution from ROM.

The P40 family also provides a ready-to-use crypto library with highly efficient software APIs for all cryptographic functions (RSA key length up to 2048 bits, ECC up to 384 bits).

Table 1. Feature table

Product type	EEPROM [KB]	User ROM [KB][1]	Total RAM [B]	RAM allocation CPU/PKCC	Coprocessor			ISO/IEC 7816 IO pads	Interface option
					PKC	DES	AES		
P40C012	13	up to 265	6144	dynamic	yes	yes	yes	1	ISO 7816
P40C040	40	up to 265	6144	dynamic	yes	yes	yes	1	
P40C072	72	up to 265	6144	dynamic	yes	yes	yes	1	

[1] Refer to Section 14.3

2. General description

2.1 General remarks

This document offers an introduction into the features and the architecture of the SmartMX2 P40 products.

The product data sheet and other detailed documentation, e.g. for Card Operating System (COS) development are available through NXP's portal for secured documentation. Access to such documents is granted on a need-to-know basis. Contact NXP sales for registration and access.

2.2 Naming conventions

Table 2. Naming conventions

P40xeee	
x	**Interface and feature configuration identifier, as currently defined, e.g.:** x = C: Asymmetric and symmetric cryptography implemented, ISO/IEC 7816 contact interface
eee	**Indication of the Non-Volatile memory size in KB** eee = 012: 13 KB EEPROM implemented eee = 040: 40 KB EEPROM implemented eee = 072: 72 KB EEPROM implemented

2.3 Contact interfaces

Operating in accordance with ISO/IEC 7816, the SmartMX2 P40 contact interface is supported by a built-in Universal Asynchronous Receiver/Transmitter (UART). P40 UART enables data rates of up to 688 kbit/s allowing for the automatic generation of all typical baud rates and supports transmission protocols T=0 and T=1.

2.4 Public Key Crypto (PKC) coprocessor

The PKCC is speeding up the computation of public-key cryptographic operations within the P40C012/040/072.

The PKC coprocessor flexible interface provides programmers with the freedom to implement their own cryptographic algorithms. A Common Criteria certified crypto library from NXP providing a large range of required functions is available for all devices listed in Table 4 in order to support customers in implementing public key-based solutions.

2.5 Coprocessor for DES and AES

The DES algorithm, widely used for symmetric encryption, is supported by a dedicated, high performance, highly attack-resistant hardware coprocessor. Relevant standards (ISO/IEC, ANSI, FIPS) are fully supported. A secure crypto library element for DES is available.

The same coprocessor supports secure AES as well. The implementation is based on FIPS197 as standardized by the National Institute for Standards and Technology (NIST), for key lengths of 128-bit, 192-bit, and 256-bit with performance levels comparable to

DES. AES is the next generation for symmetric data encryption and recommended successor to DES providing significantly improved security level. A secure crypto library element for AES is available.

2.6 Security features

Advanced 0.09 µm CMOS technology, with seven metal layers, provides enhanced protection against reverse engineering and probing attacks, and produces a highly protective mesh of active and dynamic multi-threaded shielding.

SmartMX2 P40 incorporates a wide range of both inherent and OS-controlled security features as a countermeasure against all types of attacks. NXP Semiconductors apply their extensive knowledge of chip security, very dense CMOS technology and active shielding methodology.

As attacks evolve over time, the multi-dimensional approach of the SmartMX2 P40 security architecture allows for more proactive and continuous enhancements of the security mechanisms compared to alternative and less versatile approaches. This makes SmartMX2 P40 a future-proof secure micro-controller platform neutralizing all side channel and fault attacks as well as reverse engineering efforts.

3. Features and benefits

3.1 Standard P40C012/040/072 features

- EEPROM: 13, 40 or 72 KB
- ROM: up to 265 KB
- RAM: 6144 B split into area usable for CPU and PKC coprocessor.
- Dedicated, RISC based Smart Card CPU
- PKC coprocessor
  - Boolean operations for acceleration of major Public Key Cryptography (PKC) systems such as RSA and ECC
  - 32-bit operand input/output interface
- High speed DES/AES coprocessor
- ISO/IEC 7816 contact interface with UART supporting standard protocols T=0 and T=1 as well as high speed personalization up to 688 kbit/s
- High speed 8-, 16- or 32-bit CRC engine according to ITU-T polynomial definition
- Low power Random Number Generator (RNG) in hardware, AIS-31 compliant once NXP Crypto Library functions are used
- 2.7 V to 5.5 V extended operating voltage range for class B and A (depending on product)
- -25 °C to +85 °C ambient temperature

3.2 Security features

- Security sensors
  - Low and high clock frequency sensor
  - Low and high temperature sensor
  - Low and high supply voltage sensor
  - Single Fault Injection (SFI) attack detection
  - Light sensors (incl. integrated memory light sensor functionality)
- Active shielding
- 10 bytes Unique ID for each die
- Clock input filter for protection against spikes
- Optional programmable card disable feature
- Memory security (encryption and physical measures) for RAM, NV memory and ROM

4. Applications

- Banking
- Multi-application cards
- ID cards
- Health cards
- Electronic driving licences
- Digital Signature
- High-security access management
- Other secure micro controller applications

5. Quick reference data

Table 3. Limiting values

Voltages are referenced to VSS (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			-0.5	+5.8	V
V_I	input voltage	any signal pad		-0.5	+5.8	V
V_{esd}	electrostatic discharge voltage (HBM)	pads VDD, VSS, CLK, RST_N, IO1	[1]		± 4.0	kV
	electrostatic discharge voltage (CDM)	all pads	[2]		± 1000	V
P_{tot}	Total power dissipation		[3]	-	600	mW
T_{amb}	Operating ambient temperature		[4]	-25	+85	C

[1] In accordance with ANSI/ESDA/JEDEC JS-001-2011, ESDA/JEDEC Joint Standard for Electrostatic Discharge Sensitivity Testing - Human Body Model (HBM) - Component Level.

[2] In accordance with JEDEC JESD22-C101 for Charged-Device Model (CDM).

[3] Depending on appropriate thermal resistance of the package.

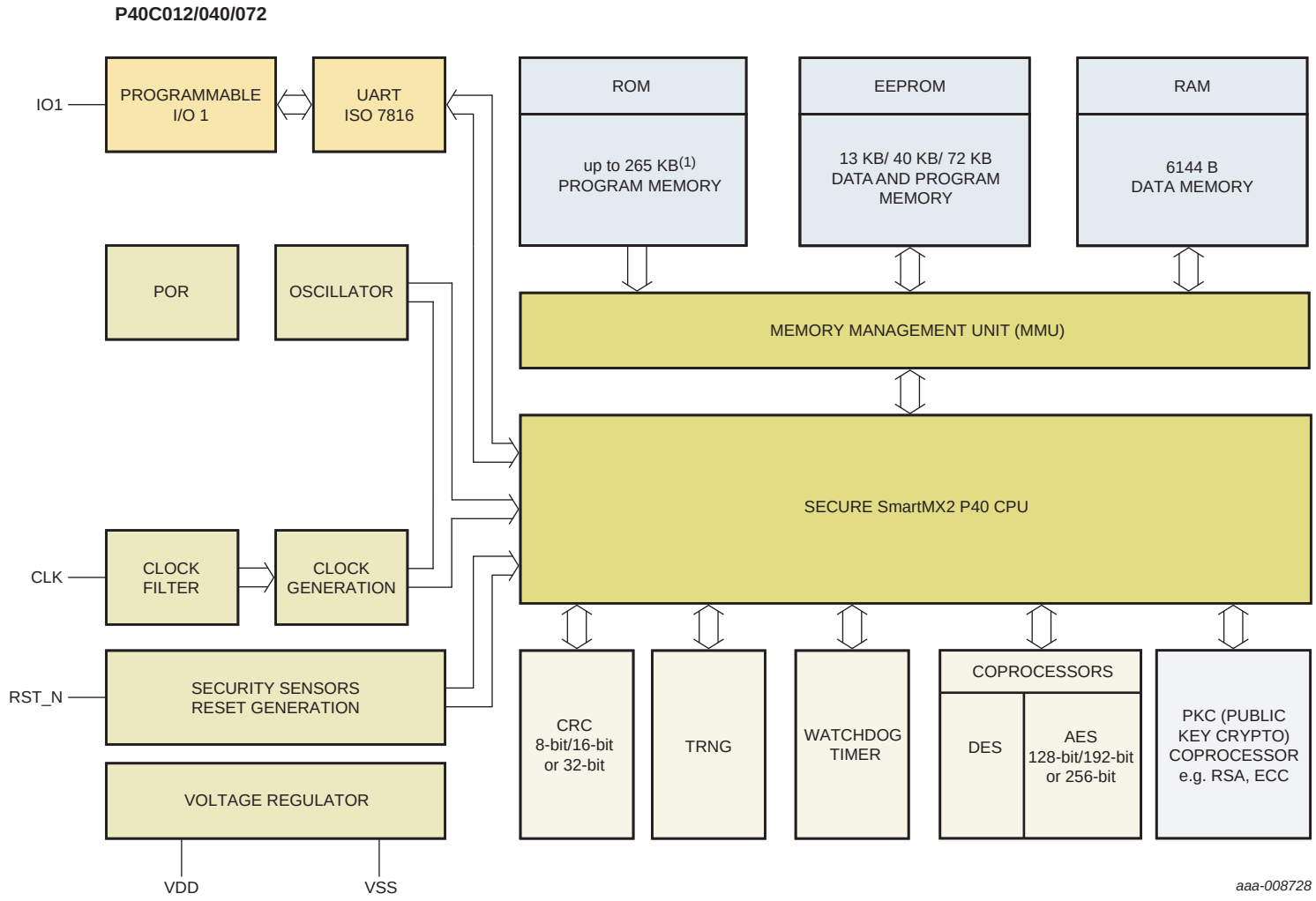
[4] All product properties and values specified within this data sheet are only valid within the operating ambient temperature range.

6. Ordering information

Table 4. Ordering information

Type number	Package		
	Name	Description	Version
P40C012U15	FFC	12 inch wafer (sawn, 150 µm thickness, on film frame carrier; electronic fail die marking according to SECSII format)	NAU000
P40C040U15			
P40C072U15			
P40C012U75	FFC	12 inch wafer (sawn, 75 µm thickness, on film frame carrier; electronic fail die marking according to SECSII format)	NAU000
P40C040U75			
P40C072U75			
P40C012X84	PCM1.5	contact chip card module (super 35 mm tape format, 8-contact); multi-source	SOT658
P40C040X84			
P40C072X84			
P40C012X85	Pd-PCM1.5	palladium plated contact chip card module (super 35 mm tape format, 8-contact); multi-source	SOT658
P40C040X85			
P40C072X85			
P40C012X60	PCM3.1	contact chip card module (super 35 mm tape format, 8-contact)	SOT658
P40C040X60			
P40C072X60			
P40C012X61	Pd-PCM3.1	palladium plated contact chip card module (super 35 mm tape format, 8-contact)	SOT658
P40C040X61			
P40C072X61			

7. Functional diagram



Remark: The diagram provides a generic overview of the architecture of the SmartMX2 P40 product family. Functional blocks, pins and connections shown in this diagram are optional and represent a super-set of those elements actually implemented in a real product.

(1) see Section 14.3 “ROM size and communication library”

Fig 1. Functional diagram P40C012/040/072

8. Revision history

Table 5. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
P40C040_C072_SMX2_FAM_SDS v3.0	20150424	Product short data sheet	-	P40C040_C072_SMX2_FAM_SDS v2.1
Modifications:	• updated to “product” status • global update: standardised graphics (formal check only, no content change)			
P40C040_C072_SMX2_FAM_SDS v2.1	20141010	Preliminary short data sheet	-	P40C040_C072_SMX2_FAM_SDS v2.0
P40C040_C072_SMX2_FAM_SDS v2.0	20140923	Preliminary short data sheet	-	P40C040_C072_SMX2_FAM_SDS v1.4
P40C040_C072_SMX2_FAM_SDS v1.4	20131217	Objective short data sheet	-	P40C040_C072_SMX2_FAM_SDS v1.3
P40C040_C072_SMX2_FAM_SDS v1.3	20131105	Objective short data sheet	-	P40C040_C072_SMX2_FAM_SDS v1.2
P40C040_C072_SMX2_FAM_SDS v1.2	20131011	Objective short data sheet		-

9. Legal information

9.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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11. Tables

12. Figures

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