TEA19161T/2

Digital controller for high-efficiency resonant power supply

Rev. 2.1 — 18 May 2021 Product data sheet

1 General description

The TEA19161T is a fully digital controller for high-efficiency resonant power supplies. Together with the TEA19162T PFC controller and the TEA1995T dual SR controller, a complete resonant power supply can be built which is easy to design and has a very low component count. This power supply meets the efficiency regulations of Energy Star, the Department of Energy (DoE), the Eco-design directive of the European Union, the European Code of Conduct, and other guidelines. So, any auxiliary low-power supply can be omitted.

In contrast to traditional resonant topologies, the TEA19161T (LLC) shows a high efficiency at low loads due to the newly introduced low-power mode. This mode operates in the power region between continuous switching (also called high-power mode) and burst mode.

Because the TEA19161T is regulated via the primary capacitor voltage, it has accurate information about the power delivered to the output. The measured output power defines the mode of operation (burst mode, low-power mode or high-power mode). A configuration pin can easily set the transition levels of the operating modes.

The TEA19161T contains a low-voltage die with a fully digital controller for output power control, start-up, initializations, and protections. These protections include OverCurrent Protection (OCP), OverVoltage Protection (OVP), Open-Loop Protection (OLP), and Capacitive Mode Regulation (CMR). It also contains a high-voltage Silicon-On-Insulator (SOI) controller for high-voltage start-up, integrated drivers, level shifter, protections, and circuitry assuring zero-voltage switching.

The TEA19161T is designed to cooperate with the TEA19162T Power Factor Control (PFC) controller. For communications about start-up and protections, the TEA19161T contains a digital control interface. The digital control enables a fast latch reset mechanism. It maximizes the overall system efficiency at low output power levels by setting the TEA19162T to operate in burst mode.

The TEA19161T/TEA19162T/TEA1995T combination gives an easy to design, highly efficient and reliable power supply, providing 90 W to 500 W, with a minimum of external components. The system provides a very low no-load input power (< 75 mW; total system including the TEA19161T/TEA19162T/TEA1995T combination) and high efficiency from minimum to maximum load. So, any additional low-power supply can be omitted, ensuring a significant system cost saving and highly simplified power supply design.

2 Features and benefits

2.1 Distinctive features

- Complete functionality as a combination with TEA19162T
- Integrated high-voltage start-up
- Integrated high-voltage Level Shifter (LS)
- Extremely fast start-up (< 500 ms at V_{mains} = 100 V (AC))
- Continuously V_{SUPIC} regulation via the SUPHV pin during start-up and protection, allowing minimum SUPIC capacitor values
- Operating frequencies are outside the audible area at all operating modes
- Integrated soft start
- Power good function
- Maximum 500 kHz half-bridge switching frequency

2.2 Green features

- Extremely high efficiency from low load to high load
- Compliant with Energy using Product directive (EuP) lot 6
- Excellent no-load input power (< 75 mW for TEA19161T/TEA19162T/TEA1995T combination)
- Regulated low optocurrent, enabling low no-load power consumption
- Very low supply current during non-switching state in burst mode
- Transition between different operation modes (high-power/low-power/burst mode) occur at integrated, externally adjustable power levels
- Adaptive non-overlap time

2.3 Protection features

- Supply UnderVoltage Protection (UVP)
- OverPower Protection (OPP)
- Integrated adjustable overpower time-out
- Adjustable latch or restart function for OverPower Protection
- On-chip OverTemperature Protection (OTP)
- Capacitive Mode Regulation (CMR)
- Accurate OverVoltage Protection (OVP)
- Maximum on-time protection for low-side and high-side driver output
- OverCurrent Protection (OCP)
- Disable input

3 Applications

- Desktop and all-in-one PCs
- LCD television
- Notebook adapter
- Printers

4 Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
TEA19161T/2	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

5 Marking

Table 2. Marking codes

Type number	Marking code
TEA19161T/2	TEA19161T

6 Block diagram

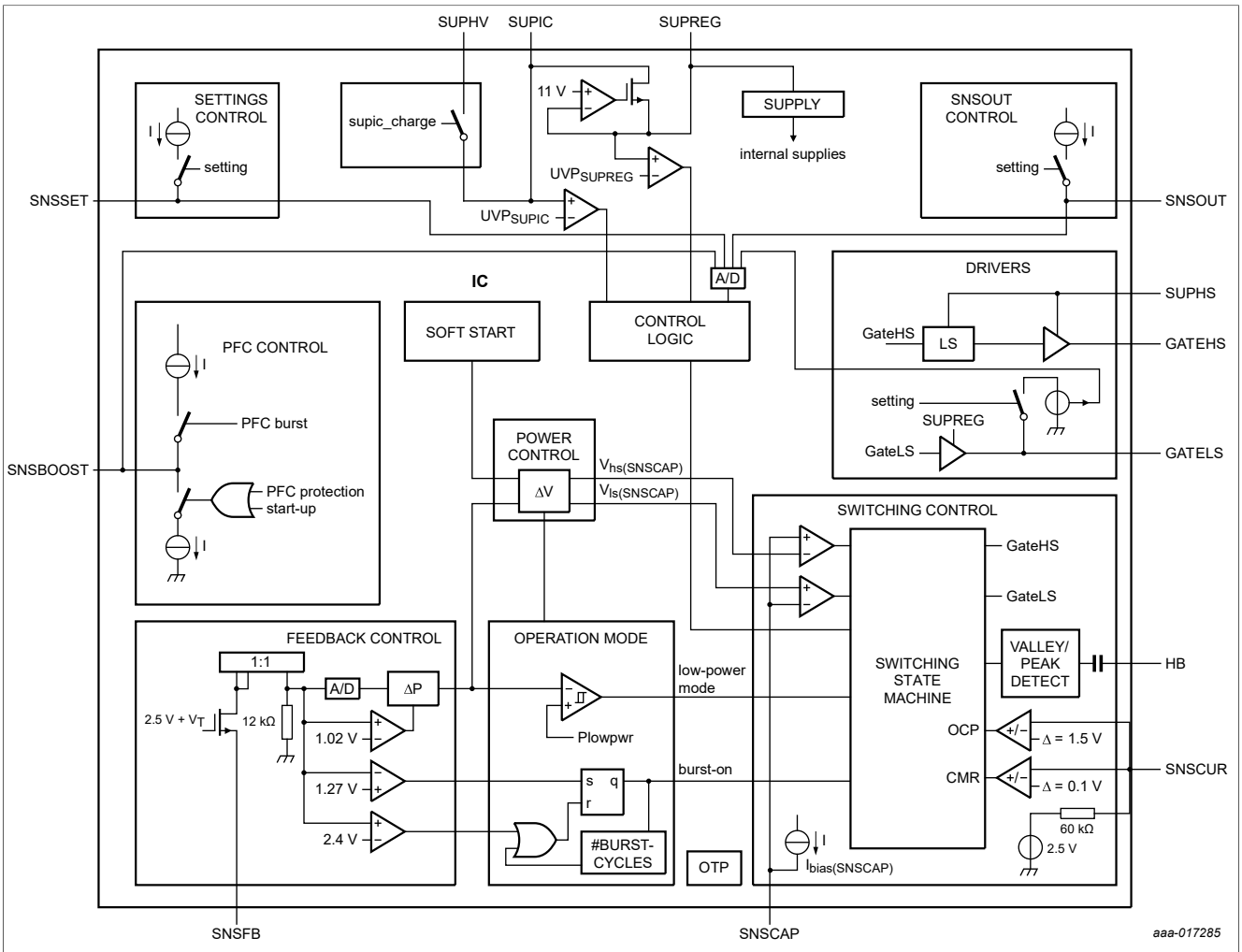


Figure 1. Block diagram

7 Pinning information

7.1 Pinning

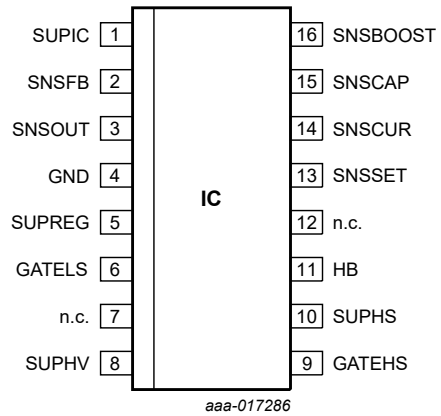


Figure 2. TEA19161T pin configuration (SOT109-1)

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
SUPIC	1	input supply voltage and output of internal HV start-up source; externally connected to an auxiliary winding of the LLC via a diode or to an external DC supply
SNSFB	2	output voltage regulation feedback sense input; externally connected to an optocoupler
SNSOUT	3	sense input for setting the burst frequency and monitoring the LLC output voltage; externally via a resistive divider and a diode connected to the auxiliary winding
GND	4	ground
SUPREG	5	regulated SUPREG IC supply; internal regulator output; input for drivers; externally connected to SUPREG buffer capacitor
GATELS	6	LLC low-side MOSFET gate driver output
n.c.	7	not connected
SUPHV	8	internal HV start-up source high-voltage supply input; externally connected to (PFC) boost voltage
GATEHS	9	LLC high-side MOSFET gate driver output
SUPHS	10	high-side driver supply input; externally connected to bootstrap capacitor (C_{SUPHS})
HB	11	low-level reference for high-side driver and input for half-bridge slope detection; externally connected to half-bridge node HB between the LLC MOSFETs
n.c.	12	not connected

Table 3. Pin description...*continued*

Symbol	Pin	Description
SNSSET	13	settings for transition levels high/low power mode and low-power/burst mode, overpower level,overpower time-out, and restart or latched. Output of the power good signal.
SNSCUR	14	LLC current sense input; externally connected to the resonant current sense resistor
SNSCAP	15	LLC capacitor voltage sense input; externally connected to divider across LLC capacitor
SNSBOOST	16	sense input for boost voltage; output for PFC burst control; externally connected to resistive divided boost voltage

8 Functional description

8.1 Supply voltages

The TEA19161T includes:

- A high-voltage supply pin for start-up (SUPHV)
- A general supply to be connected to an external auxiliary winding (SUPIC pin)
- An accurate regulated voltage (SUPREG pin)
- A floating supply for the high-side driver (SUPHS pin)

8.1.1 Start-up and supply voltage

Initially, the capacitors on the SUPIC and SUPREG pins are charged via the SUPHV pin. The SUPHV pin is connected to the output voltage of a PFC via an external resistor. Internally, a high-voltage series switch is located between the SUPHV and SUPIC pins. From the SUPIC pin, the SUPREG pin is supplied using a linear regulator (see Figure 3).

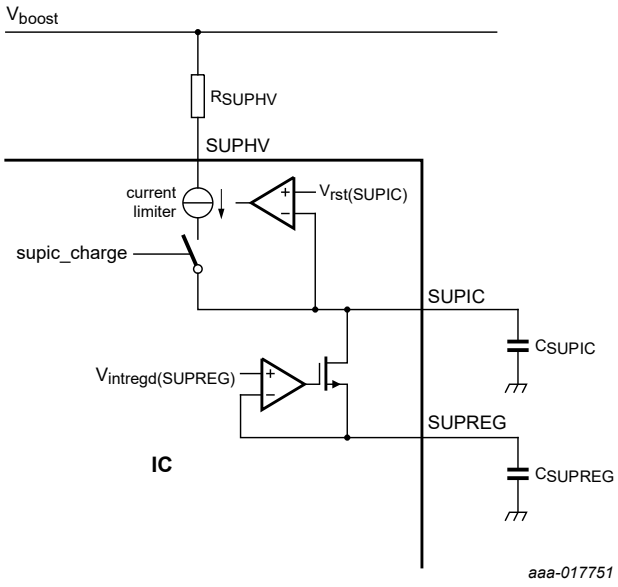


Figure 3. HV start-up

Initially, when the voltage on the SUPIC pin is below the reset level $V_{rstSUPIC)}$ (3.5 V), the SUPIC charge current is internally limited to $I_{lim(SUPHV)}$ (0.75 mA). In this way, the dissipation is limited when SUPIC is shorted to ground. When the voltage on the SUPIC pin exceeds $V_{rst(SUPIC)}$, the internal switch is closed.

To limit the IC power dissipation, an external resistor (R_{SUPHV}) is required to reduce the voltage drop between the SUPHV and SUPIC pins when charging the SUPIC capacitor. R_{SUPHV} must be dimensioned such that the maximum current is limited to below limiting value I_{SUPHV} (20 mA) and it can handle the required power dissipation. The maximum power dissipation of the external resistor can be reduced by using several resistors in series.

When the SUPIC reaches the $V_{start(SUPIC)}$ level (19.1 V), it is continuously regulated to this start level with a hysteresis ($V_{start(hys)SUPIC}$; −0.7 V). It activates the switch between the SUPHV and SUPIC pins when the SUPIC voltage drops to below $V_{start(SUPIC)} + V_{start(hys)SUPIC}$. It deactivates the switch when it exceeds $V_{start(SUPIC)}$. When start-up is complete and the LLC controller is operating, the LLC transformer auxiliary winding supplies the SUPIC pin. In this operational state, the HV start-up source is disabled (see Figure 4).

When the system enters the protection mode, the SUPIC pin is also regulated to the start level. During the non-switching period of the burst mode, the system also activates the switch between the SUPHV and SUPIC pins when the SUPIC voltage drops below $V_{low(SUPIC)}$. It regulates the voltage with a hysteresis of $V_{low(hys)SUPIC}$. In this way, the system avoids that the SUPIC undervoltage protection ($V_{uvp(SUPIC)}$) is triggered because of a long non-switching period in burst mode.

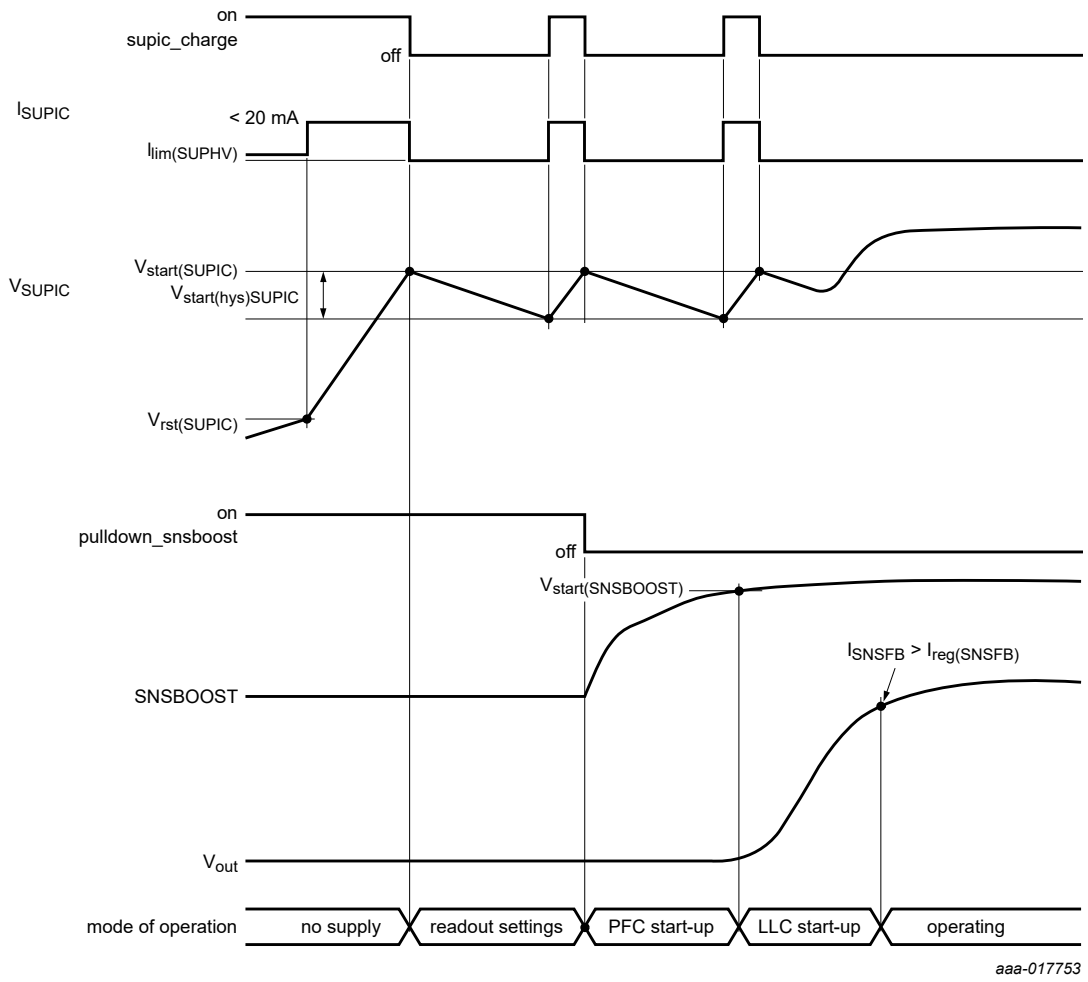


Figure 4. Start-up sequence and normal operation

8.1.2 Regulated supply (SUPREG pin)

The voltage range on the SUPIC pin exceeds that of the maximum external MOSFETs gate-source voltage. So, the TEA19161T incorporates an integrated series stabilizer. The series stabilizer creates an accurate regulated voltage ($V_{intregd(SUPREG)}$ = 11 V) at the buffer capacitor C_{SUPREG}. The stabilized voltage is used to:

- Supply the internal low-side LLC driver
- Supply the internal high-side driver using external components
- As a reference voltage for optional external circuits

To ensure that the external MOSFETs receive sufficient gate drive, the voltage on the SUPREG pin must reach $V_{uvp(SUPREG)}$ before the system starts switching. If the SUPREG voltage drops to below this undervoltage protection level, the system restarts.

8.1.3 High-side driver floating supply (SUPHS pin)

External bootstrap buffer capacitor C_{SUPHS} supplies the high-side driver. The bootstrap capacitor is connected between the high-side driver supply, the SUPHS pin, and the half-bridge node, HB. C_{SUPHS} is charged from the SUPREG pin using an external diode D_{SUPHS} (see Figure 27).

Careful selection of the appropriate diode minimizes the voltage drop between the SUPREG and SUPHS pins, especially when large MOSFETs and high switching frequencies are used. A large voltage drop across the diode reduces the gate drive of the high-side MOSFET.

8.2 System start-up

Figure 5 shows the flow diagram corresponding with Figure 4.

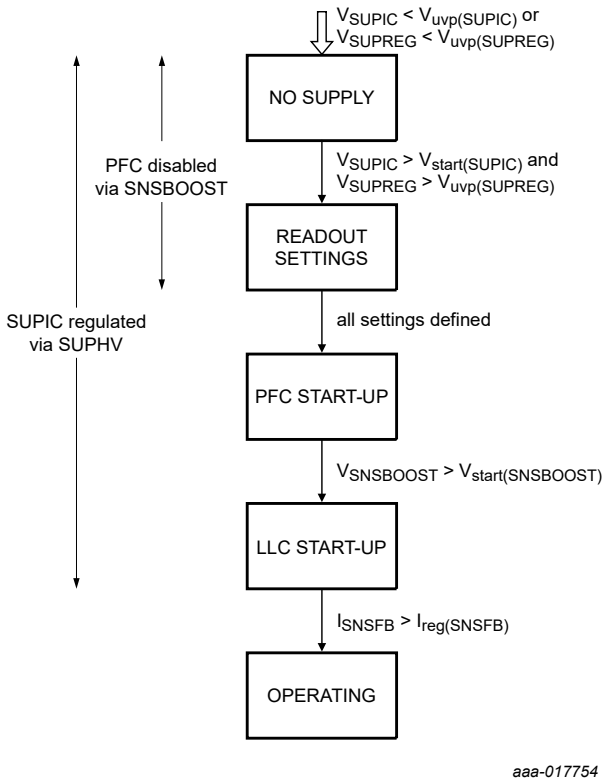


Figure 5. LLC controller flow diagram

When the SUPIC or SUPREG pins drop to below their stop levels, the TEA19161T enters the no supply state. It recharges the SUPIC and SUPREG pins to their start levels via the SUPHV pin. When the start levels are reached, measuring the external resistances on the SNSSET, SNSOUT, and GATELS pins initializes the settings.

During the no supply and readout settings states, the SNSBOOST pin is pulled low, disabling the TEA19162T PFC. When the settings have been defined, the SNSBOOST pin is released and the PFC starts up. When the SNSBOOST reaches the minimum level $V_{start(SNSBOOST)}$, the LLC starts switching.

When a small optocurrent is detected ($I_{SNSFB} < I_{reg(SNSFB)}$), the output voltage is close to its regulation level. As the SUPIC pin must then be supplied via the primary auxiliary winding, charging via the SUPHV is disabled.

8.3 LLC system regulation

A typical resonant controller regulates the output power by adapting the operating frequency.

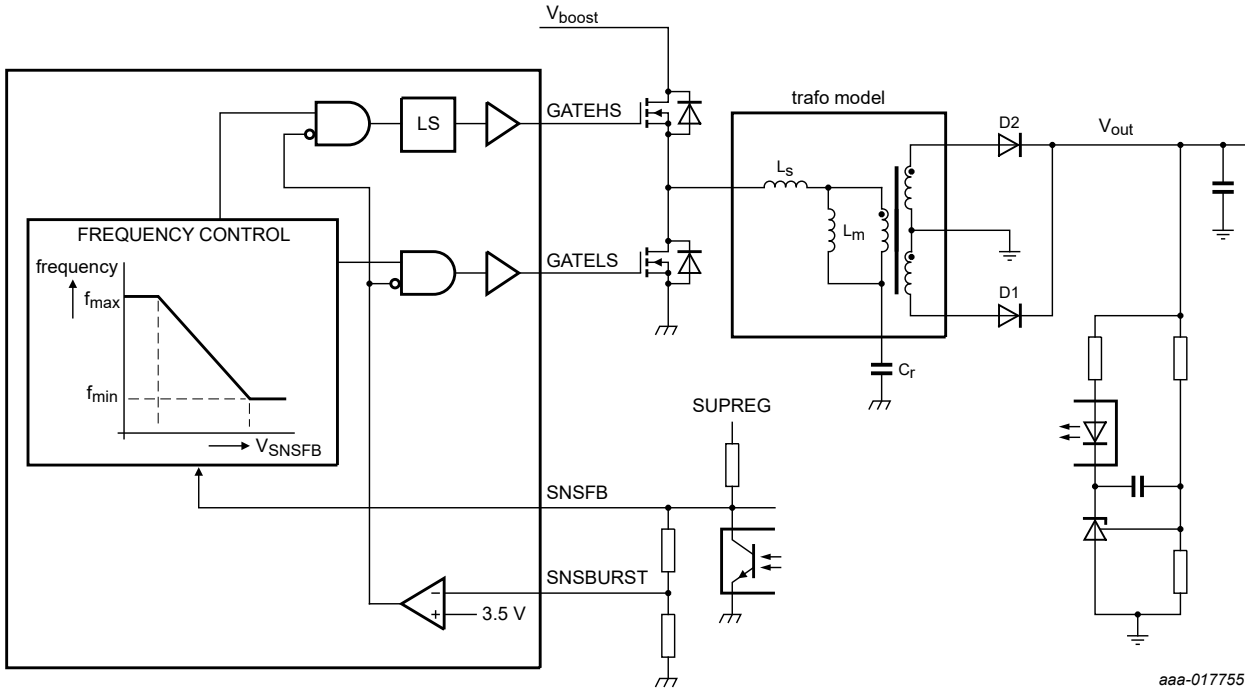


Figure 6. Resonant frequency controller

If the power drops and so the voltage of the LLC converter exceeds the targeted regulation level (12 V or 19.5 V typical), the optocurrent increases and the voltage at the SNSFB decreases (see Figure 6). The resonant controller then increases the frequency according to its internal frequency control curve. Because of the higher frequency, the power to the output is reduced and the output voltage drops. If the output voltage becomes too low, the controller lowers the system frequency, increasing the output power. In this way, the system regulates the output power to the required level.

As a small change in frequency gives a significant change in output power, frequency control has a high gain of the control loop. To increase the efficiency at low loads, most converters switch to burst mode as soon as the output power is below a minimum level.

The burst mode level is mostly derived from the voltage on the SNSFB pin. For a frequency controlled resonant converter, it implies that the burst mode is entered at a certain frequency instead of at a certain load. A small variation of the resonant components then results in a significant variation in power level at which the burst mode is activated.

In the TEA19161T, the control mechanism is different. The advantage is a constant gain of the control loop and a burst mode which is derived from the output power. The TEA19161T does not regulate the output power by adjusting the frequency but by the voltage across the primary capacitor.

The input power (related to the output power) of a resonant converter can be calculated with Equation 1:

$$P_{in} = V_{boost} \times I_{boost} = V_{boost} \times \Delta V_{Cr} \times C_r \times f_{sw} \quad (1)$$

Equation 1 shows that the input power has a linear relationship with the capacitor voltage difference ΔV_{Cr}.

Figure 7 shows an alternative explanation of the linear relationship between the input power and the energy stored in the resonant capacitor.

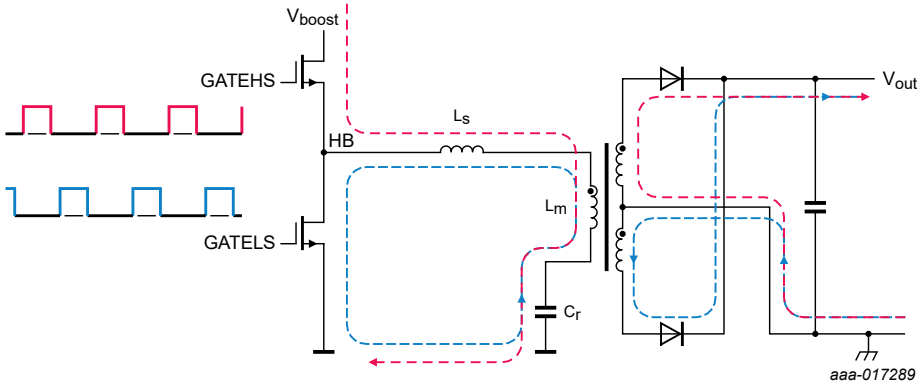


Figure 7. Linear relationship between input power and energy stored in C_r

When the high-side switch is on, a primary current is flowing through the transformer and resonant capacitor C_r as indicated by the red line. Half the energy the input delivers is transferred to the output. The other half charges resonant capacitor C_r. The voltage across the resonant capacitor increases.

When the high-side switch is off and the low-side switch is on, the energy which is stored in resonant capacitor C_r is transferred to the output and its voltage decreases. In this way, the linear relationship between the increase of the resonant capacitor voltage and the output power can be seen.

Although the TEA19161T uses the primary capacitor voltage as a regulation parameter, all application values, like the resonant inductances, resonant capacitor, and primary MOSFETs remain unchanged compared to a frequency controlled LLC converter. A secondary TL431 circuitry in combination with an optocoupler connected to the primary SNSFB pin continuously regulates the output voltage.

8.3.1 Output power regulation loop

Figure 8 shows the output power regulation loop of V_{cap} control as used by the TEA19161T. Figure 9 shows a corresponding timing diagram.

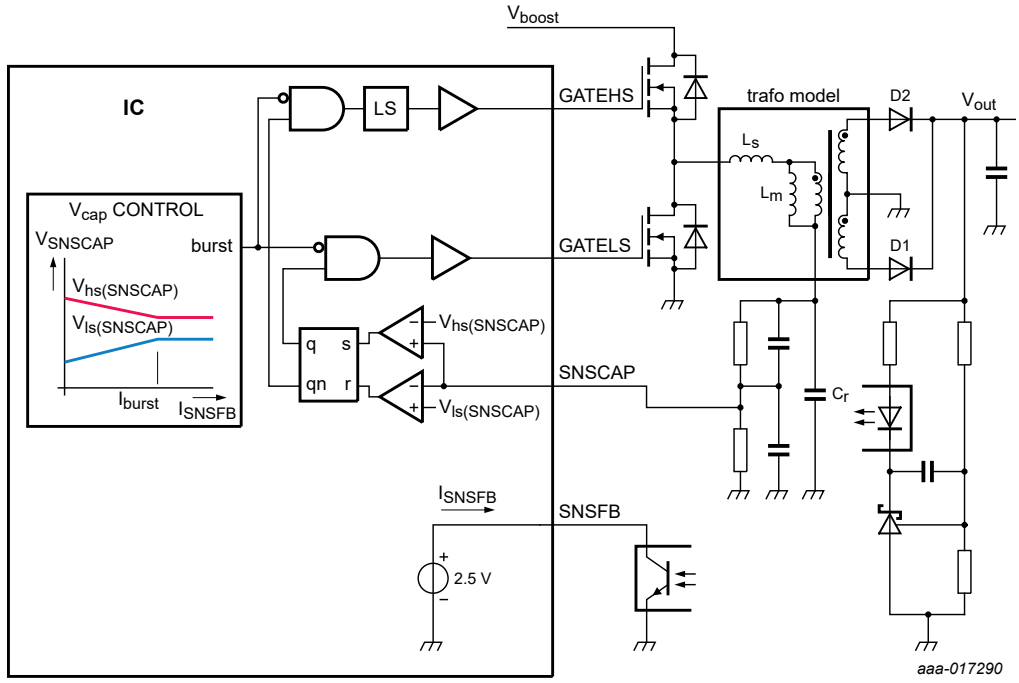


Figure 8. Regulation loop V_{cap} control

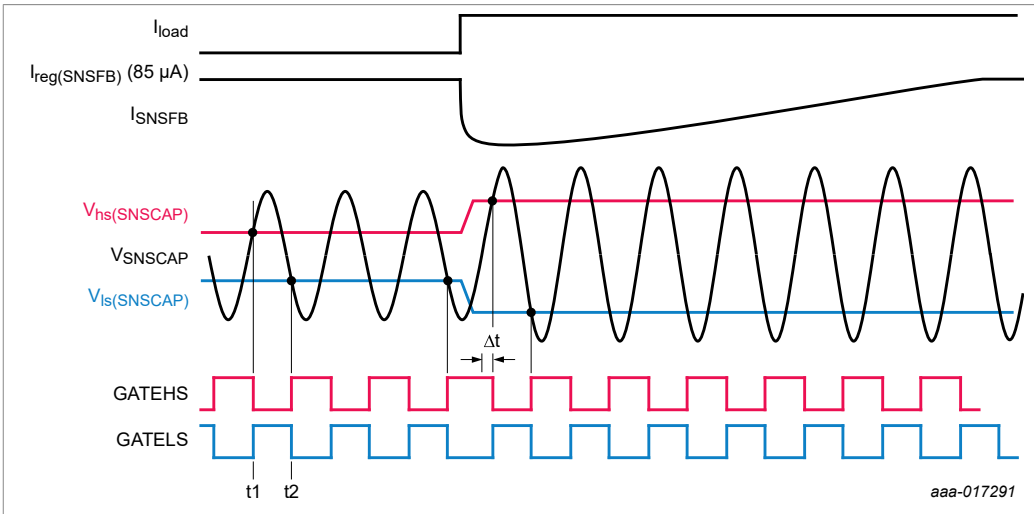


Figure 9. Timing diagram of the regulation loop

When the divided resonant capacitor voltage (V_{SNSCAP}) exceeds the capacitor voltage high level ($V_{hs(SNSCAP)}$), the high-side MOSFET is switched off (see Figure 9 (t1). After a short delay, the low-side MOSFET is switched on. Because of the resonant current, the resonant capacitor voltage initially increases further but eventually drops.

When the divided capacitor voltage (V_{SNSCAP}) drops to below the capacitor voltage low level ($V_{ls(SNSCAP)}$), the low-side MOSFET is switched off (see Figure 9 (t2)). After a short delay, the high-side MOSFET is switched on. Figure 9 shows that the switching frequency is a result of this switching behavior. In a frequency controlled system, the frequency is a control parameter and the output power is a result. The TEA19161T regulates the power and the frequency is a result.

The difference between the high and low capacitor voltage level is a measure of the delivered output power. The value of the primary optocurrent, defined by the secondary TL431 circuitry, determines the difference between the high and low capacitor voltages.

Figure 9 also shows the behavior at a transient. If the output load increases, the current pulled out of the SNSFB pin decreases. The result is that the TEA19161T increases the high-level capacitor voltage and lowers the low-level capacitor voltage. According to Equation 1 in Section 8.3, the output power increases and eventually the output voltage increases to its regulation level.

To minimize no-load input power of the system, the primary current into the optocoupler is continuously regulated to 85 µA (see Section 8.5).

8.3.2 Output voltage start-up

The system controls the output power by regulating the primary V_{Cr} (see Section 8.3). When the system is in regulation and the output voltage is stabilized, a small change in ΔV_{Cr} corresponds to a small change in the output current (see Equation 2).

$$P_{out} = V_{out} \times I_{out} \sim V_{boost} \times I_{boost} = \Delta V_{Cr} \times C_r \times f_{sw} \times V_{boost}$$
$$I_{out} \approx C_r \times f_{sw} \times V_{boost} \times \frac{\Delta V_{Cr}}{V_{out}} \quad (2)$$

However, before start-up, when the output voltage is around zero, a small capacitor voltage increase (ΔV_{Cr}) corresponds to a substantial output current increase. So, at start-up, the divided ΔV_{Cr} voltage (ΔV_{SNSCAP}) is slowly increased from a minimum value to the regulation level. As a result, the system starts up at a higher frequency. The GATELS resistor sets the starting value of the ΔV_{SNSCAP}.

8.4 Modes of operation

Figure 10 shows the control curve between the output power and the voltage difference between the high and low capacitor voltage levels.

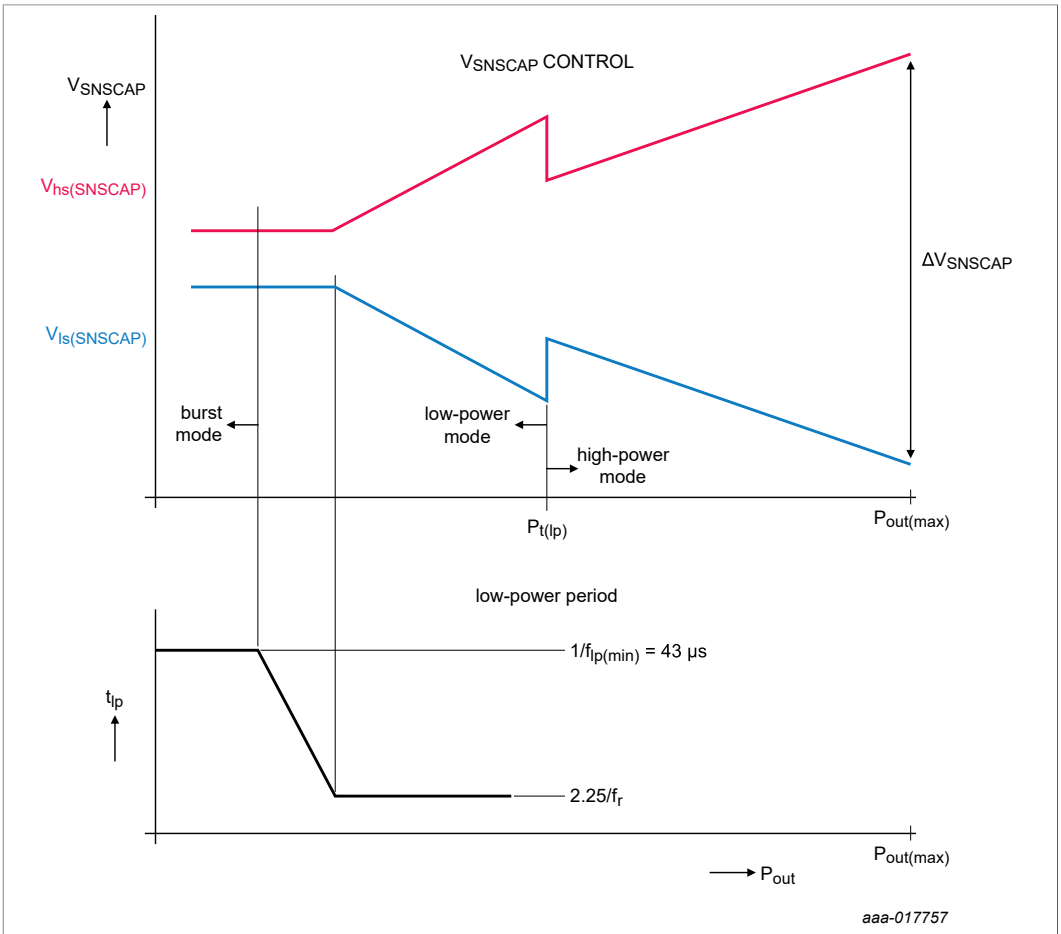


Figure 10. TEA19161T control curve

When the output power (P_{out}) is at its maximum, the low capacitor voltage level ($V_{ls(SNSCAP)}$) is at its minimum and the high capacitor voltage ($V_{hs(SNSCAP)}$) is at its maximum level. According to Equation 1, the maximum ΔV_{SNSCAP} ($V_{hs(SNSCAP)} - V_{ls(SNSCAP)}$), which is the divided ΔV_{Cr} voltage, corresponds to the maximum output power.

When the output load decreases, the ΔV_{SNSCAP} voltage decreases. As a result, the output power decreases and the output voltage is regulated. This mode is called high-power mode.

When the output power drops to below the transition level ($P_{t(lp)}$), the system enters the low-power mode. External components can set the applied $P_{t(lp)}$ level (see Section 8.7.3).

To compensate for the hold period, ΔV_{SNSCAP} is initially increased at entering the low-power mode (see Section 8.4.2). In low-power mode, the output power is initially regulated by adapting ΔV_{SNSCAP}, until it reaches a minimum. Then, the output power is regulated by lowering the duty cycle of the low-power mode with a fixed ΔV_{SNSCAP} until the period time of a low-power cycle reaches a maximum ($1 / f_{lp(min)}$). The system enters the burst mode (see Section 8.4.3).

8.4.1 High-power mode

In high-power mode, the system operates as described in Section 8.3.1. Figure 11 shows a flow diagram of the high-power mode.

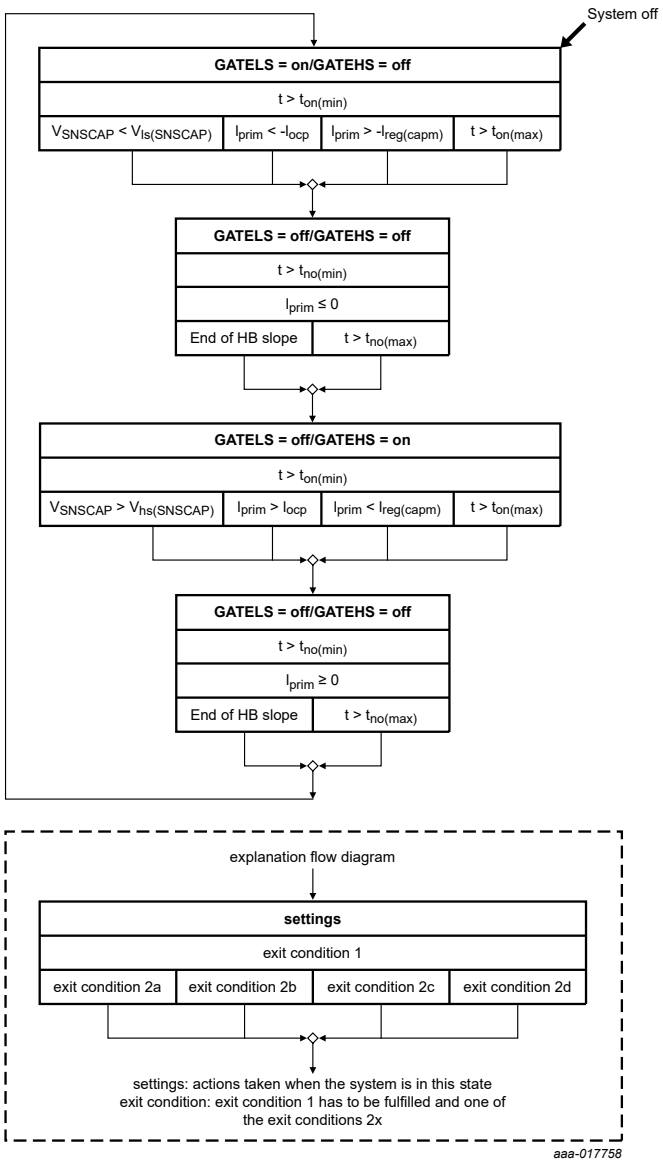


Figure 11. High-power mode flow diagram

When the system is off, GATELS is on and GATEHS is off. The external bootstrap buffer capacitor (C_{SUPHS}) is charged via the SUPREG pin and an external diode. The system remains in this state for at least the minimum on-time ($t_{on(min)}$) of GATELS. Before entering the next state, one of the following conditions must be fulfilled:

- The V_{SNSCAP} voltage drops to below the minimum V_{SNSCAP} voltage ($V_{ls(SNSCAP)}$)
- The measured current exceeds the OCP level (see Section 8.6.6)
- The system is close to capacitive mode (see Section 8.6.5)
- The maximum on-time ($t_{on(max)}$), a protection that maximizes the time the high-side or low-side MOSFET is kept on, is exceeded.

In the next state, to avoid false detection of the HB peak voltage, the system waits until the minimum non-overlap time ($t_{no(min)}$) is exceeded. When it is exceeded, the system starts to detect the end (= peak voltage) of the HB node. When it detects the peak of the HB node and the measured resonant current is negative (or zero), it enters the next state.

If the system does not detect a peak at the HB node, it also enters the next state when the maximum non-overlap time ($t_{no(max)}$) is exceeded under the condition of a negative (or zero) resonant current.

Finally, the third and fourth states (see Figure 11) describe the GATEHS and GATEHS to GATELS transition criteria which are the inverse of the first two states.

8.4.2 Low-power mode

At low loads, the operating frequency of a resonant converter increases. As a result, the magnetization and switching losses increase. For this reason, the efficiency of a resonant converter drops at low loads. A newly introduced low-power mode ensures high efficiency at lower loads as well.

When the output power drops to below the $P_{t(lp)}$ level, the system enters the low-power mode (see Figure 10 and Figure 12). It continues switching for 3 half-cycles (low-side, high-side, low-side) with a fixed duty cycle of 67 %. To ensure a constant output power level, it increases the energy per cycle ($V_{hs(SNSCAP)} - V_{ls(SNSCAP)}$) at the same time. So 1/3 of the time the converter is in a "hold" period. The result is a 33 % magnetization and switching losses reduction.

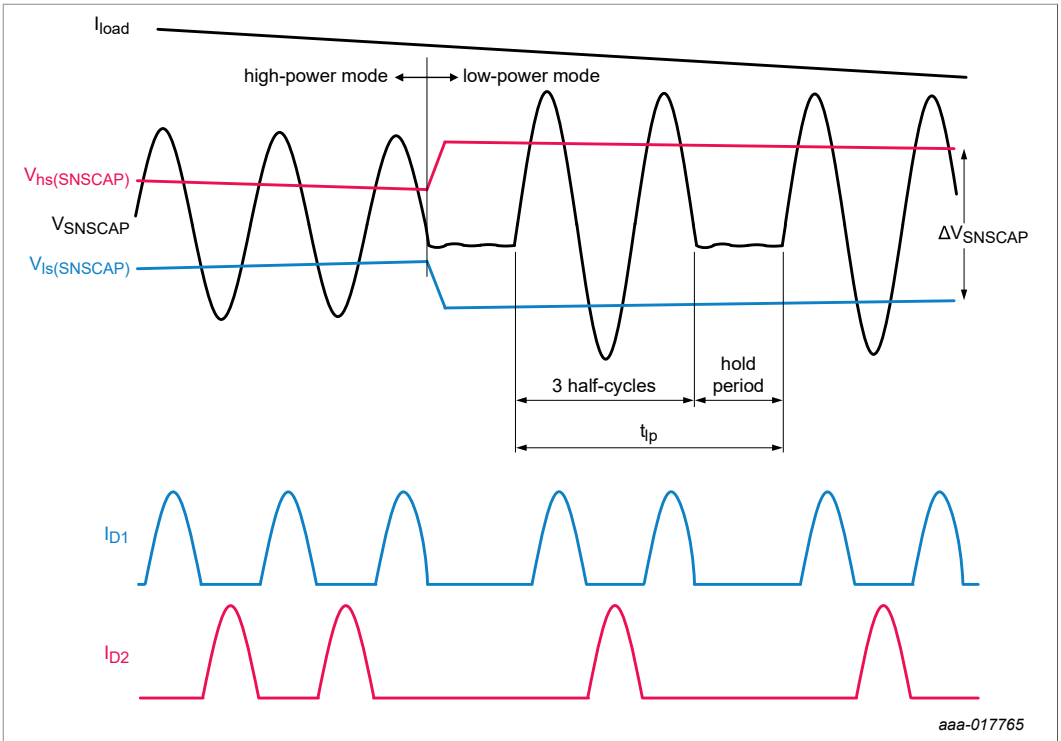


Figure 12. Timing diagram transition high-power to low-power mode

As the system continuously tracks the primary capacitor voltage, it knows exactly when to enter the "hold" period. It can also continue again at exactly the correct voltage and current levels of the resonant converter. In this way, a "hold" period can be introduced which reduces the magnetization and switching losses without any additional losses. The currents I_{D1} and I_{D2} (see Figure 12) are the secondary currents through diodes D1 and D2 (see Figure 27).

When in the low-power mode the output power is further reduced, the amount of energy per cycle (= ΔV_{SNSCAP}) is reduced and the duty cycle remains the same (see Figure 13).

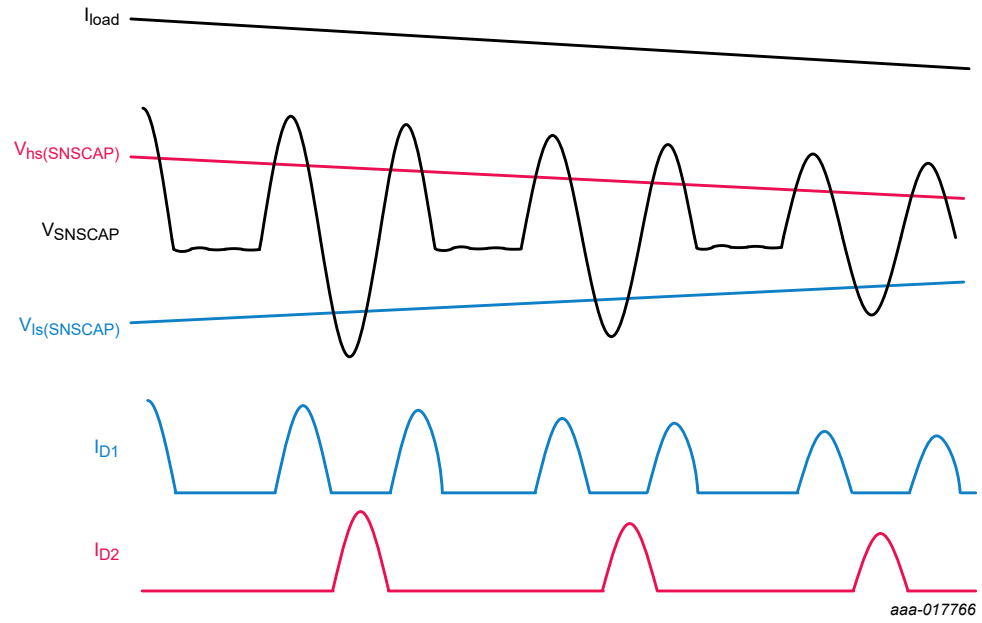


Figure 13. Low-power mode: Lowering the energy-per-cycle (ΔV_{SNCAP})

When, in low-power mode, the minimum energy per cycle is reached, the duty cycle regulates the output power (see Figure 14). Increasing the "hold" period lowers the duty cycle.

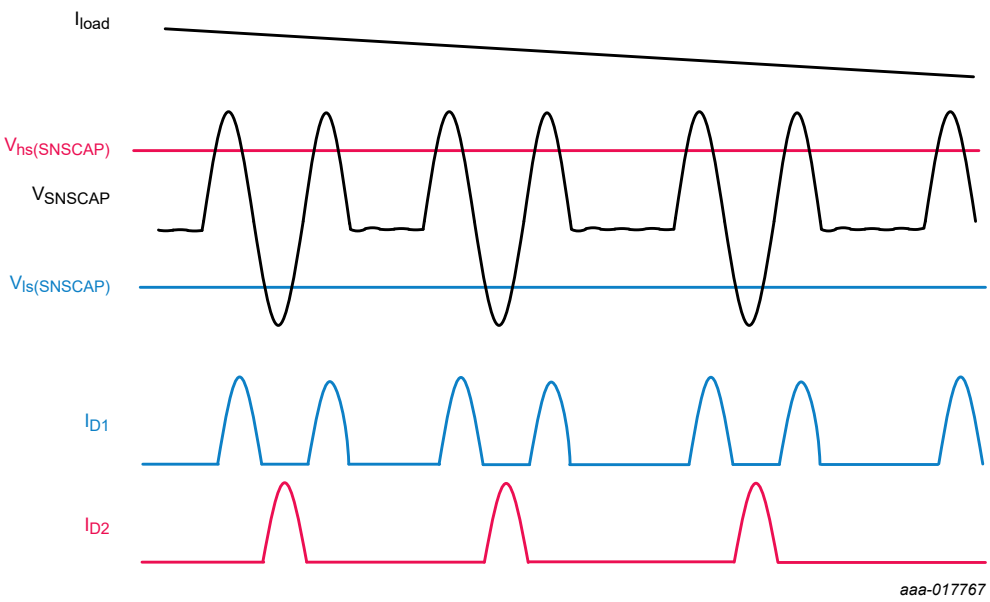


Figure 14. Low-power mode: lowering the duty cycle

To avoid audible noise, the system reduces the duty cycle until the frequency reaches $f_{lp(min)}$ (23 kHz). If the output power is lowered further, the system enters the burst mode.

8.4.3 Burst mode

In burst mode, the system alternates between operating in low-power mode and an extended hold state (see Figure 15). Because of this additional extended hold period, the magnetization and switching losses are further reduced. So, the efficiency of the system is increased.

Figure 15 shows that all operating frequencies are outside the audible area. The minimum low-power frequency is 23 kHz. Within a low-power period, the system is switching at the resonant frequency of the converter, which is typically between 50 kHz and 200 kHz.

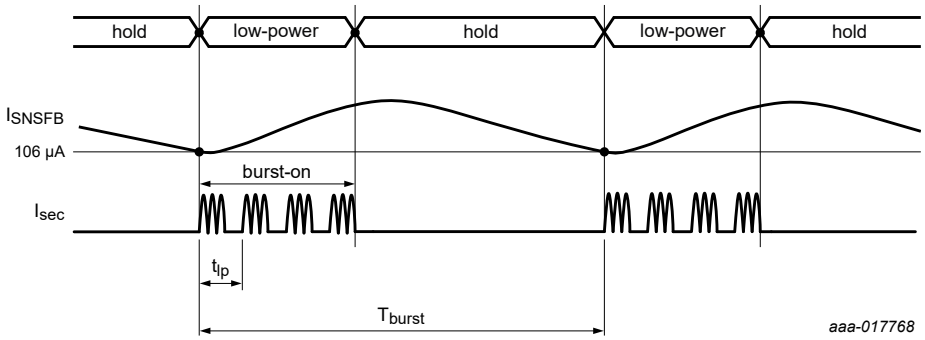


Figure 15. Burst mode

The burst frequency (1 / t_{burst}) is continuously regulated to a predefined value, which can be set externally to 200 Hz, 400 Hz, 800 Hz or 1600 Hz. I_{sec} is the secondary current flowing through either diode D1 or D2 (see Figure 27).

When the primary optocurrent (I_{SNSFB}) drops to below 106 µA, a new burst-on period is started. The end of the burst-on period depends on the calculated number of low-power cycles. The number of low-power cycles within a burst-on is continuously adjusted so that the burst period is at least the period defined by the setting (see Figure 16).

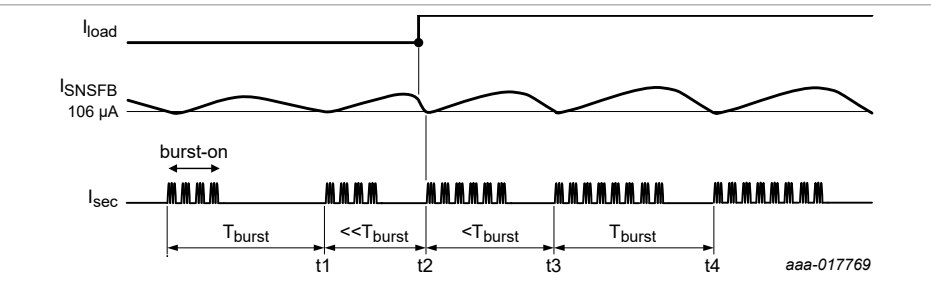


Figure 16. Burst mode: Regulating the number of low-power cycles

The system continuously measures the burst period from the start of the previous burst-on period to a new burst-on period. At t1, the measured burst period (t_{burst}) equals the required T_{burst}. So, the next number of low-power cycles equals the number of previous low-power cycles. At a constant output power, the system expects that when the next burst-on period has the same number of low-power cycles as the previous burst-on period, the burst period (t_{burst}) remains constant.

At a positive transient (t2), a new low-power cycle is started immediately to minimize the drop in output voltage. The measured time period, at time t2, is below the targeted burst period. The system increases the number of burst cycles. At t3, it measures the burst

period again. In this example, the burst period is still below the targeted burst period. So, the system increases the number of low-power cycles again and again until the measured burst period equals the target burst period, which occurs at t4.

8.5 Optobias regulation

In a typical application, the output voltage is sensed using a TL431 and connected to the SNSFB pin of the TEA19161T via an optocoupler (see Figure 27). Because of the behavior of the TL431, the current through the optocoupler is at the maximum level when the output power is at the minimum level. It is therefore one of the most critical parameters to achieve the required no-load input power. To achieve maximum efficiency at low load/no-load, the TEA19161T continuously regulates the optocurrent to a low level that is independent of the output load.

A very low optocurrent reduces the transient response of the system, because of the parasitic capacitance at the optocoupler collector. So, the TEA19161T applies a fixed voltage at the SNSFB pin. It measures the current through the optocoupler which defines the required output power. Via an additional internal circuitry, which adds an offset to the required output power, the optocurrent is continuously (slowly) regulated to the $I_{reg(SNSFB)}$ level (= 85 µA). This level is independent of the output power.

At a positive load transient, the optocurrent initially decreases (see Figure 9; I_{SNSFB}). The TEA19161T immediately increases the ΔV_{SNSCAP} which again increases the output power.

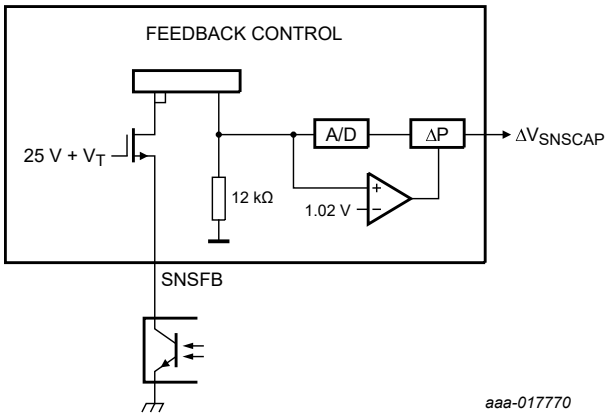


Figure 17. Optobias regulation

Figure 17 shows that when the optocurrent decreases, the internal voltage across the 12 kΩ resistor drops to below the targeted level of 1020 mV (= 85 µA × 12 kΩ). The TEA19161T then slowly increases an additional offset at the power level (ΔP). It continues to increase the additional offset until the optocurrent reaches the target of 85 µA. At a negative transient, the additional offset to the power level is decreased. As a result, the output voltage increases which again increases the optocurrent. In this way, the optocurrent is continuously regulated to the $I_{reg(SNSFB)}$ level (see Figure 9).

The behavior of the internal circuitry connected to the SNSFB pin is the same as the behavior of the traditional circuitry. The fixed voltage at the SNSFB pin and the continuous regulation of the optocurrent level does not influence the regulation level. The advantage, however, is a reduction in no-load input power and an optimization of the transient response.

When the system operates in low-power mode at the minimum energy per cycle and at minimum duty cycle, it can no longer reduce the optocurrent level to the $I_{reg(SNSFB)}$ target (» 85 µA). If the output power decreases further and the optocurrent increases to above the level of $I_{start(burst)}$ (» 106 µA), the burst mode is triggered. When the output power drops to below this level again, a new burst cycle is started (see Figure 15 and Figure 16).

8.6 Protections

Table 4 gives an overview of the available protections.

Table 4. Protections overview

Protection	Description	Action	PFC
UVP SUPIC/ SUPREG	undervoltage protection SUPIC/ SUPREG pins	LLC = off; recharge via SUPHV; restart when $V_{SUPIC} > V_{start(SUPIC)}$ and $V_{SUPREG} > V_{start(SUPREG)}$	off
UVP SUPHS	undervoltage protection SUPHS pin	GATEHS = off	
UVP SNSBOOST	undervoltage protection boost	LLC = off; restart when $V_{SNSBOOST} > V_{start(SNSBOOST)}$	
OVP output	overvoltage protection output	latched after 5 consecutive cycles [1] [2]	off
CMR	capacitive mode regulation	system ensures that mode of operation is inductive	
OCP	overcurrent protection	switch off cycle-by-cycle; After 5 consecutive cycles, it follows the OPP setting. [2]	off
OTP	overtemperature protection	latched Latched implies that the system only restarts after a mains disconnection.	off
OPP	overpower protection	latched Latched implies that the system only restarts after a mains disconnection. /safe restart [3]	off

[1] Can be longer due to the sharing of the internal ADC converter.
[2] Latched implies that the system only restarts after a mains disconnection.
[3] Can be set by external components.

When the system is in a latched or safe restart protection, the SUPIC voltage is regulated to its start level via the SUPHV pin.

8.6.1 Undervoltage protection SUPIC/SUPREG

When the voltage on the SUPIC pin or the SUPREG pin is below its undervoltage level $V_{uvp(SUPIC)}$ / $V_{uvp(SUPREG)}$, the LLC converter stops switching. The capacitors at the SUPIC and SUPREG pins are recharged via the SUPHV pin (see Figure 5). The SNSBOOST pin is pulled low, disabling the PFC. When the supply voltages exceed their start levels, the system restarts.

8.6.2 Undervoltage protection SUPHS

To ensure a minimum drive voltage at the high-side driver output (GATEHS), this driver is kept off when its voltage is below the minimum level ($V_{SUPHS} < V_{rst(SUPHS)}$).

8.6.3 Undervoltage protection boost

The PFC output voltage is measured via a resistive divider connected to the SNSBOOST pin. The voltage at the SNSBOOST pin must exceed the start level ($V_{SNSBOOST} > V_{start(SNSBOOST)}$) before the system is allowed to start switching.

When the system is operating and the voltage at the SNSBOOST pin drops to below the minimum level ($V_{SNSBOOST} < V_{uvp(SNSBOOST)}$), the LLC converter stops switching. When it exceeds the start level, it restarts.

8.6.4 Overvoltage protection

When the voltage at the SNSOUT pin exceeds the $V_{ovp(SNSOUT)}$ level for at least 5 consecutive switching cycles, the OVP protection is triggered. The voltage at the SNSOUT pin is internally measured via an ADC converter. As the same ADC converter toggles between measuring the SNSOUT and SNSBOOST pins (see Figure 1), there is an additional delay before the OVP is triggered. OVP is a latched protection. The PFC is disabled via the SNSBOOST pin.

8.6.5 Capacitive mode regulation (CMR)

The TEA19161T has a Capacitive Mode Regulation (CMR) which ensures that the system is always operating in inductive mode and avoids operation in capacitive mode.

At lower input voltage or higher output power and depending on the resonant design, the resonant current can already approach zero before the capacitor voltage reaches the regulation level.

When the resonant current has changed polarity before the switches are turned off and the other switch is turned on, hard switching occurs. This event is called capacitive mode. To avoid that the system operates in capacitive mode, the system also switches off the high-side/low-side switch when the resonant current approaches zero.

Figure 18 shows the signals that occur when a resonant converter is switching in CMR mode. At t1 (and also at t3), the low-side switch is on while the resonant current approaches zero before V_{SNSCAP} reaches $V_{ls(SNSCAP)}$. At t2, the resonant current is also close to changing polarity while the divided capacitor voltage (V_{SNSCAP}) has not reached the $V_{hs(SNSCAP)}$ level yet. To avoid a turn-off of the high-side switch at a negative current or the low-side at a positive current, the system also turns off the high-side/low-side switch when the primary current approaches zero. So at t2, the high-side switch is turned off because the primary current is close to zero. At t_3 (and also at t_1), the low-side switch is turned off, although V_{SNSCAP} did not reach the regulation level ($V_{ls(SNSCAP)}$) yet. The

primary current is measured via an external sense resistor connected to the SNSCUR pin. The capacitive mode protection levels are $V_{reg(capm)}$ (−100 mV and +100 mV, respectively).

In this mode, the amount of output power is reduced and the output voltage decreases.

The TEA19161T does not enter a so-called "capacitive mode protection", but avoids this mode of operation.

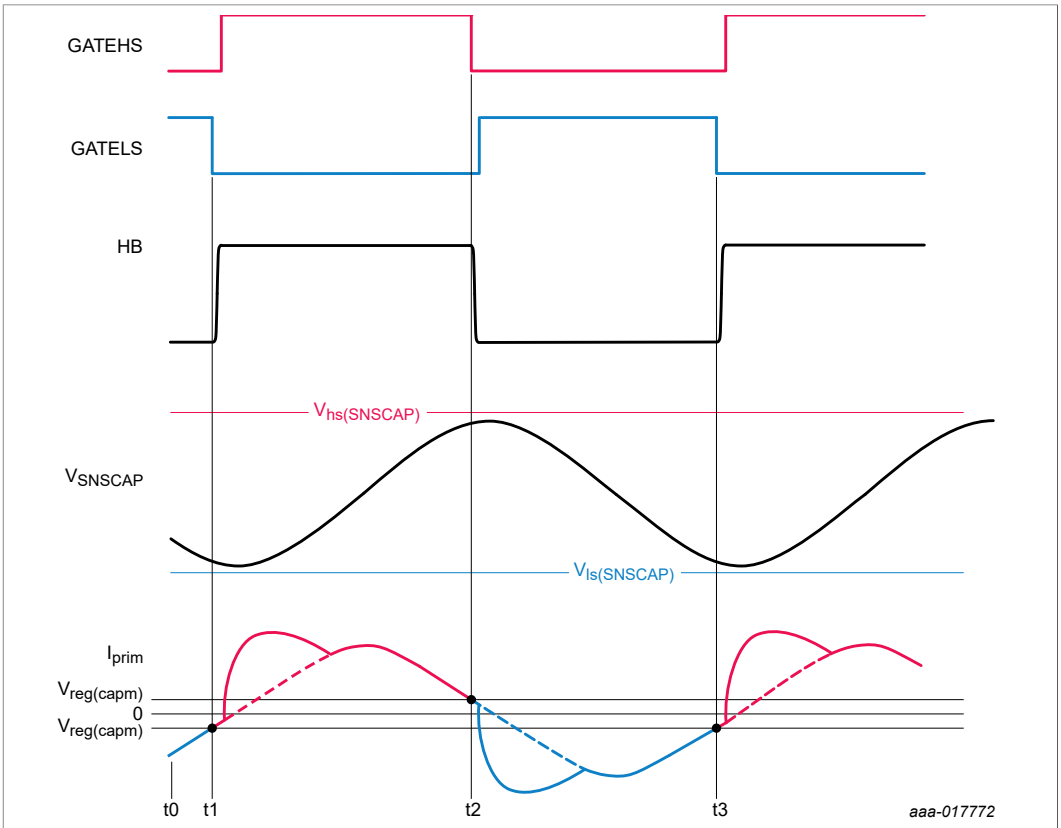


Figure 18. Near capacitive mode switching

8.6.6 Overcurrent protection

The system measures the primary current continuously via a sense resistor connected to the SNSCUR pin. If the measured voltage exceeds the overcurrent level (V_{ocp}), the corresponding switch (GATELS/GATEHS) is turned off, but the system continuous switching. In this way, the primary current is limited to the OCP level. If the OCP level is exceeded for 5 consecutive cycles (GATELS and/or GATEHS), the system stops switching and enters the latched OCP protection mode. The PFC is disabled via the SNSBOOST pin.

8.6.7 Overtemperature protection

When the internal junction temperature exceeds the T_{otp} level, the overtemperature protection is triggered. OTP is a latched protection which also disables the PFC.

8.6.8 Overpower protection

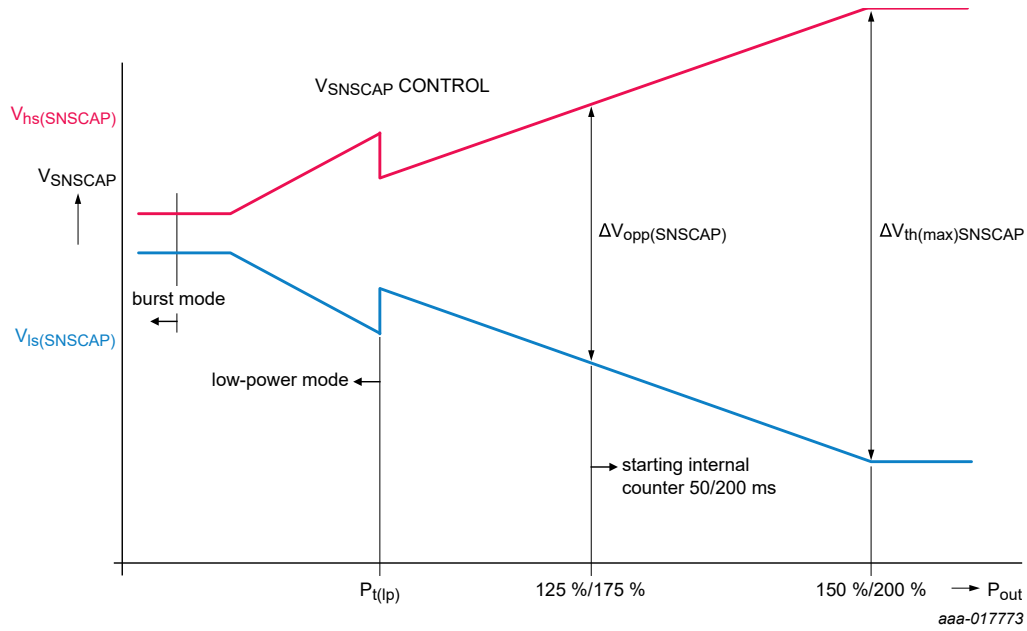


Figure 19. TEA19161T overpower

The external capacitive/resistive divider connected to the SNSCAP pin must be chosen such that:

- The voltage difference between $V_{hs(SNSCAP)}$ and $V_{ls(SNSCAP)}$ equals $\Delta V_{opp(SNSCAP)}$
- The voltage difference between $V_{hs(SNSCAP)}$ and $V_{ls(SNSCAP)}$ occurs at 125 % of the maximum output power or at 175 %, depending on the settings

When the ΔV_{SNSCAP} ($V_{hs(SNSCAP)} - V_{ls(SNSCAP)}$) exceeds the $\Delta V_{opp(SNSCAP)}$ voltage difference, an internal counter is started. When this counter exceeds $t_{d(opp)}$ (50 ms/200 ms), the system enters a latched/safe restart protection as defined by the external settings.

The voltage difference between $V_{hs(SNSCAP)}$ and $V_{ls(SNSCAP)}$ is also limited to $\Delta V_{th(max)SNSCAP}$, which then corresponds to an output power of 150 % or 200 %, depending on the settings (see Figure 19). If the output of the LLC converter requires additional power, the output voltage drops as the power delivered by the LLC converter is limited to 150 % or 200 %.

An additional option is to disable the overpower counter, using the external settings. In this way, the overpower rating can be used as an extension of the typical power level.

8.7 External settings

Before the system starts switching, it reads the external settings. Using specific resistor values at the GATELS, SNSSET, and SNSOUT pins, several internal settings can be defined.

8.7.1 Burst period

Figure 20 shows how the internal regulated burst frequency can be set using the external resistor connected to the SNSOUT pin.

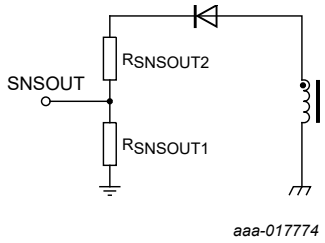


Figure 20. External setting of the burst frequency

Table 5. External setting of the burst frequency

$R_{SNSOUT1}$	Burst frequency
22 kΩ	200 Hz
15 kΩ	400 Hz
10 kΩ	800 Hz
6.8 kΩ	1600 Hz

The absolute value of the resistor connected between the SNSOUT pin and ground ($R_{SNSOUT1}$) defines the burst frequency. An accurate resistor of 1 % according to Table 5 is required. The OVP level can be set using resistor $R_{SNSOUT2}$.

A low burst frequency is best for minimum audible noise. However, a high burst frequency minimizes the output voltage ripple.

8.7.2 General settings

Variables on the OPP function can be set using resistor $R_{SNSSET1}$ connected to the SNSSET pin (see Figure 21).

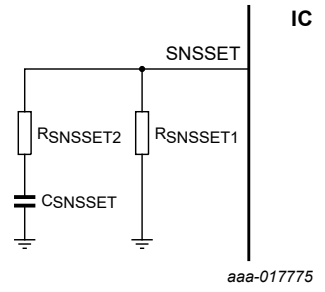


Figure 21. External setting of the SNSSET pin

Table 6. General settings

$R_{SNSSET1}$ (kΩ)	Power capability level (%)	OPP timer level (%)	End of power good timer (ms)	OPP timer (ms)	Protection
< 10		no start-up			
46.4	200	infinite			
53.6	200	175	190	200	1 s restart

Table 6. General settings...*continued*

$R_{SNSSET1}$ (kΩ)	Power capability level (%)	OPP timer level (%)	End of power good timer (ms)	OPP timer (ms)	Protection
61.9	200	175	45	50	1 s restart
71.5	150	125	190	200	1 s restart
82.5	150	125	45	50	1 s restart
95.3	200	175	190	200	latched
110	200	175	45	50	latched
127	150	125	190	200	latched
147	150	125	45	50	latched

When the measured value of $R_{SNSSET1}$ < 10 kΩ, the system assumes a shorted pin to ground and the start-up is inhibited. At a value of 46.4 kΩ, the system can of continuously delivering the maximum power of 200 %.

The output power level at which the overpower timer is started can be set to 125 % or 175 %. Two corresponding timer values can be selected, 50 ms or 200 ms. Finally, the value of $R_{SNSSET1}$ (see Table 6) can set the behavior of the overpower function (either a 1 s restart or latched). During this protection period, the SUPIC is regulated at its $V_{start(SUPIC)}$ level.

8.7.3 Low-power mode/burst mode transition levels

To ensure the best efficiency, the system must enter the low-power mode and the burst mode at high power levels. However, to ensure the best output ripple, these modes must be entered at low-power levels. To choose the optimum level for a specific application, the power transition levels at which the system enters the low-power mode and the burst mode can be set externally.

Resistor $R_{SNSSET2}$ defines the power levels at which the system enters the low-power mode and the burst mode. Table 7 gives an overview.

Table 7. External setting of the high-power/low-power and low-power/burst transition levels

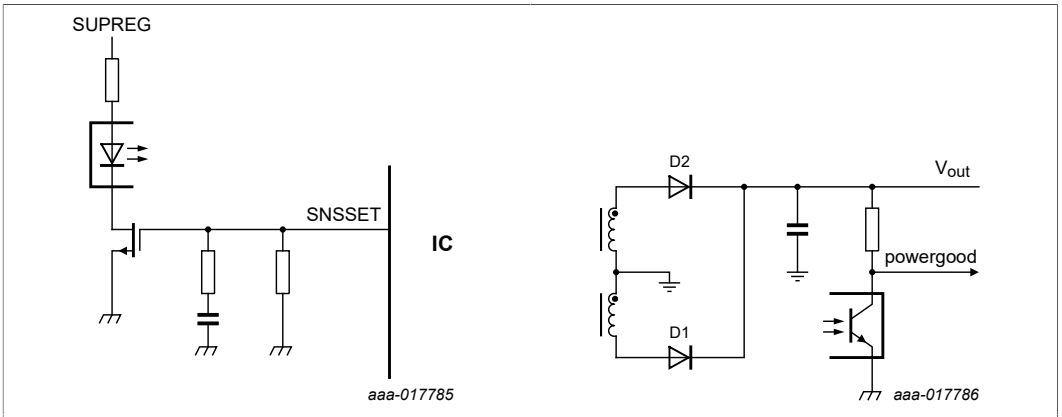
$R_{SNSSET2}$ (kΩ)	High-power => low-power (%) [1]	Burst mode [1]			
		200 Hz (%)	400 Hz (%)	800 Hz (%)	1600 Hz (%)
1	25	9	9	9	9
6.8	25	12	12	12	12
15	37.5	9	9	9	10
27	37.5	12	12	12	13
47	50	9	10	11	12
82	50	12	13	15	17
180	62.5	9	10	12	14
open	62.5	12	15	17.5	20

[1] The values in this table are including the additional shift due to the internal ($t_{PD(SNSCAP)}$) delay and a typical external delay of 150 ns and 300 ns, respectively. When an external R + C network compensates these delays, the levels in this table can be lowered.

The power level at which the system enters the burst mode also depends on the defined burst period. In this way, the optimum between efficiency and output voltage ripple can be chosen.

8.8 Power good function

The TEA19161T provides a power good function via the SNSSET pin. At initialization, the TEA19161T measures the resistors connected to the SNSSET pin to set internal variables. After that, the pin is used for the power good function.



a. Primary side b. Secondary side

Figure 22. Power good function

After the system has read the external settings (see Figure 5), the SNSSET output is active high, enabling an external MOSFET. A secondary power good signal can be pulled low using an external optocoupler.

When the system enters the operating state (see Figure 5), the SNSSET output is pulled low and the external power good signal becomes active high. Any required delay can be achieved via an external R/C network.

At low power good, the SNSSET output becomes active high when:

- The voltage on the SNSBOOST pin drops to below $V_{det(SNSBOOST)}$ (1.95 V)
- The OPP counter is at a value indicated in Table 6.

In this way, the secondary power good signal is pulled low at 5 ms or 10 ms before the output is disabled.

When the system enters protection mode (OVP, OCP, UVP or OTP), it pulls low the SNSSET pin and stops switching immediately.

8.9 PFC/LLC communication protocol

The TEA19161T is designed to cooperate with the TEA19162T (PFC) in one system. The TEA19161T and TEA19162T can be seen as a combination, split up into two packages. All required functionality between the two controllers is arranged via the combined SUPIC and SNSBOOST pins.

8.9.1 Start-up

To ensure that at start-up the TEA19161T and TEA19162T are enabled at the same time, the TEA19161T (LLC) pulls down the SNSBOOST pin to below the SNSBOOST short protection level of the PFC. The TEA19161T disables the TEA19162T (PFC) (see Figure 23) until the system enters the PFC start-up phase (see Figure 5 and Figure 23).

The SUPIC start levels and stop levels of the TEA19162T (PFC) are below the SUPIC start levels and stop levels of the TEA19161T (LLC). When the SUPIC exceeds the start level of the TEA19161T, both controllers are enabled.

In this way, both controllers are enabled/disabled at the same SUPIC start and stop levels.

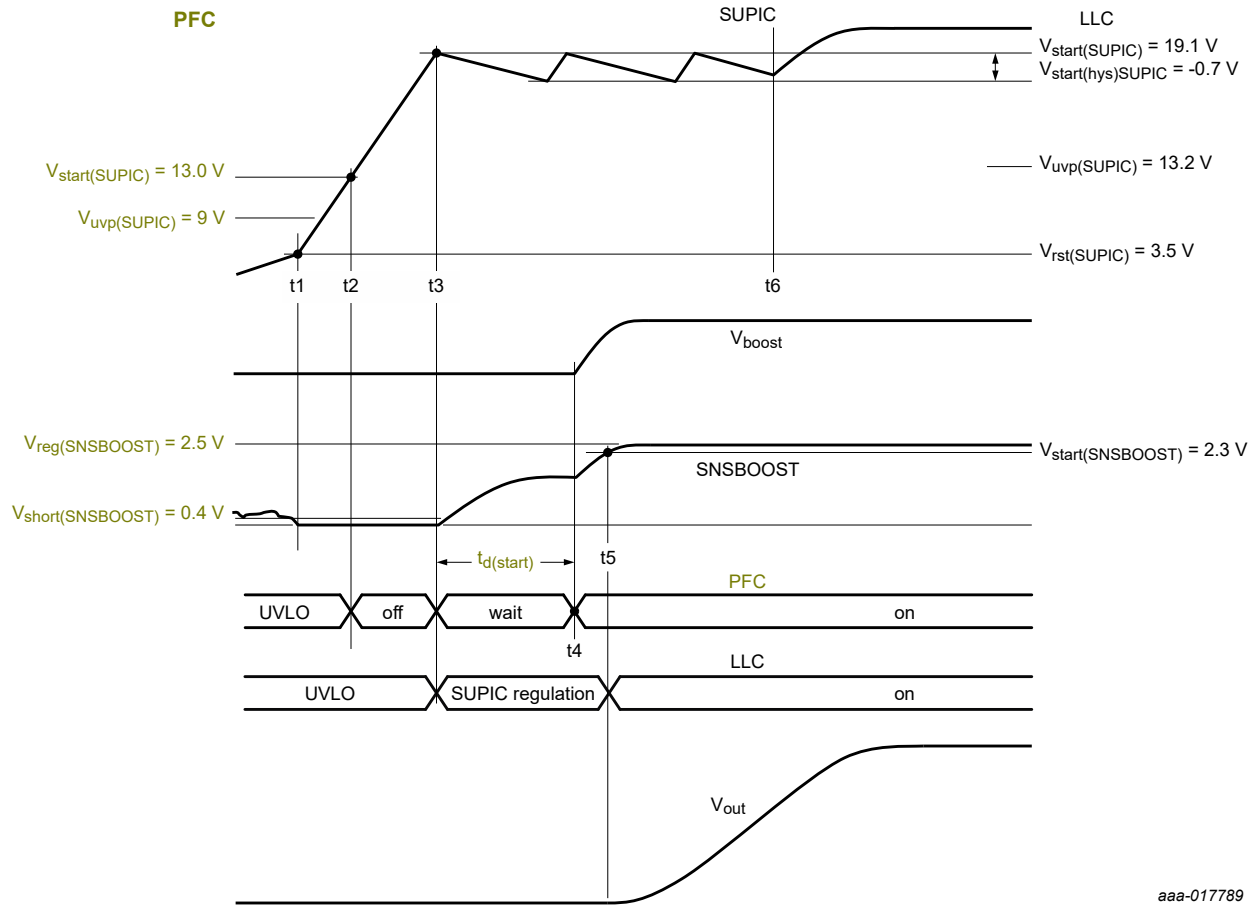


Figure 23. Start-up of the PFC and LLC

When the LLC reaches a minimum supply voltage level ($V_{rst(SUPIC)}$; t1), the LLC pulls down the SNSBOOST pin to disable the PFC.

At t2, the SUPIC reaches the start level of the PFC converter. However, as the LLC pulls low the SNSBOOST voltage to < the PFC short protection level, the PFC is still off. When at t3 the SUPIC reaches the start level of the LLC, after the LLC has read out the external settings, the SNSBOOST voltage is released. It increases because of the connected resistive divider which is connected to the PFC boost voltage. To ensure that the SNSBOOST voltage is a representative of the V_{boost} voltage before the system actually starts to switch, an additional delay (until t4) is built into the PFC controller before it starts.

When at t5 the SNSBOOST voltage reaches the start level of the LLC, the LLC converter starts to switch. At t6, the SUPIC is supplied via the primary auxiliary winding.

8.9.2 Protection

When a protection is triggered in either the PFC or LLC, it may also disable the other converter. For example, if an OVP is detected at the LLC, both converters are latched. Also, at initial start-up, the PFC disables the LLC converter until the mains voltage detects the brownin level.

The PFC can disable the LLC converter by pulling down the SNSBOOST pin to below the $V_{uvp(SNSBOOST)}$ level of the LLC converter. The LLC can disable the PFC converter by

pulling down the SNSBOOST pin to below the short protection level of the PFC converter SNSBOOST pin.

Table 4 in Section 8.6 gives an overview of protections in the LLC converter. It shows which protections also disable the PFC.

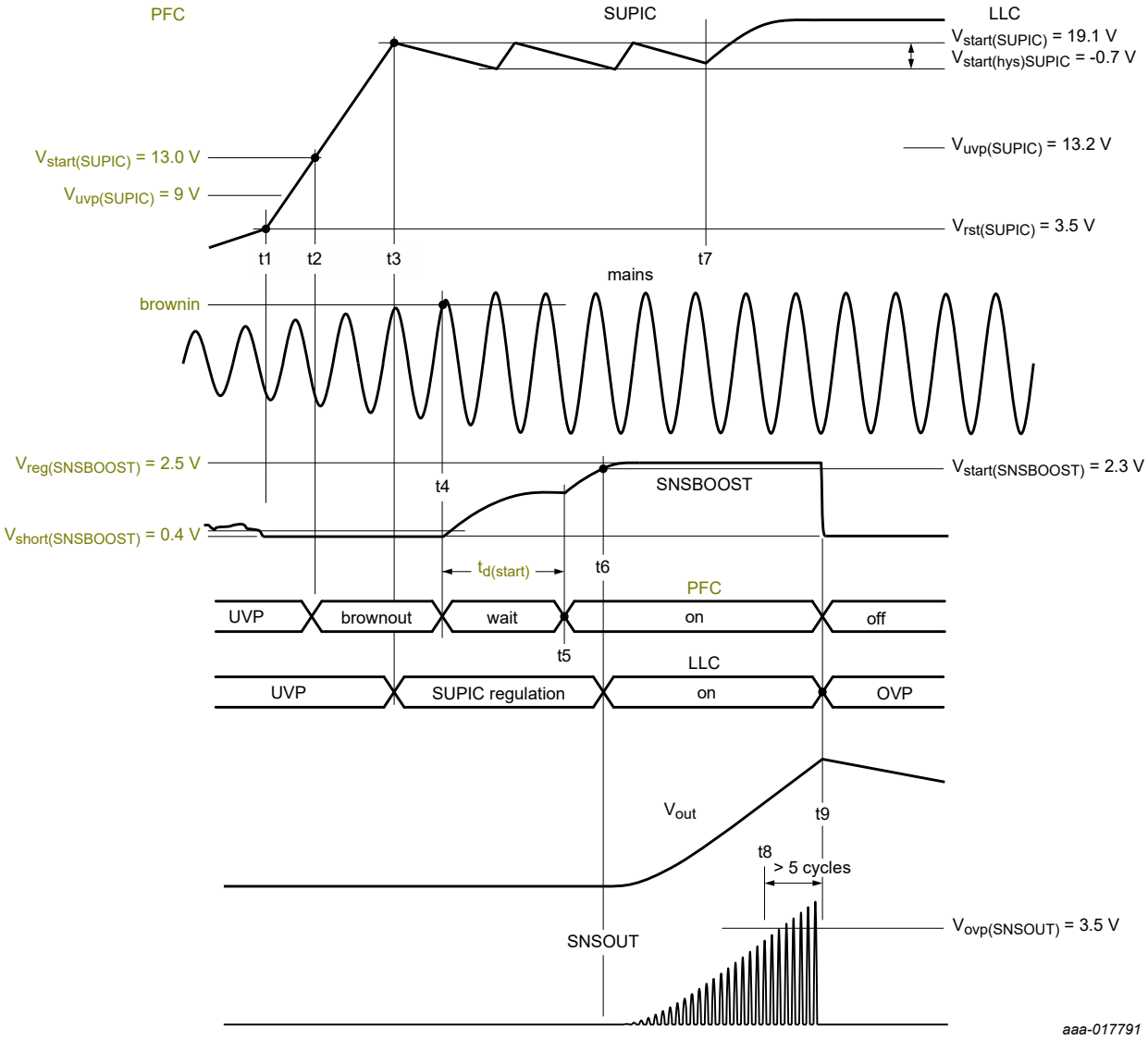


Figure 24. System protection

The start-up period up to t3 is identical in Figure 23 and Figure 24. At t3, the LLC converter releases the pull-down of the SNSBOOST pin. However, as the mains voltage is below the brownin level, the PFC converter pulls low the SNSBOOST pin. When the mains voltage exceeds the brownin level (t4), the SNSBOOST pin is released and increases because of the resistive divider connected between the PFC boost voltage and the SNSBOOST pin. To allow some external capacitance on the SNSBOOST pin, the PFC converter waits until the SNSBOOST voltage is stabilized.

At t5, the PFC converter starts to switch. At t6, the LLC converter also starts to switch, as the SNSBOOST voltage reaches the $V_{start(SNSBOOST)}$ of the LLC converter.

At t7, the primary auxiliary winding takes over the supply of the SUPIC pin.

At t8, the LLC detects an OVP at the SNSOUT pin. After at least 5 consecutive OVP cycles (t9), the LLC stops switching and pulls down the SNSBOOST pin. As a result, the PFC also stops switching.

When either the PFC or LLC is in protection, the SUPIC pin is regulated to the $V_{start(SUPIC)}$ via the SUPHV pin as soon as it drops below the $V_{start(SUPIC)}$ level.

8.9.3 Fast latch reset

The SUPIC pin is regulated to the $V_{start(SUPIC)}$ level when a (latched) protection is triggered. So, it can remain in this protection mode until the capacitor at the PFC output, which the SUPHV is connected to, is discharged. Hence, it may remain in protection mode for a long time after the mains is disconnected.

When protection modes are tested at mass-production, a long reset time is not acceptable in most cases. So, a fast latch reset function is built into the PFC and the LLC. When the mains is initially disconnected and then reconnected, all protections the PFC or the LLC initiated are released again.

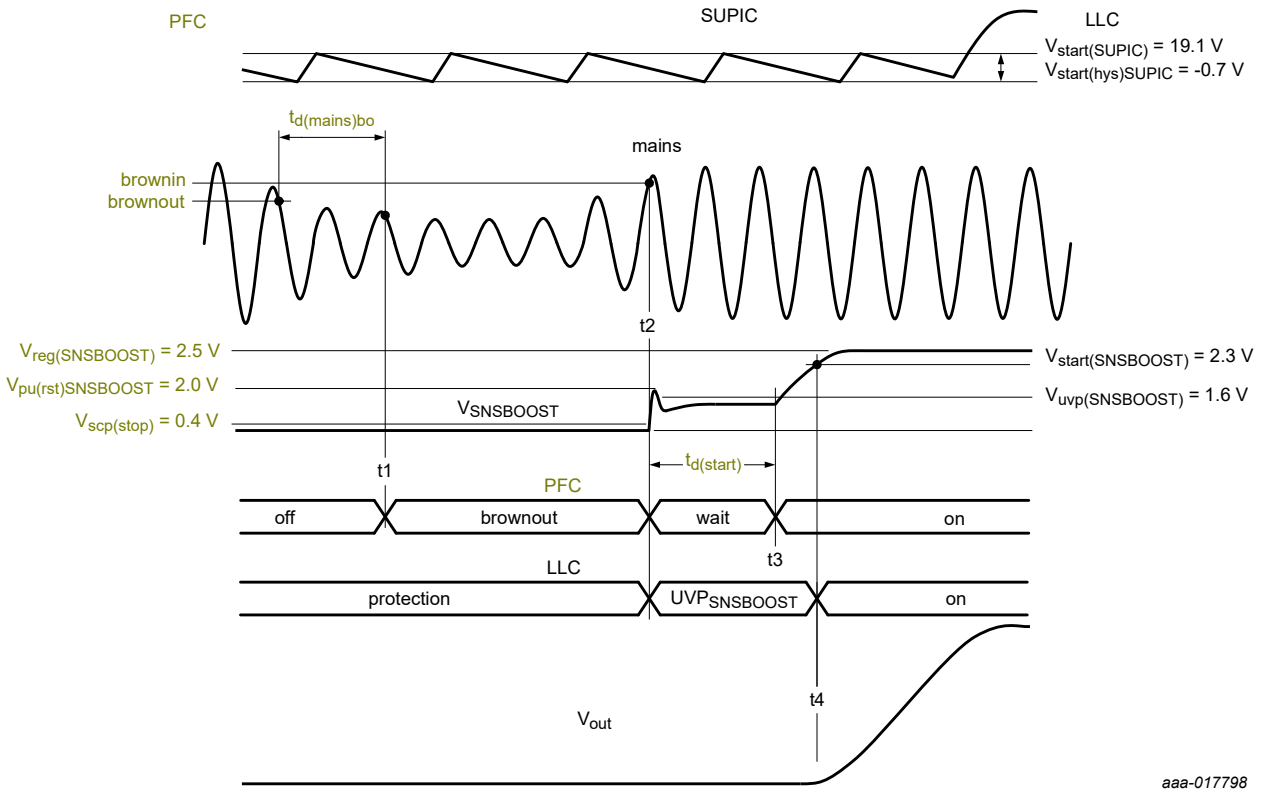


Figure 25. Fast latch reset

Before t1, the LLC is in a (latched) protection and pulls down the SNSBOOST pin, which also disables the PFC.

When the mains voltage drops to below the brownout level for a minimum period of $t_{d(mains)bo}$, the PFC enters the brownout protection mode. When the mains voltage increases again to > the brownin level (t2) in the brownout protection mode, the PFC pulls up the SNSBOOST voltage until it reaches the $V_{uvp(SNSBOOST)}$ level of the LLC

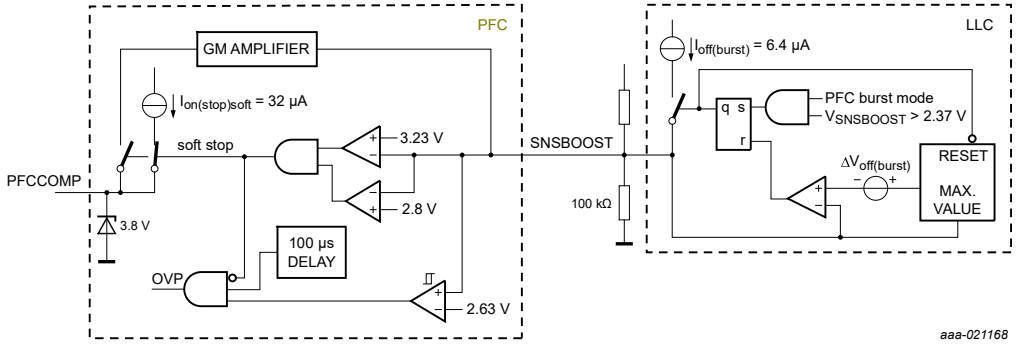
converter. The LLC converter then releases all protection modes and waits until the SNSBOOST pin exceeds its start level ($V_{start(SNSBOOST)}$). After a waiting time, the PFC converter starts (t3), followed by a start-up of the LLC converter (t4).

8.9.4 PFC burst mode

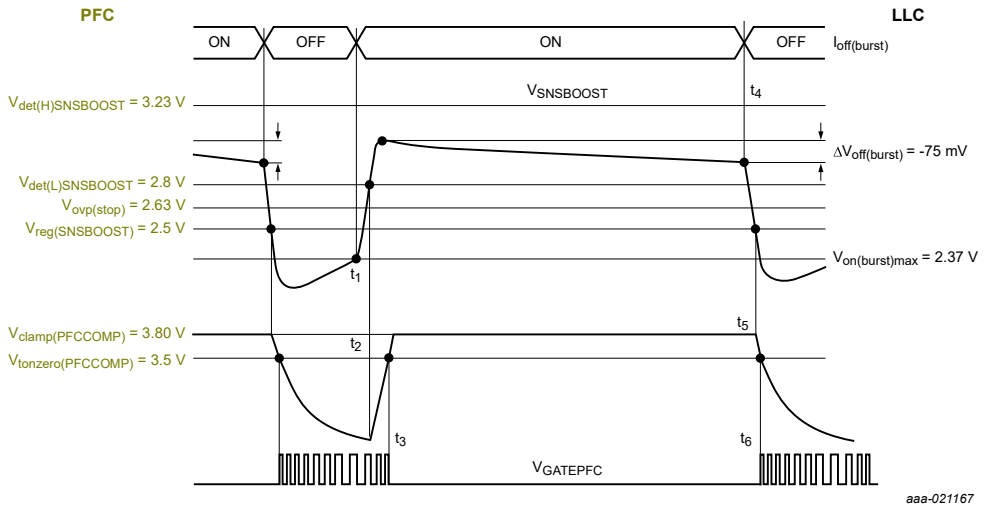
When the LLC operates in burst mode and the duty cycle of the burst is below 50 % for at least 8 consecutive burst periods, the TEA19161T (LLC) sets the TEA19162T (PFC) in burst mode as well. The corresponding output power level is then 50 % of the power level at which the LLC enters the burst mode (see Table 7).

When the output power exceeds 75 % of the power level at which the LLC enters the burst mode (see Table 7), the PFC burst is disabled again.

When the PFC burst is enabled, an additional current out of the SNSBOOST pin stops the PFC from switching via a soft stop, so the audible noise is minimized (see Figure 26).



a. Block diagram



b. Timing diagram

Figure 26. PFC burst mode

At t1, the current out of the LLC SNSBOOST pin ($I_{off(burst)}$) is activated and the voltage on the SNSBOOST pin increases. When an external 100 kΩ resistor ($R_{SNSBOOST}$) is used between the SNSBOOST pin and GND pin (see Figure 27), the SNSBOOST voltage increase is approximately 640 mV (= $I_{off(burst)}$ * $R_{SNSBOOST}$). Because of this increase, the SNSBOOST voltage is between the $V_{det(L)SNSBOOST}$ and $V_{det(H)SNSBOOST}$ levels of the

PFC (t2), so the soft stop of the PFC converter is started. At the end of the soft stop, the PFC enters the energy safe state and stops switching (t3). Because of the continuous operation of the LLC converter, even when the PFC is stopped, the PFC output capacitor is discharged.

When the PFC boost capacitor is discharged so much that the voltage on the SNSBOOST pin has dropped 75 mV ($\Delta V_{off(burst)}$; t4), the internal current source in the LLC converter is switched off. Because of the negative voltage drop at the SNSBOOST pin, the PFC starts switching again. When $V_{SNSBOOST}$ exceeds the LLC $V_{on(burst)max}$ level (2.37 V) again, the internal current source is reactivated and the PFC stops switching again (t1).

9 Limiting values

Table 8. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
Voltages					
V_{SUPHV}	voltage on pin SUPHV	maximum during mains surge;not repetitive	−0.4	+700	V
V_{SUPHS}	voltage on pin SUPHS		V_{HB}	V_{HB} + 14	V
V_{HB}	voltage on pin HB	maximum during mains surge; not repetitive	−3	+700	V
		t < 1 µs	−14	-	V
$SR_{max(HB)}$	maximum slew rate on pin HB	[1]	−70	+70	V/ns
V_{SUPIC}	voltage on pin SUPIC		−0.4	+36	V
V_{SUPREG}	voltage on pin SUPREG		−0.4	+12	V
V_{GATEHS}	voltage on pin GATEHS		V_{HB} − 0.4	V_{SUPHS} + 0.4	V
V_{GATELS}	voltage on pin GATELS		−0.4	V_{SUPREG} + 0.4	V
V_{SNSFB}	voltage on pin SNSFB		−0.4	+12	V
V_{SNSOUT}	voltage on pin SNSOUT		−0.4	+12	V
V_{SNSSET}	voltage on pin SNSSET		−0.4	+12	V
V_{SNSCUR}	voltage on pin SNSCUR		−0.4	+12	V
V_{SNSCAP}	voltage on pin SNSCAP		−0.4	+12	V
$V_{SNSBOOST}$	voltage on pin SNSBOOST		−0.4	+12	V
Currents					
I_{SUPHV}	current on pin SUPHV		-	20	mA
General					
P_{tot}	total power dissipation	T_{amb} < 75 °C	-	0.7	W
T_{stg}	storage temperature		−55	+150	°C
T_j	junction temperature		−40	+150	°C
Latch-up					
I_{lu}	latch-up current	all pins; according to JEDEC: Standard 78D	−100	+100	mA
ElectroStatic Discharge (ESD)					
V_{ESD}	electrostatic discharge voltage	human body model			
		pins SUPHV, SUPHS, GATEHS, and HB	−1000	+1000	V
		other pins	−2000	+2000	V
		charged device model; all pins	−500	+500	V

[1] To prevent erronous operation due to high HB dv/dt disturbances, a maximum slew rate of 25 V/ns is recommended.

10 Thermal characteristics

Table 9. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	In free air; JEDEC test board	107	K/W
$R_{th(j-c)}$	thermal resistance from junction to case	In free air; JEDEC test board	60	K/W

11 Characteristics

Table 10. Characteristics

T_{amb} = 25 °C; V_{SUPIC} = 19.5 V; all voltages are measured with respect to GND; currents are positive when flowing into the IC;unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SUPHV pin						
$I_{lim(SUPHV)}$	current limit on pin SUPHV	$V_{SUPIC} < V_{rst(SUPIC)}$	0.5	0.75	1.0	mA
$I_{off(SUPHV)}$	off-state current on pin SUPHV	V_{SUPIC} = 15 V	-	0.5	0.9	µA
$\Delta V_{I(SUPHV-SUPIC)}$	input voltage difference between pin SUPHV and pin SUPIC	I_{SUPHV} = 20 mA	-	7	-	V
SUPIC pin						
$V_{start(SUPIC)}$	start voltage on pin SUPIC		18.3	19.1	19.8	V
$V_{start(hys)SUPIC}$	start voltage hysteresis on pin SUPIC		-	−0.7	-	V
$V_{low(hys)SUPIC}$	low voltage hysteresis on pin SUPIC		-	0.9	-	V
$V_{low(SUPIC)}$	low voltage on pin SUPIC	tracks with $V_{uvp(SUPIC)}$	13.5	14.0	14.5	V
$V_{uvp(SUPIC)}$	undervoltage protection voltage on pin SUPIC		12.7	13.2	13.7	V
$V_{rst(SUPIC)}$	reset voltage on pin SUPIC		-	3.5	-	V
$I_{CC(SUPIC)}$	supply current on pin SUPIC	operating mode; f_{HB} = 100 kHz; GATEHS/GATELS open; I_{SNSFB} = −85 µA; I_{SNSCAP} = −100 µA	-	5.6	-	mA
		latched protection; I_{SNSFB} = 0 µA; I_{SNSCAP} = −100 µA	2.3	3.0	3.7	mA
		burst mode; I_{SNSFB} = −106 µA; I_{SNSCAP} = −100 µA	-	0.7	-	mA
SUPREG pin						
$V_{intregd(SUPREG)}$	internal regulated voltage on pin SUPREG	V_{SUPIC} > 13.8 V; I_{SUPREG} = 50 mA	10.6	11.0	11.4	V
$V_{reg(acc)SUPREG}$	regulator voltage accuracy on pin SUPREG	V_{SUPIC} > 13.8 V; 10 µA < I_{SUPREG} < 20 mA	−150	−100	−50	mV
$I_{lim(SUPREG)}$	current limit on pin SUPREG	V_{SUPIC} = 19.5 V	−44	−37	−30	mA

Table 10. Characteristics...*continued*

T_{amb} = 25 °C; V_{SUPIC} = 19.5 V; all voltages are measured with respect to GND; currents are positive when flowing into the IC;unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{uvp(SUPREG)}$	undervoltage protection voltage on pin SUPREG		8.6	9.0	9.4	V
SNSCAP pin						
$V_{AV(regd)SNSCAP}$	regulated average voltage on pin SNSCAP	regulated average of $V_{hs(SNSCAP)}$ and $V_{ls(SNSCAP)}$	-	2.50	-	V
$I_{bias(max)SNSCAP}$	maximum bias current on pin SNSCAP		−245	−210	−175	µA
$\Delta V_{th(max)SNSCAP}$	maximum threshold voltage difference on pin SNSCAP	$V_{hs(SNSCAP)} - V_{ls(SNSCAP)}$; P_{out} = 200 %; $V_{SNSBOOST}$ = 2.5 V	-	1.92	-	V
		$V_{hs(SNSCAP)} - V_{ls(SNSCAP)}$; P_{out} = 200 %; $V_{SNSBOOST}$ < 2.0 V	2.85	3.00	3.15	V
Overpower protection						
$\Delta V_{opp(SNSCAP)}$	overpower protection voltage difference on pin SNSCAP	$V_{hs(SNSCAP)} - V_{ls(SNSCAP)}$; P_{out} = 150 %; $V_{SNSBOOST}$ = 2.5 V	-	1.44	-	V
		$V_{hs(SNSCAP)} - V_{ls(SNSCAP)}$; P_{out} = 150 %; $V_{SNSBOOST}$ = 2.1 V	-	2.24	-	V
$t_{PD(SNSCAP)}$	propagation delay on pin SNSCAP	from crossing $V_{ls(SNSCAP)}/V_{hs(SNSCAP)}$ level to GATELS/GATEHS switch-off	-	150	-	ns
$t_{d(opp)}$	overpower protection delay time	See Table 6 for related $R_{SNSSET1}$	40	50	60	ms
		See Table 6 for related $R_{SNSSET1}$	160	170	180	ms
$t_{d(restart)}$	restart delay time		0.8	1.0	1.2	s
SNSCUR pin						
$V_{bias(SNSCUR)}$	bias voltage on pin SNSCUR		2.4	2.5	2.6	V
$R_{O(SNSCUR)}$	output resistance on pin SNSCUR		-	60	-	kΩ
V_{ocp}	overcurrent protection voltage	positive level; $V_{SNSCUR} - V_{bias(SNSCUR)}$	1.35	1.50	1.65	V
		negative level; $V_{SNSCUR} - V_{bias(SNSCUR)}$	−1.65	−1.50	−1.35	V
$V_{reg(capm)}$	capacitive mode regulation voltage	positive level; $V_{SNSCUR} - V_{bias(SNSCUR)}$	85	100	115	mV
		negative level; $V_{SNSCUR} - V_{bias(SNSCUR)}$	−115	−100	−85	mV
$V_{det(zero)}$	zero detection voltage	detected as ≥ 0	-	−13	-	mV
		detected as ≤ 0	-	13	-	mV

Table 10. Characteristics...*continued*

T_{amb} = 25 °C; V_{SUPIC} = 19.5 V; all voltages are measured with respect to GND; currents are positive when flowing into the IC;unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SNSBOOST pin						
$V_{start(SNSBOOST)}$	start voltage on pin SNSBOOST		2.2	2.3	2.4	V
$V_{uvp(SNSBOOST)}$	undervoltage protection voltage on pin SNSBOOST		1.5	1.6	1.7	V
$V_{det(SNSBOOST)}$	detection voltage on pin SNSBOOST	when below power good = LOW	1.8	1.95	2.1	V
PFC burst mode controller						
$\delta_{en(burst)}$	burst mode enable duty cycle	enable of PFC burst mode; duty cycle of LLC burst mode	-	50	-	%
$N_{cy(en)burst}$	burst mode enable number of cycles	enable of PFC burst mode; cycles of LLC burst mode	-	8	-	
$\delta_{dis(burst)}$	burst mode disable duty cycle	disable of PFC burst mode; duty cycle of LLC burst mode	-	75	-	%
$V_{pu(SNSBOOST)}$	pull-up voltage on pin SNSBOOST	to enter PFC burst mode off-state	-	2.95	-	V
$I_{off(burst)}$	burst mode off-state current	during PFC burst mode off-state	−7.1	−6.4	−5.7	µA
$\Delta V_{off(burst)}$	burst mode off-state voltage difference	during PFC burst mode off-state; between peak voltage and end of off-state	-	−75	-	mV
$V_{on(burst)max}$	maximum burst mode on-state voltage	during PFC burst mode on-state	2.29	2.37	2.45	V
$t_{to(det)on(burst)}$	burst mode on-state detection time-out time	during PFC burst mode on-state	3.7	4.0	4.3	ms
PFC protection controller						
$R_{pd(SNSBOOST)}$	pull-down resistance on pin SNSBOOST	at protection activation	-	550	-	Ω
$I_{pd(SNSBOOST)}$	pull-down current on pin SNSBOOST	during active protection	94	110	127	µA
$I_{prot(SNSBOOST)}$	protection current on pin SNSBOOST		-	60	-	nA
SNSOUT pin						
$V_{ovp(SNSOUT)}$	overvoltage protection voltage on pin SNSOUT		3.36	3.50	3.64	V
$I_{prot(SNSOUT)}$	protection current on pin SNSOUT	for open pin	-	−60	-	nA

Table 10. Characteristics...*continued*

T_{amb} = 25 °C; V_{SUPIC} = 19.5 V; all voltages are measured with respect to GND; currents are positive when flowing into the IC;unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SNSFB pin						
$V_{bias(SNSFB)}$	bias voltage on pin SNSFB	I_{SNSFB} = −85 µA	2.2	2.5	2.8	V
Optobias regulator						
$I_{reg(SNSFB)}$	regulation current on pin SNSFB	$I_{start(burst)}$ = 106 µA; tracks with $I_{start(burst)}$	-	−85	-	µA
$I_{reg(max)SNSFB}$	maximum regulation current on pin SNSFB	$I_{start(burst)}$ = 106 µA; tracks with $I_{start(burst)}$	-	−310	-	µA
$I_{reg(min)SNSFB}$	minimum regulation current on pin SNSFB	$I_{start(burst)}$ = 106 µA; tracks with $I_{start(burst)}$	-	−63	-	µA
Burst mode regulator						
$I_{start(burst)}$	burst mode start current	LLC burst mode	−123	−106	−89	µA
$I_{stop(burst)}$	burst mode stop current	LLC burst mode	-	−200	-	µA
GATELS and GATEHS pins						
$I_{source(GATEHS)}$	source current on pin GATEHS	$V_{GATEHS} - V_{HB}$ = 4 V	-	−340	-	mA
$I_{source(GATELS)}$	source current on pin GATELS	$V_{GATELS} - V_{GND}$ = 4 V	-	−340	-	mA
$I_{sink(GATEHS)}$	sink current on pin GATEHS	$V_{GATEHS} - V_{HB}$ = 2 V	-	580	-	mA
		$V_{GATEHS} - V_{HB}$ = 11 V	-	2	-	A
$I_{sink(GATELS)}$	sink current on pin GATELS	$V_{GATELS} - V_{GND}$ = 2 V	-	580	-	mA
		$V_{GATELS} - V_{GND}$ = 11 V	-	2	-	A
$V_{rst(SUPHS)}$	reset voltage on pin SUPHS		6.4	7	7.6	V
$V_{rst(hys)SUPHS}$	hysteresis of reset voltage on pin SUPHS	> $V_{rst(SUPHS)}$	-	0.6	-	V
$t_{on(min)}$	minimum on-time		-	0.83	-	µs
$t_{on(max)}$	maximum on-time		14.8	17.4	20.0	µs
t_{sweep}	sweep time	frequency; at start-up	1	12	14	ms
Low-power mode regulator						
$f_{lp(min)}$	minimum low-power mode frequency		20	23	26	kHz
Burst mode regulator						
$f_{burst(max)}$	maximum burst mode frequency	$R_{SNSOUT1}$ = 22 kΩ	170	200	230	Hz
		$R_{SNSOUT1}$ = 15 kΩ	340	400	460	Hz
		$R_{SNSOUT1}$ = 10 kΩ	680	800	920	Hz
		$R_{SNSOUT1}$ = 6.8 kΩ	1360	1600	1840	Hz

Table 10. Characteristics...*continued*

T_{amb} = 25 °C; V_{SUPIC} = 19.5 V; all voltages are measured with respect to GND; currents are positive when flowing into the IC;unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Power good characteristics (pin SNSSET)						
$V_{OH(SNSSET)}$	HIGH-level output voltage on pin SNSSET	I_{SNSSET} = −100 µA; power good = LOW	-	4	-	V
$I_{OH(SNSSET)}$	HIGH-level output current on pin SNSSET	V_{SNSSET} = 3 V; power good = LOW	−11	−8	−5	mA
$I_{OL(SNSSET)}$	LOW-level output current on pin SNSSET	V_{SNSSET} = 0.5 V; power good = HIGH	8	11	14	mA
$t_{d(H)SNSSET}$	HIGH-level delay time on pin SNSSET	See Table 6 for related $R_{SNSSET1}$	35	45	55	ms
		See Table 6 for related $R_{SNSSET1}$	150	190	230	ms
Settings sensor (SNSOUT, SNSSET, and GATELS pins)						
$I_{O(SNSOUT)}$	output current on pin SNSOUT	during $R_{SNSOUT1}$ measurement	-	−171	-	µA
$I_{O(SNSSET)}$	output current on pin SNSSET	during R_{SNSSET} measurement	-	−26.8	-	µA
$\Delta V_{O(GATELS-SUPREG)}$	output voltage difference between pin GATELS and pin SUPREG	during R_{GATELS} measurement	-	1.25	-	V
HB pin						
$(dV/dt)_{tno(min)}$	minimum non-overlap time rate of change of voltage		-	-	120	V/µs
$t_{no(min)}$	minimum non-overlap time		-	200	-	ns
$t_{no(max)}$	maximum non-overlap time		-	1.1	-	µs
Overtemperature protection						
T_{otp}	overtemperature protection trip		130	140	150	°C

12 Application information

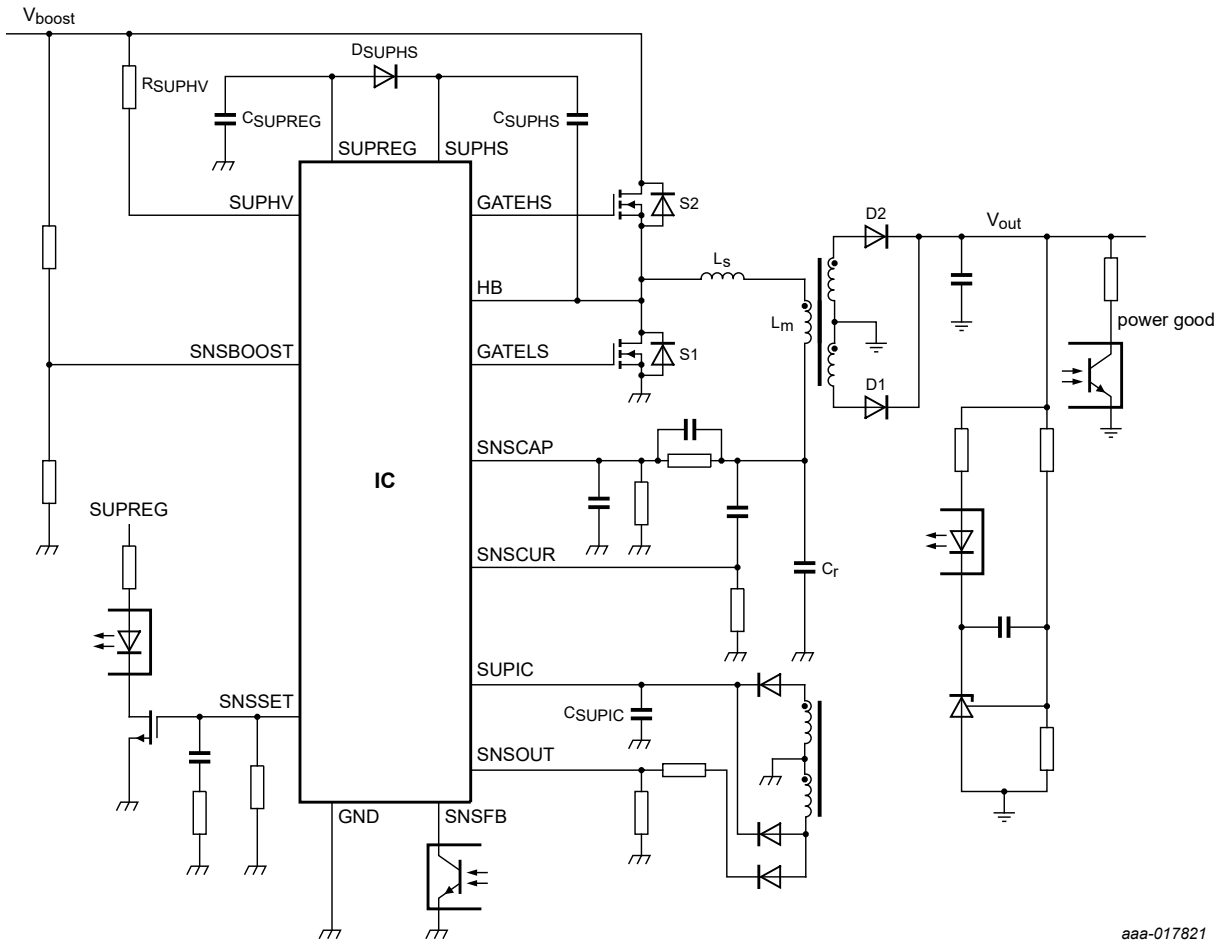
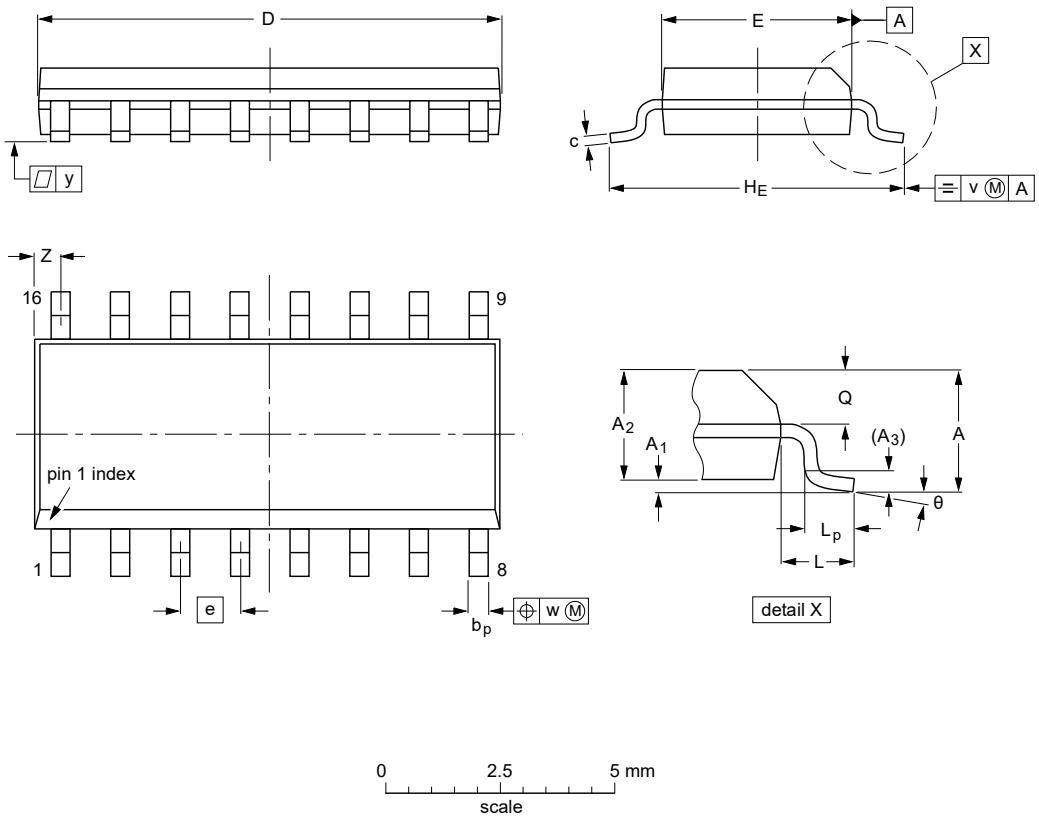


Figure 27. TEA19161T application diagram

13 Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Figure 28. Package outline SOT109-1 (SO16)

14 Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TEA19161T v.2.1	20210518	Product data sheet	-	TEA19161T v.2
Modifications:	• Section 9 "Limiting values" has been updated.			
TEA19161T v.2	20190830	Product data sheet	-	TEA19161T v.1
TEA19161T v.1	20160310	Product data sheet	-	-

15 Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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Date of release: 18 May 2021
Document identifier: TEA19161T