TEA9026T

Digital LLC controller for power supplies providing wide input voltage range and low standby

Rev. 1 — 14 June 2022 Product data sheet

1 General description

The TEA9026T is a digital LLC resonant mode controller for resonant power supplies with a wide input voltage range. The power supply is easy to design and has a very low component count. It meets the efficiency regulations of Energy Star, the Department of Energy (DoE), the Eco-design directive of the European Union, the European Code of Conduct, and other guidelines. So, no auxiliary low-power supply is required. To increase the efficiency of a low-voltage supply output, the TEA2095T dual SR controller can be added on the secondary side.

In contrast to traditional resonant topologies, the TEA9026T (LLC) achieves a high efficiency at low loads due to the newly introduced low-power mode. This mode operates in the power region between continuous switching (also called high-power mode) and burst mode.

Because the TEA9026T is regulated via the primary capacitor voltage, it has accurate information about the power delivered to the output. The measured output power defines the mode of operation (burst mode, low-power mode, or high-power mode). With a single configuration pin, the transition levels of the operating modes can be easily set.

The TEA9026T contains a low-voltage die with a fully digital controller for output power control, start-up, initializations, and protections. These protections include overcurrent protection (OCP), overvoltage protection (OVP), open-loop protection (OLP), and capacitive mode regulation (CMR). The TEA9026T also contains a high-voltage silicon-on-insulator (SOI) controller for high-voltage start-up, integrated drivers, level shifter, protections, and circuitry assuring zero-voltage switching.

The TEA9026T LLC controller enables the building of an easy to design, highly efficient, and reliable power supply. The power supply can provide 90 W to 500 W output power with a minimum of external components. It has a very low no-load input power (< 90 mW) and a high efficiency from minimum to maximum load. So, no additional low-power supply is required, which ensures a significant system cost saving and a highly simplified power supply design, while meeting the latest power supply guidelines and regulations.

2 Features and benefits

2.1 Key features

- Wide input voltage range
- Externally adjustable OPP level
- Integrated high-voltage start-up
- Integrated high-voltage Level Shifter (LS)
- Extremely fast start-up (< 500 ms at V_{mains} = 100 V (AC))
- Continuous V_{SUPIC} regulation via the SUPHV pin during start-up and protection, allowing minimum SUPIC capacitor values
- Operating frequencies are outside the audible area in all operating modes
- Integrated soft start

2.2 Green features

- Extremely high efficiency from low load to medium load
- Compliant with Energy using Product directive (EuP) lot 6
- Excellent no-load input power (< 90 mW for TEA9026T/TEA2095T combination)
- Regulated low optocurrent, enabling low no-load power consumption
- Very low supply current during non-switching state in burst mode
- Accurate transition between different operation modes
- Externally adjustable low-power mode to burst mode transition level
- Adaptive non-overlap time

2.3 Protection features

- Supply undervoltage protection (UVP)
- Overpower protection (OPP)
- On-chip overtemperature protection (OTP)
- Capacitive mode regulation (CMR)
- Accurate overvoltage protection (OVP)
- Maximum on-time protection for low-side and high-side driver output
- Overcurrent protection (OCP)
- Disable input

3 Applications

- Large screen (UHD/4K) TVs
- Printers
- E-bike chargers

4 Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
TEA9026T/1	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

5 Marking

Table 2. Marking codes

Type number	Marking code
TEA9026T/1	TEA9026T

6 Block diagram

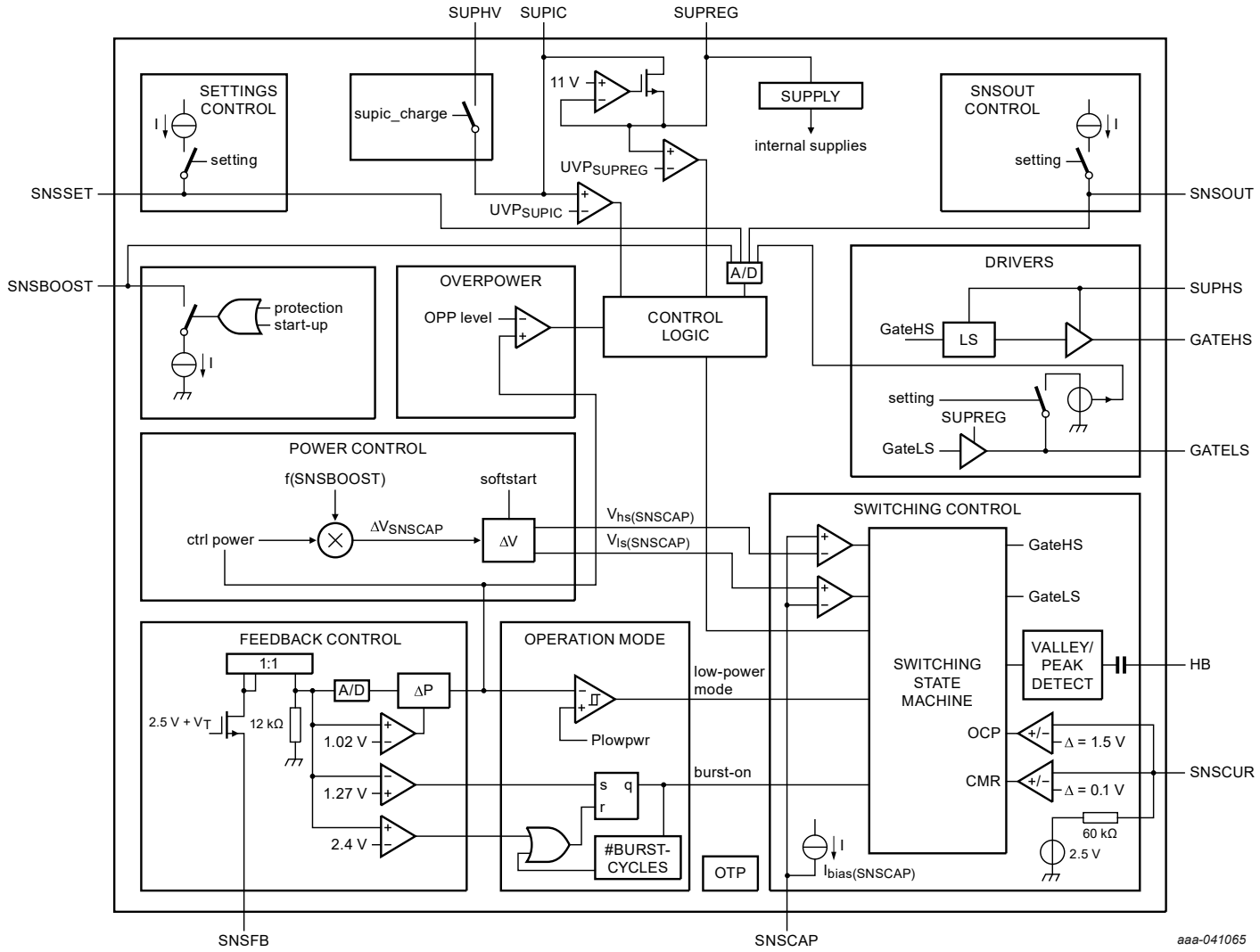


Figure 1. TEA9026T block diagram

7 Pinning information

7.1 Pinning

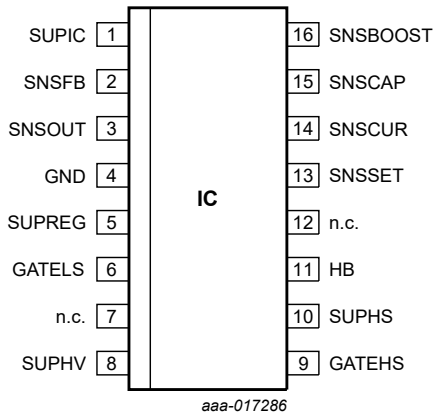


Figure 2. TEA9026T pin configuration (SOT109-1)

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
SUPIC	1	input supply voltage and output of internal HV start-up source; externally connected to an auxiliary winding of the LLC via a diode or to an external DC supply
SNSFB	2	output voltage regulation feedback sense input; externally connected to an optocoupler
SNSOUT	3	sense input for setting the low-power mode to burst mode transition level at low input voltage. And monitoring the LLC output voltage; externally via a resistive divider and a diode connected to the auxiliary winding
GND	4	ground
SUPREG	5	regulated SUPREG IC supply; internal regulator output; input for drivers; externally connected to SUPREG buffer capacitor
GATELS	6	LLC low-side MOSFET gate driver output
n.c.	7	not to be connected
SUPHV	8	internal HV start-up source high-voltage supply input; externally connected to (LLC) input voltage
GATEHS	9	LLC high-side MOSFET gate driver output
SUPHS	10	high-side driver supply input; externally connected to bootstrap capacitor (C_{SUPHS})
HB	11	low-level reference for high-side driver and input for half-bridge slope detection; externally connected to half-bridge node HB between the LLC MOSFETs
n.c.	12	not to be connected; keep floating
SNSSET	13	settings for the low-power mode to burst mode transition level at high input voltage, the high power to low-power transition level, the OPP level as function of the input voltage, and the burst frequency
SNSCUR	14	LLC current sense input; externally connected to the resonant current sense resistor
SNSCAP	15	LLC capacitor voltage sense input; externally connected to divider across LLC capacitor
SNSBOOST	16	sense input for boost voltage; externally connected to resistive divided boost voltage

8 Functional description

8.1 Supply voltages

The TEA9026T includes:

- A high-voltage supply pin for start-up (SUPHV)
- A general supply to be connected to an external auxiliary winding (SUPIC pin)
- An accurate regulated voltage (SUPREG pin)
- A floating supply for the high-side driver (SUPHS pin)

8.1.1 Start-up and supply voltage

Initially, the capacitors on the SUPIC and SUPREG pins are charged via the SUPHV pin. The SUPHV pin is connected to the LLC input voltage via an external resistor. Internally, a high-voltage series switch is located between the SUPHV and SUPIC pins. From the SUPIC pin, the SUPREG pin is supplied using a linear regulator (see Figure 3).

Table 4. Pin description

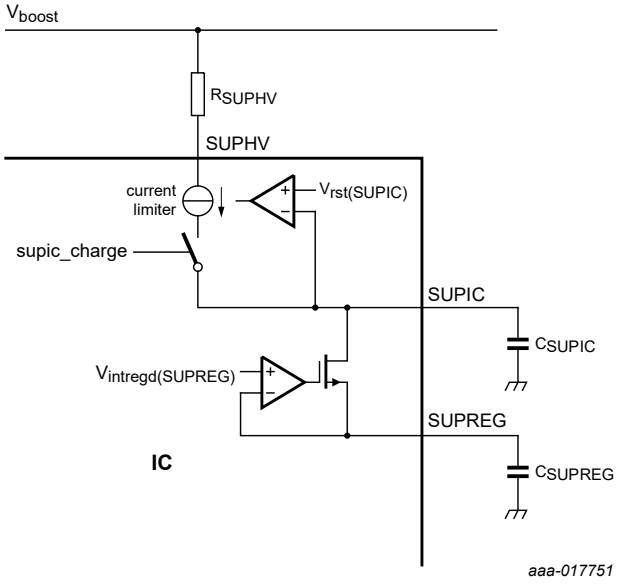


Figure 3. HV start-up

Initially, when the voltage on the SUPIC pin is below the reset level $V_{rstSUPIC)}$ (3.5 V), the SUPIC charge current is internally limited to $I_{lim(SUPHV)}$ (0.75 mA). In this way, the dissipation is limited when SUPIC is shorted to ground. When the voltage on the SUPIC pin exceeds $V_{rst(SUPIC)}$, the internal switch is closed.

To limit the IC power dissipation, an external resistor (R_{SUPHV}) is required to reduce the voltage drop between the SUPHV and SUPIC pins when charging the SUPIC capacitor. R_{SUPHV} must be dimensioned such that the maximum current is limited to below limiting value I_{SUPHV} (20 mA) and it can handle the required power dissipation. The maximum power dissipation of the external resistor can be reduced by using several resistors in series.

When the SUPIC reaches the $V_{start(SUPIC)}$ level (19.1 V), it is continuously regulated to this start level with a hysteresis ($V_{start(hys)SUPIC}$; −0.7 V). It activates the switch

between the SUPHV and SUPIC pins when the SUPIC voltage drops to below $V_{start(SUPIC)} + V_{start(hys)SUPIC}$. It deactivates the switch when it exceeds $V_{start(SUPIC)}$. When start-up is complete and the LLC controller is operating, the LLC transformer auxiliary winding supplies the SUPIC pin. In this operational state, the HV start-up source is disabled (see Figure 4).

When the system enters the protection mode, the SUPIC pin is also regulated to the start level. During the non-switching period of the burst mode, the system also activates the switch between the SUPHV and SUPIC pins when the SUPIC voltage drops below $V_{low(SUPIC)}$. It regulates the voltage with a hysteresis of $V_{low(hys)SUPIC}$. In this way, the system avoids that the SUPIC undervoltage protection ($V_{uvp(SUPIC)}$) is triggered because of a long non-switching period in burst mode.

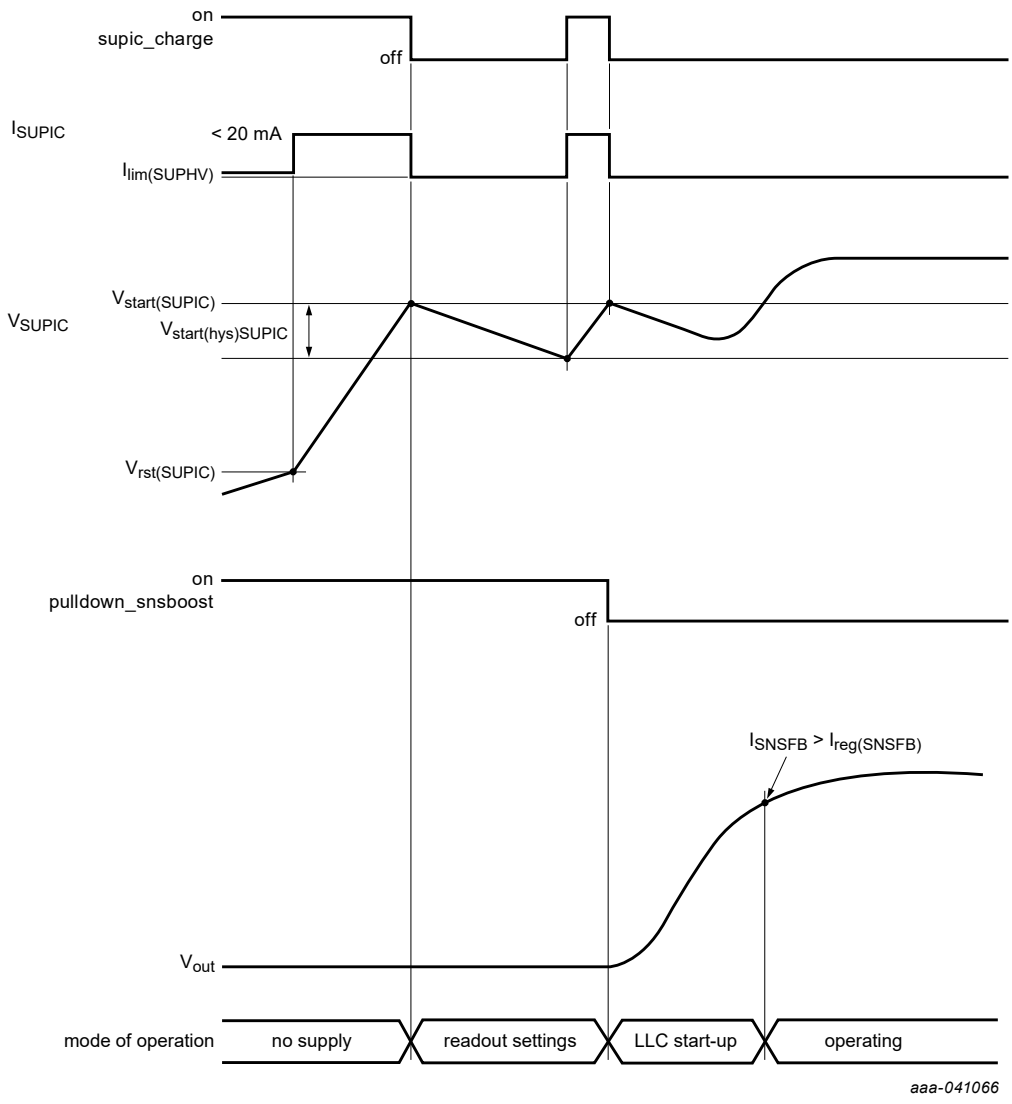


Figure 4. Start-up sequence and normal operation

8.1.2 Regulated supply (SUPREG pin)

The voltage range on the SUPIC pin exceeds that of the maximum external MOSFETs gate-source voltage. So, the TEA9026T incorporates an integrated series stabilizer. The series stabilizer creates an accurate regulated voltage ($V_{intregd(SUPREG)}$ = 11 V) at the buffer capacitor C_{SUPREG}. The stabilized voltage is used to:

- Supply the internal low-side LLC driver
- Supply the internal high-side driver using external components
- As a reference voltage for optional external circuits

To ensure that the external MOSFETs receive sufficient gate drive, the voltage on the SUPREG pin must reach $V_{uvp(SUPREG)}$ before the system starts switching. If the SUPREG voltage drops to below this undervoltage protection level, the system restarts.

8.1.3 High-side driver floating supply (SUPHS pin)

External bootstrap buffer capacitor C_{SUPHS} supplies the high-side driver. The bootstrap capacitor is connected between the high-side driver supply, the SUPHS pin, and the half-bridge node, HB. C_{SUPHS} is charged from the SUPREG pin using an external diode D_{SUPHS} (see Figure 22).

Careful selection of the appropriate diode minimizes the voltage drop between the SUPREG and SUPHS pins, especially when large MOSFETs and high switching frequencies are used. A large voltage drop across the diode reduces the gate drive of the high-side MOSFET.

8.2 System start-up

Figure 5 shows the flow diagram corresponding with Figure 4.

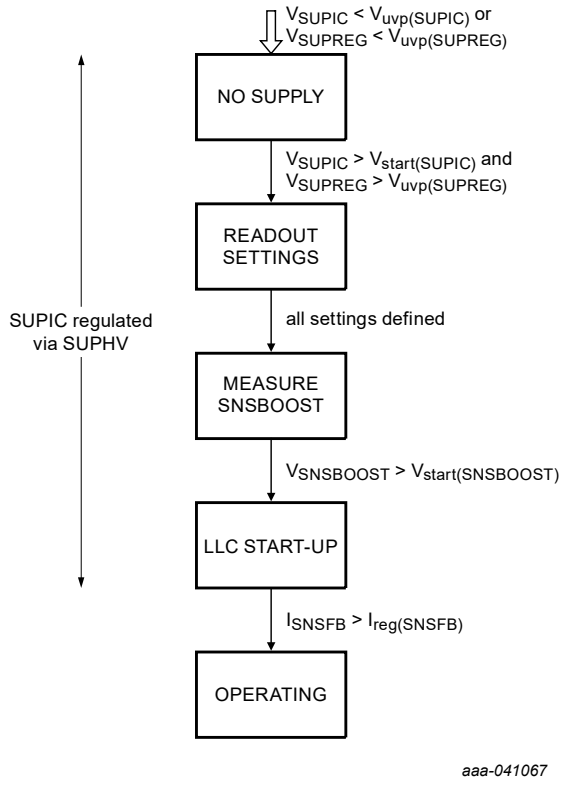


Figure 5. LLC controller flow diagram

When the SUPIC or SUPREG pins drop to below their stop levels, the TEA9026T enters the no supply state. It recharges the SUPIC and SUPREG pins to their start levels via the SUPHV pin. When the start levels are reached, measuring the external resistances on the SNSSET, SNSOUT, and GATELS pins initializes the settings.

During the no supply and readout settings states, the SNSBOOST pin is pulled low. When the settings have been defined, the SNSBOOST pin is released and the system measures the SNSBOOST voltage. When the SNSBOOST reaches the minimum level $V_{start(SNSBOOST)}$, the LLC starts switching.

When a small optocurrent is detected ($I_{SNSFB} < I_{reg(SNSFB)}$), the output voltage is close to its regulation level. As the SUPIC pin must then be supplied via the primary auxiliary winding, charging via the SUPHV is disabled.

8.3 LLC system regulation

In the TEA9026T, the control mechanism is based on a constant gain of the control loop and a burst mode which is derived from the output power. The TEA9026T does not regulate the output power by adjusting the frequency but by the voltage across the primary capacitor.

The input power (related to the output power) of a resonant converter can be calculated with Equation 1:

$$P_{in} = V_{boost} \times I_{boost} = V_{boost} \times \Delta V_{Cr} \times C_r \times f_{sw} \quad (1)$$

Equation 1 shows that the input power has a linear relationship with the capacitor voltage difference ΔV_{Cr}.

Although the TEA9026T uses the primary capacitor voltage as a regulation parameter, all application values, like the resonant inductances, resonant capacitor, and primary MOSFETs rare the same as in a frequency controlled LLC converter. A secondary TL431 circuitry in combination with an optocoupler connected to the primary SNSFB pin continuously regulates the output voltage.

8.3.1 Output power regulation loop

Figure 6 shows the output power regulation loop of V_{cap} control as used by the TEA9026T. Figure 7 shows a corresponding timing diagram.

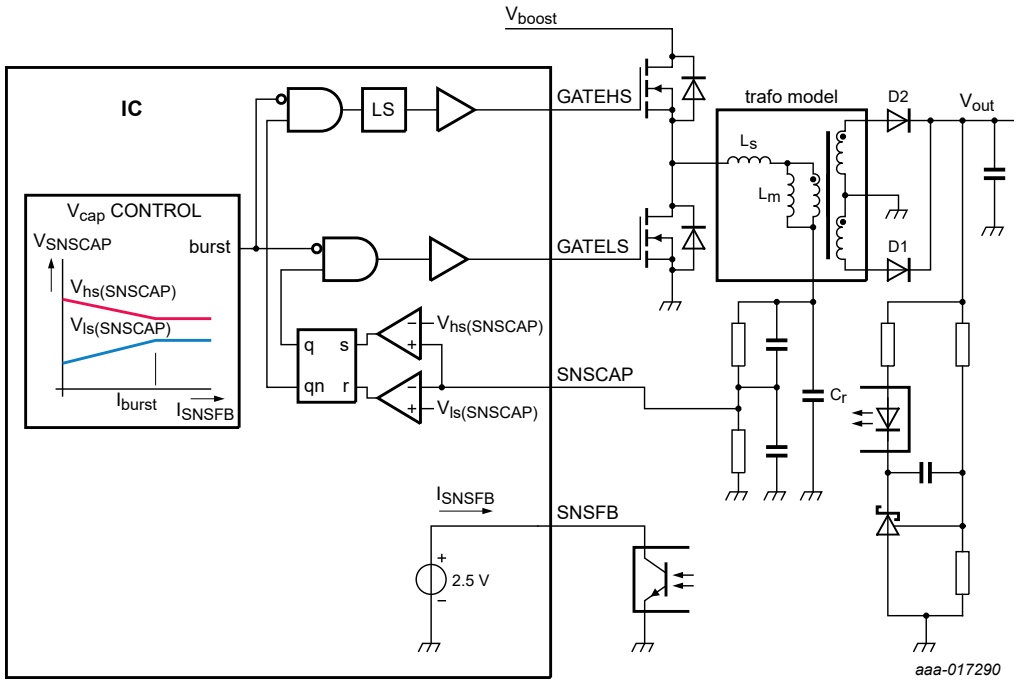


Figure 6. Regulation loop V_{cap} control

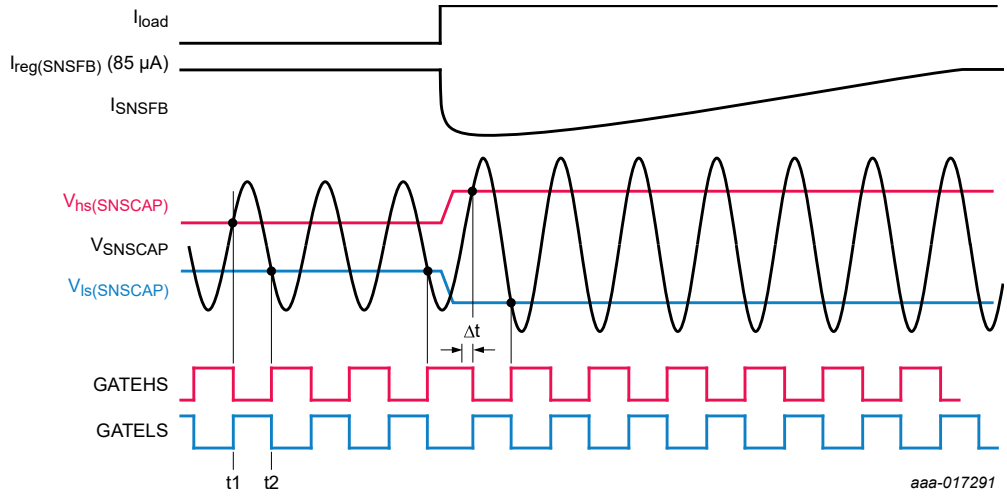


Figure 7. Timing diagram of the regulation loop

When the divided resonant capacitor voltage (V_{SNSCAP}) exceeds the capacitor voltage high level ($V_{hs(SNSCAP)}$), the high-side MOSFET is switched off (see Figure 7 (t1)). After a short delay, the low-side MOSFET is switched on. Because of the resonant current, the resonant capacitor voltage initially increases further but eventually drops.

When the divided capacitor voltage (V_{SNSCAP}) drops to below the capacitor voltage low level ($V_{ls(SNSCAP)}$), the low-side MOSFET is switched off (see Figure 7 (t2)). After a short delay, the high-side MOSFET is switched on. Figure 7 shows that the switching frequency is a result of this switching behavior. In a frequency controlled system, the frequency is a control parameter and the output power is a result. The TEA9026T regulates the power and the frequency is a result.

The difference between the high and low capacitor voltage level is a measure of the delivered output power. The value of the primary optocurrent, defined by the secondary TL431 circuitry, determines the difference between the high and low capacitor voltages.

Figure 7 also shows the behavior at a transient. If the output load increases, the current pulled out of the SNSFB pin decreases. The result is that the TEA9026T increases the high-level capacitor voltage and lowers the low-level capacitor voltage. According to Equation 1, the output power increases and eventually the output voltage increases to its regulation level.

To minimize no-load input power of the system, the primary current into the optocoupler is continuously regulated to 85 µA (see Section 8.5).

8.3.2 Output voltage start-up

The system controls the output power by regulating the primary V_{Cr} (see Section 8.3). When the system is in regulation and the output voltage is stabilized, a small change in ΔV_{Cr} corresponds to a small change in the output current (see Equation 2).

$$P_{out} = V_{out} \times I_{out} \sim V_{boost} \times I_{boost} = \Delta V_{Cr} \times C_r \times f_{sw} \times V_{boost}$$

$$I_{out} \approx C_r \times f_{sw} \times V_{boost} \times \frac{\Delta V_{Cr}}{V_{out}} \quad (2)$$

However, before start-up, when the output voltage is around zero, a small capacitor voltage increase (ΔV_{Cr}) corresponds to a substantial output current increase. So, at start-up, the divided ΔV_{Cr} voltage (ΔV_{SNSCAP}) is slowly increased from a minimum value to the regulation level. As a result, the system starts up at a higher frequency. The GATELS resistor sets the starting value of the ΔV_{SNSCAP}.

8.4 Modes of operation

Figure 8 shows the control curve between the output power and the voltage difference between the high and low capacitor voltage levels.

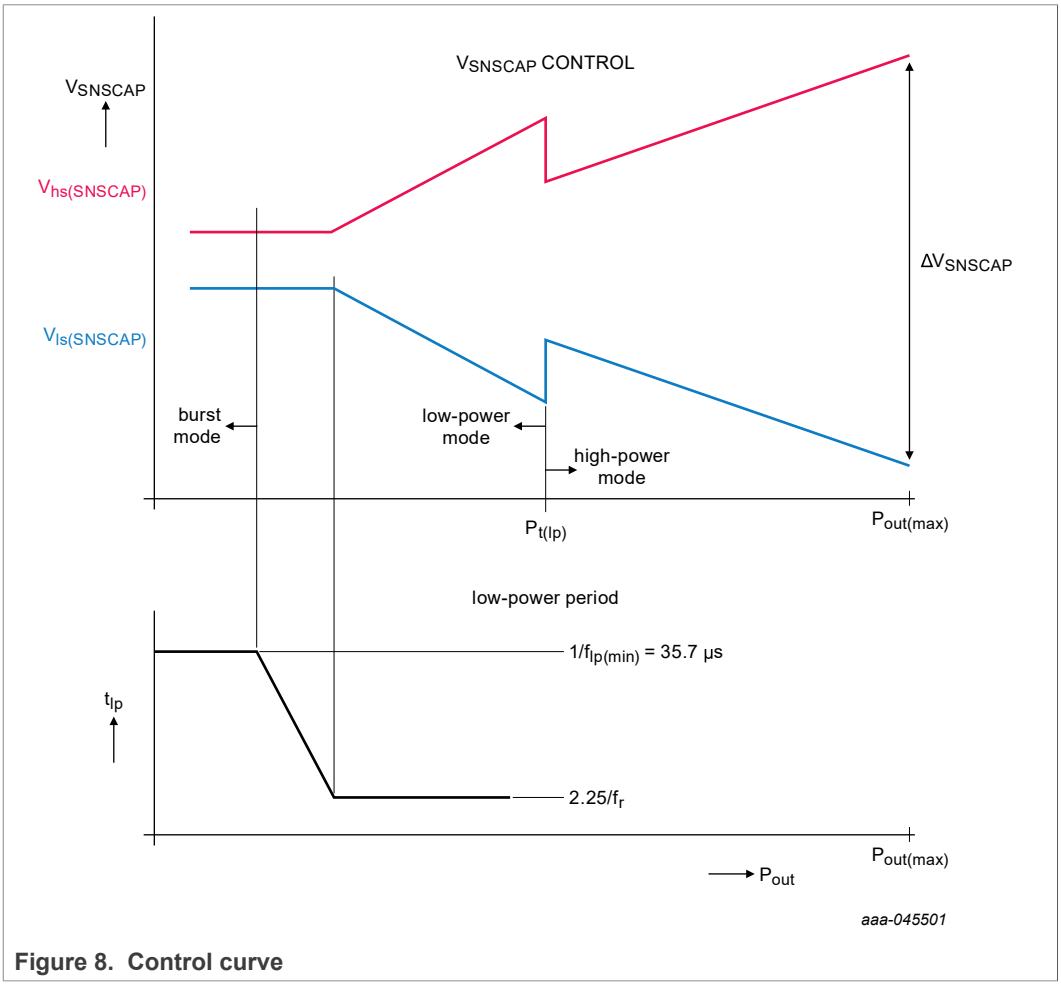


Figure 8. Control curve

When the output power (P_{out}) is at its maximum, the low capacitor voltage level ($V_{ls(SNSCAP)}$) is at its minimum and the high capacitor voltage ($V_{hs(SNSCAP)}$) is at its maximum level. According to Equation 1 in Section 8.3, the maximum ΔV_{SNSCAP} ($V_{hs(SNSCAP)} - V_{ls(SNSCAP)}$), which is the divided ΔV_{Cr} voltage, corresponds to the maximum output power.

When the output load decreases, the ΔV_{SNSCAP} voltage decreases. As a result, the output power decreases and the output voltage is regulated. This mode is called high-power mode.

When the output power drops to below the transition level ($P_{t(lp)}$), the system enters the low-power mode.

To compensate for the hold period, ΔV_{SNSCAP} is initially increased at entering the low-power mode (see Section 8.4.2). In low-power mode, the output power is initially regulated by adapting ΔV_{SNSCAP}, until it reaches a minimum. Then, the output power is regulated by lowering the duty cycle of the low-power mode with a fixed ΔV_{SNSCAP} until the period time of a low-power cycle reaches a maximum ($1 / f_{lp(min)}$). The system enters the burst mode (see Section 8.4.3).

8.4.1 High-power mode

In high-power mode, the system operates as described in Section 8.3.1. Figure 9 shows a flow diagram of the high-power mode.

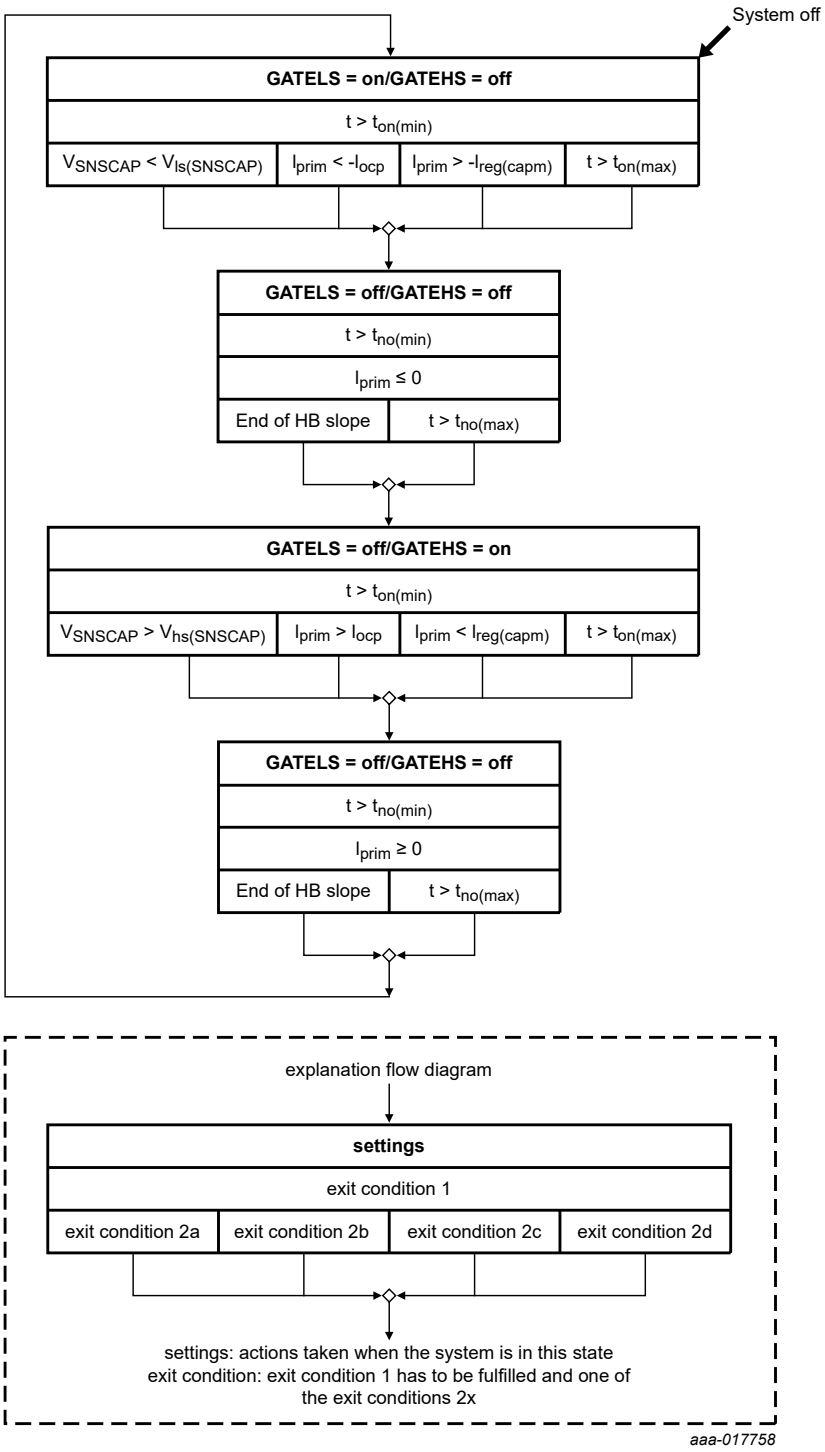


Figure 9. High-power mode flow diagram

When the system is off, GATELS is on and GATEHS is off. The external bootstrap buffer capacitor (C_{SUPHS}) is charged via the SUPREG pin and an external diode. The system remains in this state for at least the minimum on-time ($t_{on(min)}$) of GATELS. Before entering the next state, one of the following conditions must be fulfilled:

- The V_{SNSCAP} voltage drops to below the minimum V_{SNSCAP} voltage ($V_{ls(SNSCAP)}$)

- The measured current exceeds the OCP level (see Section 8.7.4)
- The system is close to capacitive mode (see Section 8.7.3)
- The maximum on-time ($t_{on(max)}$), a protection that maximizes the time the high-side or low-side MOSFET is kept on, is exceeded.

In the next state, to avoid false detection of the HB peak voltage, the system waits until the minimum non-overlap time ($t_{no(min)}$) is exceeded. When it is exceeded, the system starts to detect the end (= peak voltage) of the HB node. When it detects the peak of the HB node and the measured resonant current is negative (or zero), it enters the next state.

If the system does not detect a peak at the HB node, it also enters the next state when the maximum non-overlap time ($t_{no(max)}$) is exceeded under the condition of a negative (or zero) resonant current.

Finally, the third and fourth states (see Figure 9) describe the GATEHS and GATEHS to GATELS transition criteria which are the inverse of the first two states.

8.4.2 Low-power mode

A newly introduced low-power mode ensures high efficiency at lower loads, by keeping a high output current for each conversion cycle in combination with periods of not switching. It is a special type of burst mode.

When the output power drops to below the $P_{t(lp)}$ level, the system enters the low-power mode (see Figure 8 and Figure 10). It continues switching for 3 half-cycles (low-side, high-side, low-side) with a fixed duty cycle of 67 %. To ensure a constant output power level, it increases the energy per cycle ($V_{hs(SNSCAP)} - V_{ls(SNSCAP)}$) at the same time. So 1/3 of the time the converter is in a "hold" period. The result is a 33 % magnetization and switching losses reduction.

When the low-power frequency drops to below its minimum frequency at entering the low-power mode, the “hold” period is minimized to half a ringing time of the HB node.

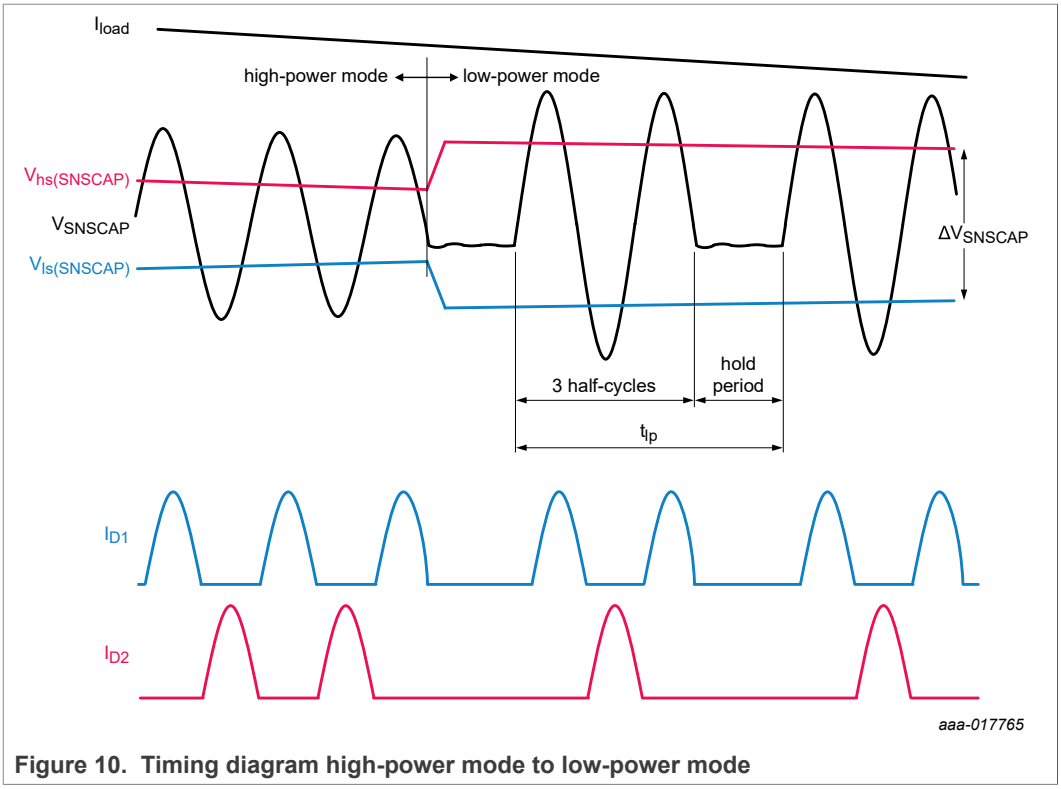


Figure 10. Timing diagram high-power mode to low-power mode

As the system continuously tracks the primary capacitor voltage, it knows exactly when to enter the "hold" period. It can also continue again at exactly the correct voltage and current levels of the resonant converter. In this way, a "hold" period can be introduced which reduces the magnetization and switching losses without any additional losses. The currents I_{D1} and I_{D2} (see Figure 10) are the secondary currents through diodes D1 and D2 (see Figure 22).

When in the low-power mode the output power is further reduced, the amount of energy per cycle (= ΔV_{SNSCAP}) is reduced and the duty cycle remains the same (see Figure 11).

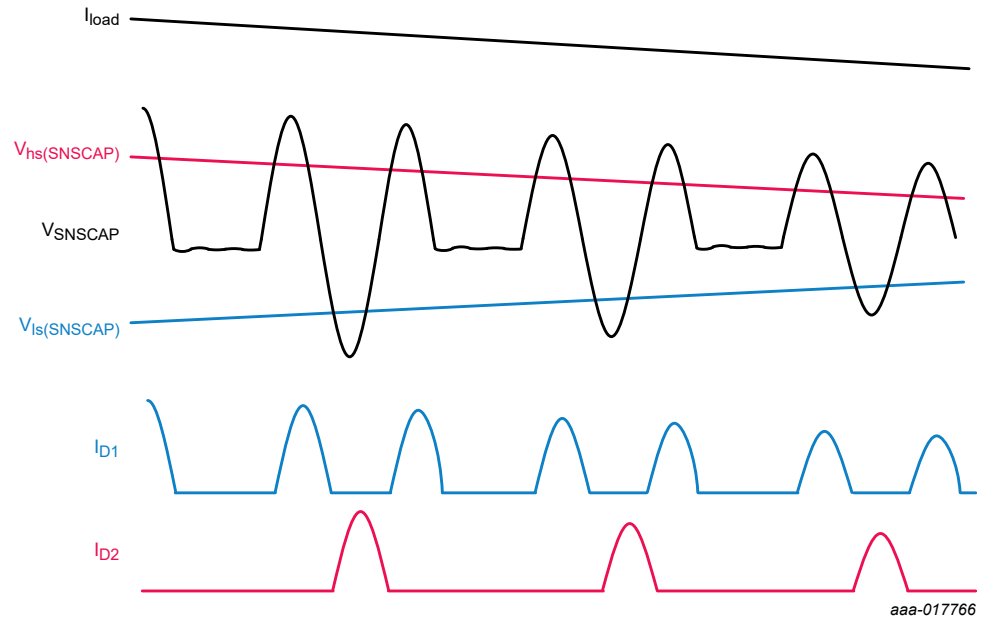


Figure 11. Low-power mode, lowering the energy per cycle (ΔV_{SNSCAP})

When, in low-power mode, the minimum energy per cycle is reached, the duty cycle regulates the output power (see Figure 12). Increasing the "hold" period lowers the duty cycle.

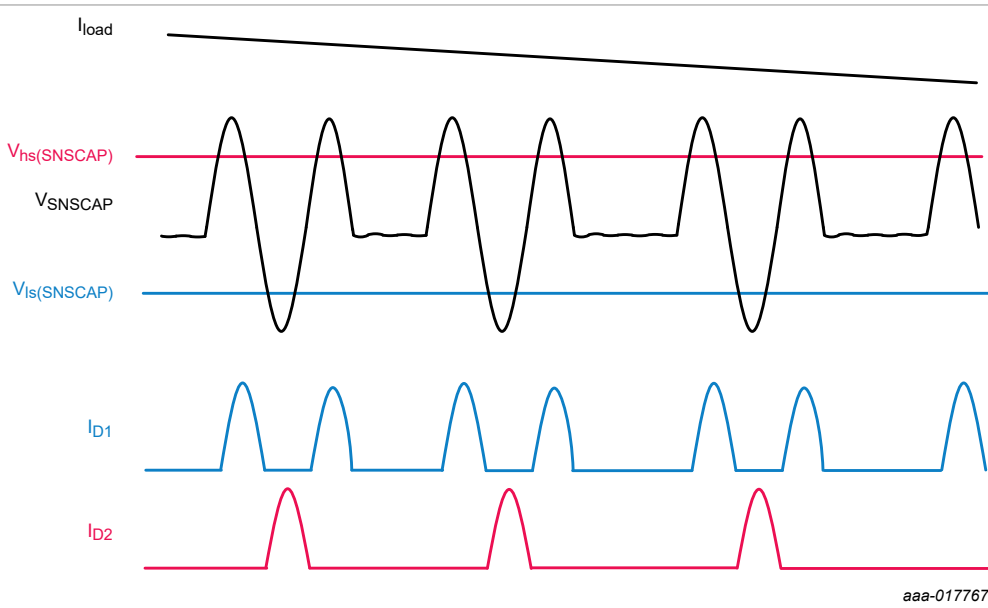


Figure 12. Low-power mode, lowering the duty cycle

To avoid audible noise, the system reduces the duty cycle until the frequency reaches $f_{lp(min)}$ (28 kHz). The actual frequency can be lower, because the high-side switch turns on at the next peak of the half-bridge node. If the output power is lowered further, the system enters the burst mode.

8.4.3 Burst mode

In burst mode, the system alternates between operating in low-power mode and an extended hold state (see Figure 13). Because of this additional extended hold period, the magnetization and switching losses are further reduced. So, the efficiency of the system is increased.

Figure 13 shows that all operating frequencies are outside the audible area. The minimum low-power frequency is 28 kHz. Within a low-power period, the system is switching at the resonant frequency of the converter, which is typically between 50 kHz and 200 kHz.

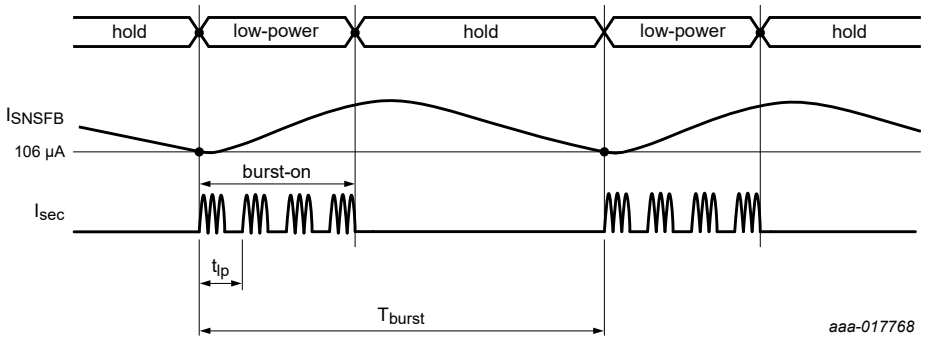


Figure 13. Burst mode

The burst frequency (1 / t_{burst}) is continuously regulated to a predefined value, which can be set externally to 800 Hz or 1600 Hz. I_{sec} is the secondary current flowing through either diode D1 or D2 (see Figure 22).

When the primary optocurrent (I_{SNSFB}) drops to below 106 µA, a new burst-on period is started. The end of the burst-on period depends on the calculated number of low-power cycles. The number of low-power cycles within a burst-on is continuously adjusted so that the burst period is at least the period defined by the setting (see Figure 14).

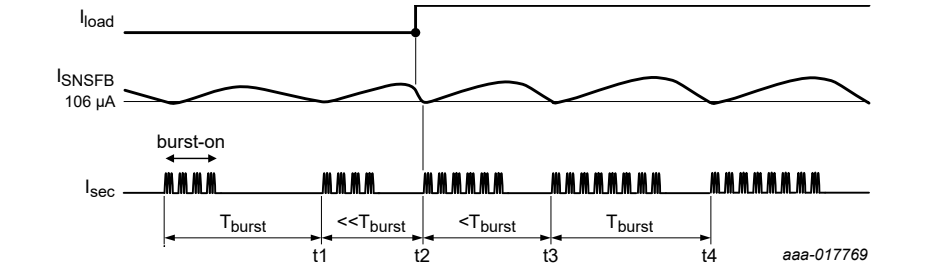


Figure 14. Burst mode: Regulating the number of low-power cycles

The system continuously measures the burst period from the start of the previous burst-on period to a new burst-on period. At t1, the measured burst period (T_{burst}) equals the required T_{burst}. So, the next number of low-power cycles equals the number of previous low-power cycles. At a constant output power, the system expects that when the next burst-on period has the same number of low-power cycles as the previous burst-on period, the burst period (T_{burst}) remains constant.

At a positive transient (t2), a new low-power cycle is started immediately to minimize the drop in output voltage. The measured time period, at time t2, is below the targeted burst period. The system increases the number of burst cycles. At t3, it measures the burst

period again. In this example, the burst period is still below the targeted burst period. So, the system increases the number of low-power cycles again and again until the measured burst period equals the target burst period, which occurs at t4.

8.5 Optobias regulation

In a typical application, the output voltage is sensed using a TL431 and connected to the SNSFB pin of the TEA9026T via an optocoupler (see Figure 22). Because of the behavior of the TL431, the current through the optocoupler is at the maximum level when the output power is at the minimum level. It is therefore one of the most critical parameters to achieve the required no-load input power. To achieve maximum efficiency at low load/no-load, the TEA9026T continuously regulates the optocurrent to a low level that is independent of the output load.

A very low optocurrent reduces the transient response of the system, because of the parasitic capacitance at the optocoupler collector. So, the TEA9026T applies a fixed voltage at the SNSFB pin. It measures the current through the optocoupler which defines the required output power. Via an additional internal circuitry, which adds an offset to the required output power, the optocurrent is continuously (slowly) regulated to the $I_{reg(SNSFB)}$ level (= 85 µA). This level is independent of the output power.

At a positive load transient, the optocurrent initially decreases (see Figure 7; I_{SNSFB}). The TEA9026T immediately increases the ΔV_{SNSCAP} which again increases the output power.

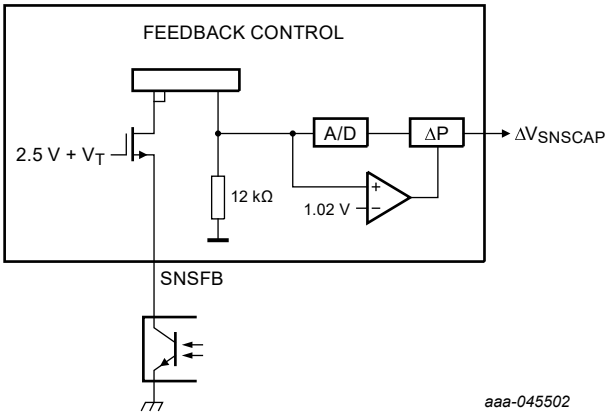


Figure 15. Optobias regulation

Figure 15 shows that when the optocurrent decreases, the internal voltage across the 12 kΩ resistor drops to below the targeted level of 1020 mV (= 85 µA × 12 kΩ). The TEA9026T then slowly increases an additional offset at the power level (ΔP). It continues to increase the additional offset until the optocurrent reaches the target of 85 µA. At a negative transient, the additional offset to the power level is decreased. As a result, the output voltage decreases which again decreases the optocurrent. In this way, the optocurrent is continuously regulated to the $I_{reg(SNSFB)}$ level (see Figure 7).

The behavior of the internal circuitry connected to the SNSFB pin is the same as the behavior of the traditional circuitry. The fixed voltage at the SNSFB pin and the continuous regulation of the optocurrent level does not influence the regulation level. The advantage, however, is a reduction in no-load input power and an optimization of the transient response.

When the system operates in low-power mode at the minimum energy per cycle and at minimum duty cycle, it can no longer reduce the optocurrent level to the $I_{reg(SNSFB)}$

target (≈ 85 µA). If the output power decreases further and the optocurrent increases to above the level of $I_{start(burst)}$ (≈ 106 µA), the burst mode is triggered. When the output power drops to below this level again, a new burst cycle is started (see Figure 13 and Figure 14).

8.6 Mains input voltage compensation

The TEA9026T is especially designed to operate with a wide range of input voltages. So, it can be directly connected to the mains. In that case, a PFC may be excluded. The implication is that the LLC must be designed for a wide range of input voltage variation. According to Equation 3, the output power equals:

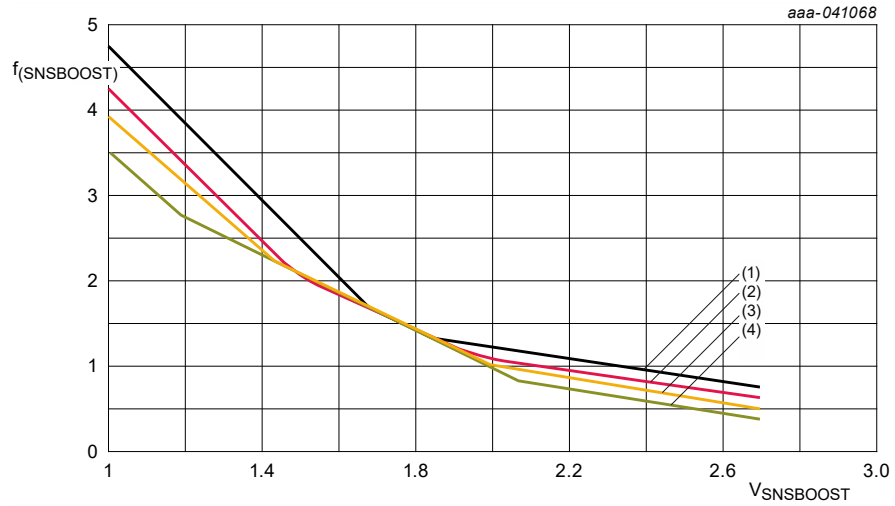
$$P_{out} = \Delta V_{Cr} \times C_r \times f_{sw} \times V_{boost} \quad (3)$$

Knowing that the resonant capacitor (C_r) is a constant, the relation between the output power and ΔV_{cr} is: $P_{out} \cdot \frac{1}{f_{sw} \cdot V_{boost}} \sim \Delta V_{Cr}$.

Figure 16 shows that the relation between ctrl_power signal and ΔV_{Cr} is:

$Ctrl\_power \cdot f(SNSBOOST) = \Delta V_{SNSCAP}$.

As ΔV_{SNSCAP} is related to ΔV_{Cr}, Ctrl_power is a measure of the output power when f(SNSBOOST) is not only related to the LLC input voltage (V_{boost}). It also compensates for the switching frequency which depends on the input voltage.



compensation value = $f_{SNSBOOST}$

(1) Compensation curve 1
(2) Compensation curve 2
(3) Compensation curve 3
(4) Compensation curve 4

Figure 16. Possible settings for f(SNSBOOST)

As the internal Ctrl_power signal is related to the output power of the converter, the OPP level and the mode transition levels (HP to LP and LP to burst) are derived from this signal.

8.7 Protections

Table 5 gives an overview of the available protections.

Table 5. Protections

Protection	Description	Action
UVP SUPIC/ SUPREG	undervoltage protection SUPIC/ SUPREG pins	LLC = off; recharge via SUPHV; restart when $V_{SUPIC} > V_{start(SUPIC)}$ and $V_{SUPREG} > V_{start(SUPREG)}$
UVP SUPHS	undervoltage protection SUPHS pin	GATEHS = off
UVP SNSBOOST	undervoltage protection boost	LLC = off; restart when $V_{SNSBOOST} > V_{start(SNSBOOST)}$
OVP output	overvoltage protection output	safe restart after 5 consecutive cycles [1] [2]
CMR	capacitive mode regulation	system ensures that mode of operation is inductive
OCP	overcurrent protection	switch off cycle-by-cycle; safe restart after 5 consecutive cycles [2]

Table 5. Protections...*continued*

Protection	Description	Action
OTP	internal overtemperature protection	restart when the temperature has dropped to below 140 °C[2]
OPP	overpower protection	safe restart[2]

[1] Can be longer due to the sharing of the internal ADC converter.
[2] Safe restart implies that the system stops switching and restarts after 1 sec.

When the system is in a protection, the SUPIC voltage is regulated to its start level via the SUPHV pin.

8.7.1 Undervoltage protection (UVP)

8.7.1.1 UVP SUPIC/SUPREG

When the voltage on the SUPIC pin or the SUPREG pin is below its undervoltage level $V_{uvp(SUPIC)}$ / $V_{uvp(SUPREG)}$, the LLC converter stops switching. The capacitors at the SUPIC and SUPREG pins are recharged via the SUPHV pin (see Figure 5). The SNSBOOST pin is pulled low. When the supply voltages exceed their start levels, the system restarts.

8.7.1.2 UVP SUPHS

To ensure a minimum drive voltage at the high-side driver output (GATEHS), this driver is kept off when its voltage is below the minimum level ($V_{SUPHS} < V_{rst(SUPHS)}$).

8.7.1.3 UVP boost

The LLC input voltage is measured via a resistive divider connected to the SNSBOOST pin. The voltage at the SNSBOOST pin must exceed the start level ($V_{SNSBOOST} > V_{start(SNSBOOST)}$) before the system is allowed to start switching.

When the system is operating and the voltage at the SNSBOOST pin drops to below the minimum level ($V_{SNSBOOST} < V_{uvp(SNSBOOST)}$), the LLC converter stops switching. When it exceeds the start level, it restarts.

8.7.2 Overvoltage protection (OVP)

When the voltage at the SNSOUT pin exceeds the $V_{ovp(SNSOUT)}$ level for at least 5 consecutive switching cycles, the OVP protection is triggered. The voltage at the SNSOUT pin is internally measured via an ADC converter. As the same ADC converter toggles between measuring the SNSOUT and SNSBOOST pins (see Figure 1), there is an additional delay before the OVP is triggered. OVP is a safe-restart protection.

8.7.3 Capacitive mode regulation (CMR)

The TEA9026T has a capacitive mode regulation (CMR) which ensures that the system is always operating in inductive mode and avoids operation in capacitive mode.

At lower input voltage or higher output power and depending on the resonant design, the resonant current can already approach zero before the capacitor voltage reaches the regulation level.

When the resonant current has changed polarity before the switches are turned off and the other switch is turned on, hard switching occurs. This event is called capacitive mode. To avoid that the system operates in capacitive mode, the system also switches off the high-side/low-side switch when the resonant current approaches zero.

Figure 17 shows the signals that occur when a resonant converter is switching in CMR mode. At t1 (and also at t3), the low-side switch is on while the resonant current approaches zero before V_{SNSCAP} reaches $V_{ls(SNSCAP)}$. At t2, the resonant current is also close to changing polarity while the divided capacitor voltage (V_{SNSCAP}) has not reached the $V_{hs(SNSCAP)}$ level yet. To avoid a turn-off of the high-side switch at a negative current or the low-side at a positive current, the system also turns off the high-side/low-side switch when the primary current approaches zero. So at t2, the high-side switch is turned off because the primary current is close to zero. At t3 (and also at t1), the low-side switch is turned off, although V_{SNSCAP} did not reach the regulation level ($V_{ls(SNSCAP)}$) yet. The primary current is measured via an external sense resistor connected to the SNSCUR pin. The capacitive mode protection levels are $V_{reg(capm)}$ (−100 mV and +100 mV, respectively).

In this mode, the amount of output power is reduced and the output voltage decreases.

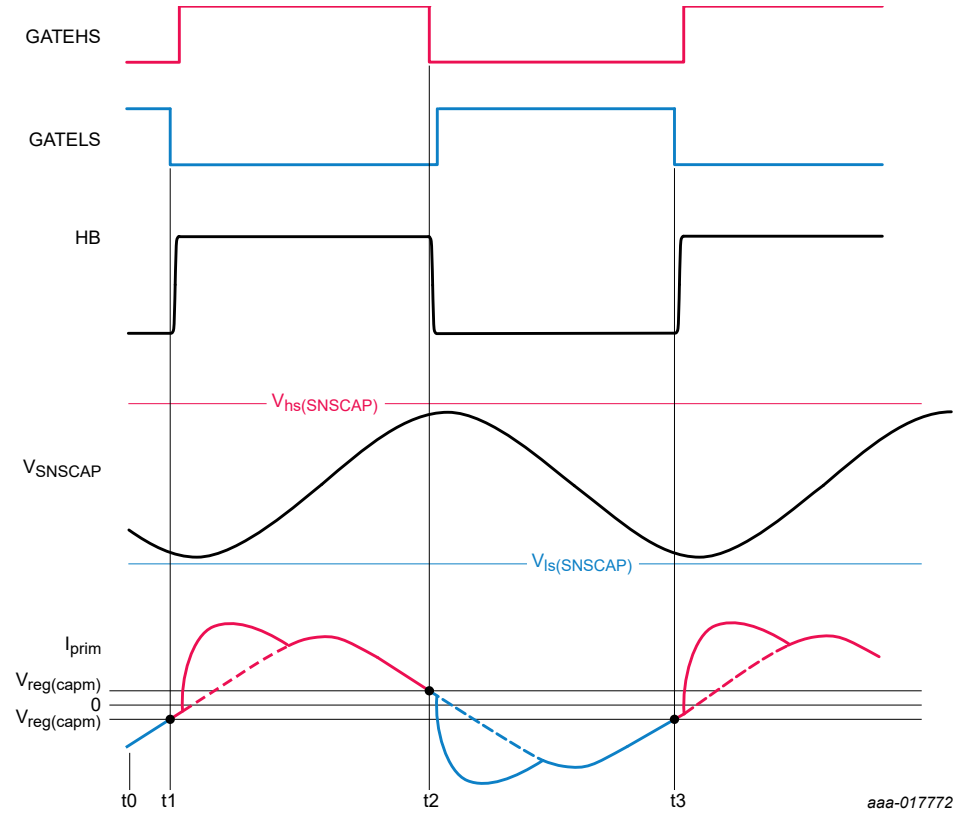


Figure 17. Near capacitive mode switching

8.7.4 Overcurrent protection (OCP)

The system measures the primary current continuously via a sense resistor connected to the SNSCUR pin. If the measured voltage exceeds the overcurrent level (V_{ocp}), the corresponding switch (GATELS/GATEHS) is turned off, but the system continuous switching. In this way, the primary current is limited to the OCP level. If the OCP level

is exceeded for 5 consecutive cycles (GATELS and/or GATEHS), the system stops switching and enters the safe-restart OCP protection mode.

8.7.5 Overtemperature protection (OTP)

When the internal junction temperature exceeds the T_{otp} level, the overtemperature protection is triggered. When the temperature has dropped to below 140 °C, the system restarts.

8.7.6 Overpower protection (OPP)

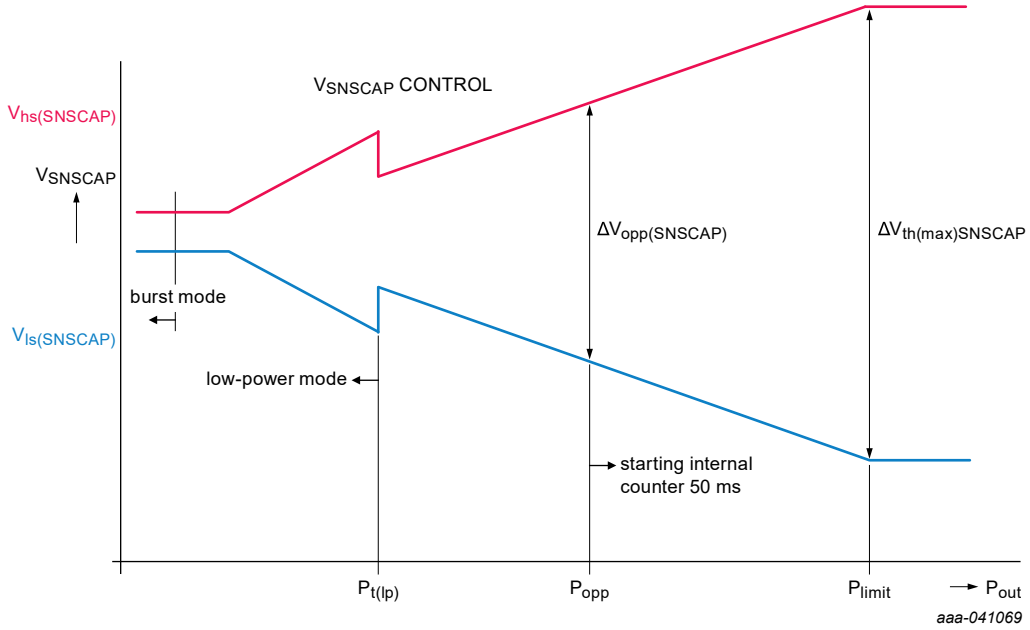


Figure 18. TEA9026T overpower protection

When the ΔV_{SNSCAP} ($V_{hs(SNSCAP)} - V_{ls(SNSCAP)}$) exceeds the OPP voltage difference ($\Delta V_{opp(SNSCAP)}$), an internal counter is started (see Figure 18). When this counter exceeds $t_{d(opp)}$ (50 ms), the system enters a safe restart protection. The external capacitive/resistive divider connected to the SNSCAP pin in combination with the SNSBOOST compensation curve (see Figure 16) must be chosen to meet the required system P_{opp} level.

The voltage difference between $V_{hs(SNSCAP)}$ and $V_{ls(SNSCAP)}$ is limited to $\Delta V_{th(max)SNSCAP}$. The resulting power limit (P_{limit}) level is also related to the external capacitive/resistive divider connected to the SNSCAP pin in combination with the SNSBOOST compensation curve (see Figure 16). If the output of the LLC converter requires additional power, the output voltage drops because the power the LLC converter delivers is limited.

8.8 External settings

Before the system starts switching, it reads the external settings. Using specific resistor values at the GATELS, SNSSET, and SNSOUT pins, several internal settings can be defined.

8.8.1 Low-power mode to burst mode level

As described in Section 8.6, the internal Ctrl_power signal is related to the output power. When this signal drops below a threshold level, the system enters burst mode.

However, at lower loads the Ctrl_power signal is less accurate as the frequency as function of the input voltage is different. Delays are also significant at lower loads.

So, external settings can adjust the threshold level at which the system enters burst mode (see Figure 19).

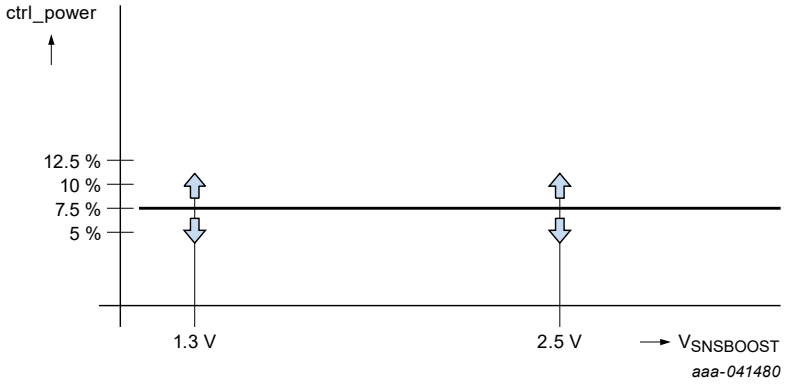


Figure 19. Possible settings low-power mode to burst mode level

The low-power mode to burst mode level can be set independently to 5 %, 7.5 %, 10 %, or 12.5 % at an SNSBOOST voltage of 1.3 V and 2.5 V. In this way, the threshold level can be optimized over the full mains input voltage range to meet the low-load requirements.

8.8.2 SNSOUT setting

Figure 20 shows how the low-power mode to burst mode level at $V_{SNSBOOST}$ = 1.3 V can be set using the external resistor connected to the SNSOUT pin.

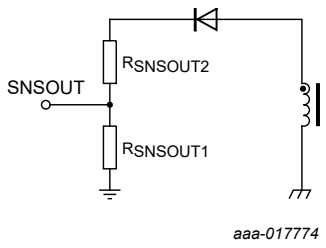


Figure 20. External setting of the burst frequency

Table 6. External setting of the burst frequency

$R_{SNSOUT1}$ (kΩ)	Low-power mode to burst mode level at $V_{SNSBOOST}$ = 1.3 V (%)
22	5
15	7.5
10	10
6.8	12.5

The absolute value of the resistor connected between the SNSOUT pin and ground ($R_{SNSOUT1}$) defines the burst frequency. As the resistor value is also used for internal calibration, an accurate resistor of 1 % according to Table 6 is required. The OVP level can be set using resistor $R_{SNSOUT2}$.

8.8.3 SNSSET settings

Variations of the SNSBOOST compensation curve (f(SNSBOOST)) and the burst frequency can be set using resistor RSNSSET1, which is connected to the SNSSET pin (see Figure 21).

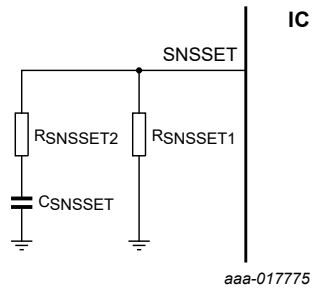


Figure 21. External setting of the SNSSET pin

Table 7. General settings $R_{SNSSET1}$

$R_{SNSSET1}$ (kΩ)	Compensation curve	Burst frequency (Hz)
< 10	no start-up	
53.6	1	800
61.9	2	800
71.5	3	800
82.5	4	800
95.3	1	1600
110	2	1600
127	3	1600
147	4	1600

$R_{SNSSET1}$ defines the compensation curve according to Figure 19 and the burst frequency. A low burst frequency is best for minimum audible noise. However, a high burst frequency minimizes the output voltage ripple. The other resistor at the SNSSET

pin, RSNSSET2, defines the low-power mode to burst mode level at $V_{SNSBOOST}$ = 2.5 V and the high power to low power transition level.

Table 8. General settings $R_{SNSSET2}$

$R_{SNSSET2}$ (kΩ)	LP-BM level at 2.5 V (%)	HP-LP level (%)
1	5	30
6.8	7.5	30
15	10	30
27	12.5	30
47	5	20
82	7.5	20
180	10	20
open	12.5	20

8.9 SNSBOOST communication protocol

The TEA9026T can be used in an application consisting of multiple converters. When the TEA9026T is in start-up or protection mode, the SNSBOOST pin is pulled low. During normal switching, the SNSBOOST voltage reflects the LLC input voltage.

If the SNSBOOST pin is pulled down externally, the TEA9026T stops switching when the SNSBOOST voltage is below the $V_{uvp(SNSBOOST)}$ level.

8.9.1 Fast protection reset

The SUPIC pin is regulated to the $V_{start(SUPIC)}$ level when a protection is triggered. It remains in this protection mode until the safe restart time of 1 second is exceeded or the capacitor at the LLC input, which the SUPHV is connected to, is discharged. If necessary, this delay can be shortened.

When the TEA9026T is in the protection state, it pulls down the SNSBOOST pin with a current of $I_{pd(SNSBOOST)}$. If the SNSBOOST voltage is increased externally to above the $V_{uvp(SNSBOOST)}$ voltage, the LLC converter releases all protections and waits until the SNSBOOST pin exceeds its start level ($V_{start(SNSBOOST)}$).

9 Limiting values

Table 9. Limiting values

Symbol	Parameter	Conditions	Min	Max	Unit
Voltages					
V_{SUPHV}	voltage on pin SUPHV	maximum during mains surge; not repetitive	−0.4	+700	V
V_{SUPHS}	voltage on pin SUPHS		V_{HB}	V_{HB} + 14	V
V_{HB}	voltage on pin HB	maximum during mains surge; not repetitive	−3	+700	V
		t < 1 µs	−14	-	V
$SR_{max(HB)}$	maximum slew rate on pin HB	[1]	−70	+70	V/ns
V_{SUPIC}	voltage on pin SUPIC		−0.4	+36	V
V_{SUPREG}	voltage on pin SUPREG		−0.4	+12	V
V_{GATEHS}	voltage on pin GATEHS		V_{HB} − 0.4	V_{SUPHS} + 0.4	V
V_{GATELS}	voltage on pin GATELS		−0.4	V_{SUPREG} + 0.4	V
V_{SNSFB}	voltage on pin SNSFB		−0.4	+12	V
V_{SNSOUT}	voltage on pin SNSOUT		−0.4	+12	V
V_{SNSSET}	voltage on pin SNSSET		−0.4	+12	V
V_{SNSCUR}	voltage on pin SNSCUR		−0.4	+12	V
V_{SNSCAP}	voltage on pin SNSCAP		−0.4	+12	V
$V_{SNSBOOST}$	voltage on pin SNSBOOST		−0.4	+12	V
Currents					
I_{SUPHV}	current on pin SUPHV		-	20	mA
General					
P_{tot}	total power dissipation	T_{amb} < 75 °C	-	0.7	W
T_{stg}	storage temperature		−55	+150	°C
T_j	junction temperature		−40	+150	°C

Table 9. Limiting values...*continued*

Symbol	Parameter	Conditions	Min	Max	Unit
Latch-up					
I_{lu}	latch-up current	all pins; according to JEDEC Standard 78D	−100	+100	mA
Electrostatic discharge (ESD)					
V_{ESD}	electrostatic discharge voltage	human body model			
		pins SUPHV, SUPHS, GATEHS, and HB	−1000	+1000	V
		other pins	−2000	+2000	V
		charged device model; all pins	−500	+500	V

[1] To prevent erroneous operation due to high HB dV/dt disturbances, a maximum slew rate of 25 V/ns is recommended.

10 Thermal characteristics

Table 10. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	In free air; JEDEC test board	107	K/W
$R_{th(j-c)}$	thermal resistance from junction to case	In free air; JEDEC test board	60	K/W

11 Characteristics

Table 11. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SUPHV pin						
$I_{lim(SUPHV)}$	current limit on pin SUPHV	$V_{SUPIC} < V_{rst(SUPIC)}$	0.5	0.75	1.0	mA
$I_{off(SUPHV)}$	off-state current on pin SUPHV	V_{SUPIC} = 15 V	-	0.5	0.9	µA
$\Delta V_{I(SUPHV-SUPIC)}$	input voltage difference between pin SUPHV and pin SUPIC	I_{SUPHV} = 20 mA	-	7	-	V
SUPIC pin						
$V_{start(SUPIC)}$	start voltage on pin SUPIC		18.3	19.1	19.8	V
$V_{start(hys)SUPIC}$	start voltage hysteresis on pin SUPIC		-	−0.7	-	V
$V_{low(hys)SUPIC}$	low voltage hysteresis on pin SUPIC		-	0.9	-	V
$V_{low(SUPIC)}$	low voltage on pin SUPIC	$V_{uvp(SUPIC)}$ = 13.2 V; tracks with $V_{uvp(SUPIC)}$	13.5	14.0	14.5	V
$V_{uvp(SUPIC)}$	undervoltage protection voltage on pin SUPIC		12.7	13.2	13.7	V
$V_{rst(SUPIC)}$	reset voltage on pin SUPIC		-	3.5	-	V
$I_{CC(SUPIC)}$	supply current on pin SUPIC	operating mode; f_{HB} = 100 kHz; GATEHS/GATELS open; I_{SNSFB} = −85 µA; I_{SNSCAP} = −100 µA	-	5.6	-	mA
		protection; I_{SNSFB} = 0 µA; I_{SNSCAP} = −100 µA	2.3	3.0	3.7	mA
		burst mode; I_{SNSFB} = −106 µA; I_{SNSCAP} = −100 µA	-	0.7	-	mA
SUPREG pin						
$V_{intregd(SUPREG)}$	internal regulated voltage on pin SUPREG	V_{SUPIC} > 13.8 V; I_{SUPREG} = 50 mA	10.6	11.0	11.4	V
$V_{reg(acc)SUPREG}$	regulator voltage accuracy on pin SUPREG	V_{SUPIC} > 13.8 V; 10 µA < I_{SUPREG} < 20 mA	−150	−100	−50	mV
$I_{lim(SUPREG)}$	current limit on pin SUPREG	V_{SUPIC} = 19.5 V	−44	−37	−30	mA
$V_{uvp(SUPREG)}$	undervoltage protection voltage on pin SUPREG		8.6	9.0	9.4	V
SNSCAP pin						
$V_{AV(regd)SNSCAP}$	regulated average voltage on pin SNSCAP	regulated average of $V_{hs(SNSCAP)}$ and $V_{ls(SNSCAP)}$	-	2.50	-	V
$I_{bias(max)SNSCAP}$	maximum bias current on pin SNSCAP		−245	−210	−175	µA
$\Delta V_{th(max)SNSCAP}$	maximum threshold voltage difference on pin SNSCAP	$V_{hs(SNSCAP)} - V_{ls(SNSCAP)}$; P_{out} = 150 %; $V_{SNSBOOST}$ = 1.0 V	2.85	3.00	3.15	V

Table 11. Characteristics...*continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Overpower protection						
$t_{PD(SNSCAP)}$	propagation delay on pin SNSCAP	from crossing $V_{ls(SNSCAP)}$/ $V_{hs(SNSCAP)}$ level to GATELS/ GATEHS switch-off	-	150	-	ns
$t_{d(opp)}$	overpower protection delay time		40	50	60	ms
$t_{d(restart)}$	restart delay time		0.8	1.0	1.2	s
SNSCUR pin						
$V_{bias(SNSCUR)}$	bias voltage on pin SNSCUR		2.4	2.5	2.6	V
$R_{O(SNSCUR)}$	output resistance on pin SNSCUR		-	60	-	kΩ
V_{ocp}	overcurrent protection voltage	positive level; $V_{SNSCUR} - V_{bias(SNSCUR)}$	1.35	1.50	1.65	V
		negative level; $V_{SNSCUR} - V_{bias(SNSCUR)}$	−1.65	−1.50	−1.35	V
$V_{reg(capm)}$	capacitive mode regulation voltage	positive level; $V_{SNSCUR} - V_{bias(SNSCUR)}$	85	100	115	mV
		negative level; $V_{SNSCUR} - V_{bias(SNSCUR)}$	−115	−100	−85	mV
$V_{det(zero)}$	zero detection voltage	detected as ≥ 0	-	−13	-	mV
		detected as ≤ 0	-	13	-	mV
SNSBOOST pin						
$V_{start(SNSBOOST)}$	start voltage on pin SNSBOOST		1.30	1.40	1.50	V
$V_{uvp(SNSBOOST)}$	undervoltage protection voltage on pin SNSBOOST		0.80	0.85	0.90	V
$R_{pd(SNSBOOST)}$	pull-down resistance on pin SNSBOOST	at protection activation	-	550	-	Ω
$I_{pd(SNSBOOST)}$	pull-down current on pin SNSBOOST	during active protection	94	110	127	µA
$I_{prot(SNSBOOST)}$	protection current on pin SNSBOOST		-	60	-	nA
SNSOUT pin						
$V_{ovp(SNSOUT)}$	overvoltage protection voltage on pin SNSOUT		3.36	3.50	3.64	V
$I_{prot(SNSOUT)}$	protection current on pin SNSOUT	for open pin	-	−60	-	nA
SNSFB pin						
$V_{bias(SNSFB)}$	bias voltage on pin SNSFB	I_{SNSFB} = −85 µA	2.2	2.5	2.8	V
Optobias regulator						
$I_{reg(SNSFB)}$	regulation current on pin SNSFB	$I_{start(burst)}$ = 106 µA; tracks with $I_{start(burst)}$	-	−85	-	µA
$I_{reg(max)SNSFB}$	maximum regulation current on pin SNSFB	$I_{start(burst)}$ = 106 µA; tracks with $I_{start(burst)}$	-	−310	-	µA

Table 11. Characteristics...*continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{reg(min)SNSFB}$	minimum regulation current on pin SNSFB	$I_{start(burst)}$ = 106 µA; tracks with $I_{start(burst)}$	-	−63	-	µA
Burst mode regulator						
$I_{start(burst)}$	burst mode start current	LLC burst mode	−123	−106	−89	µA
$I_{stop(burst)}$	burst mode stop current	LLC burst mode	-	−200	-	µA
GATELS and GATEHS pins						
$I_{source(GATEHS)}$	source current on pin GATEHS	$V_{GATEHS} - V_{HB}$ = 4 V	-	−340	-	mA
$I_{source(GATELS)}$	source current on pin GATELS	$V_{GATELS} - V_{GND}$ = 4 V	-	−340	-	mA
$I_{sink(GATEHS)}$	sink current on pin GATEHS	$V_{GATEHS} - V_{HB}$ = 2 V	-	580	-	mA
		$V_{GATEHS} - V_{HB}$ = 11 V	-	2	-	A
$I_{sink(GATELS)}$	sink current on pin GATELS	$V_{GATELS} - V_{GND}$ = 2 V	-	580	-	mA
		$V_{GATELS} - V_{GND}$ = 11 V	-	2	-	A
$V_{rst(SUPHS)}$	reset voltage on pin SUPHS		6.4	7.0	7.6	V
$V_{rst(hys)SUPHS}$	hysteresis of reset voltage on pin SUPHS	> $V_{rst(SUPHS)}$	-	0.6	-	V
$t_{on(min)}$	minimum on-time		-	0.83	-	µs
$t_{on(max)}$	maximum on-time		14.8	17.4	20.0	µs
t_{sweep}	sweep time	frequency; at start-up	1	12	14	ms
Low-power mode regulator						
$f_{lp(min)}$	minimum low-power mode frequency		25	28	31	kHz
Burst mode regulator						
$f_{burst(max)}$	maximum burst mode frequency	see Table 7 for related $R_{SNSSET1}$	-	800	-	Hz
		see Table 7 for related $R_{SNSSET1}$	-	1600	-	Hz
Settings sensor (SNSOUT, SNSSET, and GATELS pins)						
$I_{O(SNSOUT)}$	output current on pin SNSOUT	during $R_{SNSOUT1}$ measurement	-	−171	-	µA
$I_{O(SNSSET)}$	output current on pin SNSSET	during R_{SNSSET} measurement	-	−26.8	-	µA
$\Delta V_{O(GATELS-SUPREG)}$	output voltage difference between pin GATELS and pin SUPREG	during R_{GATELS} measurement	-	1.25	-	V
HB pin						
$(dV/dt)_{tno(min)}$	minimum non-overlap time rate of change of voltage		-	-	120	V/µs
$t_{no(min)}$	minimum non-overlap time		-	200	-	ns
$t_{no(max)}$	maximum non-overlap time		-	1.1	-	µs
T_{otp}	overtemperature protection trip		130	140	150	°C

12 Application information

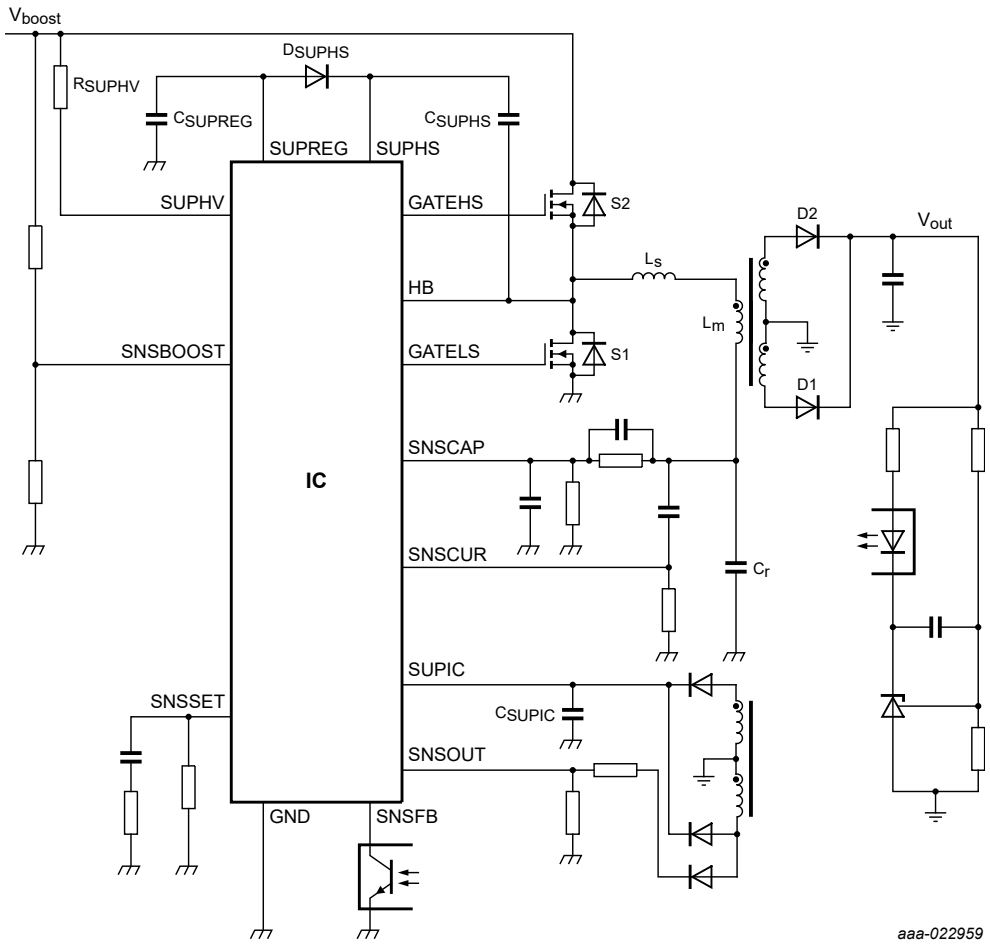
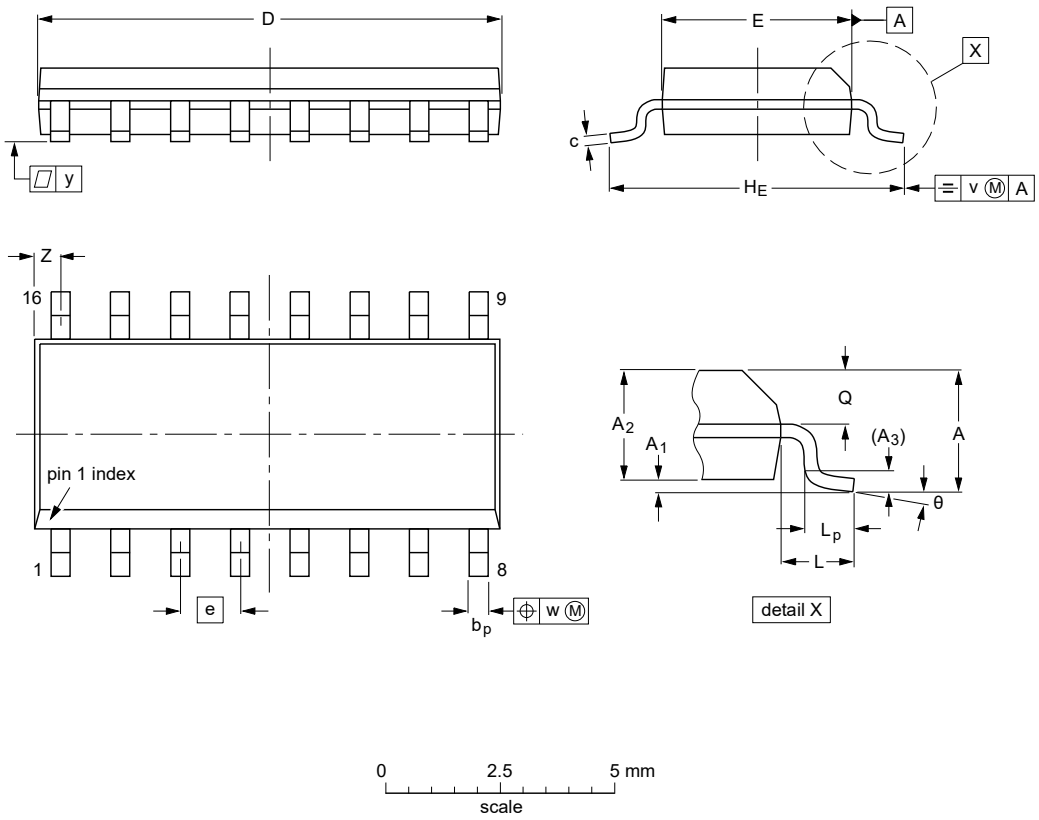


Figure 22. TEA9026T application diagram

13 Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Figure 23. Package outline SOT109-1 (SO16)

14 Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TEA9026T v.1.0	20220614	Product data sheet	-	-

15 Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

15.2 Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

15.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Suitability for use in non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document, including the legal information in that document, is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified vulnerabilities or may support established security standards or specifications with known limitations. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately.

Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP.

NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

15.4 Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

GreenChip — is a trademark of NXP B.V.

Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 14 June 2022
Document identifier: TEA9026T