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PATENT SPECIFICATION

DRAWINGS ATTACHED

Inventor: ERNEST JAMES MOOREY

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COMPLETE SPECIFICATION

Low Level D.C. Amplifier

We, DYNAMCO LIMITED, a British Company, of Hanworth Lane, Chertsey, Surrey, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to a low level D.C. amplifier.

The constantly increasing demand for lower level D.C. amplifiers with high input impedance, negligible drift and offset current facilities has resulted in the production of a D.C. amplifier which uses separate A.C. and D.C. channels. The circuit of such an amplifier is shown in Figure 1 of the accompanying drawings.

With the need to improve performance still further, however, it would appear that the practical limit of this "standard" type of amplifier is rapidly being approached.

Firstly, as the required level of voltage to be amplified decreases, the drift specification must be altered accordingly. This means that A.C. amplifier M_1 must have a larger gain, which means that for stability reasons the value of the accompanying R_2C_2 time constant must be increased. To increase the time constant it is possible to increase the value of either resistor R_2 or capacitor C_2. However the value of the resistor R_2 may not be made very large because of current noise considerations at the input of D.C. amplifier M_2. Therefore the capacitor C_2 must be increased but this gives rise to drift problems due to chemical e.m.f's and leakage of the dielectric of capacitor C_2. Also an increase in the value of the capacitor C_2 must be accompanied by an increase in the value of the capacitor C_1 which gives rise to offset current at the input due to the leakage of the capacitor C_1.

As the gain from the input terminal to the input of the amplifier M_2 at frequencies above chopper frequencies is essentially unity, then the input of the amplifier M_2 effectively becomes the sensitive input to the amplifier as a whole, accompanied by the input to the amplifier M_1—so that the noise effects are additive.

Furthermore, the loop gain to D.C. signals will be vastly different to that for A.C. signals. This could be a disadvantage for stability reasons as well as being wasteful.

A further point is that in general with separate A.C. and D.C. channels additional connections are made to the sensitive input (e.g. by way of capacitor C_1) which tends to give rise to thermal e.m.f's and capacitive leakage.

In order to meet the need for lower levels of voltage, lower drift levels, and lower offset currents while maintaining the high input impedance and wide frequency response times, the ideal amplifier would appear to be a single channel amplifier with a response from D.C. to high frequency while maintaining the above-mentioned properties.

One solution to the problem would be simply the removal of the capacitor C_1. The signal channel at all frequencies would then be via the amplifiers M_1 and M_2. When the input frequency approaches or exceeds the chopping frequency, the transfer function of the amplifier M_1 shows a wide variation of gain and phase. This makes stability impossible unless the loop gain of the system is less than unity at chopper frequency.

In order to achieve a reasonable response time, the chopper frequency must be made very high, i.e. greater than 1 Mc/s. This would give rise to very high offset input currents.

The proposed system to be considered is intended to overcome all of the previous difficulties.

According to the invention there is provided a D.C. amplifier including a signal channeling network having at least two outputs, at least two A.C. amplifiers connected respectively to the outputs of the channeling network, a summing network connected to respective outputs of the amplifiers and means to switch said amplifiers in sequence so that each amplifier is used alternately to provide continuous or substantially continuous amplification of an input signal at the output of the summing network, the A.C. amplifiers each having its input and output restored to earth potential or to a reference voltage during the periods of non-use.

It is preferred to use a circuit employing two chopper channels although three or more are possible, the signal being time shared between the channels. The preferred embodiment of the invention has a single A.C. amplifier arranged between two synchronously operated choppers in each channel.

Embodiments of the invention will now be described by way of example with reference to Figures 2 to 6 of the accompanying drawings in which:

Figure 2 is a circuit diagram showing a low level D.C. amplifier in accordance with the invention having two chopper channels;

Figures 3A and 3B show respectively wave forms of amplified D.C. and A.C. signals;

Figure 4 shows the gain/frequency characteristics for the known arrangement of Figure 1 and of the present invention;

Figure 5 shows further circuitry details of the invention in which the choppers are in the form of field effect transistors;

Figure 6A shows schematically an application of the present invention in which the D.C. amplifier made in accordance with the present invention is connected to an ordinary D.C. amplifier, and

Figure 6B shows the gain/frequency characteristics of the overall amplifier shown in Figure 6A and of one chopper amplifier employed in the D.C. amplifier circuit in accordance with the invention.

As seen in Figures 2 and 5 we provide a D.C. amplifier using two chopper channels having equal gain of the same sign operating in antiphase, to make up one effective chopper channel.

The circuit comprises a signal channeling network connected to the two channels. One channel is provided with resistors R_1, R_3, capacitors Q, R, an A.C. amplifier A_1 and two choppers B, D connected between the channel and ground and arranged to operate in synchronism with each other. Likewise the other channel has resistors R_2, R_4, capacitors S, T, an A.C. amplifier A_2 and choppers C, E connected between the channel and ground. The choppers C and E are arranged to operate in synchronism but out of phase with the choppers B, D by 180°. The resistors R_3 and R_4 form a summing network F to which may be connected an impedance converter (not illustrated). The gains of the amplifiers A_1 and A_2 are equal, and the overall gain of the D.C. amplifier is equal to the gain of one of the amplifiers A_1 or A_2.

In operation, while one channel is "open" and passing a signal (this may be a portion of a D.C. or an A.C. signal) the other channel would be "closed" D.C. restoring. Then in the other half cycle the process would be "viceversa". After separate demodulation the two signals would then be added together in the summing network F making up an amplified version of the original signal applied at the input A—whether it be D.C. or A.C.—depending only on the frequency response of two A.C. amplifier (see Figures 3A and 3B). Thus continuous or substantially continuous amplification is achieved, each amplifier being in use for a portion of the time. The amplifiers are switched to earth or to a reference voltage, during their non-amplifying periods.

In Figures 3A and 3B the various waveforms occurring at the points A, B, C, D, E and F of the circuit illustrated in Figure 2 are shown. Figure 3A shows the amplification of a D.C. input signal whilst Figure 3B shows the amplification of an A.C. input signal. In the Figures 3A and 3B, A′ represents the overall gain of the D.C. amplifier whereas A_1 and A_2 represent the gains of the respective A.C. amplifiers, each of which equals A′.

Figure 4 shows a gain frequency characteristic of the known D.C. amplifier as shown in Figure 1 in curve XY, and of the D.C. amplifier made in accordance with the present invention in curve Z.

The curve XY is a composite one and can be considered in two parts. The curve X is that of the amplifier M_1, the horizontal part of the curve corresponds to a value half M_1. M_2 (i.e. the product of half the gain of the amplifier M_1 and the gain of the amplifier M_2) and the turnover point of the curve X is due to the product of capacitor C_2 and resistor R_2 which together form a low pass filter. The curve Y is that of the amplifier M_2, the turnover point of this curve is due to the product of the capacitor C_1 and the resistor R_1.

In contrast to the composite curve XY, the curve Z is horizontal indicating that the overall gain A′ of the D.C. amplifier is constant from D.C. up to the bandwidth required, and feedback is applied at all these frequencies thus reducing the noise. The overall gain A′ is nearly equal to the gain of either of the A.C. amplifiers A_1 or A_2. One feature of the D.C. amplifier made in accord-

ance with the present invention is that the noise generated at the input stage is now only that of the input device, i.e. the most sensitive amplifying stage, of the chopper amplifier, there being no other channels at the input stage.

The input offset current is that due to the two chopper channels only and these may be coupled by small value low leakage capacitors, e.g. capacitors Q and S in Figure 2, thereby reducing this effect.

Also as the chopper frequency may have a low value, e.g. of the order 100 c/s, the offset current due to spike feed through from the drive to the chopping devices may be low.

The drift at the input stage can be minimised by enclosing the chopping unit in an environment with a low temperature gradient. The input leads to the device may be coupled straight into the environment without any external connections thus reducing drift due to thermal "leakage".

Figure 5 represents a practical embodiment of the circuit shown in Figure 2 in which the choppers comprise semiconductor devices. In this embodiment the choppers B and C consist respectively of N-type insulated gate field effect transistors (FET) 10 and 11. The drain electrode of the FET 10 is connected to the junction of the resistor R_2 and the capacitor S. The source electrodes of FETs 10 and 11 are connected to each other and to one side of a power supply and their gate electrodes are respectively connected to a source of chopping voltage (not shown) of suitable amplitude, e.g. 10V. The chopper D consists of a N-P-N transistor 12 having its collector connected to the junction between the capacitor R and the resistor R_3. The chopper E consists of a N.P.N transistor 13 of similar type as the transistor 12 having its collector connected to the junction between the capacitor T and the resistor R_4. The emitters of the transistors 12, 13 are connected to each other and to ground and their base electrodes are connected respectively to the source of chopping voltage.

In order to balance the outputs from the amplifiers A_1, A_2 a variable resistor R_5 is connected between the resistors R_3, R_4 of the summing network F and the output from the network is taken from the wiper of the variable resistor R_5. The capacitors Q and S are d.c. biassed respectively by resistors R_7 and R_6. Resistors R_8 and R_9 are provided as protection resistors for the FETs 11 and 10 respectively.

In the described circuit the components have the following values:

Gain of amplifiers A_1 and A_2	$=5\times10^4$
Chopping frequency	=100 c/s
Resistors R_1 and R_2	=220 kΩ
Resistors R_3 and R_4	=2.2 mΩ
Variable resistor R_5	=1 MΩ
Resistors R_6 and R_7	=100 MΩ
Capacitors Q and S	=10,000 pF
Capacitors R and T	=10 μF

Figure 6A shows an application of the invention in which an ordinary D.C. amplifier 20 is connected to the summing network F as shown. It is to be noted that the amplifier 20 may be replaced by filters or other suitable devices which will modify the gain/frequency characteristics of the overall amplifier 21, i.e. the chopper amplifier in accordance with the present invention and the D.C. amplifier 20.

Figure 6B shows the gain/frequency characteristic 25 of the overall amplifier 21 and the gain/frequency characteristic 26 of one of the A.C. amplifiers, e.g. amplifier A_1 obtained by applying an A.C. signal to the point K in Figure 6A and measuring the output at the output of summing network F. The characteristic 26 is a rising one due to the effect of the capacitor R, resistor R_3 and the components in the A.C. amplifier A_1. The falling part of the characteristic 25 is shaped by the response of the D.C. amplifier 20.

Figure 6B shows in broken lines the gain/frequency characteristic 27 from the input stage (point K in Figure 6A) to the output of the amplifier, i.e. the first amplifying element and its associated components, of the A.C. amplifier A_1. The thermal noise in the A.C. amplifier A_1 is for the most part generated in the input stage since it is the most sensitive. In order to reduce the effect of any noise generated in the input stage, the chopper frequency is chosen so that the overall response of the amplifier 21 (Fig. 6A) is decreasing at a frequency less than the chopper frequency, and so at the frequency where the overall gain of the amplifier 21 equals the chopper amplifier gain, i.e. where the characteristics 25 and 26 intersect, the amplification from the input stage is a maximum. Accordingly at frequencies separated from this cross-over frequency, especially at the low end, the noise from the input stage becomes negligible and signal to noise ratios of the order 1000:1 are obtained. Also, because of the output chopper action it can be shown that there is a further reduction of noise at low frequency.

By increasing the chopper frequency the characteristic curves 25, 26 and 27 tend to move to the right in Figure 6B thereby increasing the bandwidth of the overall amplifier 21. Conversely by decreasing the chopper frequency the characteristics 25, 26 and 27 tend to move to the left in Figure 6B thereby reducing the bandwidth of the overall amplifier 21. In Figure 6B the curve 25 represents the characteristic of the overall gain of amplifiers (Fig. 6A) from input of complete ampli-

fier, i.e. from point A in Figure 5 or signal splitting point, to output of D.C. amplifier 20. (The frequency response being adjusted in the D.C. amplifier). Line 26 is the response of either A.C. amplifier (Fig. 6A) from point K through amplifier A_1 or A_2. Line 27 represents the response from point F (Fig. 6A) through amplifier A_1 and the D.C. amplifier 20 to the output. Noise reduction is achieved at low frequency by the relationship of line 25 to 27. This relationship between line 25 and 27 provides for a reduction in the amplifier noise at low frequency, because an input signal to the amplifier "sees" the characteristic of line 25, while the input active device (the main cause of noise) "sees" the characteristic of line 27.

The D.C. amplifier circuit in accordance with the invention allows for overlap of the switching of the chopper channels and also for a time gap between switching without any detrimental effect upon the gain characteristic, i.e. both channels are conducting together at one time or neither is on at one time in order to allow for timing errors.

It is also possible to arrange for the choppers to operate in series connection instead of parallel connection.

Although semiconductor choppers have been described with respect to the embodiment of the invention illustrated in Figure 5 it is to be understood that the present invention is not limited to the use of semiconductor choppers only, for example, electro-mechanical choppers such as reed relays may be used.

WHAT WE CLAIM IS:—

1. A D.C. amplifier including a signal channeling network having at least two outputs, at least two A.C. amplifiers connected respectively to the outputs of the channeling network, a summing network connected to respective outputs of the amplifiers and switch means to switch said amplifiers in sequence so that each amplifier is used alternately to provide continuous or substantially continuous amplification of an input signal at the output of the summing network, the A.C. amplifiers each having its input and output restored to earth potential or to a reference voltage during the periods of non-use.

2. A D.C. amplifier as claimed in Claim 1 having two A.C. amplifiers.

3. A D.C. amplifier as claimed in Claim 1 or 2 wherein said switch means each amplifier comprises two synchronously operated choppers.

4. A D.C. amplifier as claimed in Claim 3 wherein one of said two choppers consists of an insulated gate field effect transistor.

5. A D.C. amplifier as claimed in Claim 3 wherein one of said two choppers consists of a N.P.N. transistor.

6. A D.C. amplifier as claimed in Claim 3 wherein one of said two choppers consists of a N-type insulated gate field effect transistor and the other of said two choppers consists of a NPN transistor.

7. A D.C. amplifier as claimed in Claim 3 wherein the choppers are electro-mechanical switching means.

8. A D.C. amplifier as claimed in any one of claims 3 to 7, wherein the two choppers are connected in parallel connection.

9. A D.C. amplifier as claimed in any one of claims 3 to 7, wherein the two choppers are connected in series connection.

10. A D.C. amplifier as claimed in any one of Claims 1 to 9 wherein the summing network comprises at least one resistor connected between the output of each amplifier and a common point, the output of the amplifier being taken from said common point.

11. A D.C. amplifier as claimed in any one of claims 2 to 9 wherein the summing network comprises two resistors connected respectively to the outputs of the two amplifiers and a variable resistor connected in series between said two resistors, the output of the amplifier being taken from the slider of the variable resistor.

12. A D.C. amplifier as claimed in any one of Claims 1 to 11 wherein at least one capacitor is connected between the channeling network and the input of each amplifier and wherein at least one capacitor is connected between each amplifier output and the summing network.

13. A D.C. amplifier substantially as hereinbefore described with reference to Figures 2 to 6 of the accompanying drawings.

14. A low level D.C. amplifier substantially as hereinbefore described with reference to Figure 5 of the accompanying drawings.

For the Applicants,
MATTHEWS, HADDAN & CO.,
Chartered Patent Agents,
31/32, Bedford Street,
Strand,
London, W.C.2.

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Sheet 1

Fig.1.

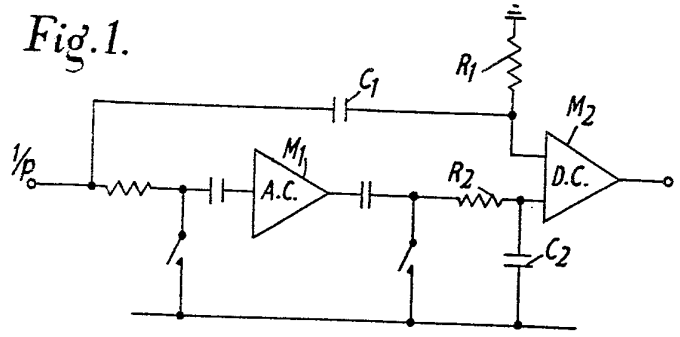


Fig.2.

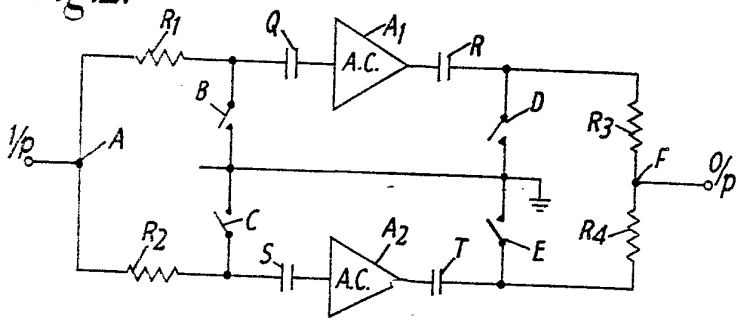


Fig.3A.

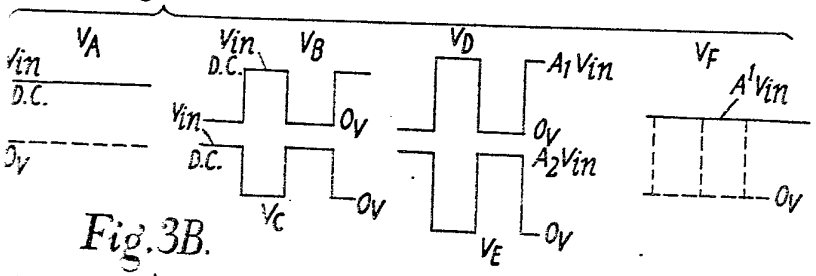
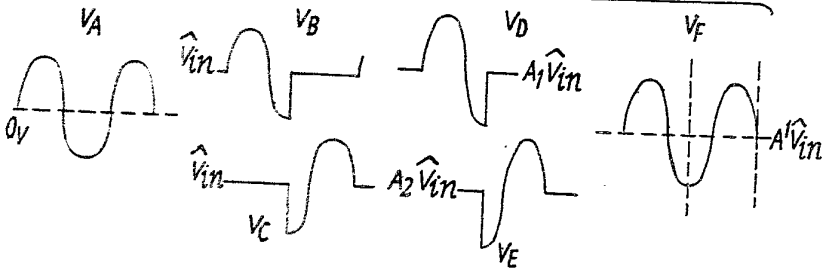


Fig.3B.



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Sheet 2

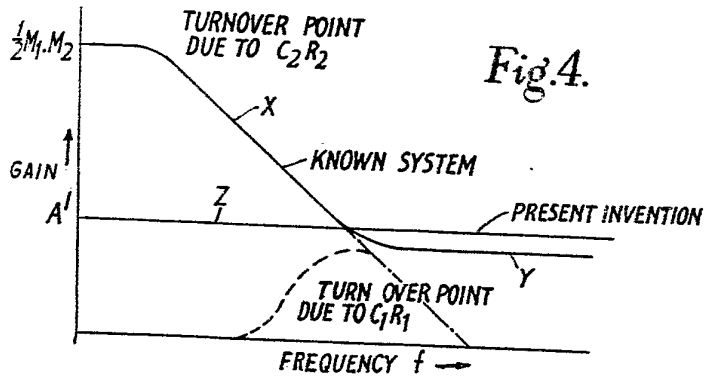
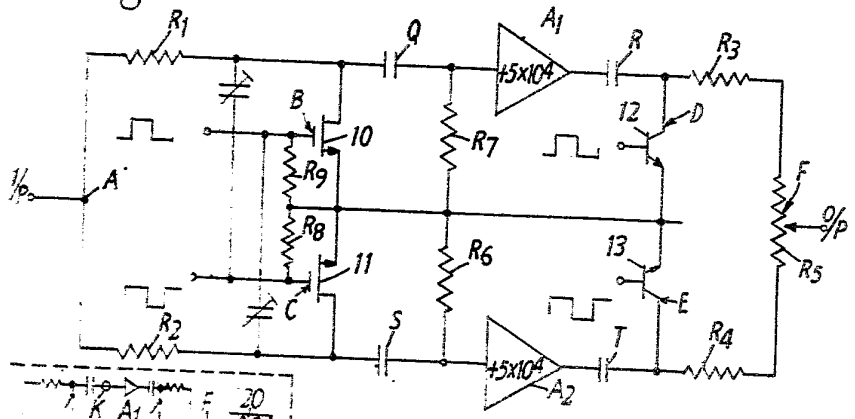


Fig.4.

Fig.5.



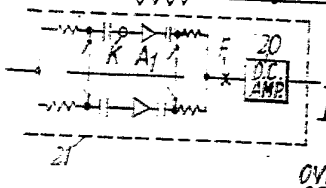


Fig.6A.

Fig.6B.