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(56) Documents cited
GB 1527847
GB 1046447
GB 0992046
GB 0984567
GB 0877998
"Electronics":-Mar 15 1963 p 107 "What shall we do with one microvolt"
July 1 1960 p 55-7 "Transistorised data amplifier
April 1955 p 135-7 "Transistor choppers"
(58) Field of search
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H3T
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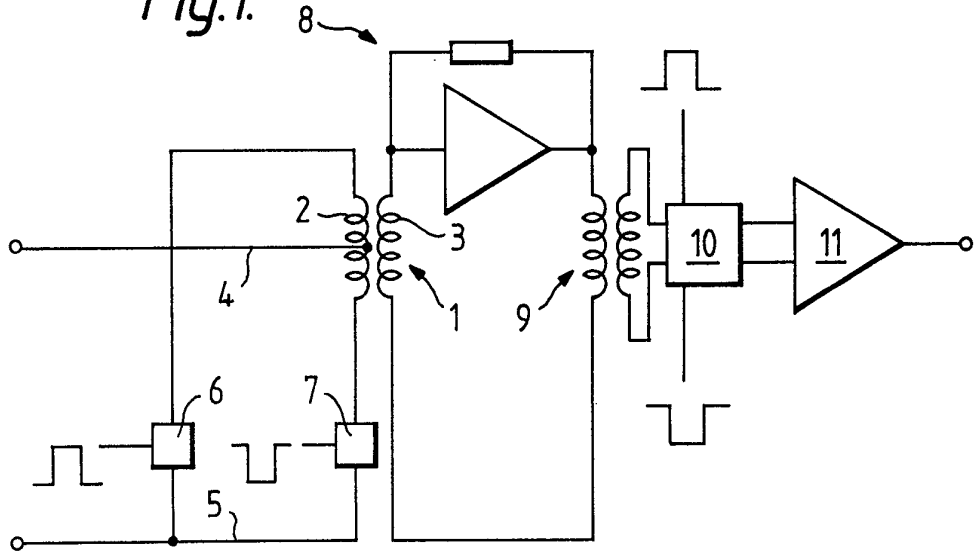
(54) **Low level D.C. amplifier**

(57) The input stage of a low-level D.C. amplifier utilises a chopping technique to convert a D.C. input signal into an A.C. signal for initial amplification by an A.C. amplifier (8). the input stage includes a transformer (1) having a centre-tapped input winding (2) with its centre tap (4) connected to receive the input signal, and an output winding (3) connected to the A.C. amplifier (8). The input stage further includes two switching devices (6, 7) arranged for cyclic, antiphase, operation to connect respective ends of the input winding (2) to a signal return line (5), the effect of this being to apply the input signal alternately across the two input-winding halves. As a result, the A.C. amplifier (8) operates during both halves of the chopping cycle and may have considerable loop gain. By making the transformer (1) a step-up transformer, the effective input noise voltage of the A.C. amplifier (8) can be reduced so that the predominant noise voltage is that resulting from the switching-device resistances when conducting.

Fig.1.



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The drawings originally filed were informal and the print here reproduced is taken from later filed formal drawings.

Fig.1.

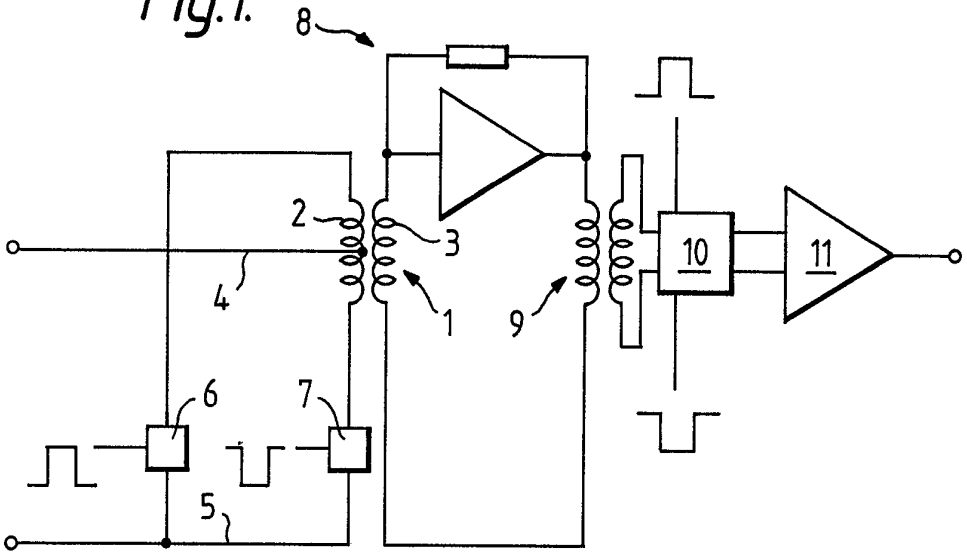


Fig.4.

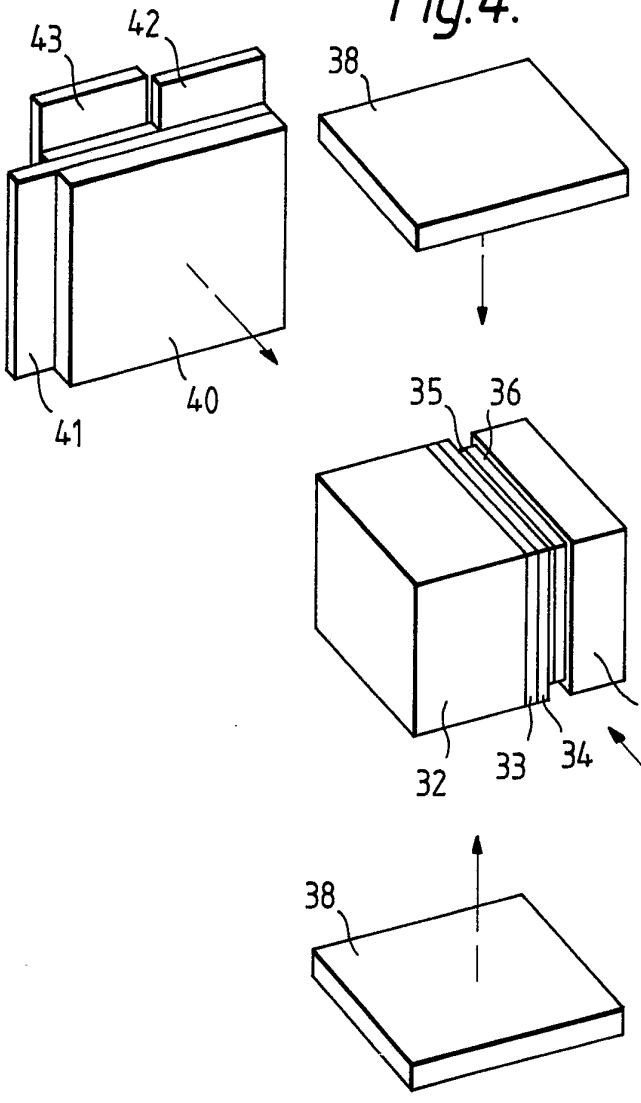
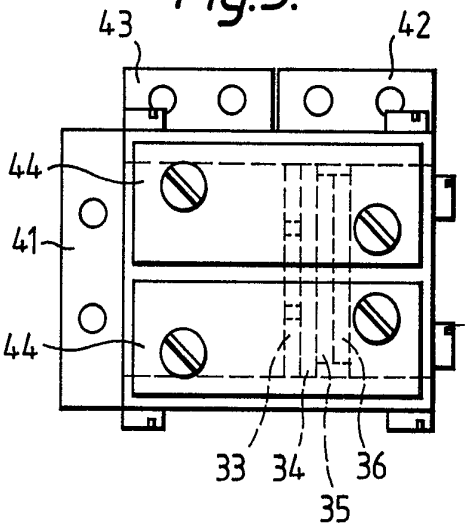
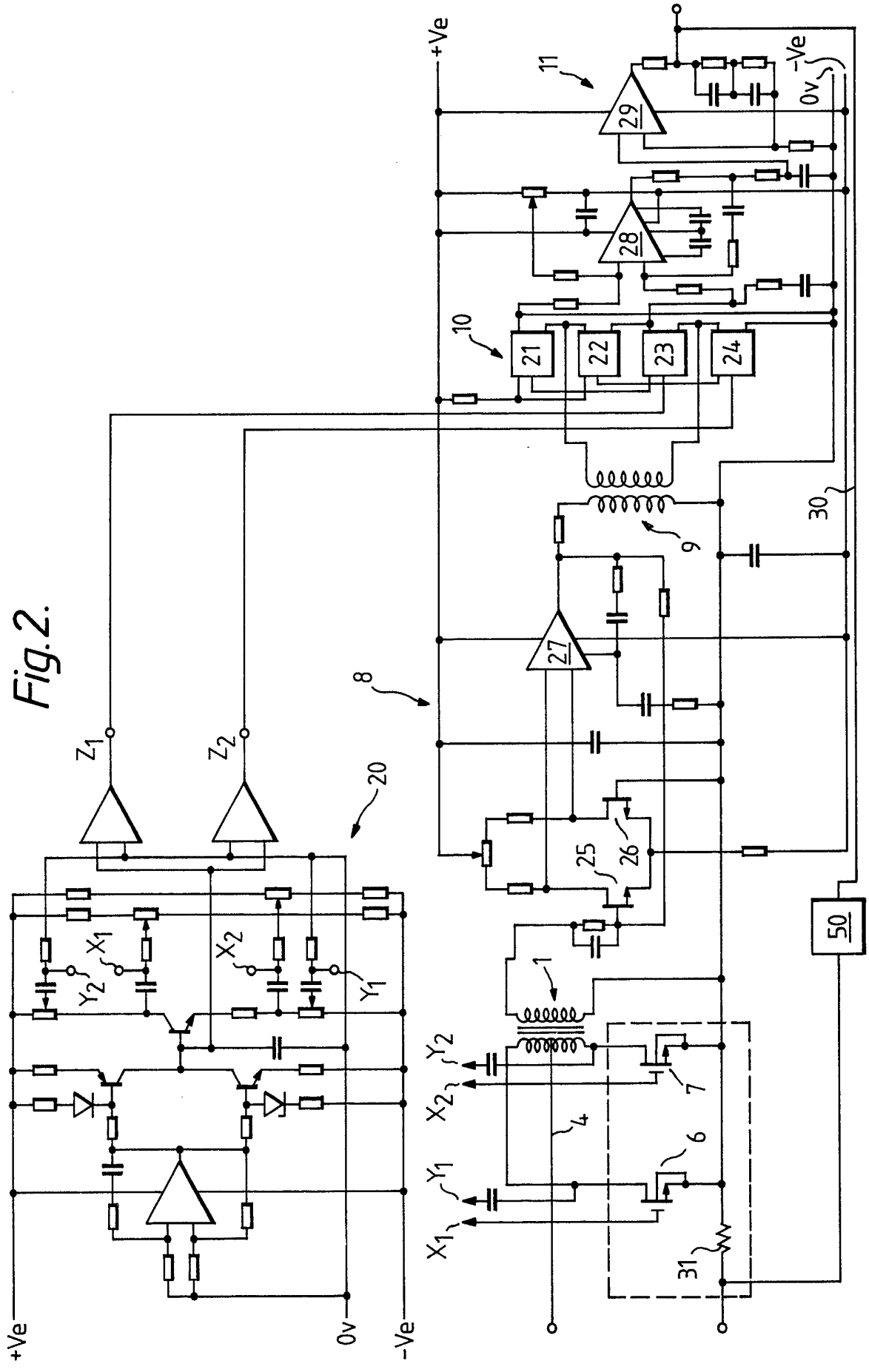


Fig.5.




+Ve
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11
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30
9
27
8
25
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50
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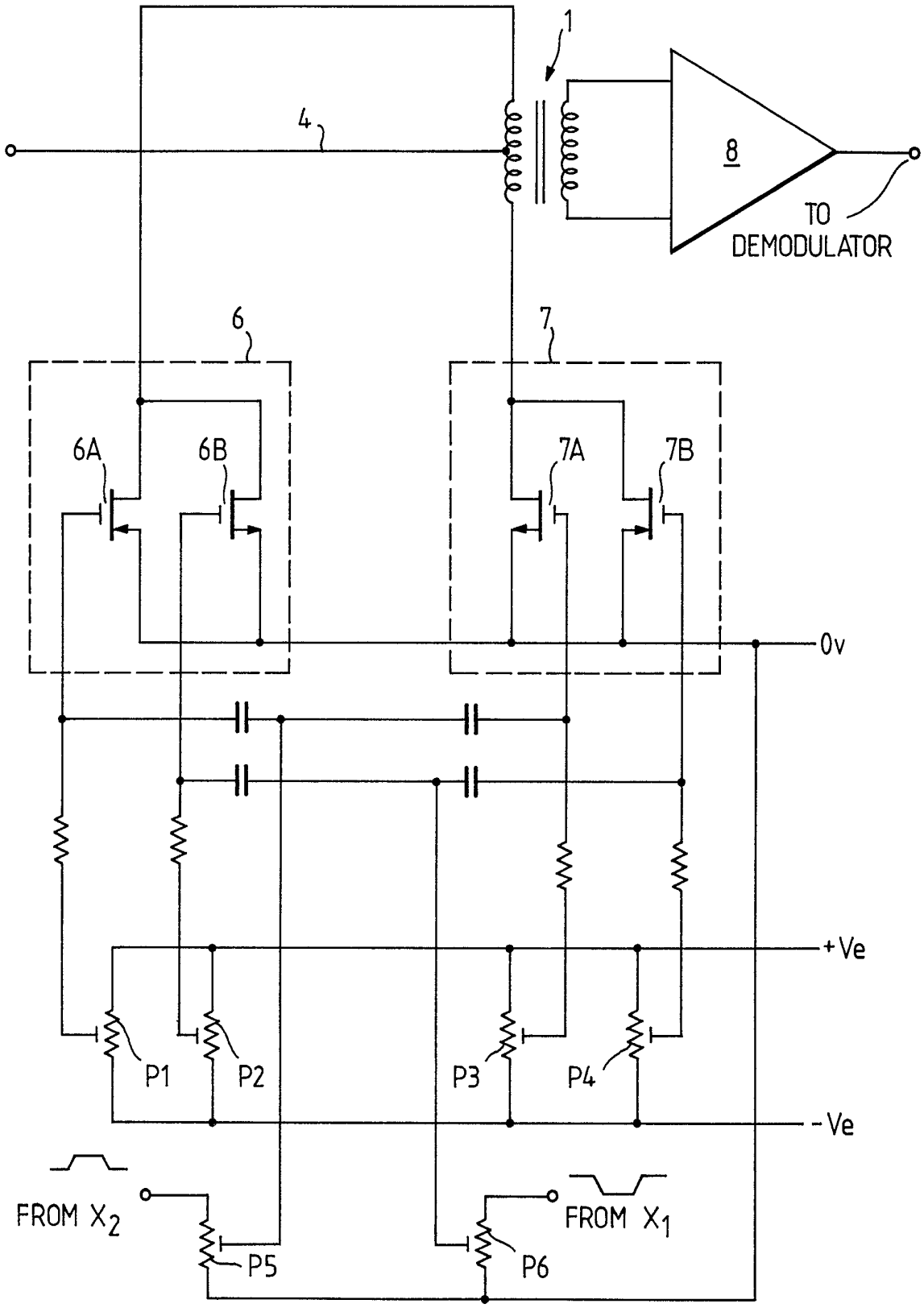
Z1
Z2
20
X1
Y2
X2
Y1
4
7
6
31

Fig.2.

Fig.3.


1
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TO
DEMODULATOR
6
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6A
6B
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0v
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P1
P2
P3
P4
P5
P6
FROM X2
FROM X1

SPECIFICATION

Low level D.C. amplifier

The present invention relates to a low level D.C. amplifier.

The amplification of low d.c. potentials depends on the ability of the amplifying system to discriminate between the required input and unwanted signals. These signals may be noise from a variety of sources, drift (very low frequency noise) or magnetic or electric interference.

In most amplifiers, the gain must be determined to some specified degree of accuracy, and to achieve this, it is usual to employ negative feedback techniques. This makes it mandatory that the open loop gain and phase response with frequency is clearly defined so that stability criteria can be achieved, and thus, a further requirement is laid on the design of the basic amplifier.

Certain advances were made, using multiple channel amplification, and these are described in British Patent No. 1,168,873. This advanced the art from the well known A.C. channel and D.C. chopper stabilised channel to a system using only chopper channels, and so improved the noise performance and stability of the amplifier; this prior art system is capable of providing resolution down to 100 nanovolts and perhaps a little lower.

The present invention seeks to provide a low level D.C. amplifier which in at least certain embodiments is capable of providing resolution down to 100 pico volts and below.

One of the main problems to be overcome in providing such an amplifier is that of noise or unwanted signal.

The thermal noise generated by a pure resistor i.e. one that adds nothing to the basic physical noise generated by thermal agitation of the electrons in the conductor, is given by the expression:

$$en = \sqrt{4KTRdF}$$

where

en is the r.m.s. value of noise in volts,

K is Boltzmans constant 1.38×10^{-23} Joules per deg. K,

T is absolute temperature in deg K,

R is the resistance value in ohms,

dF is the bandwidth in Hz.

In order to achieve a reasonable response time for the amplifier, the noise should be limited, if possible, to the thermal noise generated by a resistor of about 60 ohms or less.

According to one aspect of the present invention, there is provided a low level D.C. amplifier unit including an input transformer with a centre-tapped input winding, two switching devices arranged for cyclic, anti-phase, operation to connect respective ends of said input winding to a voltage reference during successive switching half cycles whereby a d.c. input signal fed to the centre tap of the input winding is effectively applied alternatively across the two input winding halves; and an initial active amplifying stage constituted by an A.C. amplifier connected on its input side to the output winding of said input transformer.

The voltage reference is typically ground voltage.

With this arrangement, the A.C. amplifier constituting the first active amplifying stage of the unit is operative during both halves of the chopping cycle, the amplifier being effectively inverted every half cycle. As the result, many of the advantages of the two channel system described in U.K. 1,168,873 referred to above, are obtained using only a single continuously-operating A.C. amplifier so that the amplifier unit can have considerable loop gain at the chopping frequency and still maintain stability.

Preferably, the output of the A.C. amplifier is connected via a transformer to a synchronous demodulator which is operated in synchronism with the said switching device. Thus, in operation of the amplifier unit, the input d.c. signal is first modulated by the switching devices and transformed into an A.C. signal whose peak value is proportional to the d.c. input; thereafter the A.C.. signal is amplified by the A.C. amplifier and passed through the output transformer to the demodulator. This demodulator (for example, an active bridge demodulator) outputs an amplified d.c. signal proportional to the d.c. input.

With regard to its noise characteristics, the amplifier unit of the invention enables the input noise to be reduced. More particularly, the switching device arrangement permits both devices to be connected to ground so that very little unwanted resistance, over and above the switching device resistances, is added to the input circuitry. Given the current state of technology, the most suitable switching device is the insulated gate field effect transistor (although optical switching devices may in the future also prove suitable). With FET switching devices, channel resistances of a few tens of ohms are readily attainable and resistances down to less than an ohm are possible. The thermal noise from the switching devices can therefore be held down to a level of less than 1 nV per root Hz.

In addition to the resistances of the switching devices, another major potential source of noise in the amplifier unit is the first active amplifier device (that is, the first active device of the A.C. amplifier), the best device that is presently available giving a noise voltage of about 2 nanovolts per root Hz. By arranging for the turns ratio between each input winding half of the input transformer and the transformer output winding to be greater than unity, it is possible to diminish the effective input noise voltage of the first active amplifying device. Thus, for example, if the equivalent input noise voltage of this first amplifying device is 2 nV per root Hz, and the input transformer turns ratio is 20:1, then the effective input noise voltage for the amplifier unit is 100 pV per root Hz plus the resistance noise of the switching devices which, as discussed above, can be as little as 1 nV per root Hz or less for F.E.T. devices. Of course, the input transformer will also act to increase the current noise from the first amplifying device by the turns ratio; it is thus appropriate to use for this device a low noise junction field effect transistor which has a very low input noise current of the order of 10^{-15} amps per root Hz. With such a

figure for the noise current of the first amplifying device and with a turns ratio of 20:1, the input current noise is 2×10^{-14} amps per root Hz resulting in an equivalent noise voltage of 2pV per root Hz in a 100 ohm input switching circuit.

When field effect transistors are used for the switching devices, there is an element of capacitance coupling between the chopper drive unit and the amplifier input transformer, this being due to capacitance coupling between the gate and drain circuits of the F.E.T.s. In order to compensate for the voltage change which would, if uncompensated for, appear on the F.E.T. drain electrode as a result of this capacitive coupling whenever a switching pulse is applied to the gate electrode, an opposing voltage change can be applied, via a capacitor, to the F.E.T. drain electrode.

In addition to the thermal noise generated by a pure resistor, another type of unwanted signal that may be present in practical low level D.C. amplifiers is that constituted by thermal e.m.f.s generated at junctions between dissimilar conductors when a temperature differential exists thereacross.

Thus, the alloy generally used in the leads of F.E.Ts suitable for use as the switching devices of the amplifier unit of the present invention, has a thermal e.m.f. with copper of about 40 micro volts per deg C. For the level of measurement contemplated for the present amplifier unit, the thermal offsets should preferably amount to no more than 100 pico volts per deg. C. This requires a temperature gradient of a few millionths of a degree.

According to another aspect of the present invention, there is provided a low level amplifier unit in which all the dissimilar-metal junctions of the input stage of the amplifier unit are linked together thermally in a thermal equalising block. With respect to the low level d.c. amplifier unit of the invention, the switching devices constitute said input stage and are contained in a massive, pure copper structure. Furthermore, thin, pure copper input connections are used, having high thermal resistance, and this arrangement together with thermal lagging of the input stage provides an effective thermal filter.

A low level d.c. amplifier unit embodying the invention will now be described, by way of example, with reference to the accompanying diagrammatic drawings, in which:

Figure 1 is a block schematic diagram of the amplifier unit:

Figure 2 is a circuit diagram of the unit;

Figure 3 is a circuit diagram of a modified input stage of the unit;

Figure 4 is an exploded perspective view of a thermal equalising block of the unit housing the input switching devices of the Figure 2 circuit, and

Figure 5 is a view, in the direction of arrow IV in Figure 4, of the thermal equalising block, internal detail of the block being shown in dashed outline.

As shown in Figure 1, the low level d.c. amplifier unit comprises an input switching stage constituted by an input transformer 1 and two switching devices 6 and 7, a first active amplifying stage constituted by an A.C. amplifier 8, a synchronous demodulator 10 fed from the amplifier 8 via a transformer 9 and operating in synchronism with the switching devices 6 and 7, and a d.c. output amplifier stage constituted by the amplifier 11.

The input transformer 1 has a centre-tapped input winding 2 and an output winding 3. The transformer 1 has a turns ratio of greater than unity (typically 10 to 50) between each input winding half and the output winding 3.

A d.c. signal to be amplified is applied between the centre tap 4 of the input winding 2 and a signal return line 5. The switching devices 6 and 7 are connected between the line 5 and respective ends of input winding 2. These devices 6 and 7 are two-state switching devices and will generally be constituted by field effect transistors. The two devices 6 and 7 are cyclically switched between their conducting and non-conducting states in anti-phase relation such that the d.c. input signal fed to the input-winding centre tap 4 is effectively applied alternately across the two input winding halves. This chopping action on the input signal results in the production of an A.C. signal across the output winding 3 with the peak value of this signal being proportional to the d.c. input.

The A.C. signal is then amplified by the A.C. amplifier 8 and fed via the transformer 9 to the synchronous demodulator 10 (for example, an active bridge demodulator) where it is converted back to a d.c. signal for further amplification by the amplifier 11.

It can be clearly seen that the A.C. amplifier 8 is operative during both halves of the chopping cycle, the amplifier being effectively inverted every half cycle. As a result, the amplifier unit can have considerable loop gain at the chopping frequency and still maintain stability.

The arrangement shown in Figure 1 enables the input noise to be limited substantially to that resulting from the switching device resistances. This is due, in part, to the fact that the line 5 can be grounded so that very little unwanted resistance is added to the input switching stage over and above the resistances of the devices themselves. Furthermore, as discussed above, the input transformer 1 serves to diminish the effective input noise voltage of the first active amplifying device of the unit (that is, the first active device of the amplifier 8).

Figure 2 shows the amplifier unit in greater detail. Thus the switching devices 6, 7 of the input switching stage are shown as N-channel insulated-gate field effect transistors whose gate electrodes are fed with ramped switching pulses from outputs X_1, X_2 of a chopper drive unit 20, the pulses from output X_1 being in anti-phase to the pulses from X_2. The chopper drive unit 20 also supplies demodulator drive pulses from outputs Z_1, Z_2 to the four bridge-connected optically-coupled choppers 21 to 24 constituting the demodulator 10.

The A.C. amplifier 8 is built around two low-noise input F.E.T.s 25 and 26 and an integrated circuit amplifier 27. The amplifier 11 is built around two integrated circuit amplifiers 28 and 29. The output of the amplifier 11 is fed back via a line 30 and a gain-and-phase setting circuit 50 (shown in block form only in Figure 2), to a feedback resistor 31

incorporated in the input switching stage whereby to determine the overall gain of the unit.

When as in the Figure 2 circuit, field effect transistors are used for the switching devices 6 and 7, there is an element of capacitance coupling between the chopper drive and the amplifier input transformer 1, this being due to the capacitance coupling between the gate and drain circuit of the F.E.T.s. Thus, when the drive voltage applied to the gate electrode of a switching-device F.E.T. is changed, a small current will pass through the capacitance from the gate circuit to the drain circuit. The effective coupling capacitance is in fact, very complex and varies with changes in gate voltage and drain-source voltage.

In order to compensate for this capacitance coupling, an opposing voltage change can be applied to the F.E.T. drain electrode at the same time as the switching pulse is applied to the gate electrode. Thus, in the Figure 2 circuit, in addition to the gate pulses, the unit 20 also supplies, via outputs Y_1, Y_2, ramped compensation pulses to the F.E.T's 6 and 7, these latter pulses being fed via capacitors to the drain electrodes of each F.E.T. 6, 7 in anti-phase to the gate pulses applied to that F.E.T.

A more effective compensation arrangement is illustrated in Figure 3 and involves the use of complimentary pairs of F.E.T.s for each switching device 6, 7. In the Figure 3 arrangement, the device 6 comprises a P-channel F.E.T. 6A and an N-channel F.E.T. 6B, whereas the device 7 comprises an N-channel F.E.T. 7A and a P-channel device 7B. The F.E.T.s of each device 6, 7 are switched by opposite phase pulses; thus, for example, as the F.E.T. 6A is switched on by a pulse from output X_2 of the drive unit 20 (Figure 2), the F.E.T. 6B is switched on by a pulse from the output X_1, the F.E.Ts 7A and 7B being simultaneously switched off by pulses from the outputs X_2 and X_1 respectively.

If the two F.E.T.s of each device 6, 7 were exactly complimentary, a complete compensation for capacitance feedthrough would, in theory, be achieved. Although this ideal is not achievable in practice, a high degree of compensation can be attained.

Two further advantages accrue from the use of two complimentary F.E.T.s for each switching device. Firstly, the two parallel conductive paths provided by the two F.E.T.s when switched on ensure a low "on" resistance which, as already discussed, is crucial for noise reduction. Secondly, the opposite polarity d.c. bias of the two F.E.T.s compensates for d.c. leakage.

In the Figure 3 circuit, each F.E.T. 6A, 6B, 7A, 7B can be individually biassed to achieve optimum conditions by means of potentiometers P1, P2, P3, P4 respectively. Furthermore, two further potentiometers P5 and P6 are provided to enable the offset current to be adjusted by adjusting the levels of the signals received from the drive unit outputs X_1 and X_2.

In order to minimise contamination of the d.c. input signal by thermal e.m.f.s generated in the input switching stage of the amplifier unit, all the switching stage components and junctions are preferably included in a thermal equalisation block. Thus for the Figure 2 circuit, all the components and junctions within the dashed boundary shown in Figure 2 are preferably housed within a thermal equalisation block, a suitable form of block being illustrated in Figures 4 and 5. This block basically comprises a mass of copper serving to minimise temperature gradients across dissimilar-metal junctions in the block. More particularly, the block comprises an inner stack made up of a body part 32, slab members 33, 34, 35 and 36, and an end part 37. This inner stack is surrounded by thermal connector slabs 38, 39 and 40, and external-connection elements 41, 42, 43 and 44 are provided outside the slabs 38. The block is held together by screws 45 (not shown in Figure 4).

The two switching-device F.E.T.s 6 and 7 are fitted inside the body part 32 together with the feedback resistor 31. The source electrodes and substrates of the F.E.T.s 6 and 7 connected to the slab member 34 which is at ground potential (0v) as are the connector slabs 38 to 40. The drain electrode of one F.E.T. is connected to the member 35 while the drain electrode of the other F.E.T. is connected to the member 36. The member 35 and 36 are electrically isolated from the remainder of the block by mica sheets and as a result of their dimensioning; these members 35 and 36 are, however, in good thermal contact with the other block components. The members 35 and 36 are electrically connected to the external-connection elements 42, 43.

The gate connections of the F.E.T.s 6 and 7 are brought out via slots in the slab member 33 to connect with respective ones of the external-connection elements 41. The elements 41, 42 and 43 are, of course, electrically isolated from each other.

It will be appreciated that a similar form of thermal equalisation block can be provided for the devices 6 and 7 of the Figure 3 circuit though this block will be modified to take account of the extra components involved.

Various modifications to the described amplifier unit are possible. Thus, for example, the transformer 9 and demodulator 10 could be replaced by two alternately-operating A.C. amplifiers fed from the amplifier 8, the outputs of these amplifiers being combined by any suitable means.

CLAIMS

1. A low level D.C. amplifier unit including an input transformer with a centre-tapped input winding, two switching devices arranged for cyclic, anti-phase, operation to connect respective ends of said input winding to a voltage reference during successive switching half cycles whereby a d.c. input signal fed to the centre tap of the input winding is effectively applied alternatively across the two input winding halves; and an initial active amplifying stage constituted by an A.C. amplifier connected on its input side to the output winding of said input transformer.

2. A D.C. amplifier unit according to Claim 1, wherein the turns ratio between each input winding half and the transformer output winding is greater than unity.

3. A D.C. amplifier unit according to Claim 2,

wherein the first active amplifying device of the A.C. amplifier is a low-noise junction field effect transistor.

4. A D.C. amplifier unit according to any one of the preceding claims, wherein the output of the A.C. amplifier is connected via a further transformer to a synchronous demodulator which is arranged for operation in synchronism with the said switching devices.

5. A D.C. amplifier unit according to any one of the preceding claims, wherein the two switching devices are constituted by two insulated-gate field effect transistors of the same polarity, the amplifier unit further including switching control means arranged to supply first switching pulses to one switching-device transistor, and second switching pulses, in anti-phase relation to the first pulses, to the other switching-device transistor.

6. A D.C. amplifier unit according to Claim 5, where each switching-device transistor has its drain electrode connected to a respective end of the input winding of the input transformer and its source electrode connected to the said voltage reference, the switching control means being arranged to supply said first pulses to the gate electrode of said one switching-device transistor and, via a capacitor, to the drain electrode of the said other switching-device transistor, and to supply said second pulses to the gate electrode of said other switching-device transistor and, via a capacitor, to the drain electrode of the said one switching-device transistor.

7. A D.C. amplifier unit according to any one of Claims 1 to 4, wherein each switching device is constituted by two insulated-gate field effect transistors of opposite polarity, the amplifier unit further including switching control means arranged to supply first switching pulses both to one transistor of one said switching device and to the opposite-polarity transistor of the other device, and second switching pulses, in anti-phase relation to said first pulses, to the two other switching-device transistors.

8. A D.C. amplifier unit according to any one of Claims 5 to 7, wherein the switching control means is such that the first and second pulses have a ramped start and finish.

9. A D.C. amplifier unit according to any one of the preceding claims, wherein all dissimilar-metal junctions associated with connections to the switching devices are thermally linked together in a thermal equalising block.

10. A D.C. amplifier unit according to Claim 8, wherein the thermal block is a massive copper structure enclosing the switching devices, electrical connections to these devices being effected by thin copper input leads having high thermal resistance.

11. A low level amplifier unit in which all the dissimilar-metal junctions of the input stage of the amplifier unit are linked together thermally in a thermal equalising block.

12. A D.C. low level amplifier unit substantially as hereinbefore described with reference to the accompanying drawings.

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